Philips Components

Data sheet	
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TDE8715D

8-bit high-speed analog-to-digital converter

FEATURES

- 8-bit resolution
- Sampling rate up to 50 MHz
- High signal-to-noise ratio over a large analog input frequency range (7.5 effective bits at 4.43 MHz full-scale input at a 50 MHz clock frequency)
- ECL (10KH family) compatible digital inputs and outputs
- Overflow/underflow ECL output
- Low-level AC clock input signal allowed
- Power dissipation only 325 mW (typical)
- Low analog input capacitance, no buffer amplifier required
- No sample and hold circuit required

APPLICATIONS

- High-speed analog-to-digital conversion for:
  - video data digitizing
  - radar pulse analysis
  - transient signal analysis
  - high energy physics research
  - ΣΔ modulators
  - medical imaging

DESCRIPTION

The TDE8715D is a monolithic bipolar 8-bit high-speed analog-to-digital converter (ADC) for professional video and other applications. The operating temperature range is 55 °C up to 125 °C. It converts the analog input signal into 8-bit binary-coded digital words at a maximum sampling rate of 50 MHz. All digital inputs and outputs are 10 KH ECL compatible.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDE8715D	18	DIL	ceramic (cerdip)	SOT 133BH3

PHILIPS

8-bit high-speed analog-to-digital converter TDE8715D

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{EEA}	analog supply voltage		−4.95	−5.2	−5.45	V
V_{EED}	digital supply voltage		−4.95	−5.2	−5.45	V
I_{EEA}	analog supply current		-	20	25	mA
I_{EED}	digital supply current	see note	-	52	60	mA
ILE	DC integral linearity error		-	±0.4	±0.75	LSB
DLE	DC differential linearity error		-	±0.25	±0.5	LSB
EB	effective bits (f_i = 4.43 MHz)	f_{CLK} = 50 MHz	-	7.2	-	bits
$f_{CLK}/\overline{f_{CLK}}$	maximum clock frequency		50	-	-	MHz
T_{amb}	operating ambient temperature range		−55	-	+125	°C
P_{tot}	total power dissipation	see note	-	325	425	mW

Note to the Quick Reference Data

All digital outputs connected to V_{EED} via 2.2 kΩ resistors.

8-bit high-speed analog-to-digital converter TDE8715D

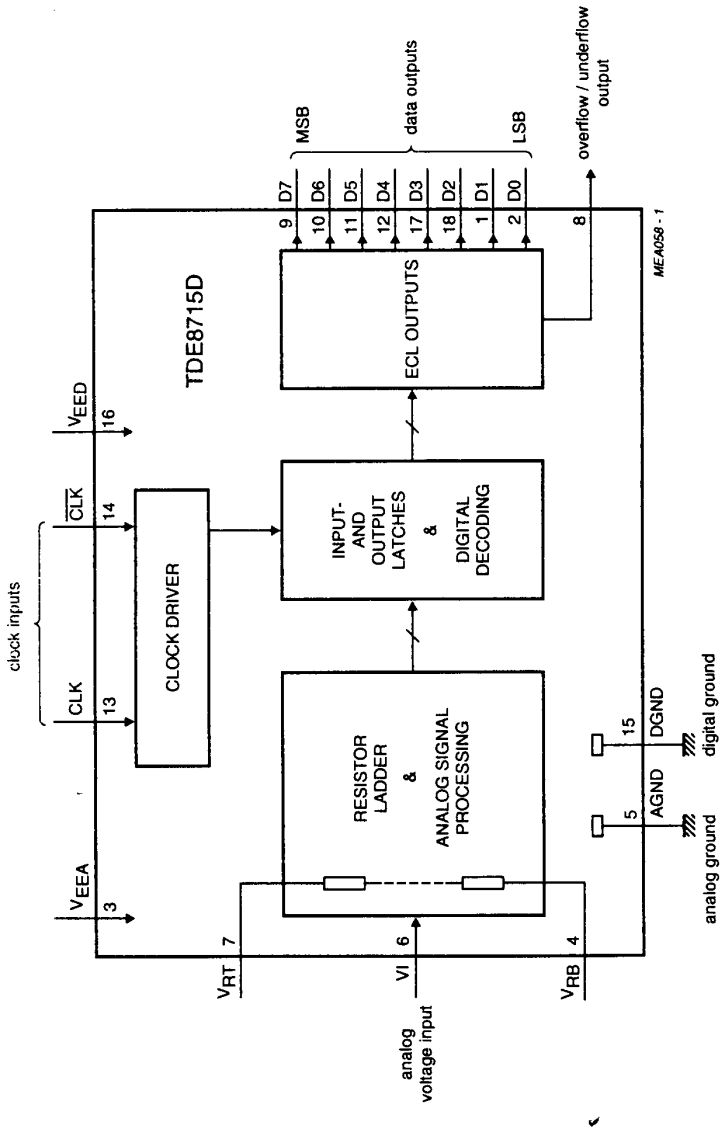


Fig.1 Block diagram.

8-bit high-speed analog-to-digital converter TDE8715D

PIN CONFIGURATION

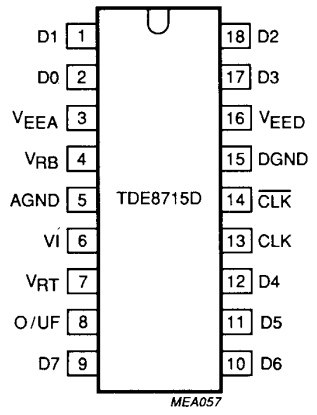


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
D1	1	data output, bit 1
D0	2	data output, bit 0 (LSB)
V_{EEA}	3	analog negative supply voltage (−5.2 V)
V_{RB}	4	reference voltage bottom input
AGND	5	analog ground
VI	6	analog voltage input
V_{RT}	7	reference voltage top input
O/UF	8	overflow/underflow data output
D7	9	data output, bit 7(MSB)
D6	10	data output, bit 6
D5	11	data output, bit 5
D4	12	data output, bit 4
CLK	13	clock input
$\overline{CLK}$	14	complementary clock input
DGND	15	digital ground
V_{EED}	16	digital negative supply voltage (−5.2 V)
D3	17	data output, bit 3
D2	18	data output, bit 2

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{EEA}	analog supply voltage range		−7	0.3	V
V_{EED}	digital supply voltage range		−7	0.3	V
V_{VI}	input voltage range		−7	0.3	V
$V_{\overline{CLK}}$/ V_{CLK}	AC input voltage for switching (peak-to-peak value)	see note	-	2.0	V
I_O	output current		−15	+10	mA
T_{stg}	storage temperature range		−55	+150	°C
T_{amb}	operating ambient temperature range		-55	+125	°C
T_j	junction temperature		-	+175	°C

Note to the Ratings

The circuit has two clock inputs CLK and $\overline{CLK}$. There are two modes of operation:

- Differential drive modes; When driving the CLK input and the $\overline{CLK}$ input directly with two complementary ECL signals imposed on a DC level of −1.3 V, sampling takes place on the LOW-to-HIGH transition of the clock signal.
- Asymmetrical drive modes; When driving the CLK input directly with a ECL signal or a sinewave signal imposed on a DC level of −1.3 V, sampling takes place on the LOW-to-HIGH transition of the clock signal.
- When driving the CLK input with a ECL signal only (Asymmetrical drive modes), it is recommended to decouple the $\overline{CLK}$ input to DGND with a capacitor and connected to V_{EED} by a 150 kΩ resistor.

THERMAL RESISTANCE

SYMBOL	PACKAGE	TYP.	UNIT
$R_{th\ j\text{-}a}$	SOT133BH3	+75	K/W

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

CHARACTERISTICS

$V_{EEA} = V_3 - V_5 = -4.95$ V to -5.45 V; $V_{EED} = V_{16} - V_{15} = -4.95$ V to -5.45 V; AGND and DGND shorted together; $T_{amb} = -55$ °C to +125 °C; unless otherwise specified (typical values measured at $V_{EEA} = -5.2$V; $V_{EED} = -5.2$ V and $T_{amb} = 25$ °C)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{EEA}	analog supply voltage		−4.95	−5.2	−5.45	V
V_{EED}	digital supply voltage		−4.95	−5.2	−5.45	V
I_{EEA}	analog supply current		-	20	25	mA
I_{EED}	digital supply current	note 5	-	52	60	mA
ΔV_{EE}	supply voltage difference $V_{EEA} - V_{EED}$		−0.5	0	+0.5	V
Reference voltages for the resistor ladder						
V_{RB}	reference voltage LOW		−3.4	−3.1	−2.8	V
V_{RT}	reference voltage HIGH		−1.0	−0.6	−0.4	V
V_{ref}	differential reference voltage V_{RT}-V_{RB}		2.4	2.5	-	V
I_{ref}	reference current		-	12.6	-	mA
R_{LAD}	resistor ladder		-	200	-	Ω
R_{TLC}	temperature coefficient of the ladder		-	0.24	-	Ω/°C
V_{OB}	voltage offset bottom	note 6	-	317	-	mV
V_{OBTC}	voltage offset bottom temperature coefficient	note 6	-	0.1	-	mV/°C
V_{OT}	voltage offset top	note 6	-	174	-	mV
V_{OTTC}	voltage offset top temperature coefficient	note 6	-	−0.3	-	mV/°C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Inputs CLOCK INPUT CLK (note 1)						
V_{IL}	input voltage LOW		−1.85	−1.77	−1.65	V
V_{IH}	input voltage HIGH		−0.96	−0.88	−0.81	V
I_{IL}	input current LOW	V_{CLK} = −1.77 V	-	−240	-	µA
I_{IH}	input current HIGH	V_{CLK} = −0.88 V	-	−14	-	µA
R_i	input resistance	f_{CLK} = 10 MHz	-	7.0	-	kΩ
		f_{CLK} = 50 MHz	-	3.5	-	kΩ
C_i	input capacitance	f_{CLK} = 10 MHz	-	1.8	-	pF
		f_{CLK} = 50 MHz	-	1.55	-	pF
CLOCK INPUT $\overline{CLK}$ (note 1)						
V_{IL}	input voltage LOW		−1.85	−1.77	−1.65	V
V_{IH}	input voltage HIGH		−0.96	−0.88	−0.81	V
I_{IL}	input current LOW	$V_{\overline{CLK}}$ = −1.77 V	-	−140	-	µA
I_{IH}	input current HIGH	$V_{\overline{CLK}}$ = −0.88 V	-	75	-	µA
R_i	input resistance	$f_{\overline{CLK}}$ = 10 MHz	-	9.3	-	kΩ
		$f_{\overline{CLK}}$ = 50 MHz	-	4.5	-	kΩ
C_i	input capacitance	$f_{\overline{CLK}}$ = 10 MHz	-	2.6	-	pF
		$f_{\overline{CLK}}$ = 50 MHz	-	2.4	-	pF
$V_{CLK(p-p)} - V_{\overline{CLK}(p-p)}$	AC input voltage for switching (peak-to-peak value)		0.5	0.9	1.1	V
VI (analog input with V_{RB} = −3.1 V and V_{RT} = −0.6 V)						
I_{IL}	input current LOW	data output 00	-	0	-	µA
I_{IH}	input current HIGH	data output FF	-	120	-	µA
R_i	input resistance	f_i = 1 MHz	-	9.4	-	kΩ
C_i	input capacitance	f_i = 1 MHz	-	13.7	20	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Outputs DIGITAL OUTPUTS (D7 - D0 and 0/UF) (Digital 10KH ECL outputs)						
V_{OL}	output voltage LOW	T_{amb} = 25 °C	−1.9	−1.77	−1.65	V
V_{OH}	output voltage HIGH	T_{amb} = 25 °C	−0.96	−0.88	−0.81	V
I_{OL}	output current LOW		-	1.8	4	mA
I_{OH}	output current HIGH		-	1.8	4	mA
Switching characteristics						
$f_{CLK}/f_{\overline{CLK}}$	maximum clock frequency		50	-	-	MHz
Analog signal processing (f_{CLK} = 50 MHz)						
B	−3 dB bandwidth	note 2	-	20.5	-	MHz
G_d	differential gain	note 3	-	0.3	2.0	%
ϕ_d	differential phase	note 3	-	0.4	1.5	deg
f_1	fundamental harmonics (full-scale)	f_i = 4.43 MHz	0	0	0	dB
F_{even}	even harmonics (full-scale)	f_i = 4.43 MHz	-	−60	-	dB
F_{odd}	odd harmonics (full-scale)	f_i = 4.43 MHz	-	−50	-	dB
Transfer function (f_{CLK} = 50 MHz)						
ILE	DC integral linearity error		-	-	± 0.75	LSB
DLE	DC differential linearity error		-	-	± 0.5	LSB
AILE	AC integral linearity error	note 4	-	± 0.75	-	LSB
EB	effective bits f_i = 600 kHz	f_{CLK} = 20 MHz	-	7.8	-	bits
EB	effective bits f_i = 4.43 MHz	f_{CLK} = 50 MHz	-	7.2	-	bits
EB	effective bits f_i = 7 MHz	f_{CLK} = 50 MHz	-	6.9	-	bits
Timing (note 7; see Fig. 3)						
t_{dS}	sampling delay		-	1	3	ns
t_{HD}	output hold time		3	4	-	ns
t_{dLH}	output delay time	LOW-to-HIGH transition	4	5	8	ns
t_{dHL}	output delay time	HIGH-to-LOW transition	6	7	10	ns

Notes to the characteristics

1. The circuit has two clock inputs CLK and $\overline{CLK}$. There are two modes of operation:

- Differential drive modes; When driving the CLK input and the $\overline{CLK}$ input directly with two complementary ECL signals imposed on a DC level of –1.3 V, sampling takes place on the LOW-to-HIGH transition of the clock signal.
- Asymmetrical drive modes; When driving the CLK input directly with a ECL signal or a sinewave signal imposed on a DC level of –1.3 V, sampling takes place on the LOW-to-HIGH transition of the clock signal.
- When driving the CLK input with a ECL signal only (Asymmetrical drive modes) , it is recommended to decouple the $\overline{CLK}$ input to DGND with a capacitor and connected to V_{EED} by a 150 kΩ resistor.

2. The –3 dB bandwidth is determined by the 3 dB reduction in the reconstructed output (full-scale signal at the input).

3. Low frequency ramp signal ($V_{VI(p-p)}$ = 1.8 V and f_i = 15 kHz) combined with a sinewave input voltage ($V_{VI(p-p)}$ = 0.5 V, f_i = 4.43 MHz) at the input.

4. Full-scale sinewave (f_i = 4.43 MHz; $f_{CLK}/f_{\overline{CLK}}$ = 50 MHz).

5. All digital outputs connected to V_{EED} via 2.2 kΩ resistors.

6. Analog input voltages producing code 00 up to and including FF

- V_{OB} (voltage offset bottom) is the difference between the analog input which produces data equal to 00 and the reference voltage bottom (V_{RB}) at T_{amb} = 25 °C.
- V_{OBTC} (voltage offset bottom temperature coefficient) is the dependence of V_{OB} with temperature.
- V_{OT} (voltage offset top) is the difference between V_{RT} (reference voltage top) and the analog input which produces data outputs equal to FF, at T_{amb} = 25 °C.
- V_{OTTC} (voltage offset top temperature coefficient) is the dependence of V_{OT} with temperature.

7. Output data acquisition

- Output data is available after the maximum delay of t_{dHL} and t_{dLH}.
- Output data is fully stable during the low level of the clock. Thus it is recommended that acquisition of this data is made after the falling edge of the clock, instead of after the maximum (t_{dHL}, t_{dLH}).

Table 1 Output coding and input voltage (typical values; V_{RB} = –3.1 V; V_{RT} = –0.6 V and V_{VI} referenced to AGND)

STEP	V_{VI}	O/UF	BINARY OUTPUT BITS							
			D7	D6	D5	D4	D3	D2	D1	D0
underflow	<–2.789	1	0	0	0	0	0	0	0	0
0	–2.783	0	0	0	0	0	0	0	0	0
1	–2.775	0	0	0	0	0	0	0	0	1
.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.
254	.	0	1	1	1	1	1	1	1	0
255	–0.774	0	1	1	1	1	1	1	1	1
overflow	>–0.770	1	1	1	1	1	1	1	1	1

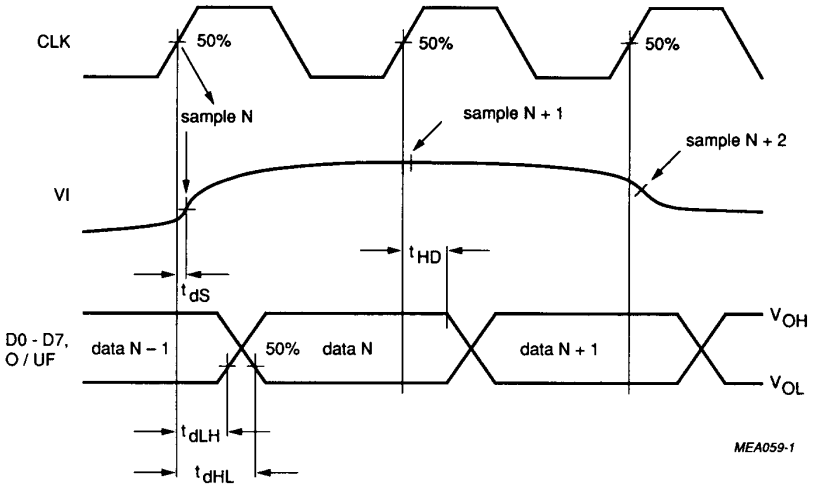


Fig.3 Timing diagram.

INTERNAL PIN CONFIGURATIONS

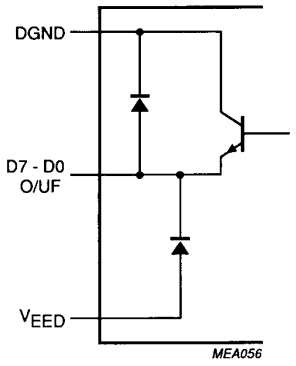


Fig.4 ECL data outputs

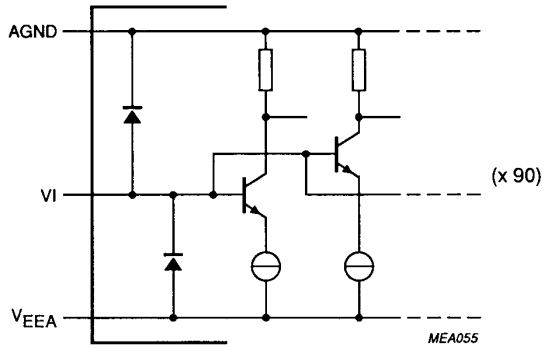


Fig.5 Analog input

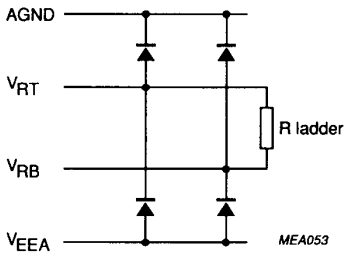


Fig.6 V_{RT} and V_{RB} inputs

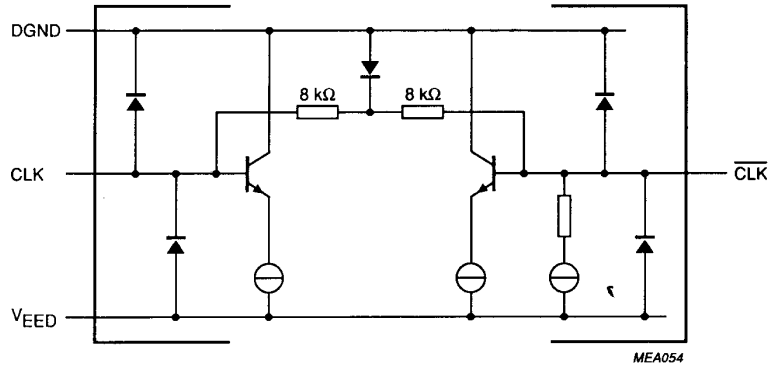


Fig.7 CLK and $\overline{CLK}$ input

8-bit high-speed analog-to-digital converter TDE8715D

APPLICATION INFORMATION

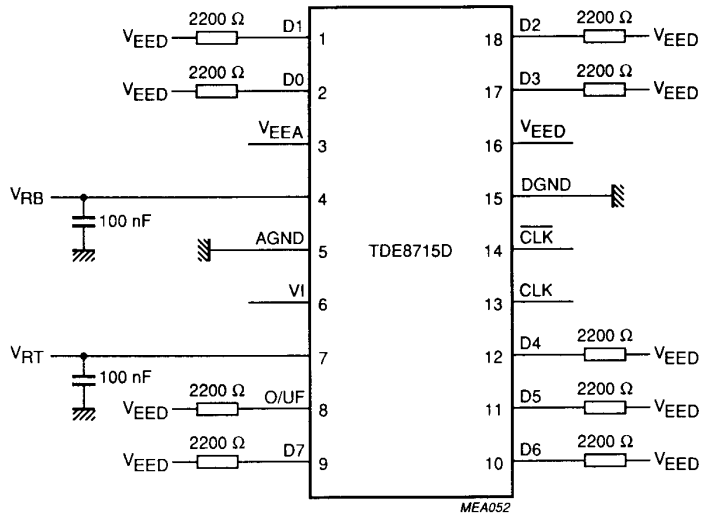
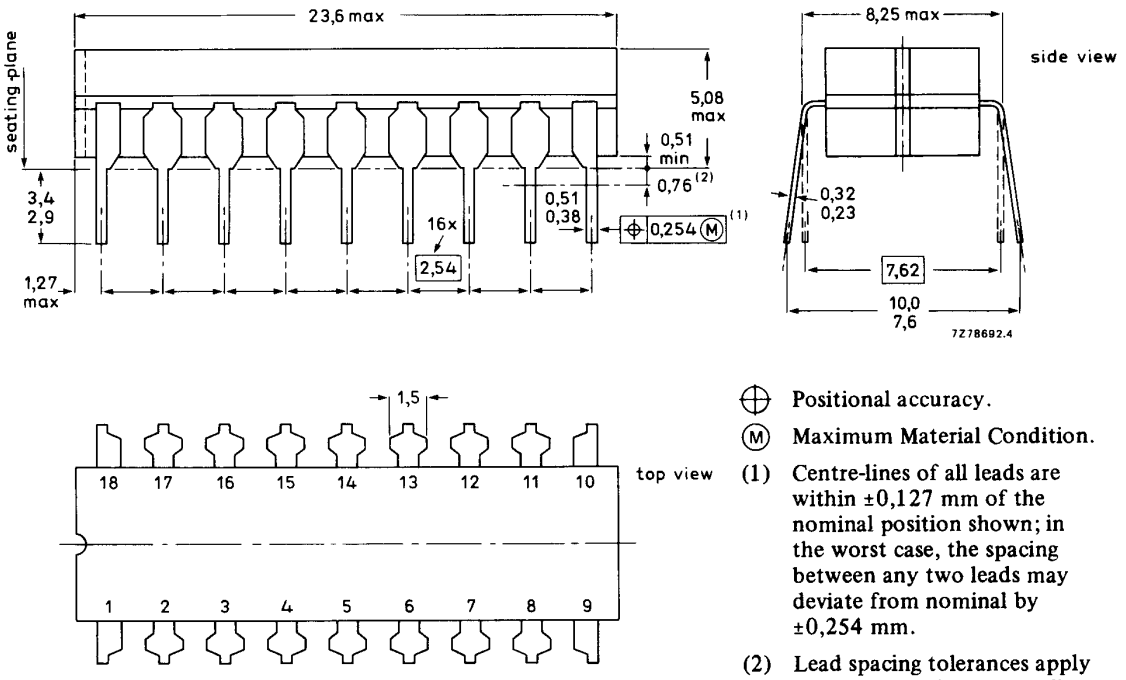


Fig.8 Application diagram.

Notes to Fig.8

- All resistors have a value of 2.2 kΩ; all capacitors have a value of 100 nF .
- Analog and digital supplies should be separated and decoupled.
- The external voltage regulator must be build in such a way that a good supply voltage ripple rejection is achieved with respect to the LSB value.
- $V_{EEA} = V_{EED} = -5.2$ V; $V_{RB} = -3.1$ V; $V_{RT} = -0.6$ V.

PACKAGE OUTLINE



Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Fig.9 18-lead dual in-line; ceramic (cerdip) (SOT133BH3).

SOLDERING

Plastic dual in-line packages

BY DIP OR WAVE

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 s. The total contact time of successive solder waves must not exceed 5 s.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been preheated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

REPAIRING SOLDERED JOINTS (BY HAND)

Apply the soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C it must not be in contact for more than 10 s; if between 300 and 400 °C, for not more than 5 s.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	

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