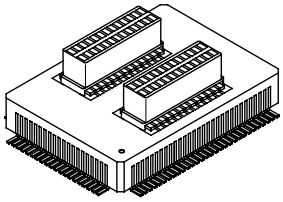
SONY

CXP922000

CMOS 16-bit Single Chip Microcomputer

Piggy/ evaluation type

100 pin PQFP (Ceramic)



(QFP supported)

Description

The CXP922000 is a CMOS 16-bit single chip microcomputer of piggyback/evaluator combined type, which is developed for evaluating the function of the CXP922032.

Features

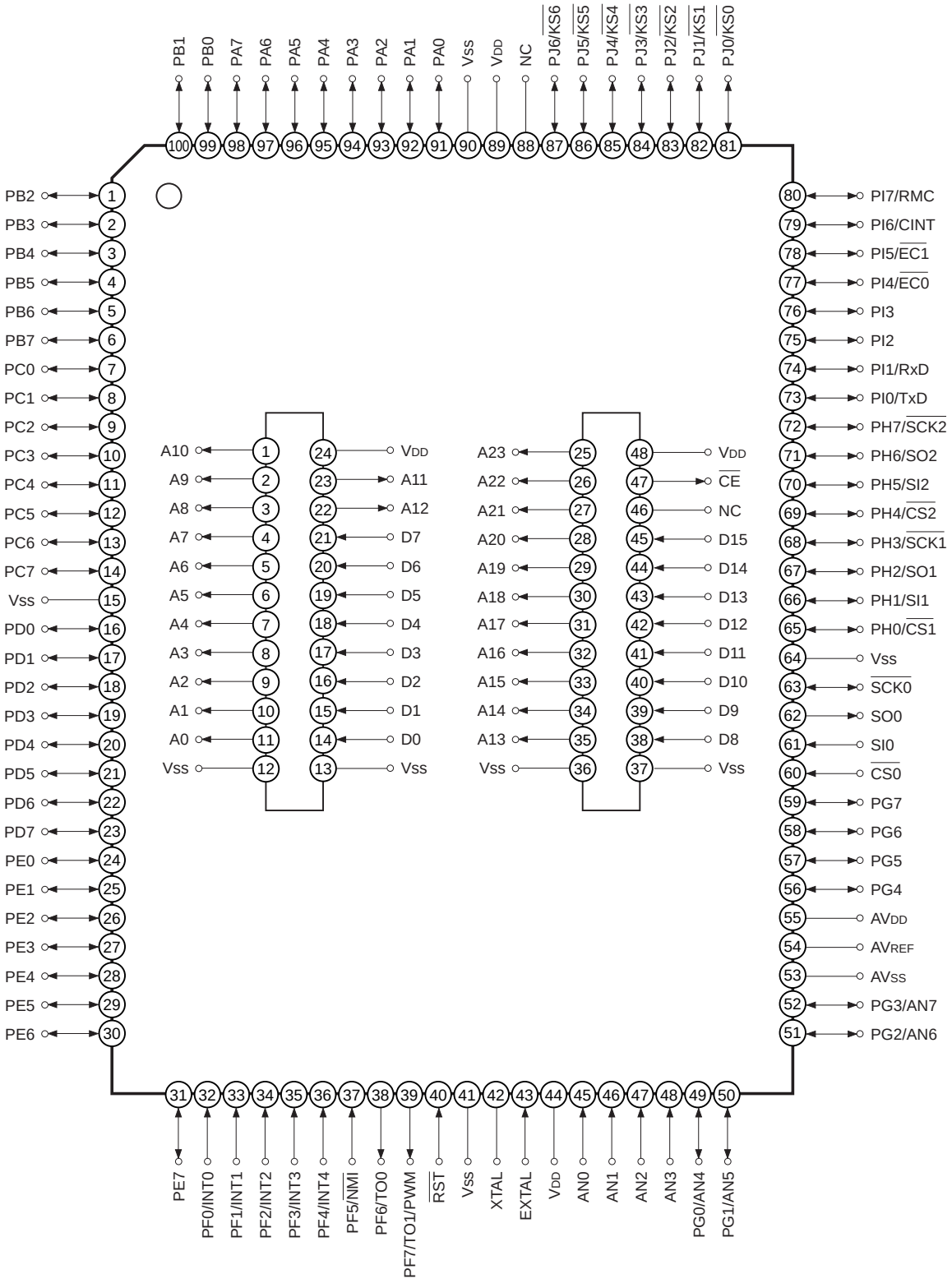
- An efficient instruction set as a controller
  - Direct addressing, numerous abbreviated forms, multiplication and division instructions
- Instruction sets for C language and RTOS
  - Highly quadratic instruction system, general-purpose register of eight 16-bit × 16-bank configuration
- Minimum instruction cycle time 100ns at 20MHz operation (3.0 to 5.5V)
  167ns at 12MHz operation (2.7 to 5.5V)
- Incorporated EPROM CXP27V1000K
- Incorporated RAM capacity 7680 bytes
- Peripheral functions
  - A/D converter 8-bit 8 analog input, successive approximation system (Conversion time: 12.4µs at 20MHz)
  - Serial interface Asynchronous serial interface (Simple UART) 128-byte buffer RAM, 3 channels
  - Timers 8-bit timer/counter, 2 channels (with timing output) 16-bit capture timer/counter (with timing output) 16-bit timer, 4 channels
  - Remote control receive circuit 8-bit pulse measurement counter, 8-stage FIFO
  - PWM output circuit 14-bit, 1 channel
- Interruption 24 factors, 24 vectors, multi-interruption and priority selection possible
- Standby mode Sleep/stop
- Package 100-pin ceramic PQFP
- Mask ROM CXP922032
- One time PROM incorporated type CXP922P032

Structure

Silicon gate CMOS IC

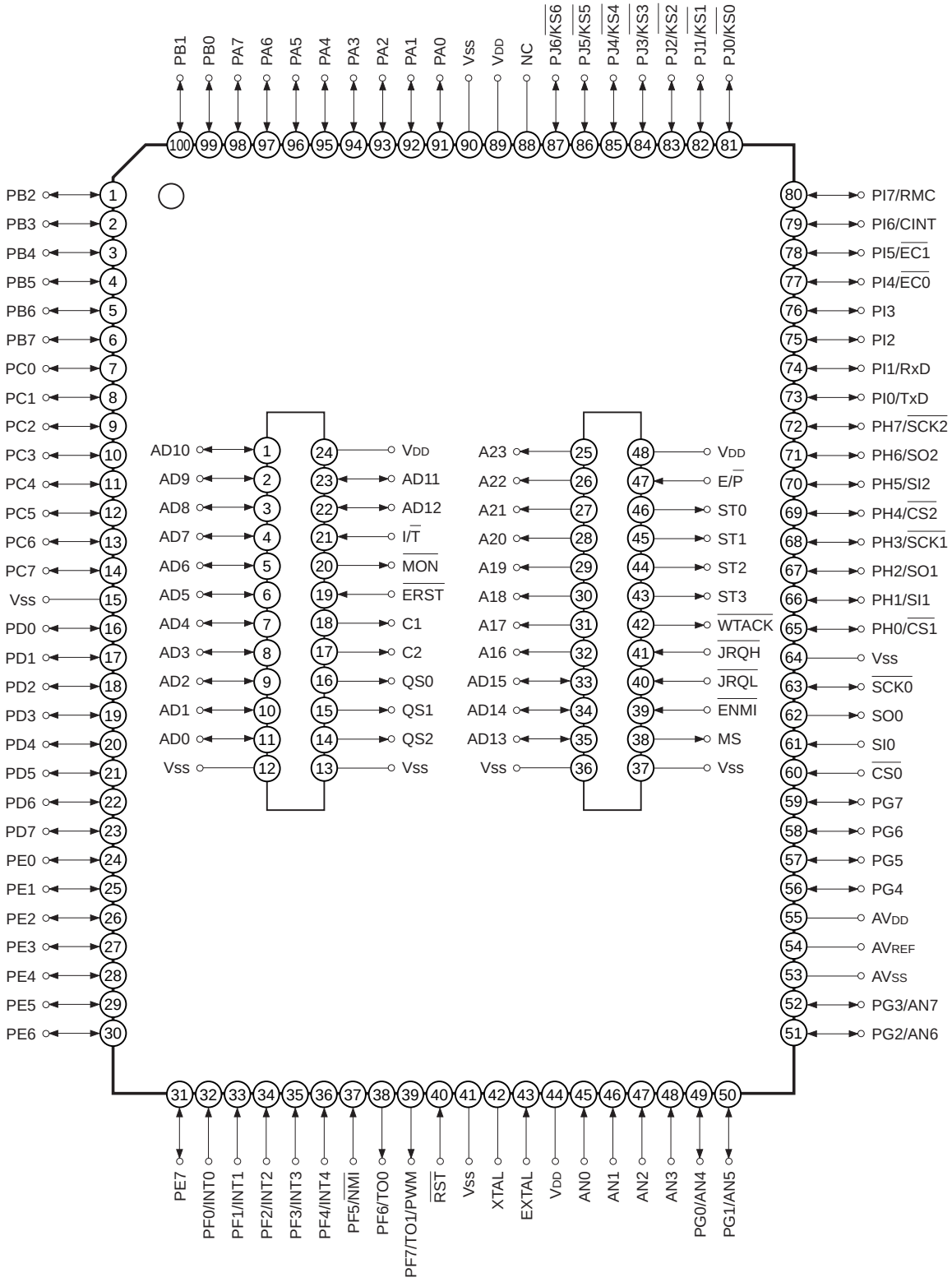
E98Z32B9X-PS

Pin Assignment in Piggyback Mode



Note) 1. Do not make any connections to NC (Pin 88).
2. Vss (Pins 15, 41, 64 and 90) are connected to GND.
3. V_{DD} (Pins 44 and 89) are both connected to V_{DD}.
4. A19 to A23 are always high level output.

Pin Assignment in Evaluator Mode



Note) 1. Do not make any connections to NC (Pin 88).
2. Vss (Pins 15, 41, 64 and 90) are connected to GND.
3. V_{DD} (Pins 44 and 89) are both connected to V_{DD}.

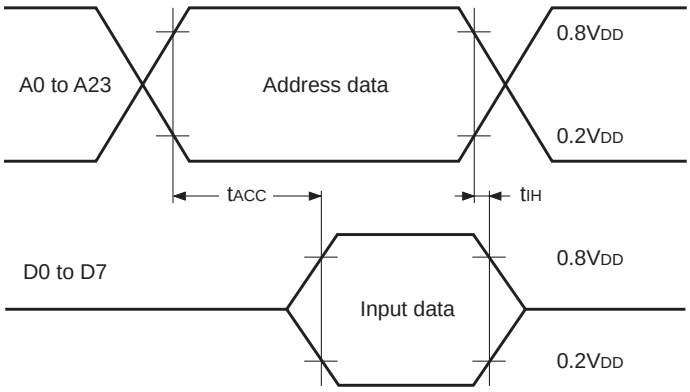
EPROM Read Timing

(Ta = –20 to +75°C, V_{DD} = 2.7 to 5.5V, Vss = 0V)

Item	Symbol	Pins	Min.	Max.	Unit
Address → data Input delay time	t_{ACC}	A0 to A23 D0 to D15		100*1	ns
				50*2	
Address → data hold time	t_{IH}	A0 to A23 D0 to D15	0		ns

*1 At 12MHz operation (V_{DD} = 3.0 to 5.5V)

*2 At 12MHz operation (V_{DD} = 2.7 to 5.5V), at 20MHz operation (V_{DD} = 3.0 to 5.5V)



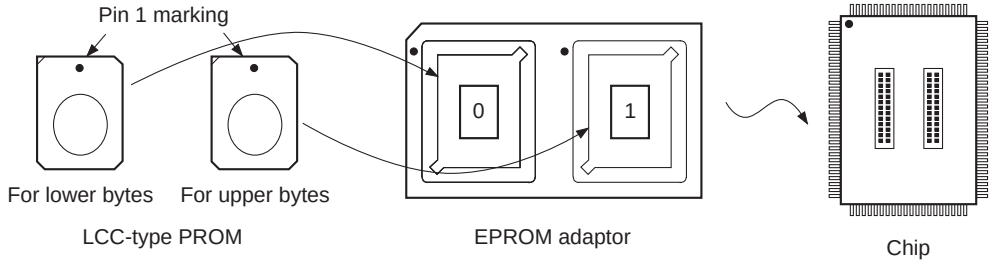
Product List

Optional item	Products	
	Mask ROM	Piggy/evaluation chip
	CXP922032	CXP922000-U01Q
Package	100-pin plastic QFP	100-pin ceramic PQFP (QFP supported)
ROM capacity	128K bytes	EPROM 128K bytes
Reset pin pull-up resistor	Existent/Non-existent	Existent

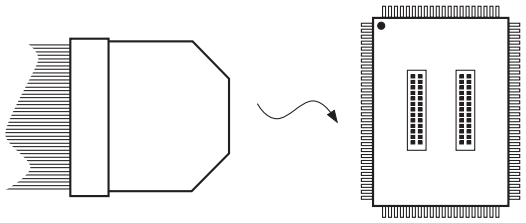
Switching of Piggyback Mode and Evaluator Mode

Piggyback mode can be used by setting two LCC-type EPROM (for upper bytes, for lower byte) and connecting to the connector of top of the chip.
Evaluator mode can be used by connecting in-circuit emulator CPU probe to the connector of top of the chip.

Piggyback mode

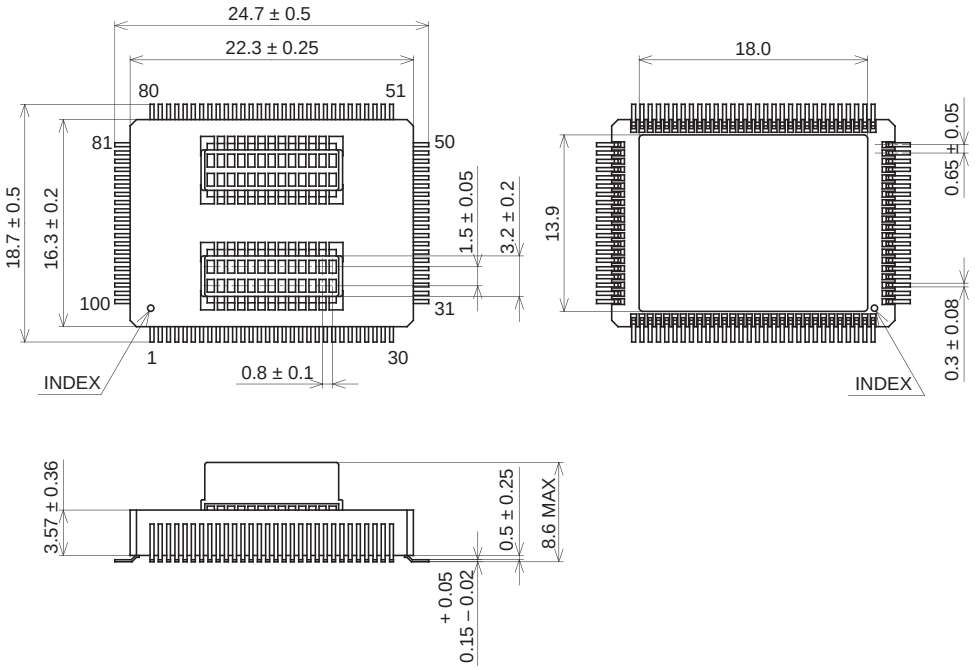


Evaluator mode



Package Outline Unit: mm

100PIN PQFP(CERAMIC)



SONY CODE	PQFP-100C-L04
EIAJ CODE	AQFP100-C-0000
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	CERAMIC
LEAD TREATMENT	GOLD PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE MASS	4.9g