

## Product Summary

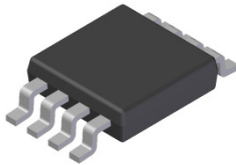
Device	V <sub>(BR)DSS</sub>	R <sub>DS(on)</sub> max	I <sub>D</sub> T <sub>A</sub> = +25°C
Q2	40V	24mΩ @ V <sub>GS</sub> = 10V	6.9A
		32mΩ @ V <sub>GS</sub> = 4.5V	6.0A
Q1	-40V	45mΩ @ V <sub>GS</sub> = -10V	-5.1A
		55mΩ @ V <sub>GS</sub> = -4.5V	-4.5A

## Description

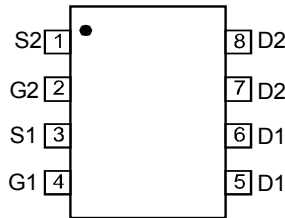
This new generation MOSFET has been designed to minimize the on-state resistance (R<sub>DS(ON)</sub>) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

## Applications

- DC-DC Converters
- Power Management Functions
- Backlighting



Top View



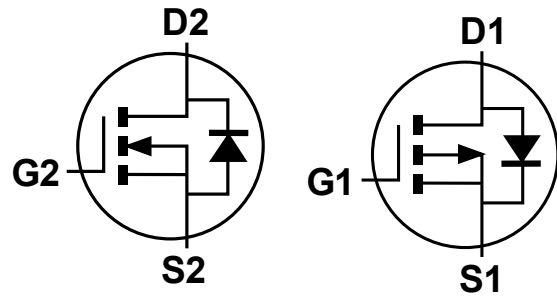
TOP VIEW  
Internal Schematic

## Features and Benefits

- Low Input Capacitance
- Low On-Resistance
- Fast Switching Speed
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **Qualified to AEC-Q101 Standards for High Reliability**

## Mechanical Data

- Case: SO-8
- Case Material: Molded Plastic, "Green" Molding Compound.  
UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections: See Diagram
- Terminals: Finish – Matte Tin annealed over Copper leadframe  
Solderable per MIL-STD-202, Method 208 (e3)
- Weight: 0.074 grams (approximate)



N-Channel MOSFET

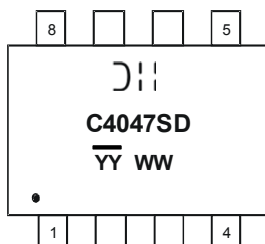
P-Channel MOSFET

## Ordering Information (Note 4)

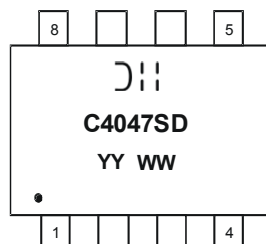
Part Number	Case	Packaging
DMC4047LSD-13	SO-8	2,500/Tape & Reel

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
  2. See [http://www.diodes.com/quality/lead\\_free.html](http://www.diodes.com/quality/lead_free.html) for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
  3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
  4. For packaging details, go to our website at <http://www.diodes.com/products/packages.html>.

## Marking Information



Chengdu A/T Site



Shanghai A/T Site

☺|| = Manufacturer's Marking  
 C4047SD = Product Type Marking Code  
 YYWW = Date Code Marking  
 YY or YY = Year (ex: 13 = 2013)  
 WW = Week (01 - 53)  
 YY = Date Code Marking for SAT (Shanghai Assembly/ Test site)  
 YY = Date Code Marking for CAT (Chengdu Assembly/ Test site)

**Maximum Ratings** (@ $T_A = +25^\circ\text{C}$ , unless otherwise specified.)

Characteristic		Symbol	Value_Q2	Value_Q1	Units
Drain-Source Voltage		$V_{DSS}$	40	-40	V
Gate-Source Voltage		$V_{GSS}$	$\pm 20$	$\pm 20$	V
Continuous Drain Current (Note 6) $V_{GS} = 10\text{V}$	Steady State	$T_A = +25^\circ\text{C}$ $T_A = +70^\circ\text{C}$	$I_D$ 7.0 5.6	-5.1 -4.1	A
	$t < 10\text{s}$	$T_A = +25^\circ\text{C}$ $T_A = +70^\circ\text{C}$	$I_D$ 9.0 7.2	-6.5 -5.2	A
Maximum Body Diode Forward Current (Note 6)		$I_S$	2.5	-2.5	A
Pulsed Drain Current (10 $\mu\text{s}$ pulse, duty cycle = 1%)		$I_{DM}$	70	-40	A
Avalanche Current (Notes 7) $L = 0.1\text{mH}$		$I_{AR}$	20	20	A
Repetitive Avalanche Energy (Notes 7) $L = 0.1\text{mH}$		$E_{AR}$	20	20	mJ

**Thermal Characteristics** (@ $T_A = +25^\circ\text{C}$ , unless otherwise specified.)

Characteristic		Symbol	Value	Units
Total Power Dissipation (Note 5)	$T_A = +25^\circ\text{C}$	$P_D$	1.3	W
	$T_A = +70^\circ\text{C}$		0.8	
Thermal Resistance, Junction to Ambient (Note 5)	Steady state	$R_{\theta JA}$	98	$^\circ\text{C/W}$
	$t < 10\text{s}$		59	
Total Power Dissipation (Note 6)	$T_A = +25^\circ\text{C}$	$P_D$	1.8	W
	$T_A = +70^\circ\text{C}$		1.1	
Thermal Resistance, Junction to Ambient (Note 6)	Steady state	$R_{\theta JA}$	71	$^\circ\text{C/W}$
	$t < 10\text{s}$		43	
Thermal Resistance, Junction to Case (Note 6)		$R_{\theta JC}$	11.8	$^\circ\text{C}$
Operating and Storage Temperature Range		$T_J, T_{STG}$	-55 to +150	$^\circ\text{C}$

**Electrical Characteristics N-Channel Q2** (@ $T_A = +25^\circ\text{C}$ , unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
<b>OFF CHARACTERISTICS (Note 8)</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	40	—	—	V	$V_{GS} = 0\text{V}, I_D = 250\mu\text{A}$
Zero Gate Voltage Drain Current	$I_{DSS}$	—	—	1	$\mu\text{A}$	$V_{DS} = 40\text{V}, V_{GS} = 0\text{V}$
Gate-Source Leakage	$I_{GSS}$	—	—	$\pm 100$	nA	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$
<b>ON CHARACTERISTICS (Note 8)</b>						
Gate Threshold Voltage	$V_{GS(th)}$	1.4	—	2.4	V	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$
Static Drain-Source On-Resistance	$R_{DS(on)}$	—	15	24	m $\Omega$	$V_{GS} = 10\text{V}, I_D = 6\text{A}$
		—	20	32		$V_{GS} = 4.5\text{V}, I_D = 5\text{A}$
Diode Forward Voltage	$V_{SD}$	—	0.7	1.0	V	$V_{GS} = 0\text{V}, I_S = 1.0\text{A}$
<b>DYNAMIC CHARACTERISTICS (Note 9)</b>						
Input Capacitance	$C_{iss}$	—	1060	—	pF	$V_{DS} = 20\text{V}, V_{GS} = 0\text{V}, f = 1.0\text{MHz}$
Output Capacitance	$C_{oss}$	—	84	—		
Reverse Transfer Capacitance	$C_{rss}$	—	58	—		
Gate Resistance	$R_G$	—	1.6	—	$\Omega$	$V_{DS} = 0\text{V}, V_{GS} = 0\text{V}, f = 1.0\text{MHz}$
Total Gate Charge ( $V_{GS} = 4.5\text{V}$ )	$Q_g$	—	8.8	—	nC	$V_{DS} = 20\text{V}, I_D = 8\text{A}$
Total Gate Charge ( $V_{GS} = 10\text{V}$ )	$Q_g$	—	19.1	—		
Gate-Source Charge	$Q_{gs}$	—	3.0	—		
Gate-Drain Charge	$Q_{gd}$	—	2.5	—		
Turn-On Delay Time	$t_{D(on)}$	—	5.3	—	nS	$V_{DD} = 25\text{V}, R_L = 2.5\Omega$ $V_{GS} = 10\text{V}, R_G = 3\Omega$
Turn-On Rise Time	$t_r$	—	7.1	—		
Turn-Off Delay Time	$t_{D(off)}$	—	15.1	—		
Turn-Off Fall Time	$t_f$	—	4.8	—		
Body Diode Reverse Recovery Time	$t_{rr}$	—	10.5	—	nS	$I_F = 8\text{A}, di/dt = 100\text{A}/\mu\text{s}$
Body Diode Reverse Recovery Charge	$Q_{rr}$	—	4.15	—	nC	$I_F = 8\text{A}, di/dt = 100\text{A}/\mu\text{s}$

**Electrical Characteristics P-Channel Q1** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
<b>OFF CHARACTERISTICS (Note 8)</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	-40	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = -250μA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	—	—	-1	μA	V <sub>DS</sub> = -40V, V <sub>GS</sub> = 0V
Gate-Source Leakage	I <sub>GSS</sub>	—	—	±100	nA	V <sub>GS</sub> = ±20V, V <sub>DS</sub> = 0V
<b>ON CHARACTERISTICS (Note 8)</b>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	-1.0	—	-2.2	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250μA
Static Drain-Source On-Resistance	R <sub>DS(ON)</sub>	—	33	45	mΩ	V <sub>GS</sub> = -10V, I <sub>D</sub> = -5A
		—	40	55		V <sub>GS</sub> = -4.5V, I <sub>D</sub> = -4A
Diode Forward Voltage	V <sub>SD</sub>	—	-0.7	-1.0	V	V <sub>GS</sub> = 0V, I <sub>S</sub> = -1.0A
<b>DYNAMIC CHARACTERISTICS (Note 9)</b>						
Input Capacitance	C <sub>iss</sub>	—	1154	—	pF	V <sub>DS</sub> = -20V, V <sub>GS</sub> = 0V f = 1.0MHz
Output Capacitance	C <sub>oss</sub>	—	84	—		
Reverse Transfer Capacitance	C <sub>riss</sub>	—	66	—		
Gate Resistance	R <sub>G</sub>	—	12.6	—	Ω	V <sub>DS</sub> = 0V, V <sub>GS</sub> = 0V, f = 1.0MHz
Total Gate Charge (V <sub>GS</sub> = -4.5V)	Q <sub>g</sub>	—	10.6	—	nC	V <sub>DS</sub> = -20V, I <sub>D</sub> = -4.9A
Total Gate Charge (V <sub>GS</sub> = -10V)	Q <sub>g</sub>	—	21.5	—		
Gate-Source Charge	Q <sub>gs</sub>	—	2.2	—		
Gate-Drain Charge	Q <sub>gd</sub>	—	3.3	—		
Turn-On Delay Time	t <sub>D(on)</sub>	—	8.7	—	nS	V <sub>DS</sub> = -20V, I <sub>D</sub> = -3.9A V <sub>GS</sub> = -4.5V, R <sub>G</sub> = 1Ω
Turn-On Rise Time	t <sub>r</sub>	—	19.6	—		
Turn-Off Delay Time	t <sub>D(off)</sub>	—	34.9	—		
Turn-Off Fall Time	t <sub>f</sub>	—	25.5	—		
Body Diode Reverse Recovery Time	t <sub>rr</sub>	—	9.61	—	nS	I <sub>S</sub> = -3.9A, dI/dt = 100A/μs
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>	—	3.30	—	nC	I <sub>S</sub> = -3.9A, dI/dt = 100A/μs

- Notes:
5. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
  6. Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.
  7. IAR and EAR rating are based on low frequency and duty cycles to keep T<sub>J</sub> = +25°C
  8. Short duration pulse test used to minimize self-heating effect.
  9. Guaranteed by design. Not subject to product testing.

**N-Channel Q2**

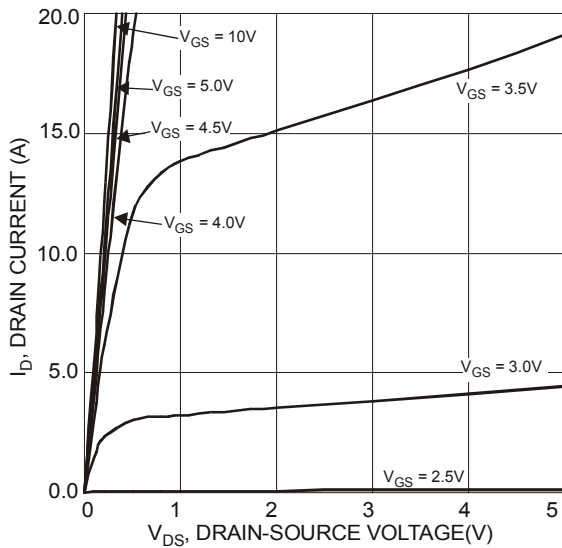


Figure 1 Typical Output Characteristics

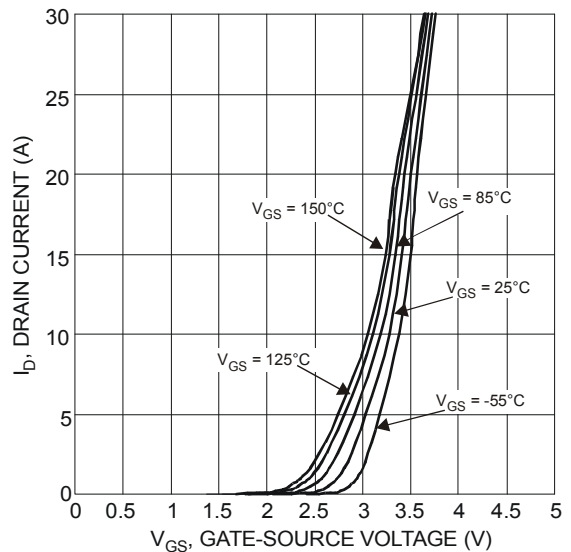


Figure 2 Typical Transfer Characteristics

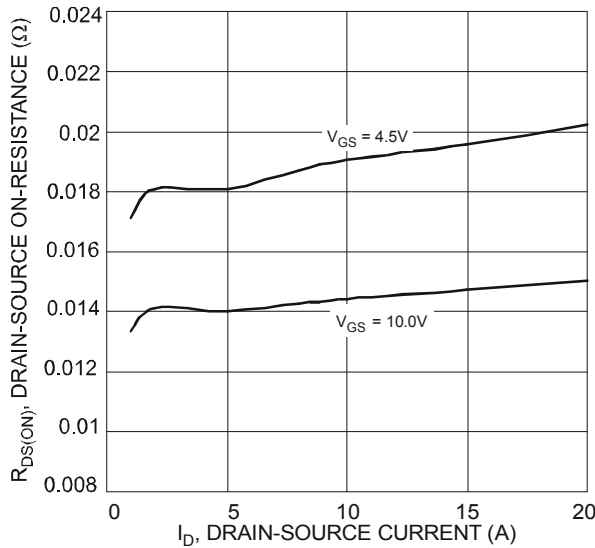


Figure 3 Typical On-Resistance vs. Drain Current and Gate Voltage

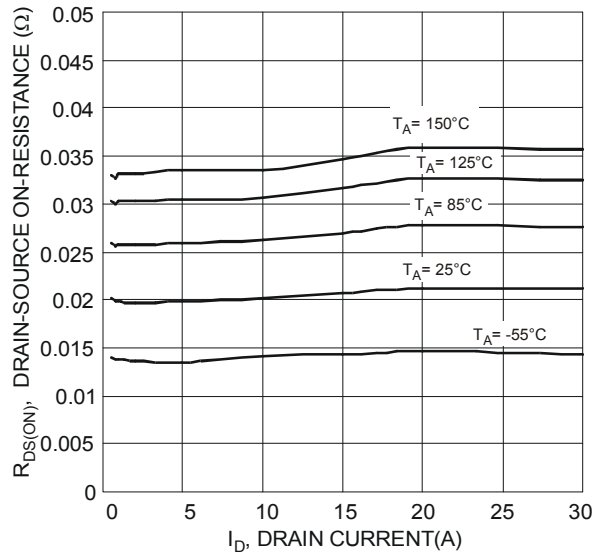


Figure 4 Typical On-Resistance vs. Drain Current and Temperature

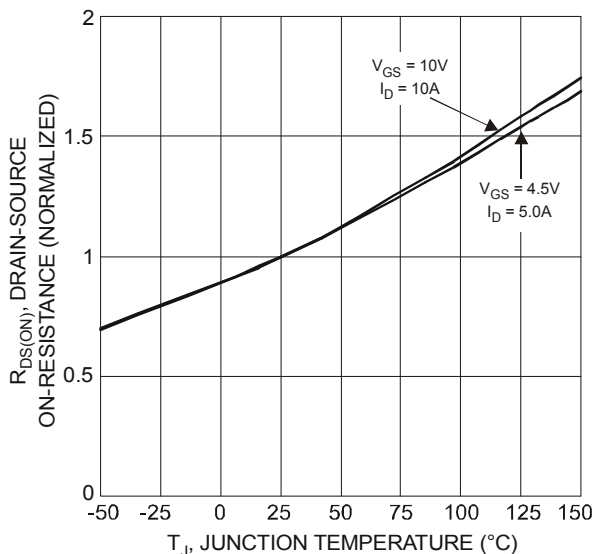


Figure 5 On-Resistance Variation with Temperature

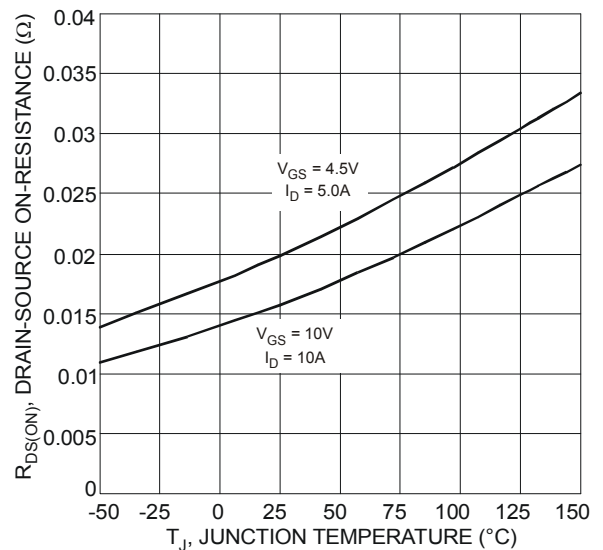


Figure 6 On-Resistance Variation with Temperature

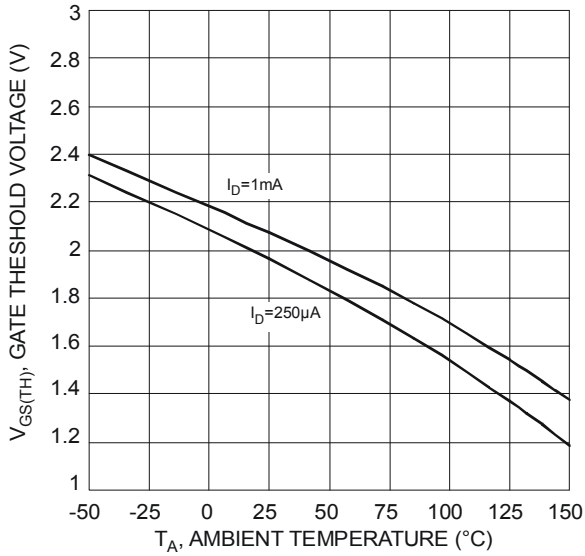


Figure 7 Gate Threshold Variation vs Ambient Temperature

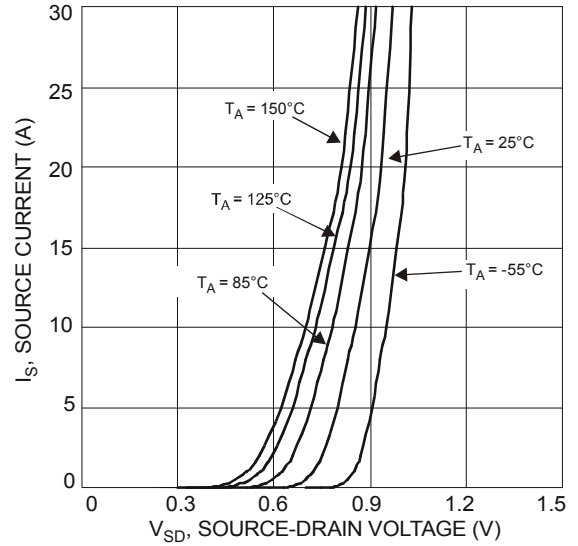


Figure 8 Diode Forward Voltage vs. Current

**P-Channel Q1**

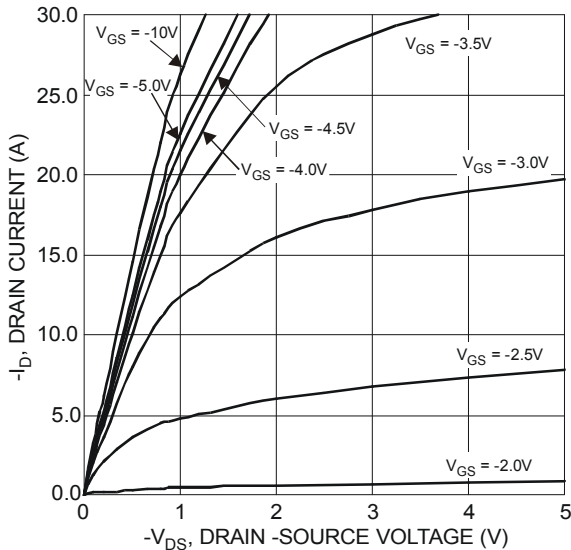


Figure 9 Typical Output Characteristics

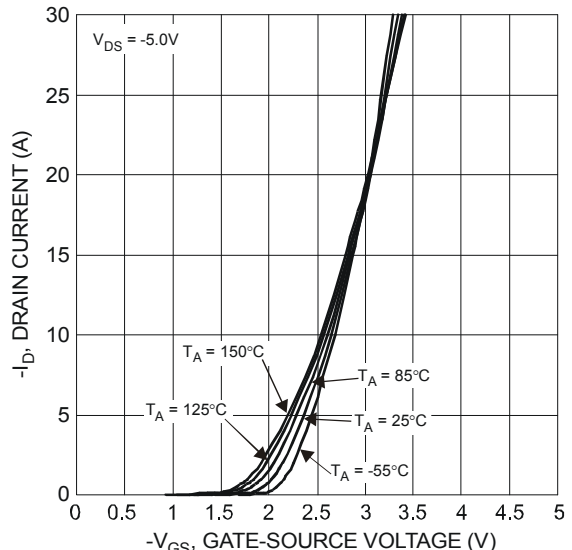


Figure 10 Typical Transfer Characteristics

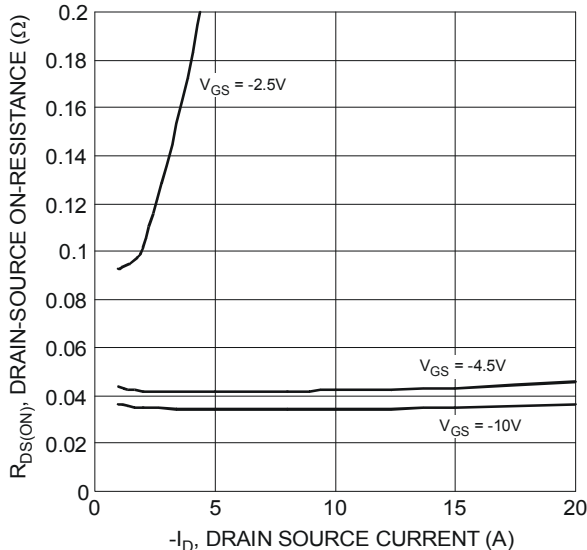


Figure 11 Typical On-Resistance vs. Drain Current and Gate Voltage

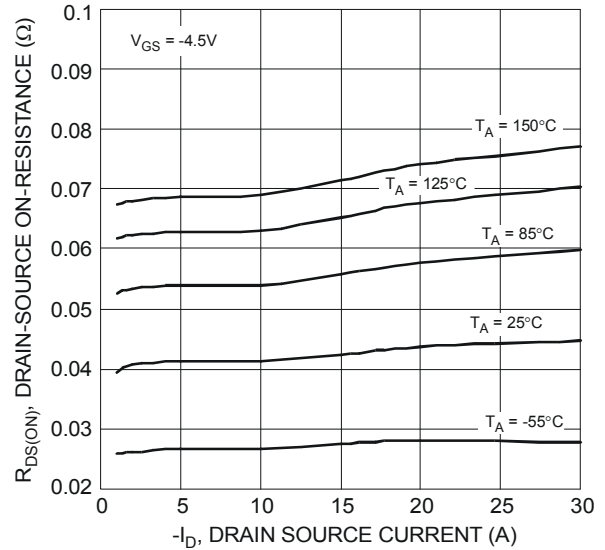


Figure 12 Typical On-Resistance vs. Drain Current and Temperature

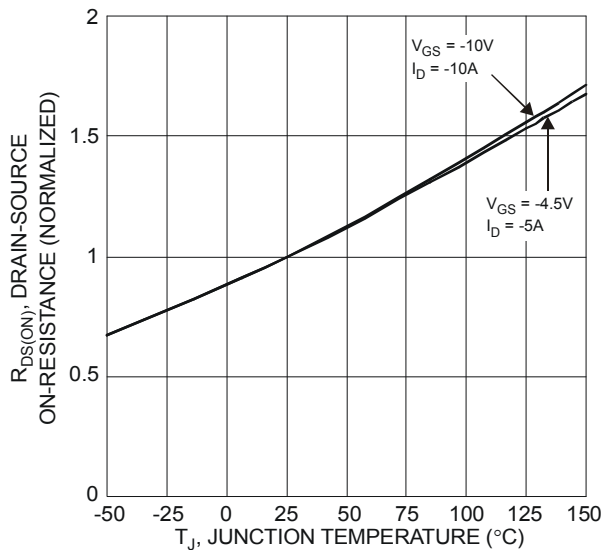


Figure 13 On-Resistance Variation with Temperature

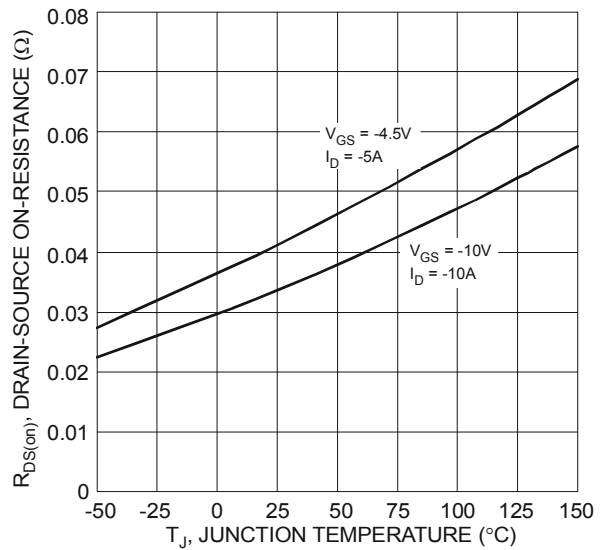


Figure 14 On-Resistance Variation with Temperature

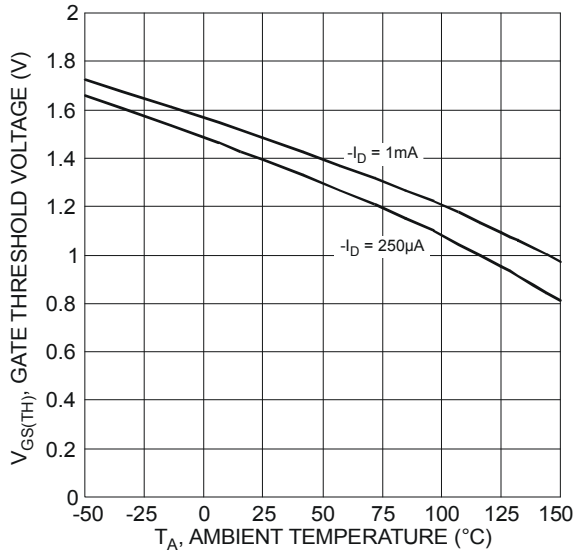


Figure 15 Gate Threshold Variation vs. Ambient Temperature

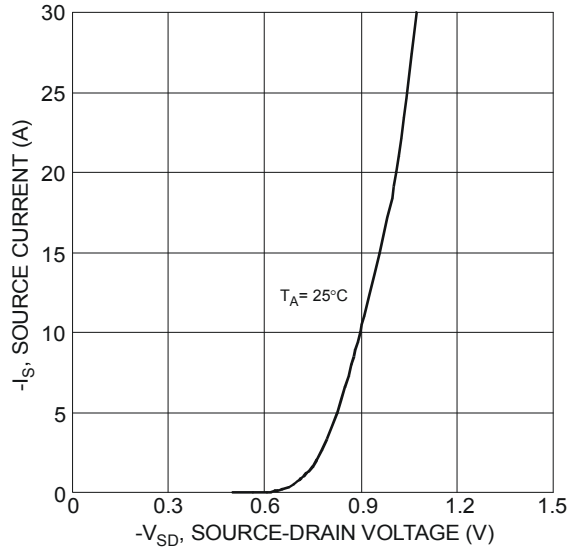


Figure 16 Diode Forward Voltage vs. Current

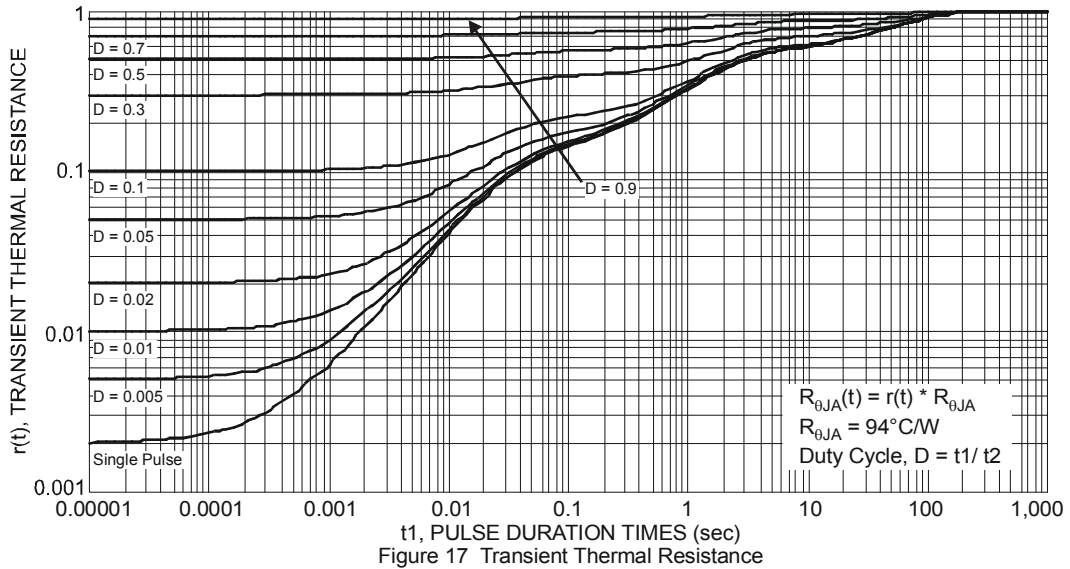
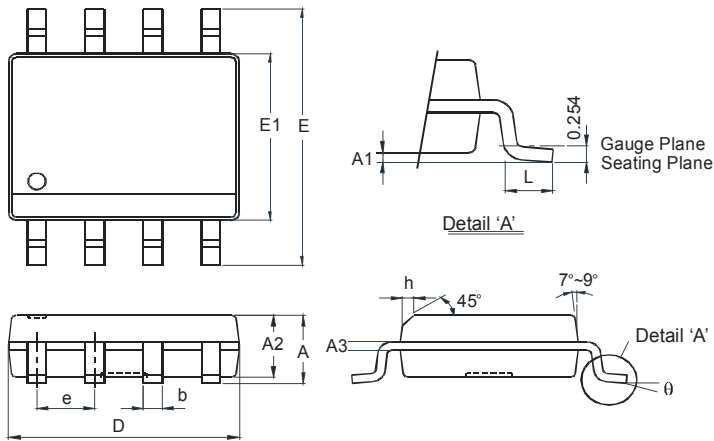


Figure 17 Transient Thermal Resistance

## Package Outline Dimensions

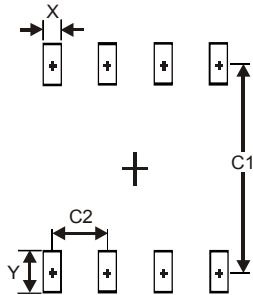
Please see AP02002 at <http://www.diodes.com/datasheets/ap02002.pdf> for latest version.



SO-8		
Dim	Min	Max
A	-	1.75
A1	0.10	0.20
A2	1.30	1.50
A3	0.15	0.25
b	0.3	0.5
D	4.85	4.95
E	5.90	6.10
E1	3.85	3.95
e	1.27 Typ	
h	-	0.35
L	0.62	0.82
$\theta$	0°	8°
All Dimensions in mm		

## Suggested Pad Layout

Please see AP02001 at <http://www.diodes.com/datasheets/ap02001.pdf> for the latest version.



Dimensions	Value (in mm)
X	0.60
Y	1.55
C1	5.4
C2	1.27



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