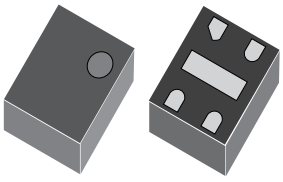
ESDAVLC8-4BN4

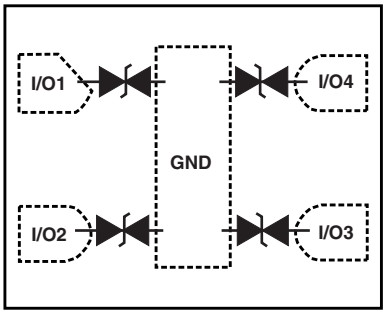
4-line very low capacitance Transil™ array for ESD protection

Datasheet – production data



µQFN-4L

Figure 1. Functional diagram (top view)



Features

- Stand-off voltage: 3 V
- Very low capacitance: 4.5 pF
- Small package: 1.0 x 0.8 mm
- Very thin package: 0.40 mm max
- Low leakage current: 50 nA at 25 °C

Benefits

- High ESD robustness of the equipment
- Suitable for high speed interface

Complies with the following standards:

- IEC 61000-4-2:
  - ±15 kV (air discharge)
  - ±8 kV (contact discharge)
- MIL STD 883G- Method 3015-7: class3B:
  - >25 kV (human body model)

Applications

Where transient overvoltage protection and electrical overstress protection in sensitive equipment is required, such as:

- Communication systems
- Cellular phone handsets and accessories
- Video equipment

Description

The ESDAVLC8-4BN4 is monolithic array designed to protect up to 4 lines against ESD transients. It has been designed specifically for the protection of the high speed interface of integrated circuits in portable equipment and miniaturized electronics devices. The µQFN-4L package minimizes PCB space.

TM: Transil is a trademark of STMicroelectronics.

1 Characteristics

Table 1. Absolute maximum ratings (T_{amb} = 25 °C)

Symbol	Parameter		Value	Unit
V_{PP}	Peak pulse voltage, IEC 61000-4-2, level 4 (contact discharge)		16	kV
P_{PP}	Peak pulse power dissipation (8/20 µs)(1) T_j initial = T_{amb}	GND to I/O I/O to GND	45 32	W
I_{pp}	Peak pulse current (8/20 µs)		1.6	A
T_j	Maximum junction temperature range		-40 to 125	°C
T_{stg}	Storage temperature range		-55 + 150	°C

1. For a surge greater than the maximum values, the diode will fail in short-circuit.

Figure 2. Electrical characteristics (definitions)

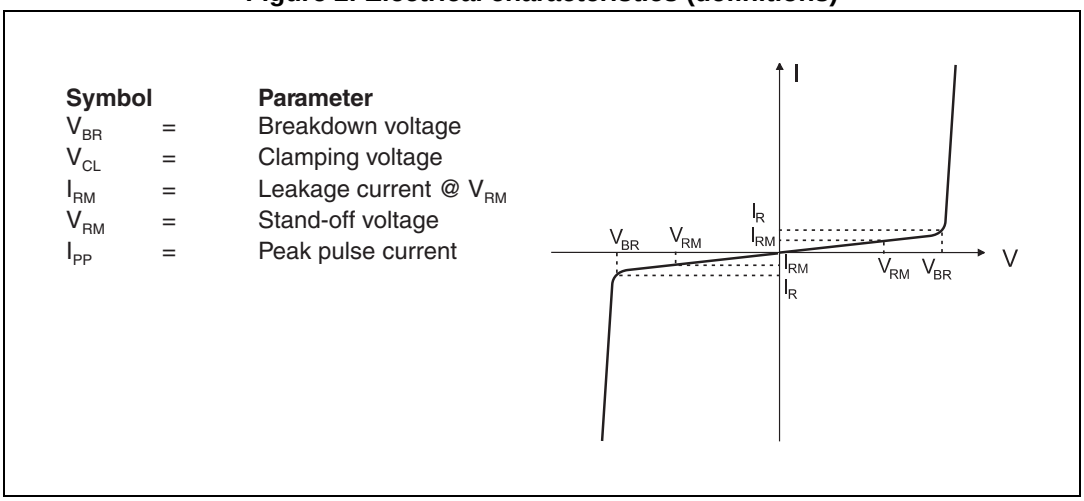


Table 2. Electrical characteristics (values, T_{amb} = 25 °C)

Symbol	Test conditions		Min.	Typ.	Max.	Unit
V_{BR1}	I_R = 1 mA, GND to I/O		8.5	11	14	V
V_{BR2}	I_R = 1 mA, I/O to GND		14.5	17	20	V
I_{RM}	V_{RM} = 3 V				50	nA
V_{CL}	I_{pp} = 1 A, 8/20 µs, GND to I/O				20	V
	I_{pp} = 1 A, 8/20 µs, I/O to GND				28	
C	$V_{I/O}$ = 0 V, F = 1 MHz, V_{osc} = 30 mV			4.5	5.5	pF
R_d	Dynamic resistance, pulse width 100 ns	I/O to GND		0.36		Ω
		GND to I/O		0.28		

Note: For component test in its final application, the minimum clamping voltage has to be 20 V on V_{BR1} (GND to I/O) and 25 V on V_{BR2} (I/O to GND).

Figure 3. Peak pulse power versus initial junction temperature (8/20 µs waveform)

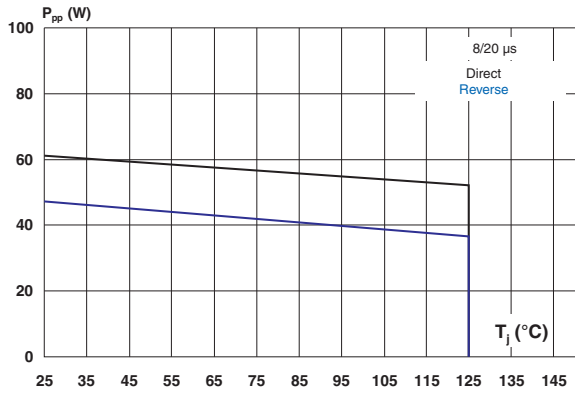


Figure 4. Peak pulse power versus exponential pulse duration

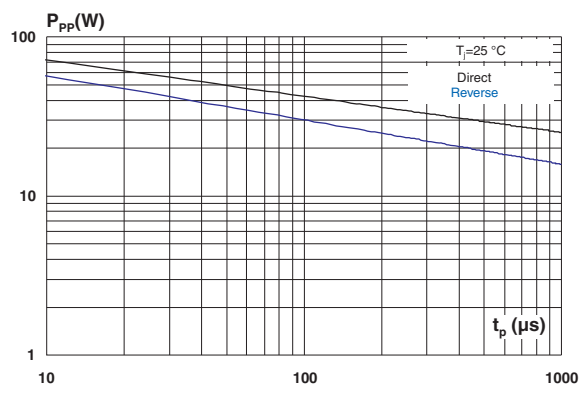


Figure 5. Clamping voltage versus peak pulse current (typical values, 8/20 µs waveform)

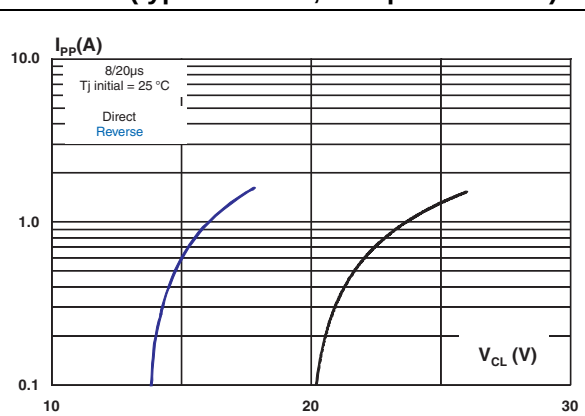


Figure 6. Junction capacitance versus reverse voltage applied (typical values)

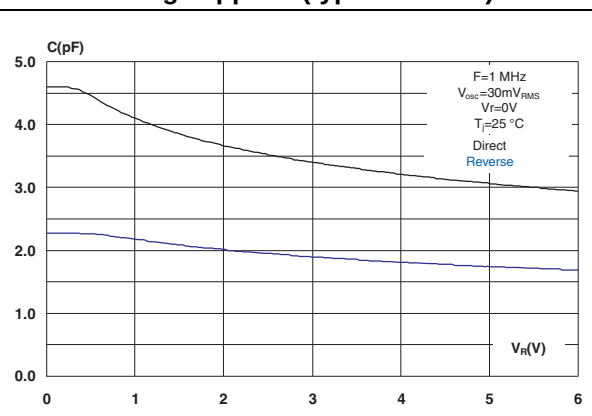


Figure 7. ESD response to IEC 61000-4-2 (+8 kV contact discharge) on each channel

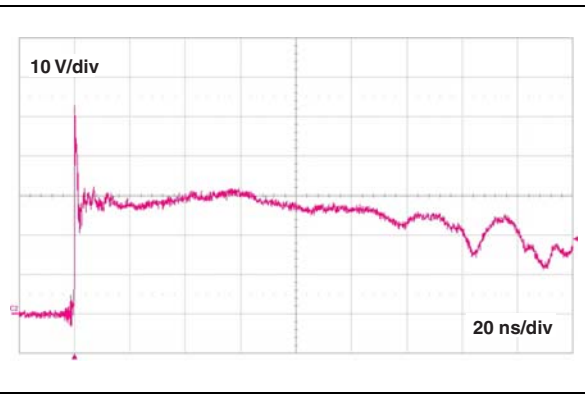


Figure 8. ESD response to IEC 61000-4-2 (-8 kV contact discharge) on each channel

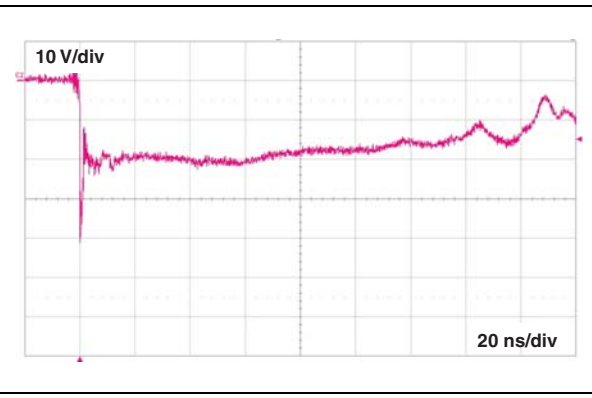


Figure 9. S21 attenuation measurement

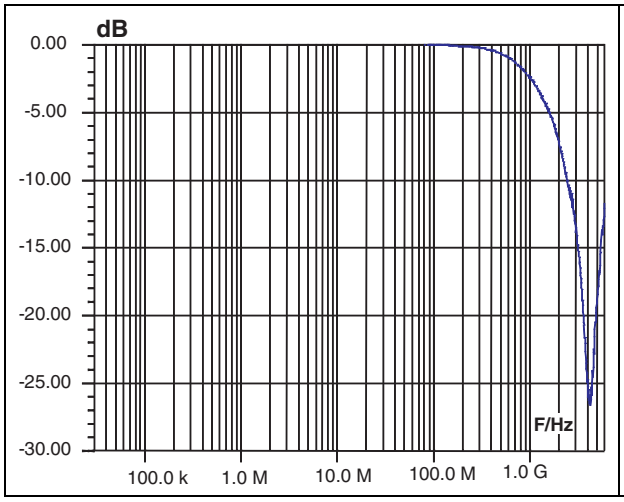


Figure 10. Analog crosstalk measurement

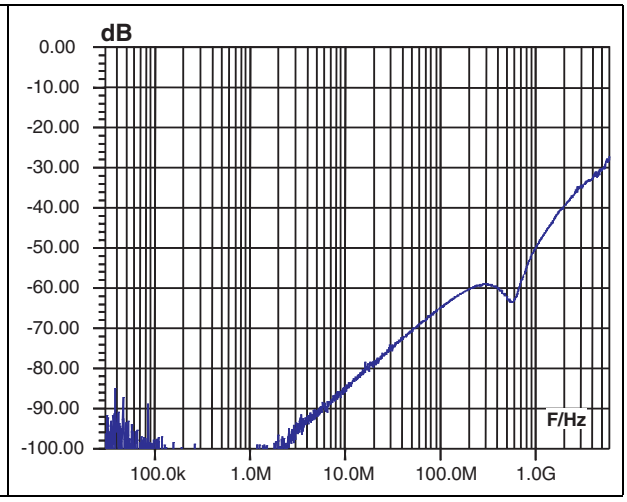


Figure 11. Leakage current versus junction temperature (typical values)

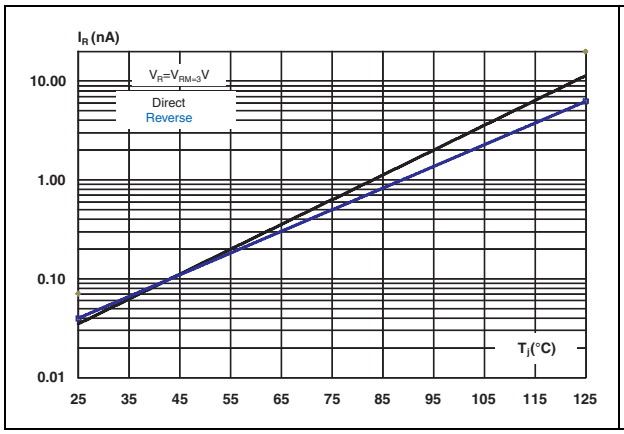
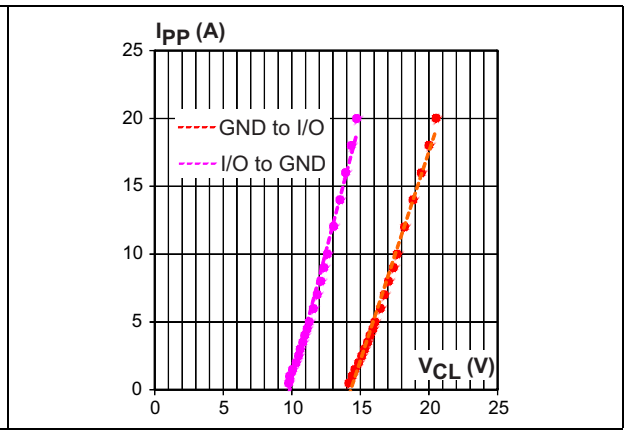


Figure 12. TLP measurement



2 Package information

- Epoxy meets UL94, V0
- Lead-free package

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com.* ECOPACK® is an ST trademark.

Figure 13. µQFN-4L dimension definitions

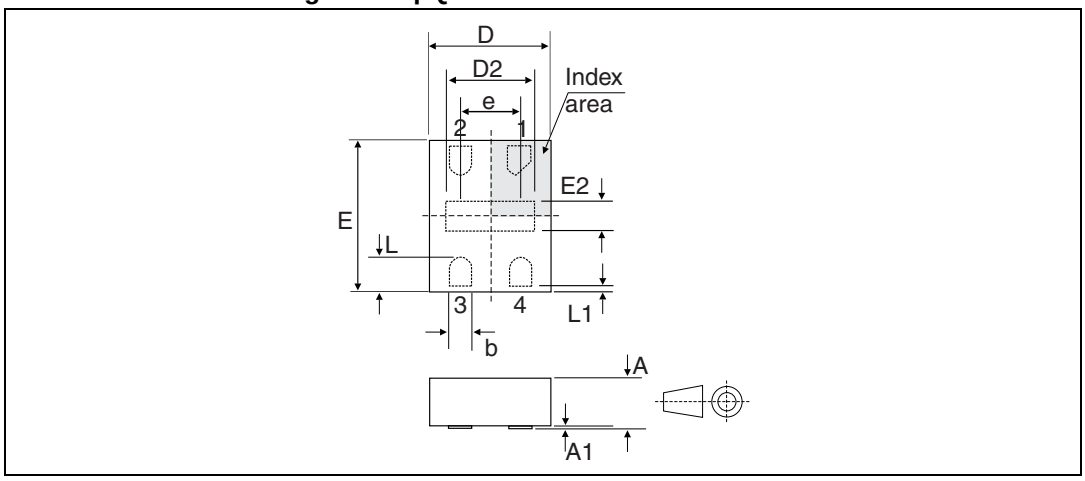


Table 3. µQFN-4L dimension values

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.31	0.38	0.40	0.012	0.015	0.016
A1	0.00	0.02	0.05	0.00	0.0008	0.002
b	0.10	0.15	0.20	0.004	0.006	0.008
D	0.70	0.80	0.90	0.028	0.031	0.035
D2	0.50	0.58	0.65	0.020	0.023	0.026
e	0.35	0.40	0.45	0.014	0.016	0.018
E	0.90	1.00	1.10	0.035	0.039	0.043
E2	0.15	0.20	0.25	0.006	0.008	0.010
L	0.18	0.23	0.28	0.007	0.009	0.011
L1	0.00	--	0.05	0.00	--	0.002

Figure 14. Footprint dimensions (in mm)

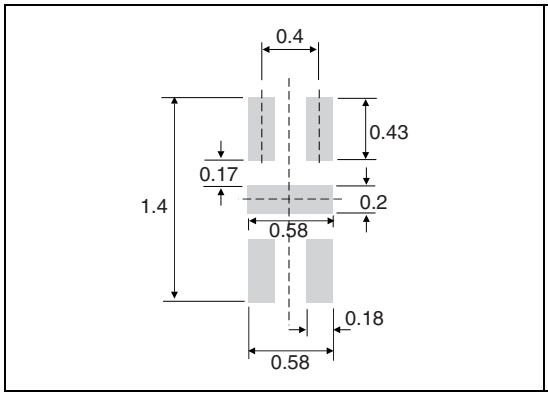
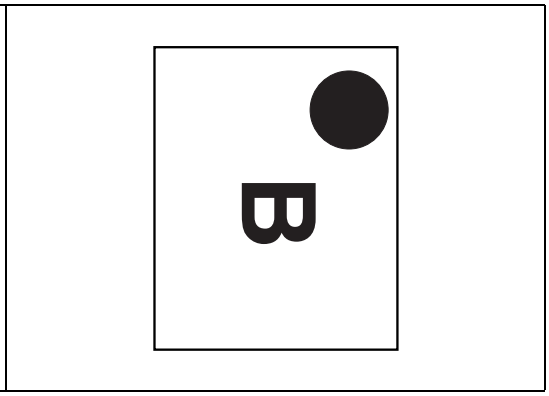
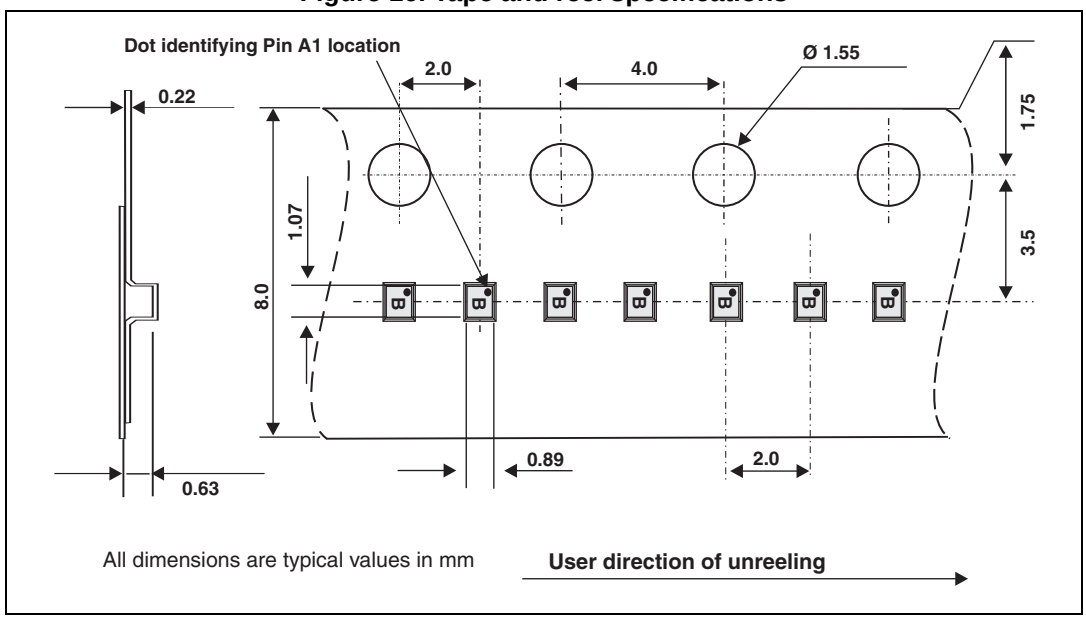


Figure 15. Marking



Note: Product marking may be rotated by multiples of 90° for assembly plant differentiation. In no case should this product marking be used to orient the component for its placement on a PCB. Only pin 1 mark is to be used for this purpose.

Figure 16. Tape and reel specifications



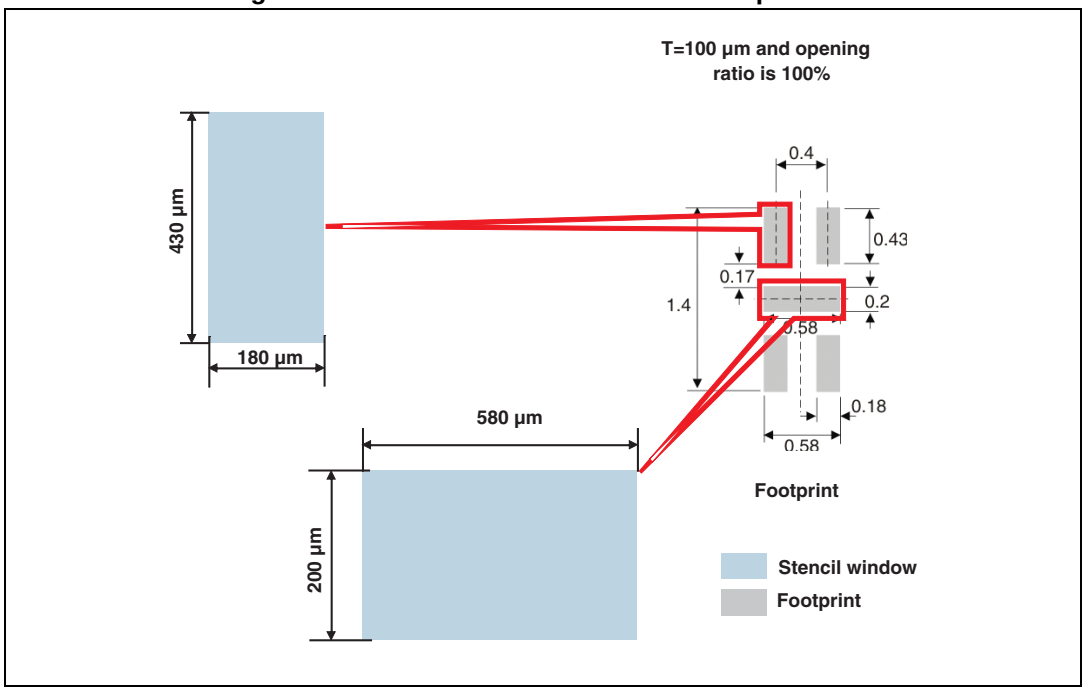
3 Recommendation on PCB assembly

3.1 Stencil opening design

Reference design

- Stencil opening thickness: 100 µm
- Stencil opening for leads: Opening to footprint ratio is 100%.

Figure 17. Recommended stencil window position



3.2 Solder paste

1. Halide-free flux qualification ROL0 according to ANSI/J-STD-004.
2. “No clean” solder paste is recommended.
3. Offers a high tack force to resist component movement during high speed.
4. Solder paste with fine particles: powder particle size is 20-45 µm.

3.3 Placement

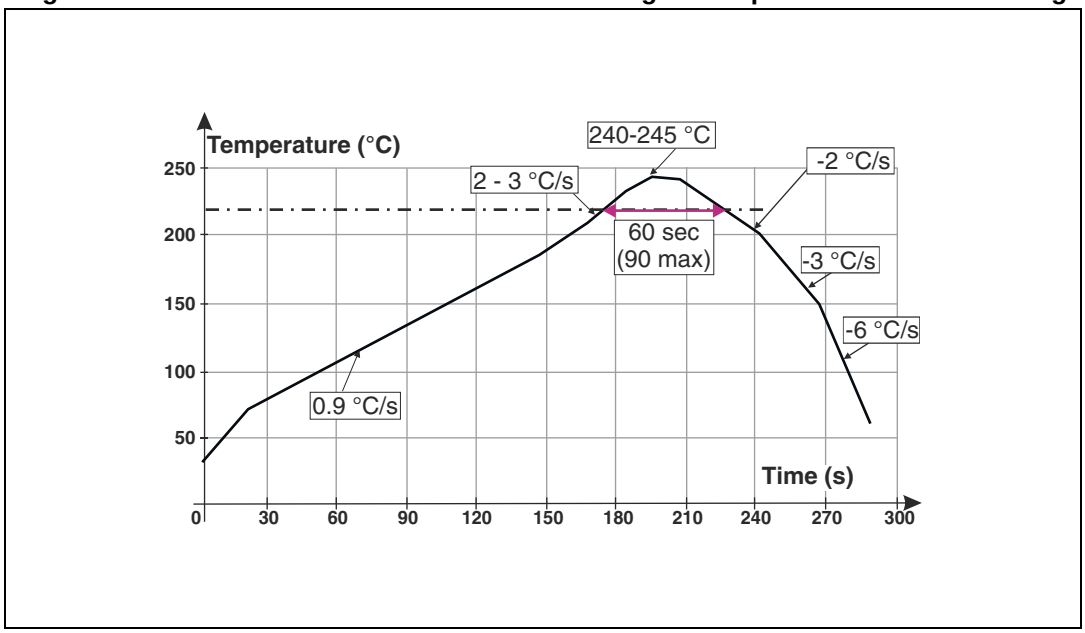
1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering.
3. Standard tolerance of ± 0.05 mm is recommended.
4. 3.5 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

3.4 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. The symmetrical layout is recommended, in case any tilt phenomena caused by asymmetrical solder paste amount due to the solder flow away.

3.5 Reflow profile

Figure 18. ST ECOPACK® recommended soldering reflow profile for PCB mounting



Note: Minimize air convection currents in the reflow oven to avoid component movement.

4 Ordering information

Figure 19. Ordering information scheme

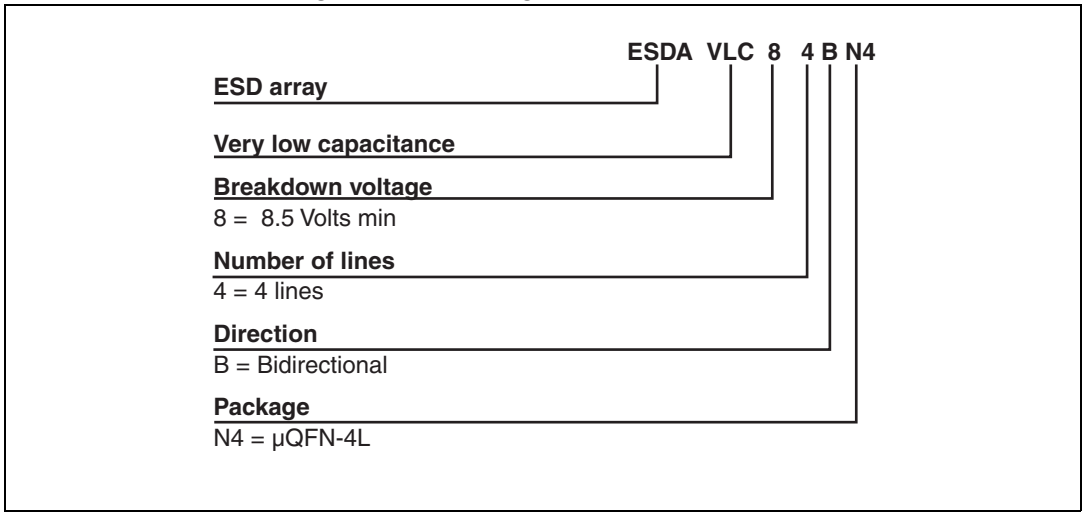


Table 4. Ordering information

Order code	Marking	Package	Weight	Base qty	Delivery mode
ESDAVLC8-4BN4	B(1)	µQFN-4L	1.17 mg	10000	Tape and reel

1. The marking can be rotated by multiples of 90° to differentiate assembly location

5 Revision history

Table 5. Document revision history

Date	Revision	Changes
06-Sep-2011	1	Initial release.
25-Sep-2012	2	Updated ECOPACK statement.
25-Mar-2014	3	For *Table 2* added maximum values for V_{BR1} and V_{BR2}, and the note following the table.Updated values for dynamic resistance in *Table 2* and added *Figure 12*.

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