

# EUROTECHNIQUE

## ET9420/9421/9422 and ET9320/9321/9322 Single-Chip N-Channel Microcontrollers

### General Description

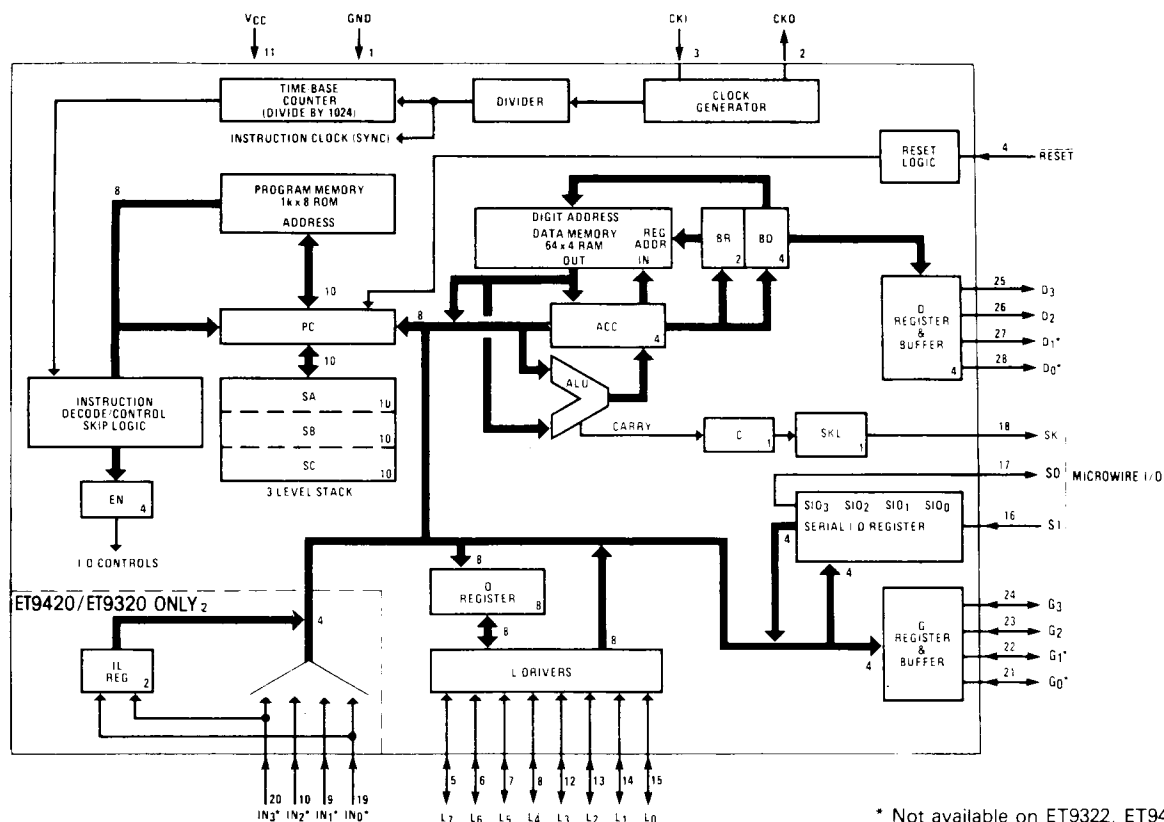
The ET9420/9421/9422, ET9320/9321 and 9322 Single-Chip N-Channel Microcontrollers are fully compatible with the COPS™ family, fabricated using N-channel, silicon gate X MOS technology. They are complete microcomputers containing all system timing, internal logic, ROM, RAM and I/O necessary to implement dedicated control functions in a variety of applications. Features include single supply operation, a variety of output configuration options, with an instruction set, internal architecture and I/O scheme designed to facilitate keyboard input, display output and BCD data manipulation. The ET9421 is identical to the ET9420, except with 19 I/O lines instead of 23; the ET9422 has 15 I/O lines. They are an appropriate choice for use in numerous human interface control environments. Standard test procedures and reliable high-density fabrication techniques provide the medium to large volume customers with a customized Controller Oriented Processor at a low end-product cost.

The ET9320 is the extended temperature range version of the ET9420 (likewise the ET9321 and ET9322 are the extended temperature range versions of the ET9421/ET9422). The ET9320/9321/9322 are exact functional equivalents of the ET9420/9421/9422.

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### Features

- Low cost
- Powerful instruction set
- 1k × 8 ROM, 64 × 4 RAM
- 23 I/O lines (ET9420, ET9320)
- True vectored interrupt, plus restart
- Three-level subroutine stack
- 4.0 μs instruction time
- Single supply operation
- Internal time-base counter for real-time processing
- Internal binary counter register with MICROWIRE™ compatible serial I/O capability
- General purpose and TRI-STATE® outputs
- TTL/CMOS compatible in and out
- LED direct drive outputs
- MICROBUS™ compatible
- Software/hardware compatible with other members of ET9400
- Extended temperature range device ET9320/9321/9322 (- 40° C to + 85° C)



\* Not available on ET9322, ET9422.

Figure 1. ET9420/9421/9422, ET9320/9321/9322 Block Diagram

## ET9420/9421/9422 and ET9320/9321/9322

### Absolute Maximum Ratings

|   |                 |  |  |
|---|-----------------|--|--|
| Voltage at Any Pin                              | -0.3V to +7V    | Package Power Dissipation<br>24 and 28 pin | 750 mW at 25°C<br>400 mW at 70°C<br>250 mW at 85°C |
| Operating Temperature Range<br>ET9420/9421/9422 | 0°C to 70°C     | Package Power Dissipation<br>20 pin        | 650 mW at 25°C<br>300 mW at 70°C<br>200 mW at 85°C |
| ET9320/9321/9322                                | -40°C to +85°C  |  |  |
| Storage Temperature Range                       | -65°C to +150°C |  |  |
| Total Sink Current                              | 75 mA           |  |  |
| Total Source Current                            | 95 mA           | Lead Temperature (soldering, 10 sec.)      | 300°C  |

Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not ensured when operating the device at absolute maximum ratings.

### ET9420/9421/9422

#### DC Electrical Characteristics $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$ , $4.5\text{V} \leq V_{CC} \leq 6.3\text{V}$ unless otherwise noted.

| Parameter                     | Conditions   | Min.         | Max. | Units         |
|-------------------------------|--|--------------|------|---------------|
| Operation Voltage             |  | 4.5          | 6.3  | V             |
| Power Supply Ripple           | Peak to Peak (Note 3)  |              | 0.4  | V             |
| Supply Current                | Outputs Open   |              | 38   | mA            |
| Supply Current                | Outputs Open,<br>$V_{CC} = 5\text{V}$ , $T_A = 25^{\circ}\text{C}$ |              | 30   | mA            |
| Input Voltage Levels          |  |              |      |               |
| CKI Input Levels              |  |              |      |               |
| Crystal Input                 |  |              |      |               |
| Logic High                    | $V_{CC} = \text{Max.}$   | 3.0          |      | V             |
| Logic High                    | $V_{CC} = 5\text{V} \pm 5\%$                                       | 2.0          |      | V             |
| Logic Low                     |  | -0.3         | 0.4  | V             |
| TTL Input                     | $V_{CC} = 5\text{V} \pm 5\%$                                       |              |      |               |
| Logic High                    |  | 2.0          |      | V             |
| Logic Low                     |  | -0.3         | 0.8  | V             |
| Schmitt Trigger Inputs        |  |              |      |               |
| RESET, CKI ( $\div 4$ )       |  |              |      |               |
| Logic High                    |  | $0.7 V_{CC}$ |      | V             |
| Logic Low                     |  | -0.3         | 0.6  | V             |
| SO Input Level (Test Mode)    |  | 2.0          | 3.0  | V             |
| All Other Inputs              |  |              |      |               |
| Logic High                    | $V_{CC} = \text{Max.}$   | 3.0          |      | V             |
| Logic High                    | $V_{CC} = 5\text{V} \pm 5\%$                                       | 2.0          |      | V             |
| Logic Low                     |  | -0.3         | 0.8  | V             |
| Input Levels High Trip Option |  |              |      |               |
| Logic High                    |  | 3.6          |      | V             |
| Logic Low                     |  | -0.3         | 1.2  | V             |
| Input Load Source Current     | $V_{CC} = 5\text{V}$ , $V_{IN} = 0\text{V}$                        |              |      |               |
| CKO                           |  | -4           | -800 | $\mu\text{A}$ |
| All Others                    |  | -100         | -800 | $\mu\text{A}$ |
| Input Capacitance             |  |              | 7    | pF            |
| Hi-Z Input Leakage            | $V_{CC} = 5\text{V}$   | -1           | +1   | $\mu\text{A}$ |
| Output Voltage levels         |  |              |      |               |
| Standard Outputs              |  |              |      |               |
| TTL Operation                 | $V_{CC} = 5\text{V} \pm 5\%$                                       |              |      |               |
| Logic High                    | $I_{OH} = -100\mu\text{A}$   | 2.4          |      | V             |
| Logic Low                     | $I_{OL} = 1.6\text{mA}$  | -0.3         | 0.4  | V             |
| CMOS Operation                |  |              |      |               |
| Logic High                    | $I_{OH} = -10\mu\text{A}$  | $V_{CC} - 1$ |      | V             |

# ET9420/9421/9422

## DC Electrical Characteristics (Cont'd) $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$ , $4.5\text{V} \leq V_{CC} \leq 6.3\text{V}$ unless otherwise noted.

| Parameter                                | Conditions   | Min.         | Max.         | Units                          |
|--|--|--------------|--------------|--------------------------------|
| Output Current Levels                    |  |              |              |                                |
| LED Direct Drive Output                  | $V_{CC} = 6\text{V}$   |              |              |                                |
| Logic High                               | $V_{OH} = 2.0\text{V}$   | 2.5          | 14           | mA                             |
| CKI Sink Current (R/C Option)            | $V_{IN} = 3.5\text{V}$   | 2            |              | mA                             |
| CKO (RAM Supply Current)                 | $V_R = 3.3\text{V}$  |              | 3            | mA                             |
| TRI-STATE® or Open Drain Leakage Current | $V_{CC} = 5\text{V}$   | -2.5         | +2.5         | $\mu\text{A}$                  |
| Output Current Levels                    |  |              |              |                                |
| Output Sink Current ( $I_{OL}$ )         | $V_{CC} = 6.3\text{V}, V_{OL} = 0.4\text{V}$<br>$V_{CC} = 4.5\text{V}, V_{OL} = 0.4\text{V}$ | -2.0<br>-1.0 |              | mA                             |
| Output Source Current ( $I_{OH}$ )       |  |              |              |                                |
| Standard Configuration                   |  |              |              |                                |
| All Outputs                              | $V_{CC} = 6.3\text{V}, V_{OH} = 3.0\text{V}$<br>$V_{CC} = 4.5\text{V}, V_{OH} = 2.0\text{V}$ | -200<br>-100 | -900<br>-500 | $\mu\text{A}$<br>$\mu\text{A}$ |
| Push-Pull Configuration                  |  |              |              |                                |
| SO, SK Outputs                           | $V_{CC} = 6.3\text{V}, V_{OH} = 3.0\text{V}$<br>$V_{CC} = 4.5\text{V}, V_{OH} = 2.0\text{V}$ | -1.0<br>-0.4 |              | mA<br>mA                       |
| TRI-STATE Configuration                  |  |              |              |                                |
| L <sub>0</sub> -L <sub>7</sub> Outputs   | $V_{CC} = 6.3\text{V}, V_{OH} = 3.0\text{V}$<br>$V_{CC} = 4.5\text{V}, V_{OH} = 2.0\text{V}$ | -2.0<br>-0.8 |              | mA<br>mA                       |
| LED Configuration                        |  |              |              |                                |
| L <sub>0</sub> -L <sub>7</sub> Outputs   | $V_{CC} = 6.3\text{V}, V_{OH} = 3.0\text{V}$<br>$V_{CC} = 4.5\text{V}, V_{OH} = 2.0\text{V}$ | -1.0<br>-0.5 |              | mA<br>mA                       |
| Allowable Sink Current                   |  |              |              |                                |
| Per Pin (L, D, G)                        |  |              | 10           | mA                             |
| Per Pin (All Others)                     |  |              | 2            | mA                             |
| Per Port (L)                             |  |              | 16           | mA                             |
| Per Port (D, G)                          |  |              | 10           | mA                             |
| Allowable Source Current                 |  |              |              |                                |
| Per Pin (L)                              |  |              | -15          | mA                             |
| Per Pin (All Others)                     |  |              | -1.5         | mA                             |

# ET9320/9321/9322

## DC Electrical Characteristics $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ , $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ unless otherwise noted.

| Parameter                                | Conditions                                  | Min.         | Max. | Units         |
|--|---|--------------|------|---------------|
| Operation Voltage                        |   | 4.5          | 5.5  | V             |
| Power Supply Ripple                      | Peak to Peak (Note 3)                       |              | 0.4  | V             |
| Supply Current                           | $T_A = -40^{\circ}\text{C}$ , Outputs Open  |              | 40   | mA            |
| Input Voltage Levels                     |   |              |      |               |
| CKI Input Levels                         |   |              |      |               |
| Crystal Input                            |   |              |      |               |
| Logic High                               |   | 2.2          |      | V             |
| Logic Low                                |   | -0.3         | 0.3  | V             |
| TTL Input                                | $V_{CC} = 5\text{V} \pm 5\%$                |              |      |               |
| Logic High                               |   | 2.2          |      | V             |
| Logic Low                                |   | -0.3         | 0.6  | V             |
| Schmitt Trigger Inputs                   |   |              |      |               |
| RESET, CKI ( $\div 4$ )                  |   |              |      |               |
| Logic High                               |   | $0.7V_{CC}$  |      | V             |
| Logic Low                                |   | -0.3         | 0.4  | V             |
| SO Input Level (Test Mode)               |   | 2.0          | 3.0  | V             |
| All Other Inputs                         |   |              |      |               |
| Logic High                               | $V_{CC} = \text{Max.}$                      | 3.0          |      | V             |
| Logic High                               | $V_{CC} = 5\text{V} \pm 5\%$                | 2.2          |      | V             |
| Logic Low                                |   | -0.3         | 0.6  | V             |
| Input Levels High Trip Option            |   |              |      |               |
| Logic High                               |   | 3.6          |      | V             |
| Logic Low                                |   | -0.3         | 1.2  | V             |
| Input Load Source Current                | $V_{CC} = 5\text{V}$ , $V_{IN} = 0\text{V}$ |              |      |               |
| CKO                                      |   | -4           | -800 | $\mu\text{A}$ |
| All Others                               |   | -100         | -800 | $\mu\text{A}$ |
| Input Capacitance                        |   |              | 7    | pF            |
| Hi-Z Input Leakage                       | $V_{CC} = 5\text{V}$                        | -2           | +2   | $\mu\text{A}$ |
| Output Voltage levels                    |   |              |      |               |
| Standard Outputs                         |   |              |      |               |
| TTL Operation                            | $V_{CC} = 5\text{V} \pm 5\%$                |              |      |               |
| Logic High                               | $I_{OH} = -75\mu\text{A}$                   | 2.4          |      | V             |
| Logic Low                                | $I_{OL} = 1.6\text{mA}$                     | -0.3         | 0.4  | V             |
| CMOS Operation                           |   |              |      |               |
| Logic High                               | $I_{OH} = -10\mu\text{A}$                   | $V_{CC} - 1$ |      | V             |
| Logic Low                                | $I_{OL} = 10\mu\text{A}$                    | -0.3         | 0.2  | V             |
| Output Current Levels                    |   |              |      |               |
| LED Direct Drive Output                  | $V_{CC} = 5\text{V}$ (Note 4)               |              |      |               |
| Logic High                               | $V_{OH} = 2.0\text{V}$                      | 1.0          | 12   | mA            |
| CKI Sink Current (R/C Option)            | $V_{IN} = 3.5\text{V}$                      | 2            |      | mA            |
| CKO (RAM Supply Current)                 | $V_R = 3.3\text{V}$                         |              | 4    | mA            |
| TRI-STATE® or Open Drain Leakage Current | $V_{CC} = 5\text{V}$                        | -5           | +5   | $\mu\text{A}$ |
| Allowable Sink Current                   |   |              |      |               |
| Per Pin (L, D, G)                        |   |              | 10   | mA            |
| Per Pin (All Others)                     |   |              | 2    | mA            |
| Per Port (L)                             |   |              | 16   | mA            |
| Per Port (D, G)                          |   |              | 10   | mA            |
| Allowable Source Current                 |   |              |      |               |
| Per Pin (L)                              |   |              | -15  | mA            |
| Per Pin (All Others)                     |   |              | -1.5 | mA            |

## AC Electrical Characteristics

ET9420/9421/9422  
ET9320/9321/9322

$0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$ ,  $4.5\text{V} \leq V_{CC} \leq 6.3\text{V}$  unless otherwise noted.  
 $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ ,  $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$  unless otherwise noted.

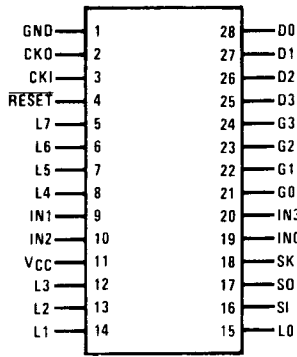
| Parameter   | Conditions   | Min. | Max. | Units         |
|---|--|------|------|---------------|
| Instruction Cycle Time  |  | 4    | 10   | $\mu\text{s}$ |
| Operating CKI Frequency   | $\div 16$ mode   | 1.6  | 4.0  | MHz           |
|   | $\div 8$ mode  | 0.8  | 2.0  | MHz           |
| CKI Duty Cycle (Note 1)   |  | 40   | 60   | %             |
| Rise Time   | Freq. = 4 MHz  |      | 60   | ns            |
| Fall Time   | Freq. = 4 MHz  |      | 40   | ns            |
| CKI Using RC (Figure 8c)  | $\div 4$ mode  |      |      |               |
| Frequency   | $R = 15\text{ k}\Omega \pm 5\%$ , $C = 100\text{ pF} \pm 10\%$                                       | 0.5  | 1.0  | MHz           |
| Instruction Cycle Time  |  | 4    | 8    | $\mu\text{s}$ |
| CKO as SYNC input (Figure 8d)                                       |  |      |      |               |
| $t_{\text{SYNC}}$   | Figure 3a  | 50   |      | ns            |
| Inputs:   |  |      |      |               |
| SI  |  |      |      |               |
| $t_{\text{SETUP}}$  |  | 0.3  |      | $\mu\text{s}$ |
| $t_{\text{HOLD}}$   |  | 250  |      | ns            |
| All Other Inputs  |  |      |      |               |
| $t_{\text{SETUP}}$  |  | 1.7  |      | $\mu\text{s}$ |
| $t_{\text{HOLD}}$   |  | 300  |      | ns            |
| Output Propagation Delay  | Test Conditions:<br>$R_L = 5\text{ k}\Omega$ , $C_L = 50\text{ pF}$ , $V_{\text{OUT}} = 1.5\text{V}$ | 300  |      | ns            |
| SO and SK   |  |      |      |               |
| $t_{\text{pd1}}$  |  |      | 1.0  | $\mu\text{s}$ |
| $t_{\text{pd0}}$  |  |      | 1.0  | $\mu\text{s}$ |
| CKO   |  |      |      |               |
| $t_{\text{pd1}}$  |  |      | 0.25 | $\mu\text{s}$ |
| $t_{\text{pd0}}$  |  |      | 0.25 | $\mu\text{s}$ |
| All Other Outputs   |  |      |      |               |
| $t_{\text{pd1}}$  |  |      | 1.4  | $\mu\text{s}$ |
| $t_{\text{pd0}}$  |  |      | 1.4  | $\mu\text{s}$ |
| MICROBUS™ Timing  | $C_L = 100\text{ pF}$ , $V_{CC} = 5\text{V} \pm 5\%$   |      |      |               |
| Read Operation (Figure 4)   |  |      |      |               |
| Chip Select Stable before $\overline{\text{RD}}$ — $t_{\text{CSR}}$ |  | 65   |      | ns            |
| Chip Select Hold Time for $\overline{\text{RD}}$ — $t_{\text{RCS}}$ |  | 20   |      | ns            |
| $\overline{\text{RD}}$ Pulse Width— $t_{\text{RR}}$                 |  | 400  |      | ns            |
| Data Delay from $\overline{\text{RD}}$ — $t_{\text{RD}}$            |  |      | 375  | ns            |
| $\overline{\text{RD}}$ to Data Floating— $t_{\text{DF}}$            |  |      | 250  | ns            |
| Write Operation (Figure 5)  |  |      |      |               |
| Chip Select Stable before $\overline{\text{WR}}$ — $t_{\text{CSW}}$ |  | 65   |      | ns            |
| Chip Select Hold Time for $\overline{\text{WR}}$ — $t_{\text{WCS}}$ |  | 20   |      | ns            |
| $\overline{\text{WR}}$ Pulse Width— $t_{\text{WW}}$                 |  | 400  |      | ns            |
| Data Set-Up Time for $\overline{\text{WR}}$ — $t_{\text{DW}}$       |  | 320  |      | ns            |
| Data Hold Time for $\overline{\text{WR}}$ — $t_{\text{WD}}$         |  | 100  |      | ns            |
| INTR Transition Time from $\overline{\text{WR}}$ — $t_{\text{WI}}$  |  |      | 700  | ns            |

**Note 1:** Duty cycle =  $t_{W1}/(t_{W1} + t_{W0})$ .

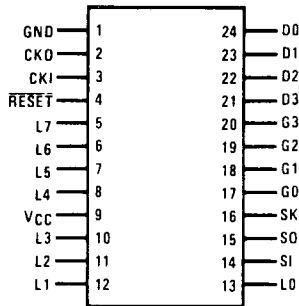
**Note 2:** See Figure 9 for additional I/O characteristics.

**Note 3:** Voltage change must be less than 0.5 volts in a 1 ms period.

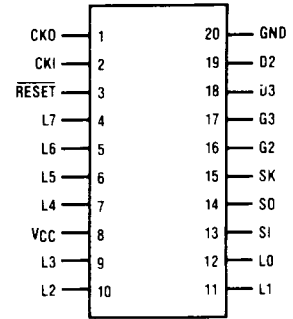
**Note 4:** Exercise great care not to exceed maximum device power dissipation limits when direct driving LEDs (or sourcing similar loads) at high temperature.



Order Number ET 9420/N ET 9320/N  
Package N28A



Order Number ET 9421/N, ET 9321/N  
Package N24A



Order Number ET 9422/N ET 9322/N  
Package N20A

Figure 2. Connection Diagrams

| Pin                              | Description   | Pin   | Description   |
|----------------------------------|---|-------|---|
| L <sub>7</sub> -L <sub>0</sub>   | 8 bidirectional I/O ports with TRI-STATE <sup>®</sup> | SK    | Logic-controlled clock (or general purpose output)                      |
| G <sub>3</sub> -G <sub>0</sub>   | 4 bidirectional I/O ports                             | CKI   | System oscillator input   |
| D <sub>3</sub> -D <sub>0</sub>   | 4 general purpose outputs                             | CKO   | System oscillator output (or general purpose input or RAM power supply) |
| IN <sub>3</sub> -IN <sub>0</sub> | 4 general purpose inputs (COP420/320 only)            | RESET | System reset input  |
| SI                               | Serial input (or counter input)                       | VCC   | Power supply  |
| SO                               | Serial output (or general purpose output)             | GND   | Ground  |

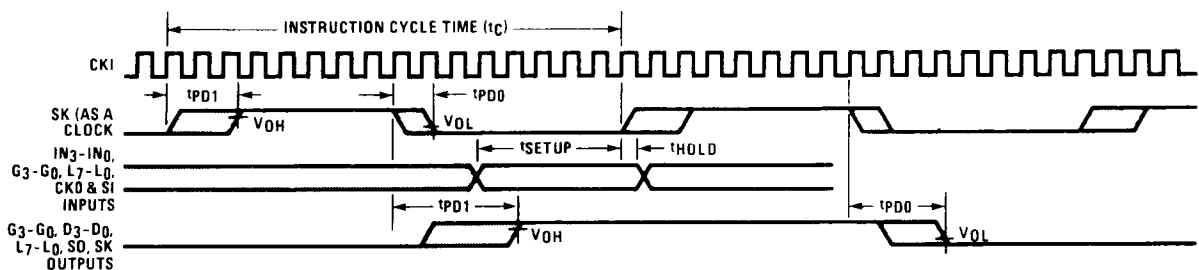


Figure 3. Input/Output Timing Diagrams (crystal divide by 16 mode)

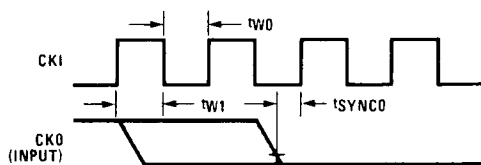


Figure 3A. Synchronization Timing

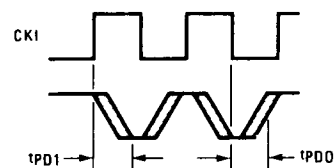


Figure 3B. CKO Output Timing

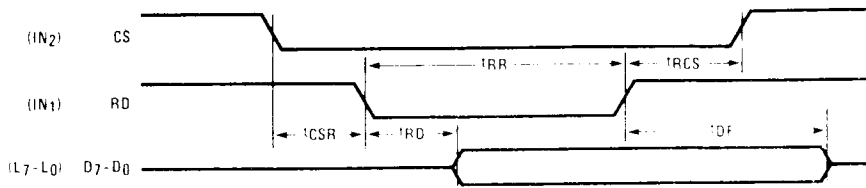


Figure 4. MICROBUS™ Read Operation Timing

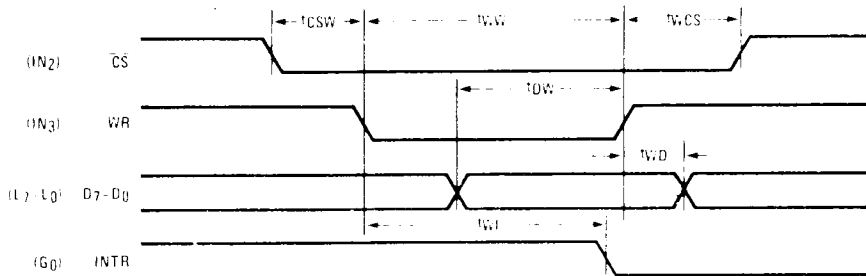


Figure 5. MICROBUS™ Write Operation Timing

## Functional Description ET9420/9421/9422, ET9320/9321/9322

For ease of reading this description, only ET9420 and/or ET9421 are referenced; however, all such references apply equally to the ET9422, 9322, 9320 and/or ET9321, respectively.

A block diagram of the ET9420 is given in figure 1. Data paths are illustrated in simplified form to depict how the various logic elements communicate with each other in implementing the instruction set of the device. Positive logic is used. When a bit is set, it is a logic "1" (greater than 2 volts). When a bit is reset, it is a logic "0" (less than 0.8 volts).

### Program Memory

Program Memory consists of a 1,024 byte ROM. As can be seen by an examination of the ET9420/9421 instruction set, these words may be program instructions, program data or ROM addressing data. Because of the special characteristics associated with the JP, JSRP, JID and LQID instructions, ROM must often be thought of as being organized into 16 pages of 64 words each.

ROM addressing is accomplished by a 10-bit PC register. Its binary value selects one of the 1,024 8-bit words contained in ROM. A new address is loaded into the PC register during each instruction cycle. Unless the instruction is a transfer of control instruction, the PC register is loaded with the next sequential 10-bit binary count value. Three levels of subroutine nesting are implemented by the 10-bit subroutine save registers, SA, SB and SC, providing a last-in, first-out (LIFO) hardware subroutine stack.

ROM instruction words are fetched, decoded and executed by the Instruction Decode, Control and Skip Logic circuitry.

### Data Memory

Data memory consists of a 256-bit RAM, organized as 4 data registers of 16 4-bit digits. RAM addressing is implemented by a 6-bit **B register** whose upper 2 bits (Br) select 1 of 4 data registers and lower 4 bits (Bd) select 1

of 16 4-bit digits in the selected data register. While the 4-bit contents of the selected RAM digit (M) is usually loaded into or from, or exchanged with, the A register (accumulator), it may also be loaded into or from the Q latches or loaded from the L ports. RAM addressing may also be performed directly by the LDD and XAD instructions based upon the 6-bit contents of the operand field of these instructions. The Bd register also serves as a source register for 4-bit data sent directly to the D outputs.

### Internal Logic

The 4-bit **A register** (accumulator) is the source and destination register for most I/O, arithmetic, logic and data memory access operations. It can also be used to load the Br and Bd portions of the B register, to load and input 4 bits of the 8-bit Q latch data, to input 4 bits of the 8-bit L I/O port data and to perform data exchanges with the SIO register.

A 4-bit **adder** performs the arithmetic and logic functions of the ET9420/9421, storing its results in A. It also outputs a carry bit to the 1-bit **C register**, most often employed to indicate arithmetic overflow. The C register, in conjunction with the XAS instruction and the EN register, also serves to control the SK output. C can be outputted directly to SK or can enable SK to be a sync clock each instruction cycle time. (See XAS instruction and EN register description, below.)

Four **general-purpose inputs**,  $IN_3$ - $IN_0$ , are provided;  $IN_1$ ,  $IN_2$  and  $IN_3$  may be selected, by a mask-programmable option, as Read Strobe, Chip Select and Write Strobe inputs, respectively, for use in MICROBUS™ applications.

The **D register** provides 4 general-purpose outputs and is used as the destination register for the 4-bit contents of Bd.

The **G register** contents are outputs to 4 general-purpose bidirectional I/O ports.  $G_0$  may be mask-programmed as an output for MICROBUS™ applications.

The **Q register** is an internal, latched, 8-bit register, used to hold data loaded to or from M and A, as well as 8-bit data from ROM. Its contents are output to the L I/O ports when the L drivers are enabled under program control. (See LEI instruction). With the MICROBUS™ option selected, Q can also be loaded with the 8-bit contents of the L I/O ports upon the occurrence of a write strobe from the host CPU.

The **8 L drivers**, when enabled, output the contents of latched Q data to the L I/O ports. Also, the contents of L may be read directly into A and M. As explained above, the MICROBUS™ option allows L I/O port data to be latched into the Q register. L I/O ports can be directly connected to the segments of a multiplexed LED display (using the LED Direct Drive output configuration option) with Q data being outputted to the Sa-Sg and decimal point segments of the display.

The **SIO register** functions as a 4-bit serial-in/serial-out shift register or as a binary counter depending on the contents of the EN register. (See EN register description, below.) Its contents can be exchanged with A, allowing it to input or output a continuous serial data stream. SIO may also be used to provide additional parallel I/O by connecting SO to external serial-in/parallel-out shift registers.

The XAS instruction copies C into the SKL latch. In the counter mode, SK is the output of SKL; in the shift register mode, SK outputs SKL ANDed with the clock.

The **EN register** is an internal 4-bit register loaded under program control by the LEI instruction. The state of each bit of this register selects or deselects the particular feature associated with each bit of the EN register (EN<sub>3</sub>-EN<sub>0</sub>).

1. The least significant bit of the enable register, EN<sub>0</sub>, selects the SIO register as either a 4-bit shift register or a 4-bit binary counter. With EN<sub>0</sub> set, SIO is an asynchronous binary counter, *decrementing* its value by one upon each low-going pulse ("1" to "0") occurring on the SI input. Each pulse must be at least two instruction cycles wide. SK outputs the value of SKL. The SO output is equal to the value of EN<sub>3</sub>. With EN<sub>0</sub> reset, SIO is a serial shift register shifting left each instruction cycle time. The data present at SI goes into the least significant bit of SIO. SO can be enabled to output the most significant bit of SIO each cycle time. (See 4 below.) The SK output becomes a logic-controlled clock.
2. With EN<sub>1</sub> set the IN<sub>1</sub> input is enabled as an interrupt input. Immediately following an interrupt, EN<sub>1</sub> is reset to disable further interrupts.
3. With EN<sub>2</sub> set, the L drivers are enabled to output the data in Q to the L I/O ports. Resetting EN<sub>2</sub> disables the L drivers, placing the L I/O ports in a high-impedance input state.
4. EN<sub>3</sub>, in conjunction with EN<sub>0</sub>, affects the SO output. With EN<sub>0</sub> set (binary counter option selected) SO will output the value loaded into EN<sub>3</sub>. With EN<sub>0</sub> reset (serial shift register option selected), setting EN<sub>3</sub> enables SO as the output of the SIO shift register, outputting serial shifted data each instruction time. Resetting EN<sub>3</sub> with the serial shift register option selected disables SO as the shift register output; data continues to be shifted through SIO and can be exchanged with A via an XAS instruction but SO remains reset to "0." The table below provides a summary of the modes associated with EN<sub>3</sub> and EN<sub>0</sub>.

Enable Register Modes — Bits EN<sub>3</sub> and EN<sub>0</sub>

| EN <sub>3</sub> | EN <sub>0</sub> | SIO            | SI                      | SO         | SK   |
|-----------------|-----------------|----------------|-------------------------|------------|--|
| 0               | 0               | Shift Register | Input to Shift Register | 0          | If SKL = 1, SK = CLOCK<br>If SKL = 0, SK = 0 |
| 1               | 0               | Shift Register | Input to Shift Register | Serial Out | If SKL = 1, SK = CLOCK<br>If SKL = 0, SK = 0 |
| 0               | 1               | Binary Counter | Input to Binary Counter | 0          | If SKL = 1, SK = 1<br>If SKL = 0, SK = 0     |
| 1               | 1               | Binary Counter | Input to Binary Counter | 1          | If SKL = 1, SK = 1<br>If SKL = 0, SK = 0     |



## Interrupt

The following features are associated with the IN<sub>1</sub> interrupt procedure and protocol and must be considered by the programmer when utilizing interrupts.

- a. The interrupt, once acknowledged as explained below, pushes the next sequential program counter address (PC + 1) onto the stack, pushing in turn the contents of the other subroutine-save registers to the next lower level (PC + 1 → SA → SB → SC). Any previous contents of SC are lost. The program counter is set to hex address 0FF (the last word of page 3) and EN<sub>1</sub> is reset.
- b. An interrupt will be acknowledged only after the following conditions are met:
  1. EN<sub>1</sub> has been set.
  2. A low-going pulse ("1" to "0") at least two instruction cycles wide occurs on the IN<sub>1</sub> input.
  3. A currently executing instruction has been completed.
  4. All successive transfer of control instructions and successive LBIs have been completed (e.g., if the main program is executing a JP instruction which transfers program control to another JP instruction, the interrupt will not be acknowledged until the second JP instruction has been executed).
- c. Upon acknowledgement of an interrupt, the skip logic status is saved and later restored upon popping of the stack. For example, if an interrupt occurs during the execution of ASC (Add with Carry, Skip on Carry) instruction which results in carry, the skip logic status is saved and program control is transferred to the interrupt servicing routine at hex address 0FF. At the *end* of the interrupt routine, a RET instruction is executed to "pop" the stack and return program control to the instruction following the original ASC. *At this time*, the skip logic is enabled and skips this instruction because of the previous ASC carry. Subroutines and LQID instructions should not be nested within the interrupt service routine, since their popping the stack will enable any previously saved main program skips, interfering with the orderly execution of the interrupt routine.
- d. The first instruction of the interrupt routine at hex address 0FF must be a NOP.
- e. A LEI instruction can be put immediately before the RET to re-enable interrupts.

## Microbus™ Interface

The ET9420 has an option which allows it to be used as a peripheral microprocessor device. Inputting and outputting data from and to a host microprocessor (μP). IN<sub>1</sub>, IN<sub>2</sub> and IN<sub>3</sub> general purpose inputs become **MICROBUS™ compatible** read-strobe, chip-select, and write-strobe lines, respectively. IN<sub>1</sub> becomes  $\overline{RD}$  — a logic "0" on this input will cause Q latch data to be enabled to the L ports for input to the μP. IN<sub>2</sub> becomes  $\overline{CS}$  — a logic "0" on this line selects the ET9420 as the μP peripheral device by enabling the operation of the  $\overline{RD}$  and  $\overline{WR}$  lines and allows for the selection of one of several peripheral components. IN<sub>3</sub> becomes  $\overline{WR}$  — a logic "0" on this line will write bus data from the L ports to the Q latches for input to the ET9420. G<sub>0</sub> becomes INTR a "ready" output, reset by a write pulse from the

μP on the  $\overline{WR}$  line, providing the "handshaking capability necessary for asynchronous data transfer between the host CPU and the ET9420.

This option has been designed for compatibility with National's MICROBUS™ — a standard interconnect system for 8-bit parallel data transfer between MOS/LSI CPUs and interfacing devices. (See MICROBUS™ National Publication.) The functioning and timing relationships between the ET9420 signal lines affected by this option are as specified for the MICROBUS™ interface, and are given in the AC electrical characteristics and shown in the timing diagrams (figures 4 and 5). Connection of the ET9420 to the MICROBUS™ is shown in Figure 6.

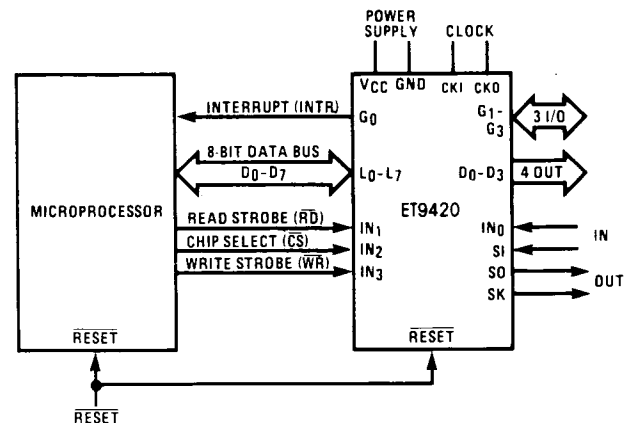


Figure 6. MICROBUS™ Option Interconnect

## Initialization

The Reset Logic, internal to the ET9420/9421, will initialize (clear) the device upon power-up if the power supply rise time is less than 1ms and greater than 1μs. If the power supply rise time is greater than 1ms, the user must provide an external RC network and diode to the  $\overline{RESET}$  pin as shown below. The  $\overline{RESET}$  pin is configured as a Schmitt trigger input. If not used it should be connected to V<sub>CC</sub>. Initialization will occur whenever a logic "0" is applied to the  $\overline{RESET}$  input, provided it stays low for at least three instruction cycle times.

Upon initialization, the PC register is cleared to 0 (ROM address 0) and the A, B, C, D, EN, and G registers are cleared. The SK output is enabled as a SYNC output, providing a pulse each instruction cycle time. *Data Memory (RAM) is not cleared upon initialization.* The first instruction at address 0 must be a CLRA.

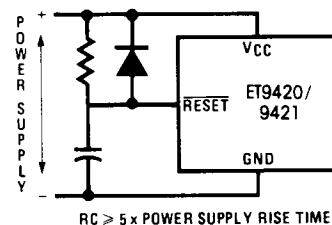


Figure 7. Power-Up Clear Circuit

## Oscillator

There are four basic clock oscillator configurations available as shown by figure 8.

- Crystal Controlled Oscillator.** CKI and CKO are connected to an external crystal. The instruction cycle time equals the crystal frequency divided by 16 (optional by 8).
- External Oscillator.** CKI is an external clock input signal. The external frequency is divided by 16 (optional by 8) to give the instruction cycle time. CKO is now available to be used as the RAM power supply ( $V_R$ ) or as a general purpose input.
- RC Controlled Oscillator.** CKI is configured as a single pin RC controlled Schmitt trigger oscillator. The instruction cycle equals the oscillation frequency divided by 4. CKO is available for non-timing functions.
- Externally Synchronized Oscillator.** Intended for use in multi-COP systems, CKO is programmed to function as an input connected to the SK output of another ET9420/9421 with CKI connected as shown. In this configuration, the SK output connected to CKO must provide a SYNC (instruction cycle) signal to CKO, thereby allowing synchronous data transfer between the COPs using only the SI and SO serial I/O pins in conjunction with the XAS instruction. Note that on power-up SK is automatically enabled as a SYNC output (See Functional Description, Initialization, above).

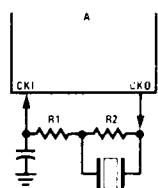
## CKO Pin Options

In a crystal controlled oscillator system, CKO is used as an output to the crystal network. As an option CKO can be a SYNC input as described above. As another option CKO can be a general purpose input, read into bit 2 of A (accumulator) upon execution of an INIL instruction. As another option, CKO can be a RAM power supply pin ( $V_R$ ), allowing its connection to a standby/backup power supply to maintain the integrity of RAM data with minimum power drain when the main supply is inoperative or shut down to conserve power. Using either option is appropriate in applications where the ET9420/9421 system timing configuration does not require use of the CKO pin.

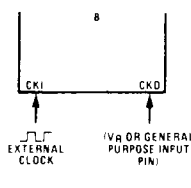
## RAM Keep-Alive Option (Not available on ET9422)

Selecting CKO as the RAM power supply ( $V_R$ ) allows the user to shut off the chip power supply ( $V_{CC}$ ) and maintain data in the RAM. To insure that RAM data integrity is maintained, the following conditions must be met:

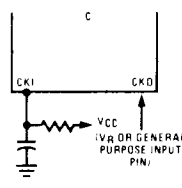
- $\overline{\text{RESET}}$  must go low before  $V_{CC}$  goes below spec during power off;  $V_{CC}$  must be within spec before  $\overline{\text{RESET}}$  goes high on power up.
- $V_R$  must be within the operating range of the chip, and equal to  $V_{CC} \pm 1V$  during normal operation.
- $V_R$  must be  $\geq 3.3V$  with  $V_{CC}$  off.



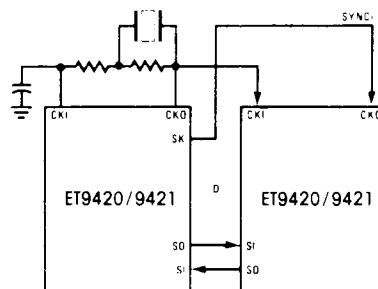
Crystal Oscillator



External Oscillator



RC Controlled Oscillator



Externally Synchronized Oscillator

### Crystal Oscillator

| Crystal Value | Component Values |                 |        |
|---------------|------------------|-----------------|--------|
|               | R1 ( $\Omega$ )  | R2 ( $\Omega$ ) | C (pF) |
| 4 MHz         | 1k               | 1M              | 27     |
| 3.58 MHz      | 1k               | 1M              | 27     |
| 2.09 MHz      | 1k               | 1M              | 56     |

### RC Controlled Oscillator

| R (k $\Omega$ ) | C (pF) | Instruction Cycle Time ( $\mu$ s) |
|-----------------|--------|-----------------------------------|
| 12              | 100    | $5 \pm 20\%$                      |
| 6.8             | 220    | $5.3 \pm 23\%$                    |
| 8.2             | 300    | $8 \pm 29\%$                      |
| 22              | 100    | $8.6 \pm 16\%$                    |

Note:  $50\text{ k}\Omega \geq R \geq 5\text{ k}\Omega$   
 $360\text{ pF} \geq C \geq 50\text{ pF}$

Figure 8. ET9420/9421/ET9320/9321 Oscillator

## I/O Options

ET9420/9421 outputs have the following optional configurations, illustrated in Figure 9a :

- a. Standard** — an enhancement mode device to ground in conjunction with a depletion-mode device to  $V_{CC}$ , compatible with TTL and CMOS input requirements. Available on SO, SK, and all D and G outputs.
- b. Open-Drain** — an enhancement-mode device to ground only, allowing external pull-up as required by the user's application. Available on SO, SK, and all D and G outputs.
- c. Push-Pull** — An enhancement-mode device to ground in conjunction with a depletion-mode device paralleled by an enhancement-mode device to  $V_{CC}$ . This configuration has been provided to allow for fast rise and fall times when driving capacitive loads. Available on SO and SK outputs only.
- d. Standard L** — same as **a.**, but may be disabled. Available on L outputs only.
- e. Open Drain L** — same as **b.**, but may be disabled. Available on L outputs only.
- f. LED Direct Drive** — an enhancement-mode device to ground and to  $V_{CC}$ , meeting the typical current sourcing requirements of the segments of an LED display. The sourcing device is clamped to limit current flow. These devices may be turned off under program control (See Functional Description, EN Register), placing the outputs in a high-impedance state to provide required LED segment blanking for a multiplexed display.
- g. TRI-STATE® Push-Pull** — an enhancement-mode device to ground and  $V_{CC}$ . These outputs are TRI-STATE outputs, allowing for connection of these outputs to a data bus shared by other bus drivers.

ET9420/9421 inputs have the following optional configurations :

- h.** An on-chip depletion load device to  $V_{CC}$ .
- i.** A Hi-Z input which must be driven to a "1" or "0" by external components.

The above input and output configurations share common enhancement-mode and depletion-mode devices. Specifically, all configurations use one or more of six devices (numbered 1-6, respectively). Minimum and maximum current ( $I_{OUT}$  and  $V_{OUT}$ ) curves are given in Figure 9b for each of these devices to allow the designer to effectively use these I/O configurations in designing a ET9420/9421 system.

The SO, SK outputs can be configured as shown in **a.**, **b.**, or **c.** The D and G outputs can be configured as shown in **a.** or **b.** Note that when inputting data to the G ports, the G outputs should be set to "1." The L outputs can be configured as in **d.**, **e.**, **f.** or **g.**

An important point to remember if using configuration **d.** or **f.** with the L drivers is that even when the L drivers are disabled, the depletion load device will source a small amount of current (see Figure 9b, device 2); however, when the L lines are used as inputs, the disabled depletion device can *not* be relied on to source sufficient current to pull an input to logic "1".

## ET9421

If the ET9420 is bonded as a 24-pin device, it becomes the ET9421, illustrated in Figure 2, ET9420/9421 Connection Diagrams. Note that the ET9421 does not contain the four general purpose IN inputs ( $IN_3 - IN_0$ ). Use of this option precludes, of course, use of the IN options, interrupt feature, and the MICROBUS™ option which uses  $IN_1 - IN_3$ . All other options are available for the ET9421.

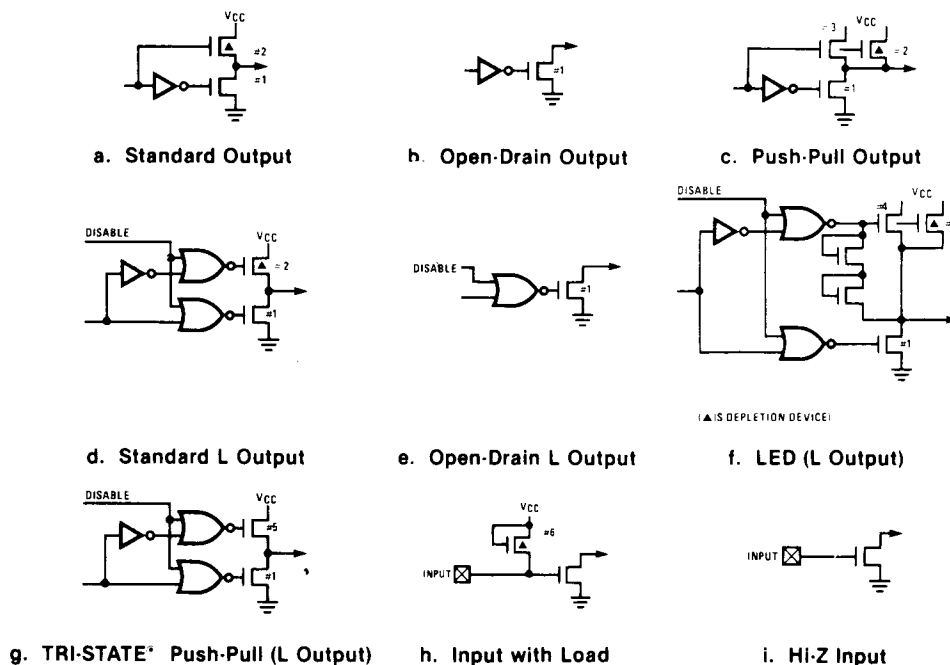


Figure 9a. Input/Output Configurations

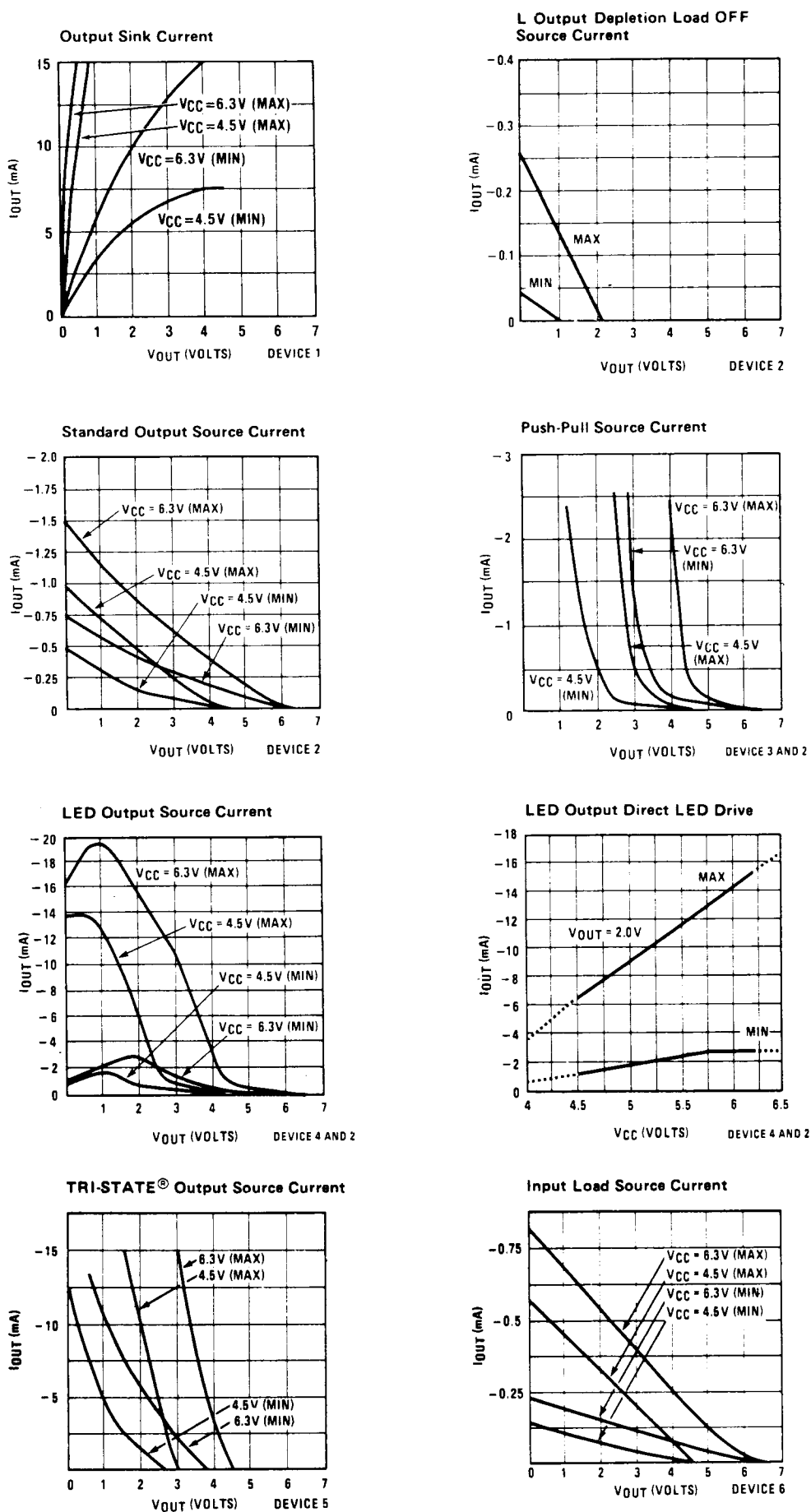


Figure 9b. ET9420/9421 Input/Output Characteristics

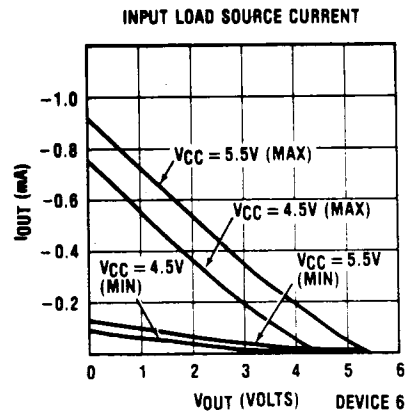
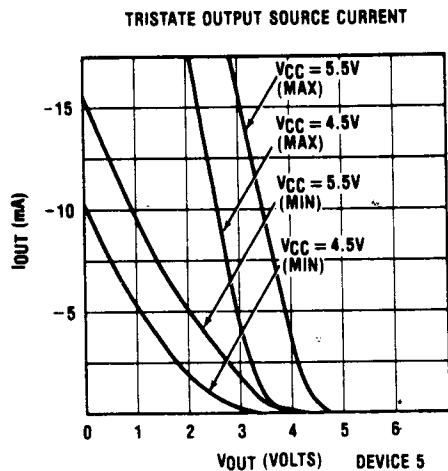
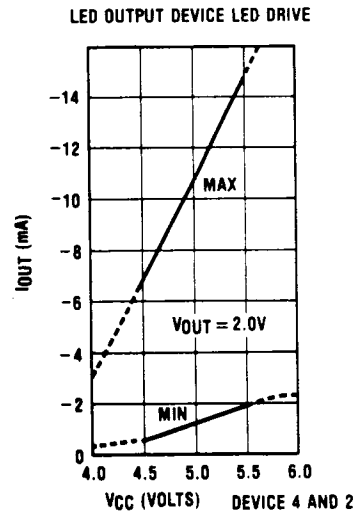
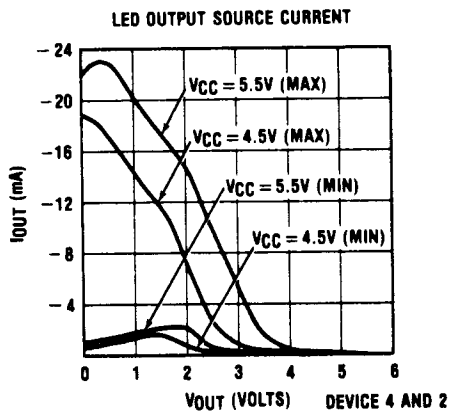
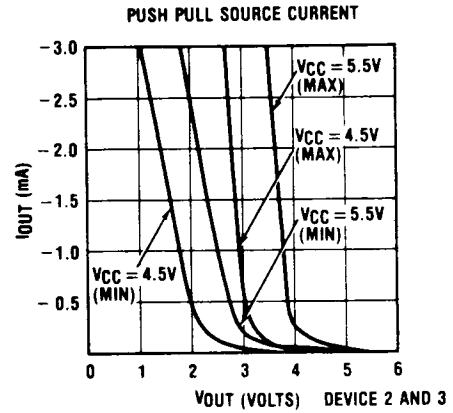
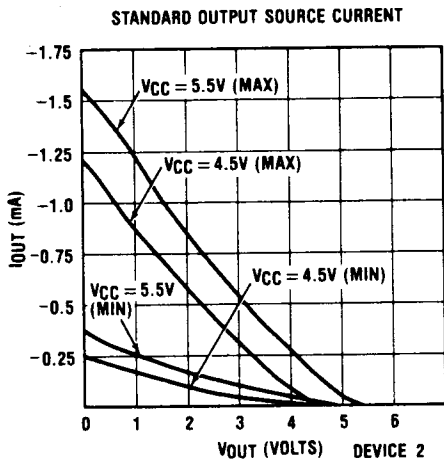
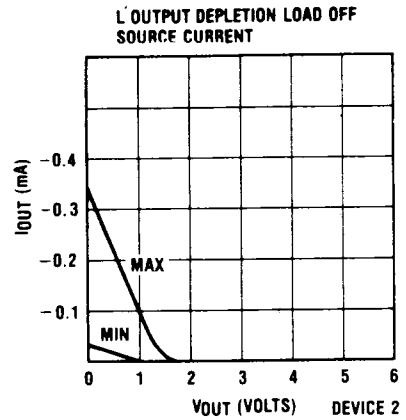
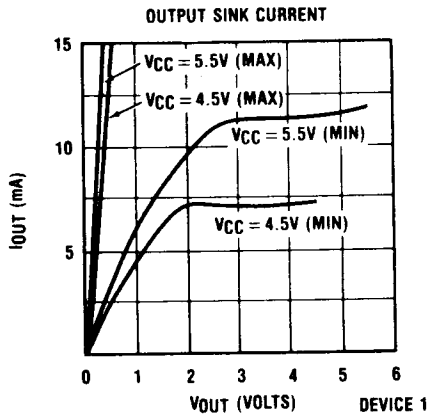


Figure 9c. ET9320/9321 Input/Output Characteristics

## ET9420/9421/9422.ET9320/9321/9322 Instruction Set

Table 1 is a symbol table providing internal architecture, instruction operand and operational symbols used in the instruction set table.

Table 2 provides the mnemonic, operand, machine code, data flow, skip conditions, and description associated with each instruction in the ET9420/9421/9422 instruction set.

Table 2. ET9420/9421/9422.ET9320/9321/9322 Instruction Set Table Symbols

| Symbol                        | Definition  | Symbol                      | Definition  |
|-------------------------------|---|-----------------------------|---|
| INTERNAL ARCHITECTURE SYMBOLS |   | INSTRUCTION OPERAND SYMBOLS |   |
| A                             | 4-bit Accumulator   | d                           | 4-bit Operand Field, 0-15 binary (RAM Digit Select)   |
| B                             | 6-bit RAM Address Register  | r                           | 2-bit Operand Field, 0-3 binary (RAM Register Select) |
| Br                            | Upper 2 bits of B (register address)  | a                           | 10-bit Operand Field, 0-1023 binary (ROM Address)     |
| Bd                            | Lower 4 bits of B (digit address)   | y                           | 4-bit Operand Field, 0-15 binary (Immediate Data)     |
| C                             | 1-bit Carry Register  | RAM(s)                      | Contents of RAM location addressed by s               |
| D                             | 4-bit Data Output Port  | ROM(t)                      | Contents of ROM location addressed by t               |
| EN                            | 4-bit Enable Register   | OPERATIONAL SYMBOLS         |   |
| G                             | 4-bit Register to latch data for G I/O Port                                     | +                           | Plus  |
| IL                            | Two 1-bit latches associated with the IN <sub>3</sub> or IN <sub>0</sub> inputs | -                           | Minus   |
| IN                            | 4-bit Input Port  | →                           | Replaces  |
| L                             | 8-bit TRI-STATE <sup>®</sup> I/O Port   | ↔                           | Is exchanged with                                     |
| M                             | 4-bit contents of RAM Memory pointed to by B Register                           | =                           | Is equal to   |
| PC                            | 10-bit ROM Address Register (program counter)                                   | $\bar{A}$                   | The one's complement of A                             |
| Q                             | 8-bit Register to latch data for L I/O Port                                     | ⊕                           | Exclusive-OR  |
| SA                            | 10-bit Subroutine Save Register A   | :                           | Range of values                                       |
| SB                            | 10-bit Subroutine Save Register B   |                             |   |
| SC                            | 10-bit Subroutine Save Register A   |                             |   |
| SIO                           | 4-bit Shift Register and Counter  |                             |   |
| SK                            | Logic-Controlled Clock Output   |                             |   |

Table 2. ET9420/9421/9422.ET9320/9321/9322 Instruction Set

| Mnemonic                | Operand | Hex Code | Machine Language Code (Binary) | Data Flow   | Skip Conditions | Description                                  |
|-------------------------|---------|----------|--------------------------------|---|-----------------|--|
| ARITHMETIC INSTRUCTIONS |         |          |                                |   |                 |  |
| ASC                     |         | 30       | 0011 0000                      | $A + C + RAM(B) \rightarrow A$<br>Carry $\rightarrow C$       | Carry           | Add with Carry. Skip on Carry                |
| ADD                     |         | 31       | 0011 0001                      | $A + RAM(B) \rightarrow A$                                    | None            | Add RAM to A                                 |
| ADT                     |         | 4A       | 0100 1010                      | $A + 10_{10} \rightarrow A$                                   | None            | Add Ten to A                                 |
| AISC                    | y       | 5-       | 0101  y                        | $A + y \rightarrow A$   | Carry           | Add Immediate. Skip on Carry (y ≠ 0)         |
| CASC                    |         | 10       | 0001 0000                      | $\bar{A} + RAM(B) + C \rightarrow A$<br>Carry $\rightarrow C$ | Carry           | Complement and Add with Carry. Skip on Carry |
| CLRA                    |         | 00       | 0000 0000                      | $0 \rightarrow A$   | None            | Clear A                                      |
| COMP                    |         | 40       | 0100 0000                      | $\bar{A} \rightarrow A$                                       | None            | One's complement of A to A                   |
| NOP                     |         | 44       | 0100 0100                      | None  | None            | No Operation                                 |
| RC                      |         | 32       | 0011 0010                      | "0" $\rightarrow C$   | None            | Reset C                                      |
| SC                      |         | 22       | 0010 0010                      | "1" $\rightarrow C$   | None            | Set C  |
| XOR                     |         | 02       | 0000 0010                      | $A \oplus RAM(B) \rightarrow A$                               | None            | Exclusive-OR RAM with A                      |

Table 2. ET9420/9421/9422.ET9320/9321/9322 Instruction Set (continued)

| Mnemonic  | Operand   | Hex Code         | Machine Language Code (Binary)   | Data Flow   | Skip Conditions  | Description  |                           |  |   |                                 |      |                    |
|---|---|------------------|--|---|------------------|--|---------------------------|--|---|---------------------------------|------|--------------------|
| <b>TRANSFER OF CONTROL INSTRUCTIONS</b>   |   |                  |  |   |                  |  |                           |  |   |                                 |      |                    |
| JID   |   | FF               | <table border="1"><tr><td>1111</td><td>1111</td></tr></table>  | 1111  | 1111             | ROM (PC <sub>9:8</sub> , A,M) → PC <sub>7:0</sub>                          | None                      | Jump Indirect (Note 3)                     |   |                                 |      |                    |
| 1111  | 1111  |                  |  |   |                  |  |                           |  |   |                                 |      |                    |
| JMP   | a   | 6-               | <table border="1"><tr><td>0110</td><td>00</td><td>a<sub>9:8</sub></td></tr><tr><td colspan="3">a<sub>7:0</sub></td></tr></table> | 0110  | 00               | a <sub>9:8</sub>   | a <sub>7:0</sub>          |  |   | a → PC                          | None | Jump               |
| 0110  | 00  | a <sub>9:8</sub> |  |   |                  |  |                           |  |   |                                 |      |                    |
| a <sub>7:0</sub>  |   |                  |  |   |                  |  |                           |  |   |                                 |      |                    |
| JP  | a   | --               | <table border="1"><tr><td>1</td><td>a<sub>6:0</sub></td></tr></table><br>(pages 2,3 only)  | 1   | a <sub>6:0</sub> | a → PC <sub>6:0</sub>  | None                      | Jump within Page (Note 4)                  |   |                                 |      |                    |
|   |   |                  | 1  | a <sub>6:0</sub>  |                  |  |                           |  |   |                                 |      |                    |
| or<br><table border="1"><tr><td>11</td><td>a<sub>5:0</sub></td></tr></table><br>(all other pages) | 11  | a <sub>5:0</sub> | a → PC <sub>5:0</sub>  |   |                  |  |                           |  |   |                                 |      |                    |
| 11  | a <sub>5:0</sub>  |                  |  |   |                  |  |                           |  |   |                                 |      |                    |
| JSRP  | a   | --               | <table border="1"><tr><td>10</td><td>a<sub>5:0</sub></td></tr></table>   | 10  | a <sub>5:0</sub> | PC + 1 → SA → SB → SC<br>0010 → PC <sub>9:6</sub><br>a → PC <sub>5:0</sub> | None                      | Jump to Subroutine Page (Note 5)           |   |                                 |      |                    |
| 10  | a <sub>5:0</sub>  |                  |  |   |                  |  |                           |  |   |                                 |      |                    |
| JSR   | a   | 6-               | <table border="1"><tr><td>0110</td><td>10</td><td>a<sub>9:8</sub></td></tr><tr><td colspan="3">a<sub>7:0</sub></td></tr></table> | 0110  | 10               | a <sub>9:8</sub>   | a <sub>7:0</sub>          |  |   | PC + 1 → SA → SB → SC<br>a → PC | None | Jump to Subroutine |
|   |   |                  | 0110   | 10  | a <sub>9:8</sub> |  |                           |  |   |                                 |      |                    |
| a <sub>7:0</sub>  |   |                  |  |   |                  |  |                           |  |   |                                 |      |                    |
| --  | <table border="1"><tr><td colspan="3">a<sub>7:0</sub></td></tr></table> | a <sub>7:0</sub> |  |   |                  |  |                           |  |   |                                 |      |                    |
| a <sub>7:0</sub>  |   |                  |  |   |                  |  |                           |  |   |                                 |      |                    |
| RET   |   | 48               | <table border="1"><tr><td>0100</td><td>1000</td></tr></table>  | 0100  | 1000             | SC → SB → SA → PC  | None                      | Return from Subroutine                     |   |                                 |      |                    |
| 0100  | 1000  |                  |  |   |                  |  |                           |  |   |                                 |      |                    |
| RETSK   |   | 49               | <table border="1"><tr><td>0100</td><td>1001</td></tr></table>  | 0100  | 1001             | SC → SB → SA → PC  | Always Skip on Return     | Return from Subroutine then Skip           |   |                                 |      |                    |
| 0100  | 1001  |                  |  |   |                  |  |                           |  |   |                                 |      |                    |
| <b>MEMORY REFERENCE INSTRUCTIONS</b>  |   |                  |  |   |                  |  |                           |  |   |                                 |      |                    |
| CAMQ  |   | 33               | <table border="1"><tr><td>0011</td><td>0011</td></tr></table>  | 0011  | 0011             | A → Q <sub>7:4</sub>   | None                      | Copy A, RAM to Q                           |   |                                 |      |                    |
|   |   |                  | 0011   | 0011  |                  |  |                           |  |   |                                 |      |                    |
| 3C  | <table border="1"><tr><td>0011</td><td>1100</td></tr></table>           | 0011             | 1100   | RAM(B) → Q <sub>3:0</sub>                                     |                  |  |                           |  |   |                                 |      |                    |
| 0011  | 1100  |                  |  |   |                  |  |                           |  |   |                                 |      |                    |
| CQMA  |   | 33               | <table border="1"><tr><td>0011</td><td>0011</td></tr></table>  | 0011  | 0011             | Q <sub>7:4</sub> → RAM(B)  | None                      | Copy Q to RAM, A                           |   |                                 |      |                    |
|   |   |                  | 0011   | 0011  |                  |  |                           |  |   |                                 |      |                    |
| 2C  | <table border="1"><tr><td>0010</td><td>1100</td></tr></table>           | 0010             | 1100   | Q <sub>3:0</sub> → A  |                  |  |                           |  |   |                                 |      |                    |
| 0010  | 1100  |                  |  |   |                  |  |                           |  |   |                                 |      |                    |
| LD  | r   | -5               | <table border="1"><tr><td>00</td><td>r</td><td>0101</td></tr></table>  | 00  | r                | 0101   | RAM(B) → A<br>Br ⊕ r → Br | None                                       | Load RAM into A, Exclusive-OR Br with r |                                 |      |                    |
| 00  | r   | 0101             |  |   |                  |  |                           |  |   |                                 |      |                    |
| LDD   | r,d   | 23               | <table border="1"><tr><td>0010</td><td>0011</td></tr></table>  | 0010  | 0011             | RAM(r,d) → A   | None                      | Load A with RAM pointed to directly by r,d |   |                                 |      |                    |
|   |   |                  | 0010   | 0011  |                  |  |                           |  |   |                                 |      |                    |
| --  | <table border="1"><tr><td>00</td><td>r</td><td>d</td></tr></table>      | 00               | r  | d   |                  |  |                           |  |   |                                 |      |                    |
| 00  | r   | d                |  |   |                  |  |                           |  |   |                                 |      |                    |
| LQID  |   | BF               | <table border="1"><tr><td>1011</td><td>1111</td></tr></table>  | 1011  | 1111             | ROM(PC <sub>9:8</sub> ,A,M) → Q<br>SB → SC                                 | None                      | Load Q Indirect (Note 3)                   |   |                                 |      |                    |
| 1011  | 1111  |                  |  |   |                  |  |                           |  |   |                                 |      |                    |
| RMB   | 0   | 4C               | <table border="1"><tr><td>0100</td><td>1100</td></tr></table>  | 0100  | 1100             | 0 → RAM(B) <sub>0</sub>  | None                      | Reset RAM Bit                              |   |                                 |      |                    |
|   |   |                  | 0100   | 1100  |                  |  |                           |  |   |                                 |      |                    |
|   |   |                  | 45   | <table border="1"><tr><td>0100</td><td>0101</td></tr></table> | 0100             | 0101   |                           |  | 0 → RAM(B) <sub>1</sub>                 |                                 |      |                    |
|   |   |                  | 0100   | 0101  |                  |  |                           |  |   |                                 |      |                    |
| 42  | <table border="1"><tr><td>0100</td><td>0010</td></tr></table>           | 0100             | 0010   | 0 → RAM(B) <sub>2</sub>                                       |                  |  |                           |  |   |                                 |      |                    |
| 0100  | 0010  |                  |  |   |                  |  |                           |  |   |                                 |      |                    |
| 43  | <table border="1"><tr><td>0100</td><td>0011</td></tr></table>           | 0100             | 0011   | 0 → RAM(B) <sub>3</sub>                                       |                  |  |                           |  |   |                                 |      |                    |
| 0100  | 0011  |                  |  |   |                  |  |                           |  |   |                                 |      |                    |
| SMB   | 0   | 4D               | <table border="1"><tr><td>0100</td><td>1101</td></tr></table>  | 0100  | 1101             | 1 → RAM(B) <sub>0</sub>  | None                      | Set RAM Bit                                |   |                                 |      |                    |
|   |   |                  | 0100   | 1101  |                  |  |                           |  |   |                                 |      |                    |
|   |   |                  | 47   | <table border="1"><tr><td>0100</td><td>1101</td></tr></table> | 0100             | 1101   |                           |  | 1 → RAM(B) <sub>1</sub>                 |                                 |      |                    |
|   |   |                  | 0100   | 1101  |                  |  |                           |  |   |                                 |      |                    |
| 46  | <table border="1"><tr><td>0100</td><td>0110</td></tr></table>           | 0100             | 0110   | 1 → RAM(B) <sub>2</sub>                                       |                  |  |                           |  |   |                                 |      |                    |
| 0100  | 0110  |                  |  |   |                  |  |                           |  |   |                                 |      |                    |
| 4B  | <table border="1"><tr><td>0100</td><td>1011</td></tr></table>           | 0100             | 1011   | 1 → RAM(B) <sub>3</sub>                                       |                  |  |                           |  |   |                                 |      |                    |
| 0100  | 1011  |                  |  |   |                  |  |                           |  |   |                                 |      |                    |

Table 2. ET9420/9421/9422, ET9320/9321/9322 Instruction Set (continued)

| Mnemonic   | Operand | Hex Code | Machine Language Code (Binary)  | Data Flow                                      | Skip Conditions  | Description  |
|--|---------|----------|---|--|--|--|
| <b>MEMORY REFERENCE INSTRUCTIONS (continued)</b> |         |          |   |  |  |  |
| STII   | y       | 7-       | $\boxed{0111} \boxed{y}$  | y → RAM(B)<br>Bd + 1 → Bd                      | None   | Store Memory Immediate and Increment Bd                      |
| X  | r       | -6       | $\boxed{00} \boxed{r} \boxed{0110}$   | RAM(B) ↔ A<br>Br ⊕ r → Br                      | None   | Exchange RAM with A, Exclusive-OR Br with r                  |
| XAD  | r,d     | 23       | $\boxed{0010} \boxed{0011}$<br>-- $\boxed{10} \boxed{r} \boxed{d}$  | RAM(r,d) ↔ A                                   | None   | Exchange A with RAM pointed to directly by r,d               |
| XDS  | r       | -7       | $\boxed{00} \boxed{r} \boxed{0111}$   | RAM(B) ↔ A<br>Bd - 1 → Bd<br>Br ⊕ r → Br       | Bd decrements past 0                                   | Exchange RAM with A and Decrement Bd, Exclusive-OR Br with r |
| XIS  | r       | -4       | $\boxed{00} \boxed{r} \boxed{0100}$   | RAM(B) ↔ A<br>Bd + 1 → Bd<br>Br ⊕ r → Br       | Bd increments past 15                                  | Exchange RAM with A and Increment Bd, Exclusive-OR Br with r |
| <b>REGISTER REFERENCE INSTRUCTIONS</b>           |         |          |   |  |  |  |
| CAB  |         | 50       | $\boxed{0101} \boxed{0000}$   | A → Bd   | None   | Copy A to Bd   |
| CBA  |         | 4E       | $\boxed{0100} \boxed{1110}$   | Bd → A   | None   | Copy Bd to A   |
| LBI  | r,d     | --       | $\boxed{00} \boxed{r} \boxed{(d-1)}$<br>(d = 0, 9:15)<br>or<br>33 $\boxed{0011} \boxed{0011}$<br>-- $\boxed{10} \boxed{r} \boxed{d}$<br>(any d) | r,d → B  | Skip until not a LBI                                   | Load B immediate with r,d (Note 6)                           |
| LEI  | y       | 33       | $\boxed{0011} \boxed{0011}$   | y → EN   | None   | Load EN Immediate (Note 7)                                   |
|  |         | 6-       | $\boxed{0110} \boxed{y}$  |  |  |  |
| XABR   |         | 12       | $\boxed{0001} \boxed{0010}$   | A ↔ Br (0,0 → A <sub>3</sub> ,A <sub>2</sub> ) | None   | Exchange A with Br   |
| <b>TEST INSTRUCTIONS</b>                         |         |          |   |  |  |  |
| SKC  |         | 20       | $\boxed{0010} \boxed{0000}$   |  | C = "1"  | Skip if C is True  |
| SKE  |         | 21       | $\boxed{0010} \boxed{0001}$   |  | A = RAM(B)   | Skip if A Equals RAM   |
| SKGZ   |         | 33       | $\boxed{0011} \boxed{0011}$   |  | G <sub>3:0</sub> = 0                                   | Skip if G is Zero (all 4 bits)                               |
|  |         | 21       | $\boxed{0010} \boxed{0001}$   |  |  |  |
| SKGBZ  |         | 33       | $\boxed{0011} \boxed{0011}$   | 1st byte                                       |  | Skip if G Bit is Zero  |
|  | 0       | 01       | $\boxed{0000} \boxed{0001}$   |  | G <sub>0</sub> = 0                                     |  |
|  | 1       | 11       | $\boxed{0001} \boxed{0001}$   |  | G <sub>1</sub> = 0                                     |  |
|  | 2       | 03       | $\boxed{0000} \boxed{0011}$   | 2nd byte                                       | G <sub>2</sub> = 0                                     |  |
|  | 3       | 13       | $\boxed{0001} \boxed{0011}$   |  | G <sub>3</sub> = 0                                     |  |
| SKMBZ  | 0       | 01       | $\boxed{0000} \boxed{0001}$   |  | RAM(B) <sub>0</sub> = 0                                | Skip if RAM Bit is Zero                                      |
|  | 1       | 11       | $\boxed{0001} \boxed{0001}$   |  | RAM(B) <sub>1</sub> = 0                                |  |
|  | 2       | 03       | $\boxed{0000} \boxed{0011}$   |  | RAM(B) <sub>2</sub> = 0                                |  |
|  | 3       | 13       | $\boxed{0001} \boxed{0011}$   |  | RAM(B) <sub>3</sub> = 0                                |  |
| SKT  |         | 41       | $\boxed{0100} \boxed{0001}$   |  | A time-base counter carry has occurred since last test | Skip on Timer (Note 3)                                       |



Table 2. ET9420/9421/9422, ET9320/9321/9322 Instruction Set (continued)

| Mnemonic Operand                 | Hex Code | Machine Language Code (Binary) | Data Flow   | Skip Conditions | Description                    |
|----------------------------------|----------|--------------------------------|---|-----------------|--------------------------------|
| <b>INPUT/OUTPUT INSTRUCTIONS</b> |          |                                |   |                 |                                |
| ING                              | 33       | 0011 0011                      | G → A   | None            | Input G Ports to A             |
|                                  | 2A       | 0010 1010                      |   |                 |                                |
| ININ                             | 33       | 0011 0011                      | IN → A  | None            | Input IN Inputs to A (Note 2)  |
|                                  | 28       | 0010 1000                      |   |                 |                                |
| INIL                             | 33       | 0011 0011                      | IL <sub>3</sub> , CKO, "0", IL <sub>0</sub> → A   | None            | Input iL Latches to A (Note 3) |
|                                  | 29       | 0010 1001                      |   |                 |                                |
| INL                              | 33       | 0011 0011                      | L <sub>7:4</sub> → RAM(B)<br>L <sub>3:0</sub> → A | None            | Input L Ports to RAM,A         |
|                                  | 2E       | 0010 1110                      |   |                 |                                |
| OBD                              | 33       | 0011 0011                      | Bd → D  | None            | Output Bd to D Outputs         |
|                                  | 3E       | 0011 1110                      |   |                 |                                |
| OGI y                            | 33       | 0011 0011                      | y → G   | None            | Output to G Ports Immediate    |
|                                  | 5-       | 0101  y                        |   |                 |                                |
| OMG                              | 33       | 0011 0011                      | RAM(B) → G  | None            | Output RAM to G Ports          |
|                                  | 3A       | 0011 1010                      |   |                 |                                |
| XAS                              | 4F       | 0100 1111                      | A ↔ SIO, C → SKL                                  | None            | Exchange A with SIO (Note 3)   |

**Note 1:** All subscripts for alphabetical symbols indicate bit numbers unless explicitly defined (e.g., Br and Bd are explicitly defined). Bits are numbered 0 to N where 0 signifies the least significant bit (low-order, right-most bit). For example, A<sub>3</sub> indicates the most significant (left-most) bit of the 4-bit A register.

**Note 2:** The ININ instruction is not available on the ET9421/ET932 and ET9422/ET9322 since these devices do not contain the IN inputs.

**Note 3:** For additional information on the operation of the XAS, JID, LQID, INIL, and SKT instructions, see below.

**Note 4:** The JP instruction allows a jump, while in subroutine pages 2 or 3, to any ROM location within the two-page boundary of pages 2 or 3. The IP instruction, otherwise, permits a jump to a ROM location within the current 64-word page. JP may not jump to the last word of a page.

**Note 5:** A JSRP transfers program control to subroutine page 2 (0010 is loaded into the upper 4 bits of P). A JSRP may not be used when in pages 2 or 3. JSRP may not jump to the last word in page 2.

**Note 6:** LBI is a single-byte instruction if d = 0, 9, 10, 11, 12, 13, 14, or 15. The machine code for the lower 4 bits equals the binary value of the "d" data minus 1, e.g., to load the lower four bits of B (Bd) with the value 9 (1001<sub>2</sub>), the lower 4 bits of the LBI instruction equal 8 (1000<sub>2</sub>). To load 0, the lower 4 bits of the LBI instruction should equal 15 (1111<sub>2</sub>).

**Note 7:** Machine code for operand field y for LEI instruction should equal the binary value to be latched into EN, where a "1" or "0" in each bit of EN corresponds with the selection or deselection of a particular function associated with each bit. (See Functional Description, EN Register.)

The following information is provided to assist the user in understanding the operation of several unique instructions and to provide notes useful to programmers in writing ET9420/9421 programs.

### XAS Instruction

XAS (Exchange A with SIO) exchanges the 4-bit contents of the accumulator with the 4-bit contents of the SIO register. The contents of SIO will contain serial-in/serial-out shift register or binary counter data, depending on the value of the EN register. An XAS instruction will also affect the SK output. (See Functional Description, EN Register, above.) If SIO is selected as a shift register, an XAS instruction must be performed once every 4 instruction cycles to effect a continuous data stream.

### JID Instruction

JID (Jump Indirect) is an indirect addressing instruction, transferring program control to a new ROM location pointed to indirectly by A and M. It loads the lower 8 bits of the ROM address register PC with the contents of ROM addressed by the 10-bit word, PC<sub>9,8</sub>, A, M. PC<sub>9</sub> and PC<sub>8</sub> are not affected by this instruction.

Note that JID requires 2 instruction cycles to execute.

### INIL Instruction

INIL (Input IL Latches to A) inputs 2 latches, IL<sub>3</sub> and IL<sub>0</sub> (see figure 10) and CKO into A. The IL<sub>3</sub> and IL<sub>0</sub> latches are set if a low-going pulse ("1" to "0") has occurred on the IN<sub>3</sub> and IN<sub>0</sub> inputs since the last INIL instruction, provided the input pulse stays low for at least two instruction times. Execution of an INIL inputs IL<sub>3</sub> and IL<sub>0</sub> into A3 and A0 respectively, and resets these latches to allow them to respond to subsequent low-going pulses on the IN<sub>3</sub> and IN<sub>0</sub> lines. If CKO is mask programmed as a general purpose input, an INIL will input the state of CKO into A2. If CKO has not been so programmed, a "1" will be placed in A2. A "0" is always placed in A1 upon the execution of an INIL. The general purpose inputs IN<sub>3</sub>-IN<sub>0</sub> are input to A upon execution of an ININ instruction. (See table 2, ININ instruction.) INIL is useful in recognizing pulses of short duration or pulses which occur too often to be read conveniently by an ININ instruction.

Note: IL latches are not cleared on reset.

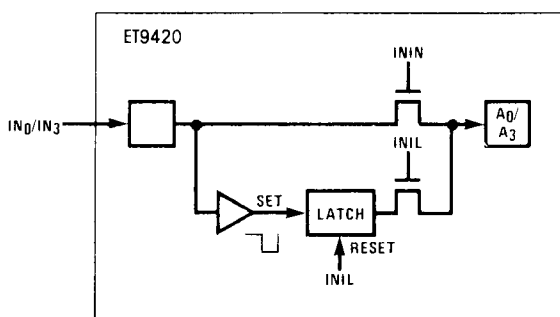


Figure 10.

### LQID Instruction

LQID (Load Q Indirect) loads the 8-bit Q register with the contents of ROM pointed to by the 10-bit word PC<sub>9</sub>, PC<sub>8</sub>, A, M. LQID can be used for table lookup or code conversion such as BCD to seven-segment. The LQID instruction "pushes" the stack (PC + 1 → SA → SB → SC) and replaces the least significant 8 bits of PC as follows: A → PC<sub>7,4</sub>, RAM(B) → PC<sub>3,0</sub>, leaving PC<sub>9</sub> and PC<sub>8</sub> unchanged. The ROM data pointed to by the new address is fetched and loaded into the Q latches. Next, the stack is "popped" (SC → SB → SA → PC), restoring the saved value of PC to continue sequential program execution. Since LQID pushes SB → SC, the previous contents of SC are lost. Also, when LQID pops the stack, the previously pushed contents of SB are left in SC. The net result is that the contents of SB are placed in SC (SB → SC). Note that LQID takes two instruction cycle times to execute.

### SKT Instruction

The SKT (Skip On Timer) instruction tests the state of an internal 10-bit time-base counter. This counter divides the instruction cycle clock frequency by 1024 and provides a latched indication of counter overflow. The SKT instruction tests this latch, executing the next program instruction if the latch is not set. If the latch has been set since the previous test, the next program instruction is skipped and the latch is reset. The features associated with this instruction, therefore, allow the ET9420/9421 to generate its own time-base for real-time processing rather than relying on an external input signal.

For example, using a 2.097 MHz crystal as the time-base to the clock generator, the instruction cycle clock frequency will be 131 kHz (crystal frequency ÷ 16) and the binary counter output pulse frequency will be 128 Hz. For time-of-day or similar real-time processing, the SKT instruction can call a routine which increments a "seconds" counter every 128 ticks.

### Instruction Set Notes

- The first word of a ET9420/9421 program (ROM address 0) must be a CLRA (Clear A) instruction.
- Although skipped instructions are not executed, one instruction cycle time is devoted to skipping each byte of the skipped instruction. Thus all program paths take the same number of cycle times whether instructions are skipped or executed except JID and LQID. LQID and JID take two cycle times if executed and one if skipped.
- The ROM is organized into 16 pages of 64 words each. The Program Counter is a 10-bit binary counter, and will count through page boundaries. If a JP, JSRP, JID or LQID instruction is located in the last word of a page, the instruction operates as if it were in the next page. For example: a JP located in the last word of a page will jump to a location in the next page. Also, a LQID or JID located in the last word of page 3, 7, 11 or 15 will access data in the next group of four pages.

## Option List

The ET9420/9421/9422 mask-programmable options are assigned numbers which correspond with the ET9420 pins.

The following is a list of ET9420 options. When specifying a ET9421 or ET9422 chip, Options 9, 10, 19, 20 and 29 must all be set to zero. When specifying a ET9422 chip, Options 21, 22, 27 and 28 must also be zero, and Option 2 must not be a 1. The options are programmed at the same time as the ROM pattern to provide the user with the hardware flexibility to interface to various I/O components using little or no external circuitry.

Option 1 = 0: Ground Pin — no options available

Option 2: CKO Pin

- = 0: clock generator output to crystal  
(0 not available if option 3 = 4 or 5)
- = 1: pin is RAM power supply ( $V_R$ ) input  
(Not available on ET9422, ET9322)
- = 2: general purpose input with load device
- = 3: multi-COP SYNC input
- = 4: general purpose Hi Z input

Option 3: CKI Input

- = 0: crystal input divided by 16
- = 1: crystal input divided by 8
- = 2: TTL external clock input divided by 16
- = 3: TTL external clock input divided by 8
- = 4: single-pin RC controlled oscillator (+4)
- = 5: Schmitt trigger clock input (+4)

Option 4: RESET Pin

- = 0: Load devices to  $V_{CC}$
- = 1: Hi-Z input

Option 5:  $L_7$  Driver

- = 0: Standard output (figure 9D)
- = 1: Open-Drain output (E)
- = 2: LED direct drive output (F)
- = 3: TRI-STATE® push-pull output (G)

Option 6:  $L_6$  Driver

same as Option 5

Option 7:  $L_5$  Driver

same as Option 5

Option 8:  $L_4$  Driver

same as Option 5

Option 9:  $IN_1$  Input

- = 0: load device to  $V_{CC}$  (H)
- = 1: Hi-Z input (I)

Option 10:  $IN_2$  Input

same as Option 9

Option 11 = 0:  $V_{CC}$  Pin — no options available

Option 12:  $L_3$  Driver

same as Option 5

Option 13:  $L_2$  Driver

same as Option 5

Option 14:  $L_1$  Driver

same as Option 5

Option 15:  $L_0$  Driver

same as Option 5

Option 16: SI Input

same as Option 9

Option 17: SO Driver

- = 0: standard output (A)
- = 1: open-drain output (B)
- = 2: push-pull output (C)

Option 18: SK Driver

same as Option 17

Option 19:  $IN_0$  Input

same as Option 9

Option 20:  $IN_3$  Input

same as Option 9

Option 21:  $G_0$  I/O Port

- = 0: Standard output (A)
- = 1: Open-Drain output (B)

Option 22:  $G_1$  I/O Port

same as Option 21

Option 23:  $G_2$  I/O Port

same as Option 21

Option 24:  $G_3$  I/O Port

same as Option 21

Option 25:  $D_3$  Output

- = 0: Standard output (A)
- = 1: Open-Drain output (B)

Option 26:  $D_2$  Output

same as Option 25

Option 27:  $D_1$  Output

same as Option 25

Option 28:  $D_0$  Output

same as Option 25

Option 29: COP Function

- = 0: normal operation
- = 1: MICROBUS™ option

Option 30: COP Bonding

- = 0: ET9420 (28-pin device)
- = 1: ET9421 (24-pin device)
- = 2: 28 and 24-pin versions
- = 3: ET9422 (20-pin device)
- = 4: 28- and 20-pin versions
- = 5: 24- and 20-pin versions
- = 6: 28-, 24-, and 20-pin versio

Option 31: IN Input Levels

- = 0: normal input levels
- = 1: Higher voltage input leve  
("0" = 1.2V, "1" = 3.6V)

Option 32: G Input Levels

same as Option 31

Option 33: L Input Levels

same as Option 31

Option 34: CKO Input Levels

same as Option 31

Option 35: SI Input Levels

same as Option 31

## TEST MODE (Non-Standard Operation)

The SO output has been configured to provide for standard test procedures for the custom-programmed ET9420. With SO forced to logic "1", two test modes are provided, depending upon the value of SI :

- a. RAM and Internal Logic Test Mode (SI = 1)
- b. ROM Test Mode (SI = 0)

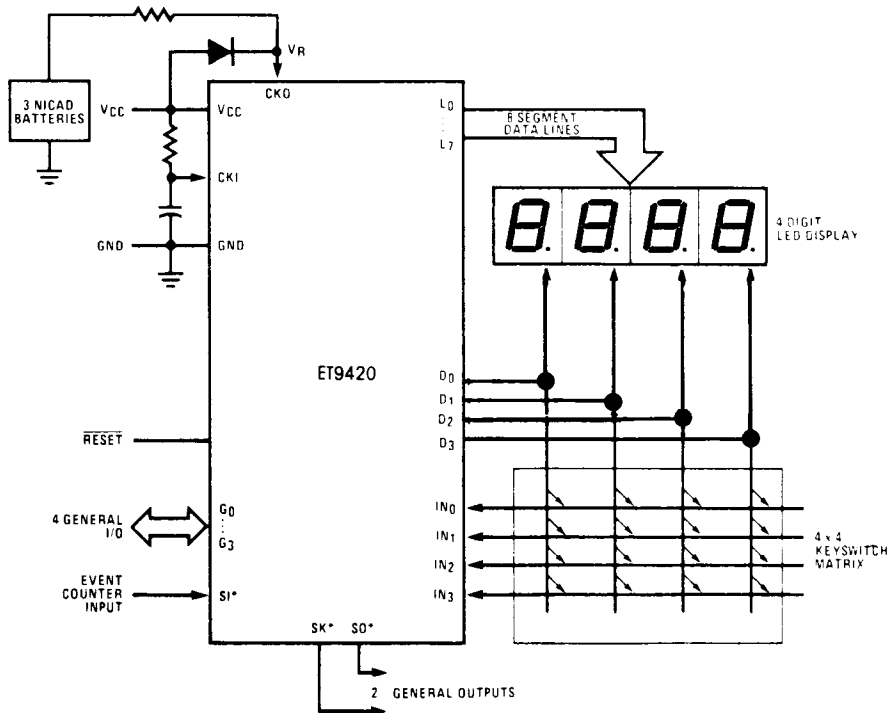
These special test modes should not be employed by the user; they are intended for manufacturing test only.

## APPLICATION EXAMPLE : ET9420 General Controller

Figure 9 shows an interconnect diagram for a ET9420 used as a general controller. Operation of the system is as follows :

1. The L<sub>7</sub>-L<sub>0</sub> outputs are configured as LED Direct Drive outputs, allowing direct connection to the segments of the display.

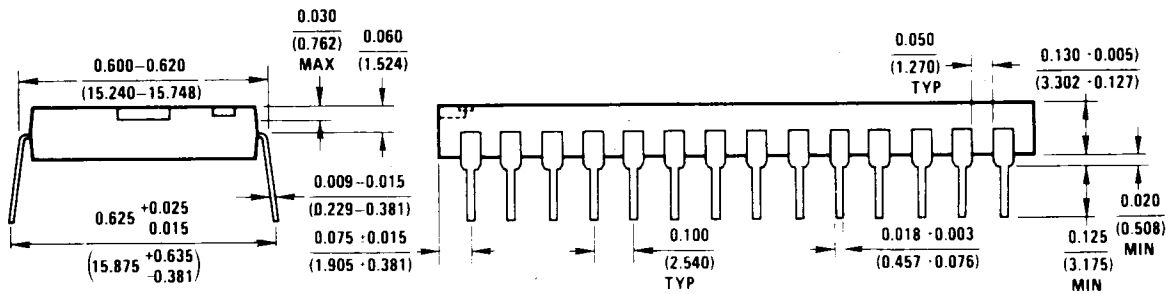
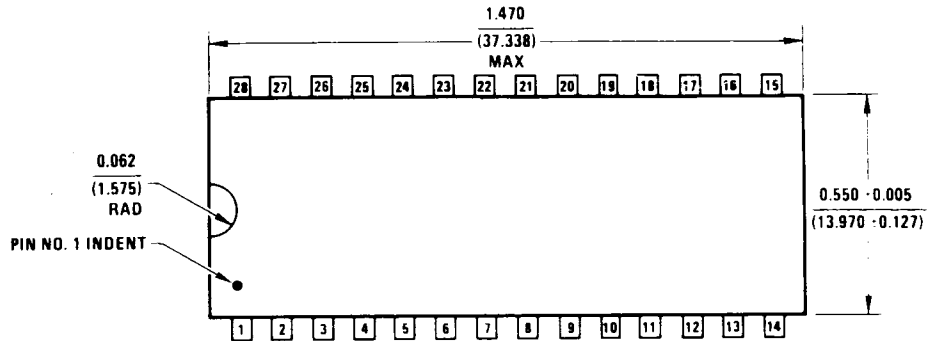
2. The D<sub>3</sub>-D<sub>0</sub> outputs drive the digits of the multiplexed display directly and scan the columns of the 4 × 4 keyboard matrix.
3. The IN<sub>3</sub>-IN<sub>0</sub> inputs are used to input the 4 rows of the keyboard matrix. Reading the IN lines in conjunction with the current value of the D outputs allows detection, debouncing, and decoding of any one of the 16 keyswitches.
4. CKI is configured as a single-pin oscillator input allowing system timing to be controlled by a single-pin RC network. CKO is therefore available for use as a V<sub>R</sub> RAM power supply pin. RAM data integrity is thereby assured when the main power supply is shut down (see RAM Keep-Alive Option description).
5. SI is selected as the input to a binary counter input. With SIO used as a binary counter, SO and SK can be used as general purpose outputs.
6. The 4 bidirectional G I/O ports (G<sub>3</sub>-G<sub>0</sub>) are available for use as required by the user's application.



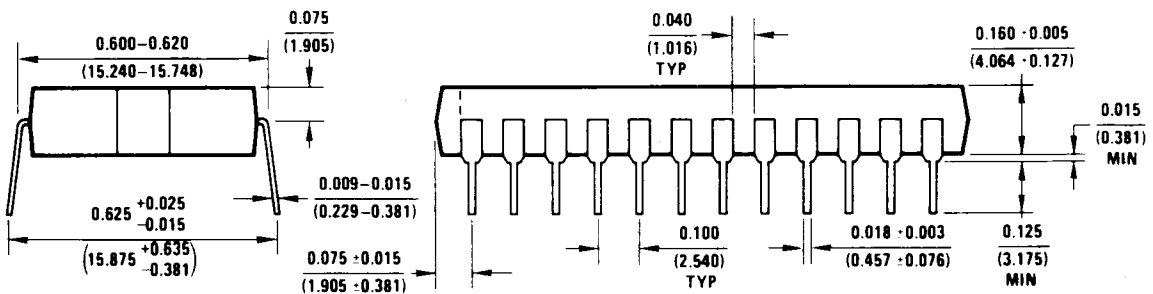
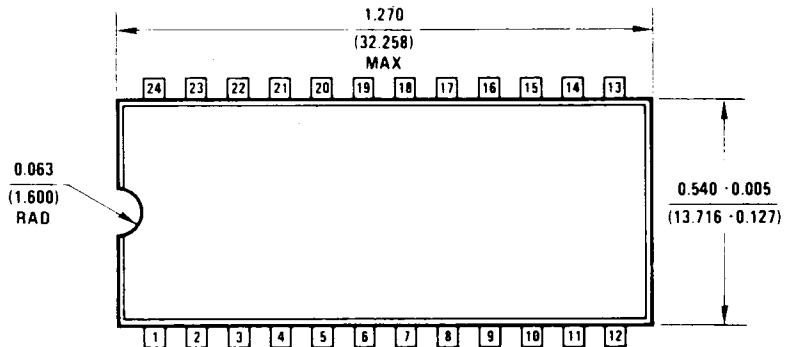
\*SI, SO and SK may also be used for serial I/O

Figure 11. ET9420 Keyboard/Display Interface

**Physical Dimensions** inches (millimeters)



**Molded Dual-In-Line Package (N)**  
**Order Number ET9420 N or ET9320 N**  
**Package Number N28A**



**Molded Dual-In-Line Package (N)**  
**Order Number ET9421N or ET9321 N**  
**Package Number N24A**

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