![Analog Devices logo] **ANALOG DEVICES**

Dual, 16-Bit, 1130 MSPS, TxDAC+ Digital-to-Analog Converter

Enhanced Product

AD9122-EP

FEATURES

Flexible LVDS interface allows word, byte, or nibble load
Single-carrier W-CDMA ACLR = 82 dBc at 122.88 MHz IF
Analog output: adjustable 8.7 mA to 31.7 mA
Integrated 1x/2×/4×/8× interpolator/complex modulator
    allows carrier placement anywhere in the DAC bandwidth
Gain, dc offset, and phase adjustment for sideband
    suppression
Multiple chip synchronization interfaces
High performance, low noise PLL clock multiplier
Digital inverse sinc filter
Low power: 1.5 W at 1.2 GSPS, 800 mW at 500 MSPS, full
    operating conditions
72-lead, exposed paddle LFCSP

ENHANCED PRODUCT FEATURES

Supports defense and aerospace applications (AQEC standard)
Military temperature range (such as −55°C to +105°C)
Controlled manufacturing baseline
One assembly/test site
One fabrication site
Enhanced product change notification
Qualification data available on request

APPLICATIONS

Wireless infrastructure
W-CDMA, CDMA2000, TD-SCDMA, WiMAX, GSM, LTE
Digital high or low IF synthesis
Transmit diversity
Wideband communications: LMDS/MMDS, point-to-point

GENERAL DESCRIPTION

The AD9122-EP is a dual, 16-bit, high dynamic range digital-to-analog converter (DAC) that provides a sample rate of 1130 MSPS, permitting multicarrier generation up to the Nyquist frequency.

The AD9122-EP TxDAC+® includes features optimized for direct conversion transmit applications, including complex digital modulation, and gain and offset compensation. The DAC outputs are optimized to interface seamlessly with analog quadrature modulators, such as the ADL537x F-MOD series from Analog Devices, Inc. A 4-wire serial port interface provides for programming/readback of many internal parameters. Full-scale output current can be programmed over a range of 8.7 mA to 31.7 mA. The AD9122-EP comes in a 72-lead LFCSP. Additional application and technical information can be found in the AD9122 data sheet.

PRODUCT HIGHLIGHTS

1. Ultralow noise and intermodulation distortion (IMD) enable high quality synthesis of wideband signals from baseband to high intermediate frequencies (IF).
2. Proprietary DAC output switching technique enhances dynamic performance.
3. Current outputs are easily configured for various single-ended or differential circuit topologies.
4. Flexible LVDS digital interface allows the standard 32-wire bus to be reduced to one-half or one-quarter of the width.

COMPANION PRODUCTS

IQ Modulators: ADL5370, ADL537x family
IQ Modulators with PLL and VCO: ADRF6701, ADRF670x family
Clock Drivers: AD9516, AD951x family
Voltage Regulator Design Tool: ADIsimPower
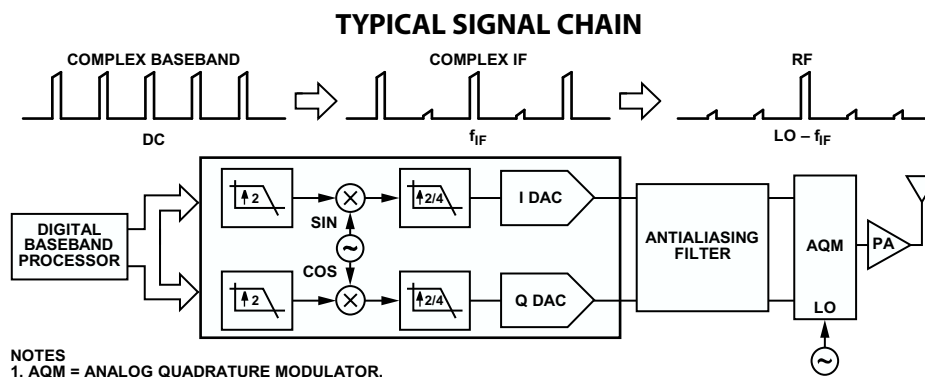**Additional companion products on the AD9122 product page**

TYPICAL SIGNAL CHAIN

NOTES
1. AQM = ANALOG QUADRATURE MODULATOR.

Figure 1.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
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REVISION HISTORY

8/12—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

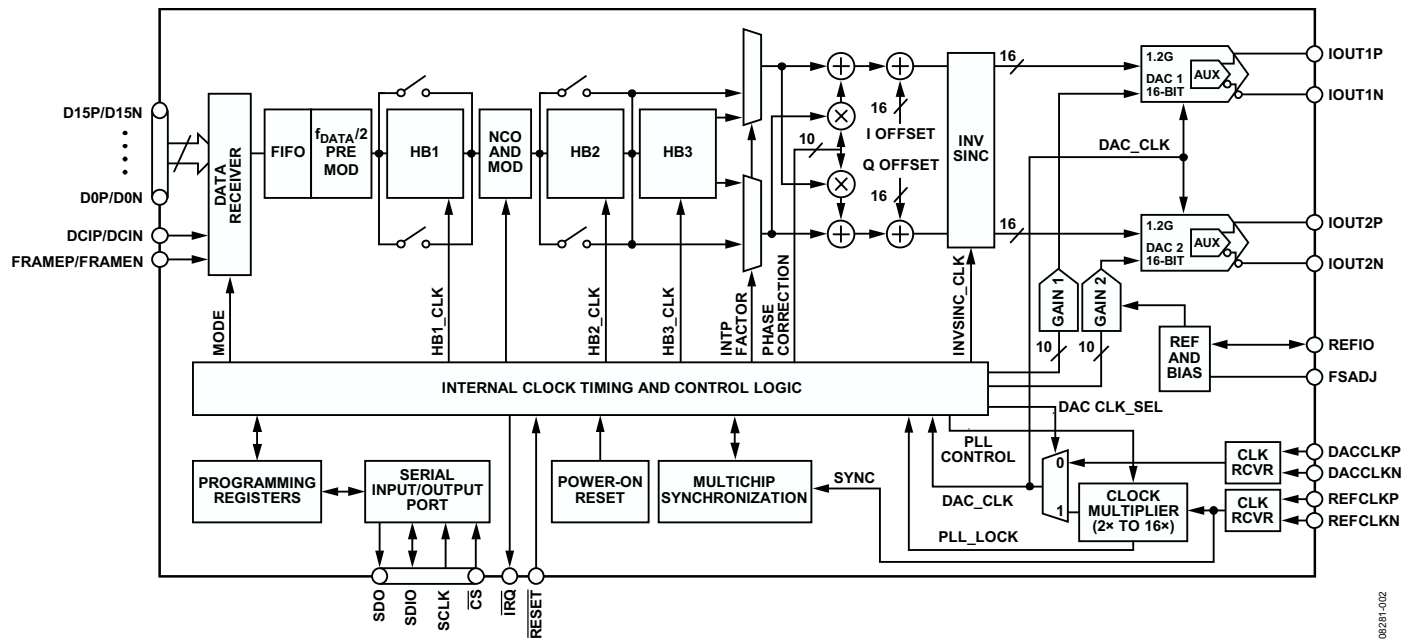*Figure 2.*

SPECIFICATIONS

DC SPECIFICATIONS

T_{MIN} to T_{MAX}, AVDD33 = 3.3 V, DVDD18 = 1.8 V, CVDD18 = 1.8 V, I_{FS} = 20 mA, maximum sample rate, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit
RESOLUTION		16		Bits
ACCURACY				
Differential Nonlinearity (DNL)		±2.1		LSB
Integral Nonlinearity (INL)		±3.7		LSB
MAIN DAC OUTPUTS				
Offset Error	−0.001	0	+0.001	% FSR
Gain Error (with Internal Reference)	−4.6	±2	+4.6	% FSR
Full-Scale Output Current[1]	8.66	19.6	31.66	mA
Output Compliance Range	−1.0		+1.0	V
Power Supply Rejection Ratio, AVDD33	−0.3		+0.3	% FSR/V
Output Resistance		10		MΩ
Gain DAC Monotonicity		Guaranteed		
Settling Time to Within ±0.5 LSB		20		ns
MAIN DAC TEMPERATURE DRIFT				
Offset		0.04		ppm/°C
Gain		100		ppm/°C
Reference Voltage		30		ppm/°C
REFERENCE				
Internal Reference Voltage		1.2		V
Output Resistance		5		kΩ
ANALOG SUPPLY VOLTAGES				
AVDD33	3.13	3.3	3.47	V
CVDD18	1.71	1.8	1.89	V
DIGITAL SUPPLY VOLTAGES				
DVDD18	1.71	1.8	1.89	V
IOVDD	1.71	1.8/3.3	3.47	V
POWER CONSUMPTION				
2× Mode, f_{DAC} = 491.22 MSPS, IF = 10 MHz, PLL Off		834		mW
2× Mode, f_{DAC} = 491.22 MSPS, IF = 10 MHz, PLL On		913		mW
8× Mode, f_{DAC} = 800 MSPS, IF = 10 MHz, PLL Off		1135	1259	mW
AVDD33		55	57	mA
CVDD18		85	90	mA
DVDD18		444	505	mA
Power-Down Mode (Register 0x01 = 0xF0)		6.5	18.8	mW
POWER-UP TIME		260		ms
OPERATING RANGE	−55	+25	+105	°C

[1] Based on a 10 kΩ external resistor between FSADJ and AVSS.

DIGITAL SPECIFICATIONS

T_{MIN} to T_{MAX}, AVDD33 = 3.3 V, IOVDD = 3.3 V, DVDD18 = 1.8 V, CVDD18 = 1.8 V, I_{FS} = 20 mA, maximum sample rate, unless otherwise noted.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
CMOS INPUT LOGIC LEVEL					
Input V_{IN} Logic High	IOVDD = 1.8 V	1.2			V
	IOVDD = 2.5 V	1.6			V
	IOVDD = 3.3 V	2.0			V
Input V_{IN} Logic Low	IOVDD = 1.8 V			0.6	V
	IOVDD = 2.5 V, 3.3 V			0.8	V
CMOS OUTPUT LOGIC LEVEL					
Output V_{OUT} Logic High	IOVDD = 1.8 V	1.4			V
	IOVDD = 2.5 V	1.8			V
	IOVDD = 3.3 V	2.4			V
Output V_{OUT} Logic Low	IOVDD = 1.8 V, 2.5 V, 3.3 V			0.4	V
LVDS RECEIVER INPUTS[1]	Applies to data, DCI, and FRAME inputs				
Input Voltage Range, V_{IA} or V_{IB}		825		1675	mV
Input Differential Threshold, V_{IDTH}		−100		+100	mV
Input Differential Hysteresis, V_{IDTHH} to V_{IDTHL}			20		mV
Receiver Differential Input Impedance, R_{IN}		80		120	Ω
LVDS Input Rate	See Table 5				
DAC CLOCK INPUT (DACCLKP, DACCLKN)					
Differential Peak-to-Peak Voltage		100	500	2000	mV
Common-Mode Voltage	Self-biased input, ac-coupled		1.25		V
Maximum Clock Rate		1230			MHz
REFCLK INPUT (REFCLKP, REFCLKN)					
Differential Peak-to-Peak Voltage		100	500	2000	mV
Common-Mode Voltage			1.25		V
REFCLK Frequency (PLL Mode)	1 GHz ≤ f_{VCO} ≤ 2.1 GHz	15.625		600	MHz
REFCLK Frequency (SYNC Mode)	See the Multichip Synchronization section of the AD9122 data sheet for conditions	0		600	MHz
SERIAL PORT INTERFACE					
Maximum Clock Rate (SCLK)		40			MHz
Minimum Pulse Width High (t_{PWH})				12.5	ns
Minimum Pulse Width Low (t_{PWL})				12.5	ns
Setup Time, SDIO to SCLK (t_{DS})		2.1			ns
Hold Time, SDIO to SCLK (t_{DH})		0.75			ns
Data Valid, SDO to SCLK (t_{DV})		2.85			ns
Setup Time, $\overline{CS}$ to SCLK (t_{DCSB})			1.4		ns

[1] LVDS receiver is compliant with the IEEE 1596 reduced range link, unless otherwise noted.

DIGITAL INPUT DATA TIMING SPECIFICATIONS

Table 3.

Parameter	Value	Unit
LATENCY (DACCLK CYCLES)		
1× Interpolation (With or Without Modulation)	64	Cycles
2× Interpolation (With or Without Modulation)	135	Cycles
4× Interpolation (With or Without Modulation)	292	Cycles
8× Interpolation (With or Without Modulation)	608	Cycles
Inverse Sinc	20	Cycles
Fine Modulation	8	Cycles

AC SPECIFICATIONS

T_{MIN} to T_{MAX}, AVDD33 = 3.3 V, DVDD18 = 1.8 V, CVDD18 = 1.8 V, I_{FS} = 20 mA, maximum sample rate, unless otherwise noted.

Table 4.

Parameter	Min	Typ	Max	Unit
SPURIOUS-FREE DYNAMIC RANGE (SFDR)				
f_{DAC} = 100 MSPS, f_{OUT} = 20 MHz		78		dBc
f_{DAC} = 200 MSPS, f_{OUT} = 50 MHz		80		dBc
f_{DAC} = 400 MSPS, f_{OUT} = 70 MHz		69		dBc
f_{DAC} = 800 MSPS, f_{OUT} = 70 MHz		72		dBc
TWO-TONE INTERMODULATION DISTORTION (IMD)				
f_{DAC} = 200 MSPS, f_{OUT} = 50 MHz		84		dBc
f_{DAC} = 400 MSPS, f_{OUT} = 60 MHz		86		dBc
f_{DAC} = 400 MSPS, f_{OUT} = 80 MHz		84		dBc
f_{DAC} = 800 MSPS, f_{OUT} = 100 MHz		81		dBc
NOISE SPECTRAL DENSITY (NSD), EIGHT-TONE, 500 kHz TONE SPACING				
f_{DAC} = 200 MSPS, f_{OUT} = 80 MHz		−162		dBm/Hz
f_{DAC} = 400 MSPS, f_{OUT} = 80 MHz		−163		dBm/Hz
f_{DAC} = 800 MSPS, f_{OUT} = 80 MHz		−164		dBm/Hz
W-CDMA ADJACENT CHANNEL LEAKAGE RATIO (ACLR), SINGLE-CARRIER				
f_{DAC} = 491.52 MSPS, f_{OUT} = 10 MHz		84		dBc
f_{DAC} = 491.52 MSPS, f_{OUT} = 122.88 MHz		82		dBc
f_{DAC} = 983.04 MSPS, f_{OUT} = 122.88 MHz		83		dBc
W-CDMA SECOND ACLR, SINGLE-CARRIER				
f_{DAC} = 491.52 MSPS, f_{OUT} = 10 MHz		88		dBc
f_{DAC} = 491.52 MSPS, f_{OUT} = 122.88 MHz		86		dBc
f_{DAC} = 983.04 MSPS, f_{OUT} = 122.88 MHz		88		dBc

Table 5. Maximum Rate (MSPS) with DVDD and CVDD Supply Regulation

Bus Width	Interpolation Factor	$f_{INTERFACE}$ (MSPS) DVDD18, CVDD18 =			f_{DAC} (MSPS) DVDD18, CVDD18 =		
		1.8 V ± 5%	1.8 V ± 2%	1.9 V ± 2%	1.8 V ± 5%	1.8 V ± 2%	1.9 V ± 2%
Nibble (4 Bits)	1×	1000	1100	1130	125	137.5	141.25
	2×	1000	1100	1130	250	275	282.5
	4×	1000	1100	1130	500	550	565
	8×	1000	1100	1130	1000	1100	1130
Byte (8 Bits)	1×	1000	1100	1130	250	275	282.5
	2×	1000	1100	1130	500	550	565
	4×	1000	1100	1130	1000	1100	1130
	8×	500	550	565	1000	1100	1130
Word (16 Bits)	1×	1000	1100	1130	500	550	565
	2× (HB1)	800	900	900	800	900	900
	2× (HB2)	1000	1100	1130	1000	1100	1130
	4×	500	550	565	1000	1100	1130
	8×	250	275	282.5	1000	1100	1130

The setup (t_S) and hold (t_H) times, with respect to the edges, are shown in Figure 3. The minimum setup and hold times are shown in Table 6.
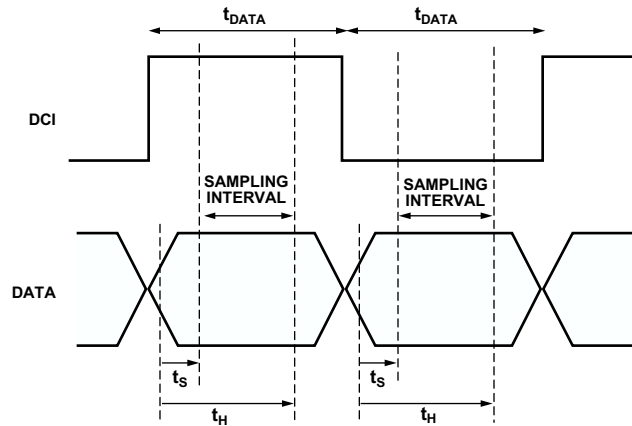

Figure 3. Timing Diagram for Input Data Port

Table 6. Data to DCI Setup and Hold Times

DCI Delay Register 0x16, Bits[1:0]	Minimum Setup Time, t_S (ns)	Minimum Hold Time, t_H (ns)	Sampling Interval (ns)
00	−0.01	0.65	0.64
01	−0.19	0.95	0.76
10	−0.38	1.22	0.84
11	−0.44	1.38	0.94

The data interface timing can be verified by using the sample error detection (SED) circuitry. See the Interface Timing Validation section in the AD9122 data sheet for more information.

ABSOLUTE MAXIMUM RATINGS

Table 7.

Parameter	Rating
AVDD33 to AVSS, EPAD, CVSS, DVSS	−0.3 V to +3.6 V
IOVDD to AVSS, EPAD, CVSS, DVSS	−0.3 V to +3.6 V
DVDD18, CVDD18 to AVSS, EPAD, CVSS, DVSS	−0.3 V to +2.1 V
AVSS to EPAD, CVSS, DVSS	−0.3 V to +0.3 V
EPAD to AVSS, CVSS, DVSS	−0.3 V to +0.3 V
CVSS to AVSS, EPAD, DVSS	−0.3 V to +0.3 V
DVSS to AVSS, EPAD, CVSS	−0.3 V to +0.3 V
FSADJ, REFIO, IOUT1P, IOUT1N, IOUT2P, IOUT2N to AVSS	−0.3 V to AVDD33 + 0.3 V
D[15:0]P, D[15:0]N, FRAMEP, FRAMEN, DCIP, DCIN to EPAD, DVSS	−0.3 V to DVDD18 + 0.3 V
DACCLKP, DACCLKN, REFCLKP, REFCLKN to CVSS	−0.3 V to CVDD18 + 0.3 V
$\overline{\text{RESET}}$, $\overline{\text{IRQ}}$, $\overline{\text{CS}}$, SCLK, SDIO, SDO to EPAD, DVSS	−0.3 V to IOVDD + 0.3 V
Junction Temperature	125°C
Storage Temperature Range	−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

The exposed pad (EPAD) of the 72-lead LFCSP must be soldered to the ground plane (AVSS). The EPAD provides an electrical, thermal, and mechanical connection to the board.

Typical θ_{JA}, θ_{JB}, and θ_{JC} values are specified for a 4-layer board in still air. Airflow increases heat dissipation, effectively reducing θ_{JA} and θ_{JB}.

Table 8. Thermal Resistance

| Package	θ_{JA}	θ_{JB}	θ_{JC}	Unit	Conditions
72-Lead LFCSP	20.7	10.9	1.1	°C/W	EPAD soldered to ground plane

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS
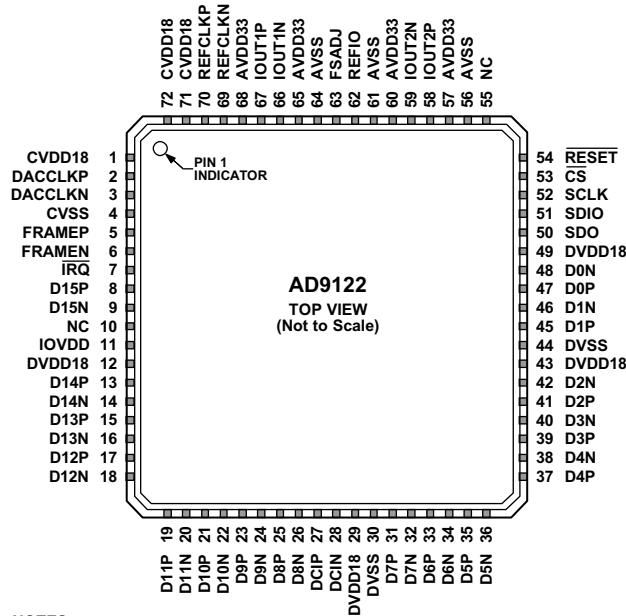
NOTES
1. EXPOSED PAD (EPAD) MUST BE SOLDERED TO THE GROUND PLANE (AVSS). THE EPAD PROVIDES AN ELECTRICAL, THERMAL, AND MECHANICAL CONNECTION TO THE BOARD.
2. NC = NO CONNECT. DO NOT CONNECT TO THIS PIN.

Figure 4. Pin Configuration

Table 9. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	CVDD18	1.8 V Clock Supply. Supplies clock receivers, clock distribution, and PLL circuitry.
2	DACCLKP	DAC Clock Input, Positive.
3	DACCLKN	DAC Clock Input, Negative.
4	CVSS	Clock Supply Common.
5	FRAMEP	Frame Input, Positive. This pin must be tied to DVSS if not used.
6	FRAMEN	Frame Input, Negative. This pin must be tied to DVDD18 if not used.
7	$\overline{IRQ}$	Interrupt Request. Open-drain, active low output. Connect an external pull-up to IOVDD through a 10 kΩ resistor.
8	D15P	Data Bit 15 (MSB), Positive.
9	D15N	Data Bit 15 (MSB), Negative.
10	NC	No Connect. Do not connect to this pin.
11	IOVDD	Supply Pin for Serial Port I/O Pins, $\overline{RESET}$, and $\overline{IRQ}$. 1.8 V to 3.3 V can be supplied to this pin.
12	DVDD18	1.8 V Digital Supply. Supplies power to digital core and digital data ports.
13	D14P	Data Bit 14, Positive.
14	D14N	Data Bit 14, Negative.
15	D13P	Data Bit 13, Positive.
16	D13N	Data Bit 13, Negative.
17	D12P	Data Bit 12, Positive.
18	D12N	Data Bit 12, Negative.
19	D11P	Data Bit 11, Positive.
20	D11N	Data Bit 11, Negative.
21	D10P	Data Bit 10, Positive.
22	D10N	Data Bit 10, Negative.
23	D9P	Data Bit 9, Positive.
24	D9N	Data Bit 9, Negative.

Pin No.	Mnemonic	Description
25	D8P	Data Bit 8, Positive.
26	D8N	Data Bit 8, Negative.
27	DCIP	Data Clock Input, Positive.
28	DCIN	Data Clock Input, Negative.
29	DVDD18	1.8 V Digital Supply. Supplies power to digital core and digital data ports.
30	DVSS	Digital Common.
31	D7P	Data Bit 7, Positive.
32	D7N	Data Bit 7, Negative.
33	D6P	Data Bit 6, Positive.
34	D6N	Data Bit 6, Negative.
35	D5P	Data Bit 5, Positive.
36	D5N	Data Bit 5, Negative.
37	D4P	Data Bit 4, Positive.
38	D4N	Data Bit 4, Negative.
39	D3P	Data Bit 3, Positive.
40	D3N	Data Bit 3, Negative.
41	D2P	Data Bit 2, Positive.
42	D2N	Data Bit 2, Negative.
43	DVDD18	1.8 V Digital Supply. Supplies power to digital core and digital data ports.
44	DVSS	Digital Common.
45	D1P	Data Bit 1, Positive.
46	D1N	Data Bit 1, Negative.
47	D0P	Data Bit 0 (LSB), Positive.
48	D0N	Data Bit 0 (LSB), Negative.
49	DVDD18	1.8 V Digital Supply. Supplies power to digital core and digital data ports.
50	SDO	Serial Port Data Output (CMOS Levels with Respect to IOVDD).
51	SDIO	Serial Port Data Input/Output (CMOS Levels with Respect to IOVDD).
52	SCLK	Serial Port Clock Input (CMOS Levels with Respect to IOVDD).
53	$\overline{CS}$	Serial Port Chip Select, Active Low (CMOS Levels with Respect to IOVDD).
54	$\overline{RESET}$	Reset, Active Low (CMOS Levels with Respect to IOVDD).
55	NC	No Connect. Do not connect to this pin.
56	AVSS	Analog Supply Common.
57	AVDD33	3.3 V Analog Supply.
58	IOUT2P	Q DAC Positive Current Output.
59	IOUT2N	Q DAC Negative Current Output.
60	AVDD33	3.3 V Analog Supply.
61	AVSS	Analog Supply Common.
62	REFIO	Voltage Reference. Nominally 1.2 V output. Should be decoupled to AVSS.
63	FSADJ	Full-Scale Current Output Adjust. Place a 10 kΩ resistor from this pin to AVSS.
64	AVSS	Analog Supply Common.
65	AVDD33	3.3 V Analog Supply.
66	IOUT1N	I DAC Negative Current Output.
67	IOUT1P	I DAC Positive Current Output.
68	AVDD33	3.3 V Analog Supply.
69	REFCLKN	PLL Reference Clock Input, Negative. This pin has a secondary function as a synchronization input.
70	REFCLKP	PLL Reference Clock Input, Positive. This pin has a secondary function as a synchronization input.
71	CVDD18	1.8 V Clock Supply. Supplies clock receivers, clock distribution, and PLL circuitry.
72	CVDD18	1.8 V Clock Supply. Supplies clock receivers, clock distribution, and PLL circuitry.
	EPAD	The exposed pad (EPAD) must be soldered to the ground plane (AVSS). The EPAD provides an electrical, thermal, and mechanical connection to the board.

Table 22A is unique to the AD9122-EP. Refer to the Digital Datapath section of the AD9122 data sheet for further information. All other tables, which have been omitted, can be found in the AD9122 data sheet.

Table 22A. Summary of Data Rates and Bandwidths vs. Interpolation Modes (DVDD18, CVDD18 = 1.9 V ± 2%)

Bus Width	Filter Modes			f_{BUS} (Mbps)	f_{DATA} (Mbps)	Real Signal Bandwidth (MHz)	f_{DAC} (MHz)
	HB3	HB2	HB1				
Nibble (4 Bits)	0	0	0	1130	141.25	69	141.25
	0	0	1	1130	141.25	55	282.5
	0	1	0	1130	141.25	34.5	282.5
	0	1	1	1130	141.25	55	565
	1	1	0	1130	141.25	34.5	565
	1	1	1	1130	141.25	55	1130
Byte (8 Bits)	0	0	0	1130	282.5	188	282.5
	0	0	1	1130	282.5	110	565
	0	1	0	1130	282.5	69	565
	0	1	1	1130	282.5	110	1130
	1	1	0	1130	282.5	69	1130
	1	1	1	565	141.25	55	1130
Word (16 Bits)	0	0	0	1130	565	275	565
	0	0	1	900	450	180	900
	0	1	0	1130	565	138	1130
	0	1	1	565	282.5	110	1130
	1	1	0	565	282.5	69	1130
	1	1	1	282.5	141.25	55	1130

OUTLINE DIMENSIONS
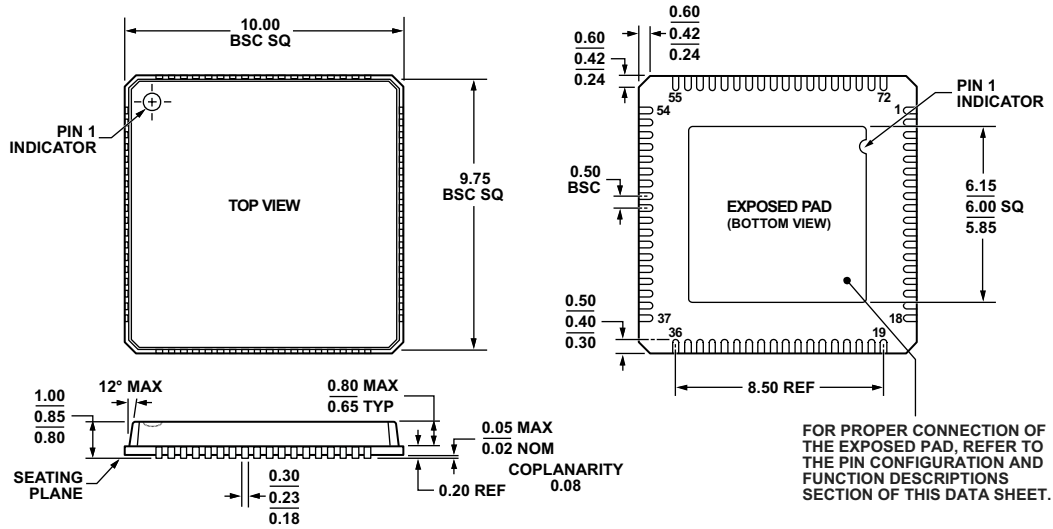
COMPLIANT TO JEDEC STANDARDS MO-220-VNND-4

Figure 5. 72-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
10 mm × 10 mm Body, Very Thin Quad
(CP-72-7)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD9122SCPZ-EP	−55°C to +105°C	72-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-72-7
AD9122SCPZ-EP-RL	−55°C to +105°C	72-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-72-7

[1] Z = RoHS Compliant Part.

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