AN2829
Application note

Dual step-down controller with auxilary voltages for notebook system power

Introduction

The PM6681A is a dual step-down controller with adjustable output voltages that can be used in notebook power systems. This demonstration board represents a typical application circuit. The PM6681A demonstration board allows testing of all functions of the device and provides two switching sections, with (typ.) 1.5 V (OUT1) and 1.05 V (OUT2) outputs from 5.5 V to 28 V input battery voltage. The typical operating switching frequency of the two sections is 200 kHz/300 kHz, respectively. Each switching section delivers more than 5 A of output current. An internal linear regulator provides a fixed 5 V output voltage. Another internal linear regulator provides an adjustable output voltage (default 3.3 V). Both linear regulators can deliver up to 100 mA peak current.

Figure 1. PM6681A demonstration board

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Contents

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1 Main features

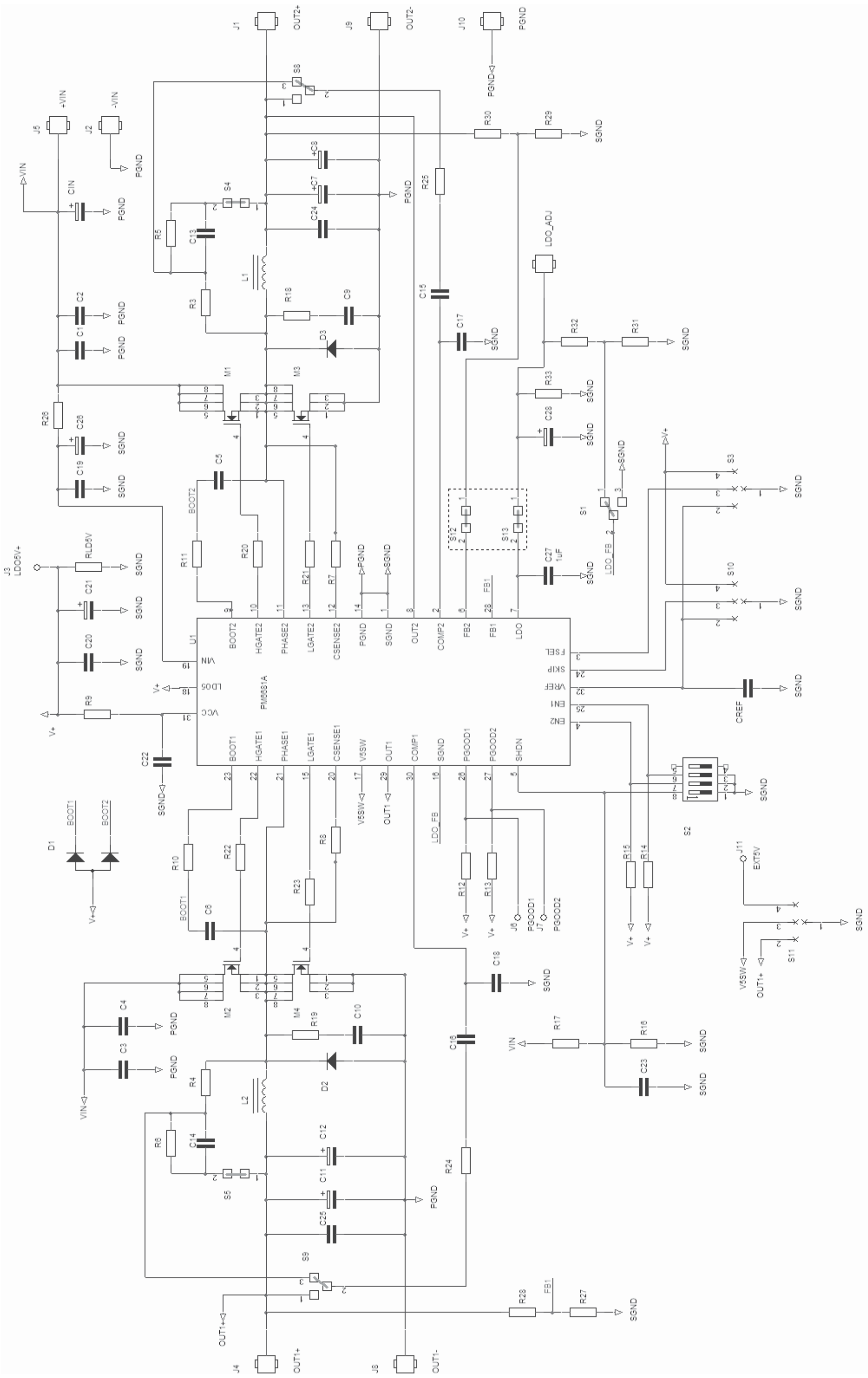
- 5.5 V to 36 V input voltage range
- Adjustable output voltages
- 0.9-3.3 V adjustable LDO delivers 100 mA peak current
- 5 V LDO delivers 100 mA peak current
- 1.237 V ±1% reference voltage available
- Lossless current sensing using low side MOSFET $R_{DS(on)}$
- Negative current limit
- Soft-start internally fixed at 2 ms
- Soft output discharge
- Latched UVP
- Non-latched OVP
- Selectable pulse skipping at light loads
- Selectable minimum frequency (33 kHz) in pulse skip mode
- 4 mW maximum quiescent power
- Independent Power Good signals
- Output voltage ripple compensation.

2 Applications

- Notebook, tablet and slate computers
- Mobile system power supplies
- 3-4 cell Li+ battery-powered devices

3 Demonstration board schematic

Figure 2. Demonstration board schematic diagram



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4 Component list

Table 1. Bill of materials

Qty	Component	Description	Package	Part number	MFR	Value
3	C1:C3	Ceramic capacitor	1812	UMK325BJ106KM-T	Taiyo-Yuden	10 µF - 50 V
1	C4	Ceramic capacitor	1812	NM		10 µF - 50
2	C5, C6	Ceramic capacitor	0805			100 nF - 50 V
1	C19	Ceramic capacitor	0805			100 nF - 50 V
1	C7	POSCAP capacitor	7343	NM	Sanyo	
2	C9, C10	Ceramic capacitor	0805	NM		
1	C11	POSCAP capacitor	7343	NM	Sanyo	
1	C8	POSCAP capacitor	7343	6TPB330M	Sanyo	330 µF - 12 mR - 6 V
1	C12	POSCAP capacitor	7343	6TPB330M	Sanyo	330 µF - 12 mR - 6 V
2	C13, C14	Ceramic capacitor	0603			5.6 nF - 50 V
2	C15, C16	Ceramic capacitor	0603			1 nF - 50 V
2	C17, C18	Ceramic capacitor	0603			47 pF - 50 V
1	C20	Ceramic capacitor	0805			1 µF - 10 V
1	C21	Tantalum capacitor	3216			4.7 µF - 16 V
1	C22	Ceramic capacitor	0805			220 nF - 10 V
1	C23	Ceramic capacitor	0805			10 pF
1	CIN	Electrolytic capacitor	D=10 mm	NM		
1	CREF	Ceramic capacitor	0805			100 nF - 50 V
1	C26	Tantalum capacitor	6032			4.7 µF - 35 V

Table 1. Bill of materials (continued)

Qty	Component	Description	Package	Part number	MFR	Value
1	C24, C25	Tantalum capacitor	0805			10 µF - 6.3 V
1	C27	Tantalum capacitor	0805			10 µF - 6.3 V
1	C28	Tantalum capacitor	3216			4.7 µF - 16 V
1	D1	Dual schottky diode	SOT23	BAT54A	STMicroelectronics	
2	D2, D3	Diode 1 A - 30 V	DO216AA	STPS1L30M	STMicroelectronics	
1	IC1	PM6681A device	QFN-32	PM6681A	STMicroelectronics	
1	L1	Inductor	13 mm x 13 mm	MLC1538-152ML	Coilcraft	1.5 µH - 12 A
1	L2	Inductor	13 mm x 13 mm	MLC1515-252ML	Coilcraf	2.5 µH - 8 A
4	M1:M4	MOSFET control FET	SO-8	STS12NH3LL		
1	R3	Resistor	0805			22 kΩ - 1%
1	R4	Resistor	0805			36 kΩ - 1%
1	R5	Resistor	0805			3.3 kΩ - 1%
1	R6	Resistor	0805			3 kΩ - 1%
2	R7, R8	Resistor	0805			680 Ω - 1%
1	R9	Resistor	0805			47 Ω - 1%
2	R10, R11	Resistor	0805			10 Ω - 1%
4	R12:R15	Resistor	0805			100 kΩ - 1%
1	R16	Resistor	0805			150 kΩ - 1%
1	R17	Resistor	0805			560 kΩ - 1%
2	R18, R19	Resistor	0805	NM		
4	R20, R21, R22, R23	Resistor	0805			0 Ω - 1%
1	R24	Resistor	0805			1.1 kΩ - 1%
1	R25	Resistor	0805			820 Ω - 1%
1	R26	Resistor	1206			3.9 Ω - 1%
1	R27	Resistor	0805			10 kΩ - 1%
1	R29	Resistor	0805			11 kΩ - 1%
1	R28	Resistor	0805			6.8 kΩ - 1%
1	R30	Resistor	0805			1.8 kΩ - 1%

Table 1. Bill of materials (continued)

Qty	Component	Description	Package	Part number	MFR	Value
1	R31	Resistor	0603			5.6 kΩ - 1%
1	R32	Resistor	0603			15 kΩ - 1%
1	RLD5V, RLD3V	Resistor	0805	NM		

5 Demonstration board layout

Figure 3. PM6681A demonstration board layout - top layer (PGND plane and component side)

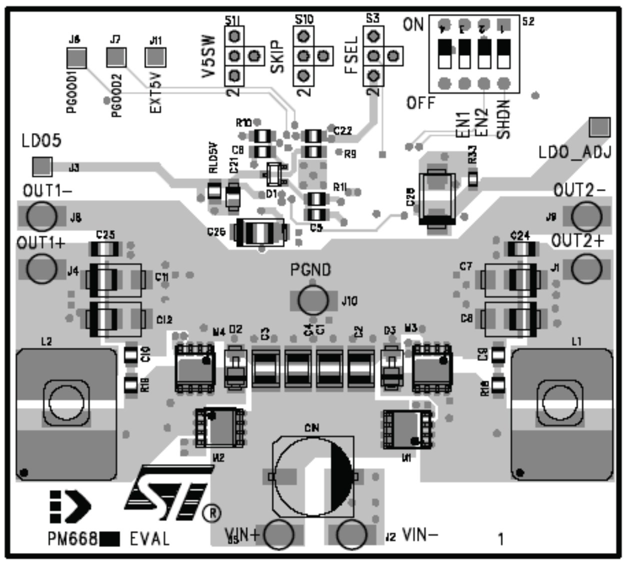

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Figure 4. PM6681A demonstration board layout - inner layer 1 (SGND layer and V_{IN} plane)

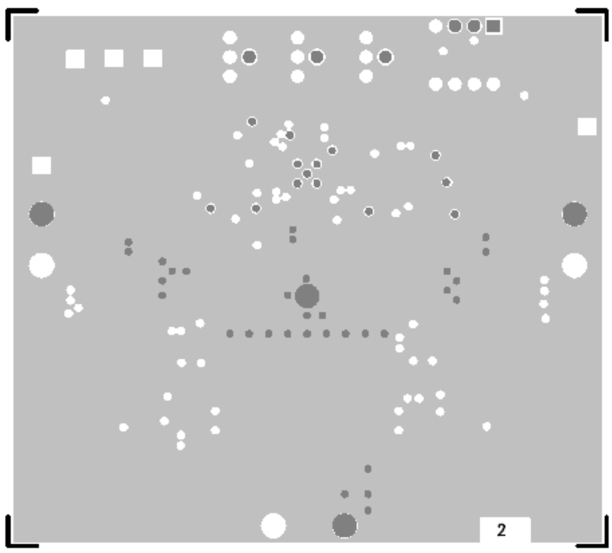

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Figure 5. PM6681A demonstration board layout - inner layer 2 (SGND layer and signals)

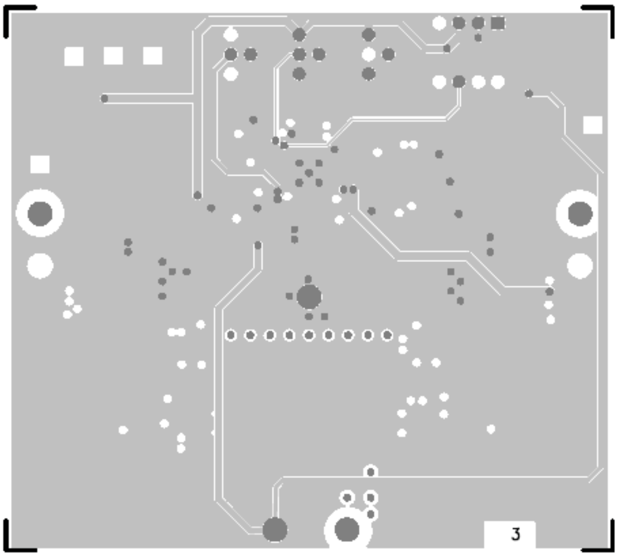

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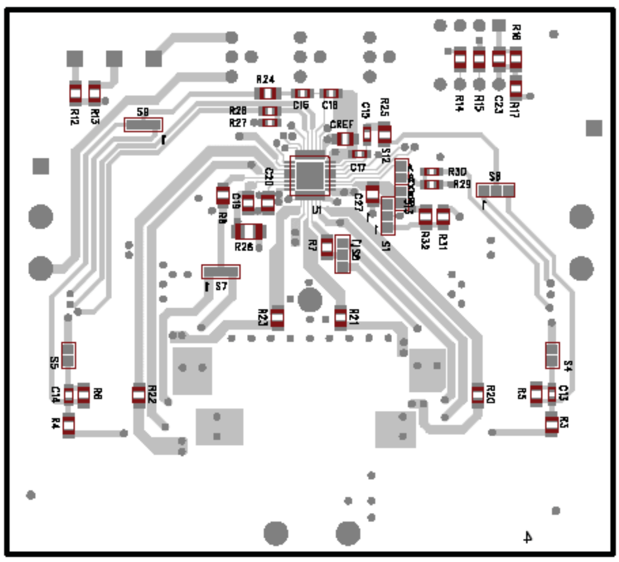
Figure 6. PM6681A demonstration board layout - bottom layer (PM6681A and component side)



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6 I/O interface

The demonstration board has the following test points:

Table 2. Demonstration board test points

Test point	Description
V_{IN}+	Input voltage
V_{IN}-	Input voltage ground
LDO5	5 V linear regulator output
LDO_ADJ	Adjustable linear regulator output
EXT5V	5 V external input
OUT1+	OUT1 switching section output
OUT1-	OUT1 switching section output ground
PGOOD1	OUT1 switching section Power Good
OUT2+	OUT2 switching section output
OUT2+	OUT2 switching section output ground
PGOOD2	OUT2 switching section Power Good
J10	Junction pin between PGND and SGND planes

7 Recommended equipment

- 5.5 V to 36 V power supply, notebook battery or AC adapter
- Active loads
- Digital multimeters
- 500 MHz four-trace oscilloscope

8 Quick start

1. Connect VIN+ and VIN- test points of the demonstration board to an external power supply.
2. Ensure that all switches of DIP-switch "S2" are "OFF". In this condition all outputs are disabled (shutdown-mode).
3. Turn "S21"on (SHDN pin high). The LDO5 and LDO_ADJ outputs turn-on (standby-mode).
4. Turn "S22" on (EN1 pin high). The 1.5 V switching controller brings its output into regulation. The PGood1 pin goes high after soft-start.
5. Turn "S23" on (EN2 pin high). The 1.05 V switching controller brings its output into regulation. The PGood2 pin goes high after soft-start.
6. In order to load the switching outputs, loads must be connected between the "+" and the "-" output test points, respectively.
7. In order to load the LDO5 linear output, loads must be connected between J10 and LDO5 or resistor RLD5V can be mounted on the demonstration board.
8. In order to load the LDO_ADJ linear output, loads must be connected between J10 and LDO_ADJ or the alternative resistor R33 can be mounted on the demonstration board.

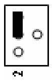
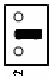
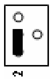
9 Jumper settings

It is possible to select different working conditions by using the jumpers:

Note: *Please note that jumpers S1, S12 and S13 are already soldered on the demonstration board, and it is not necessary to change them. Refer to the schematic to check their proper connection.*

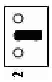
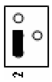
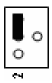
- External bypass connections for the linear regulator LDO5(V5SW)

Table 3. Jumper S11 (connect V5SW pin to S11)

Position	LDO5 working conditions
OUT5V 	When the main ouput voltage is greater than the bootstrap-switchover threshold, an internal 3 Ω (max) P-channel MOSFET switch connects the V5SW pin to the LDO5 pin, shutting down the LDO5 internal linear regulator. If not used, it must be connected to ground.
SGND 	The internal linear regulator LDO5 is always on. In this case LDO5 supplies all gate drivers and the internal circuitry. It can provide an output peak current of 100mA.
EXT5V 	The internal linear regulator LDO5 remains off if an alternative 5 V external voltage is applied to the EXT5V test-point. An internal 3 Ω (max) P-channel MOSFET switch connects the V5SW pin to the LDO5 output. The gate drivers and internal circuitry are supplied by the same 5 V external voltage applied.

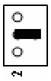
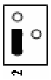
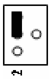
- SMPS frequency selection (FSEL)

Table 4. Jumper S3 (connect FSEL pin to S3)

Position	SMPS OUT1	SMPS OUT2
SGND 	200 kHz	325 kHz
VREF 	290 kHz	425 kHz
LDO5 	390 kHz	590 kHz

- SMPS mode selection (skip)

Table 5. Jumper S10 (connect SKIP pin to S10)

Position	Switching operating mode
GND 	If the SKIP pin is tied to ground, pulse-skip mode occurs at light loads. A zero crossing comparator prevents the inductor current from going negative.
VREF 	Connecting the SKIP pin to the VREF pin enables pulse skip mode with a minimum switching frequency of approximately 25 kHz (ultrasonic mode).
LDO5 	If the SKIP pin is tied to 5 V, fixed PWM mode occurs. The switching output is in a position to sink and source current from the load.

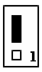
10 Feedback output connections

- Loop compensation network for very low output voltage ripple.

Table 6. Jumper S4, S5

Position	Output ripple compensation
Short	Virtual ESR output ripple is generated by using a compensation network connected between the output and the PHASE pin of the switching section.

Table 7. Jumper S8, S9

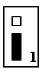
Position	Feedback connection
	Controller feedback signal connected to the compensation network.

- Loop compensation network for high output voltage ripple

Table 8. Jumper S4, S5

Position	Output ripple compensation
Open	ESR output ripple is used.

Table 9. Jumper S8, S9

Position	Feedback connection
	Controller feedback signal connected directly to the output capacitor.

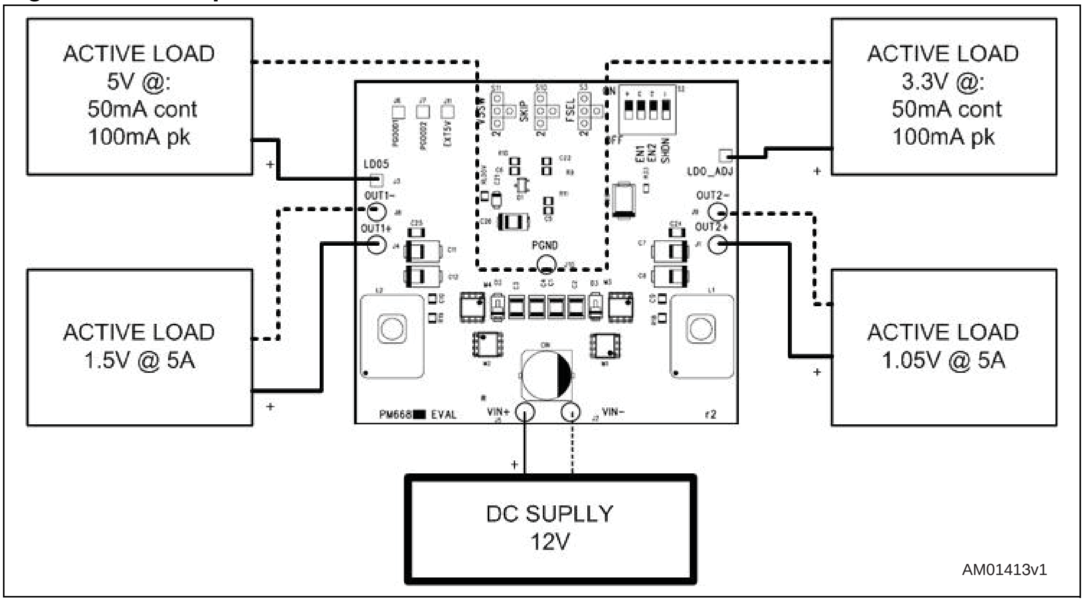
11 Test setup and performance summary

11.1 Test setup

The PM6681A demonstration board has the following input/output connections:

– 12 V input through J5-J2 (V_{IN}+ and V_{IN}-)
– 1.5 V SMPS output through J4-J13 (OUT1+ and OUT1-)
– 1.05 V SMPS output through J1-J12 (OUT2+ and OUT2-)
– 3.3 V linear regulator output through LDO_ADJ - J10
– 5 V linear regulator output through LDO5 - J3 (LDO5)
– A power supply capable of supplying at least 6 A should be connected to V_{IN}+, V_{IN}- and two active loads should be connected respectively to OUT1+, OUT1- and OUT2+, OUT2-.

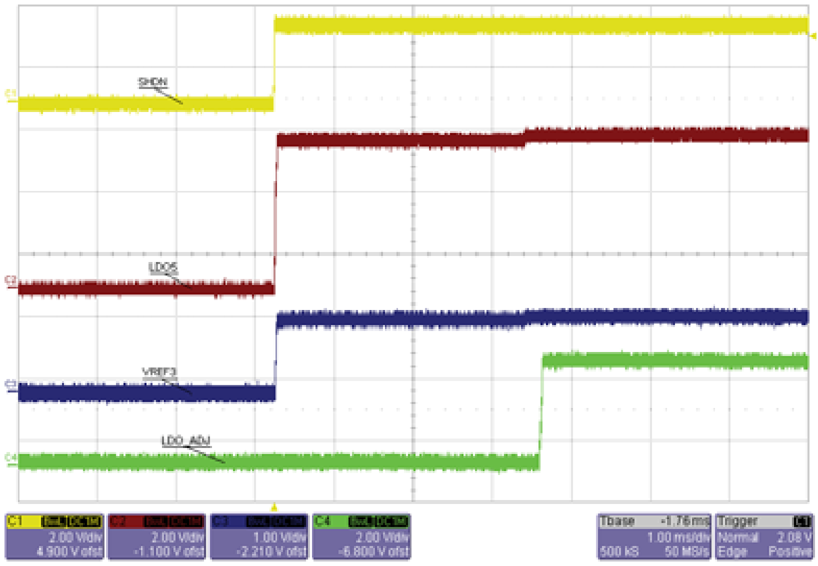
Figure 7. Setup connections



11.2 Power-up

As shown in *Figure 8*, power-up starts when the input voltage is applied and the voltage on the SHDN pin is above the device on threshold (1.5 V). First the LDO5 goes up with a masking time of about 4 ms. If the LDO5 output is above the UVLO threshold at this time, the device enters standby mode and the adjustable internal linear regulator LDO is turned on.

Figure 8. REF, LDO5 and LDO power-up



11.3 Soft-start and shutdown waveforms

Figure 9, *10*, *11* and *12* show, respectively, the soft-start and shutdown waveforms.

The PM681A has an independent internal digital soft-start for each switching section. During the soft-start phase the internal current limit increases from 25% to 100% with steps of 25% to avoid the inductor current rising abruptly.

Figure 9. Section 1 soft-start waveforms

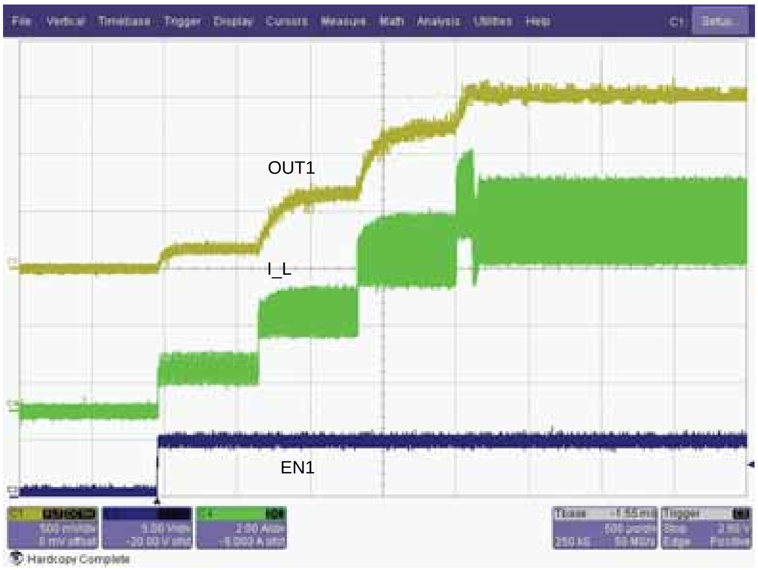


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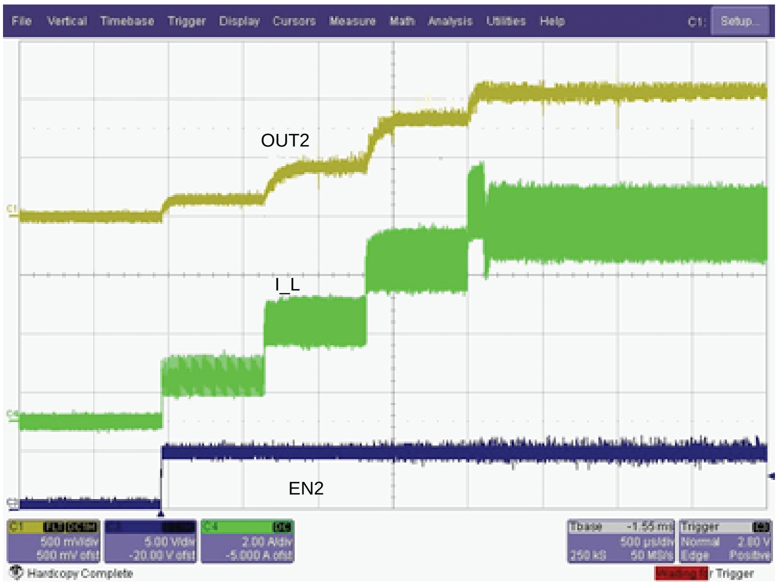
Figure 10. Section 2 soft-start waveforms



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Driving the EN1, EN2 pins below the EN off threshold (0.8 V), the switching outputs are connected to ground through an internal 12 Ω P-MOSFET and are discharged gradually, (discharge mode). When the output voltages reach 0.3 V, the low-side MOSFETs are turned on, quickly discharging them to ground.

Figure 11. Section 1 shutdown waveforms

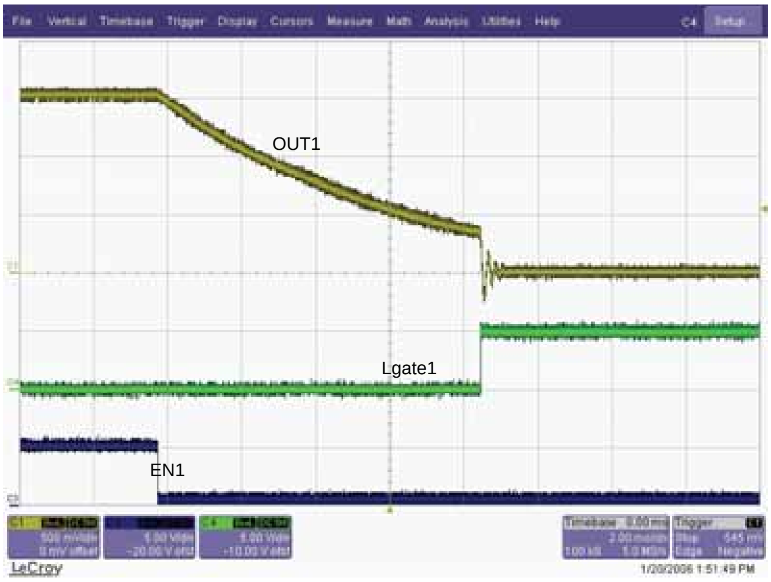

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Figure 12. Section 2 shutdown waveforms

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11.4 1.5 V and 1.05 output efficiency vs. load current

Figure 13 and *14* show the efficiency versus load current at different input voltage values in PWM mode, skip mode and no audible skip mode. Three different input voltages are used:

- Blue: V_{IN}=9 V
- Green: V_{IN}=12 V
- Red: V_{IN}=18 V

Figure 13. 1.5 V SMPS efficiency

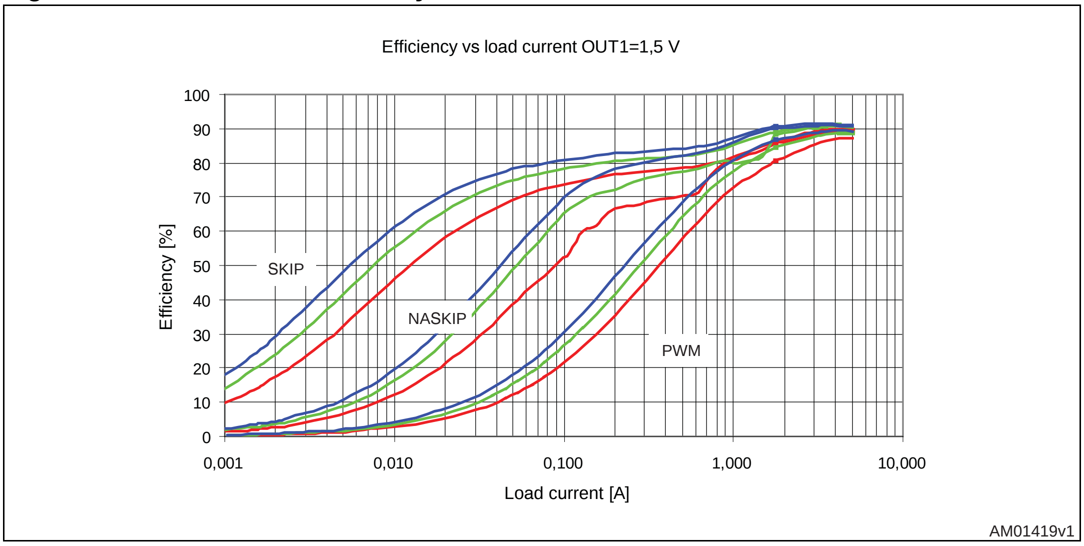
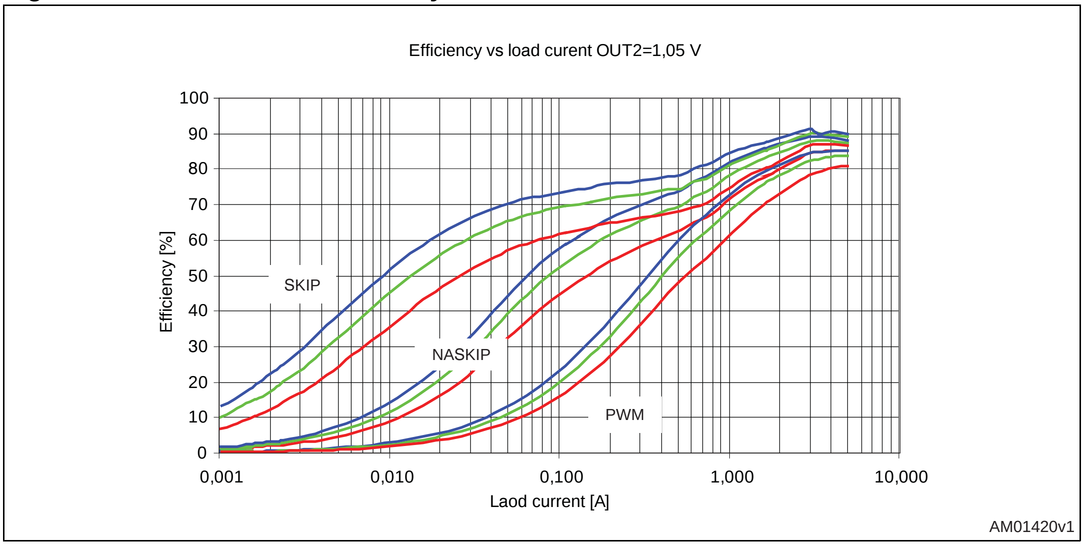


Figure 14. 1.05 V SMPS efficiency



11.5 Power consumption analysis

To measure the consumption of the device in real working conditions, an external power supply of +5 V is connected to EXT5V.

The two traces on the following figures show the differentiation in the two input currents. Once the internal linear regulator is turned on, the device consumption increases.

Figure 15 shows the input current consumption measured at V_{IN}+ (including ISHDN) and the input device current consumption measured by the VCC pin. Both switching sections work in forced PWM mode. No load is applied on the outputs.

Figure 15. Input current vs. input voltage

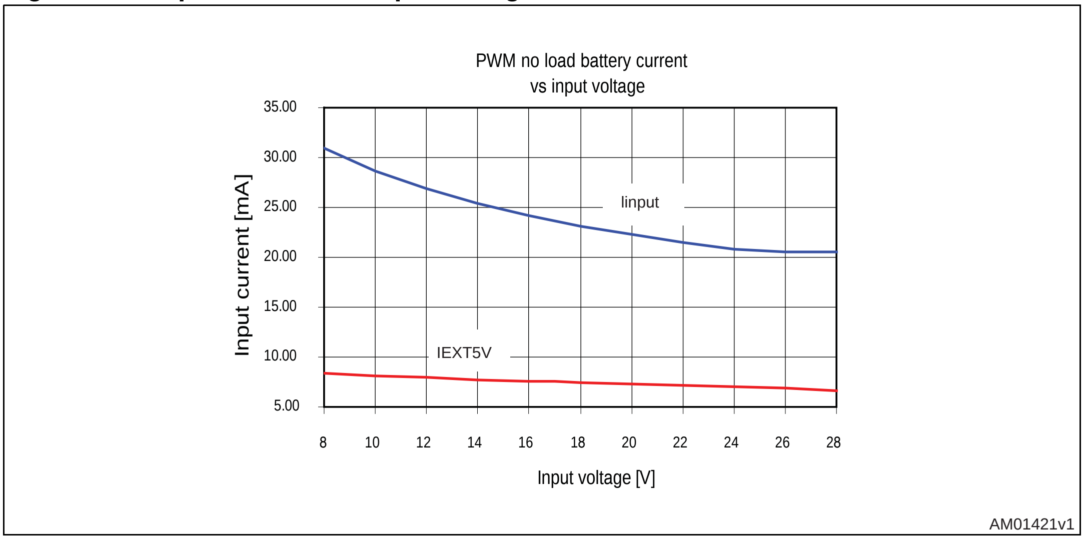


Figure 16 shows the input current consumption measured at V_{IN}+. Both switching sections work in pulse skip mode. No load is applied on the outputs.

Figure 16. Input current vs. input voltage

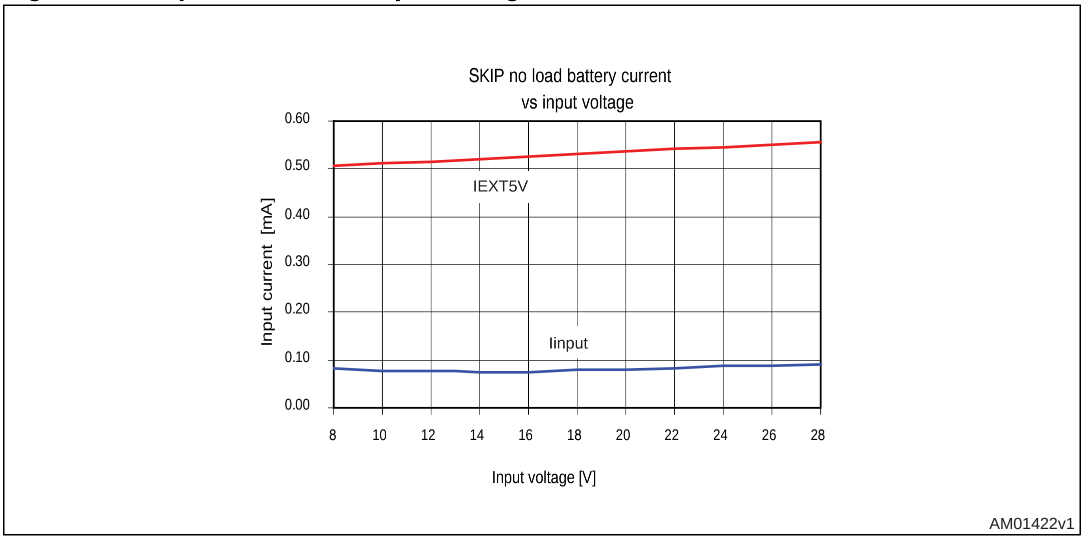
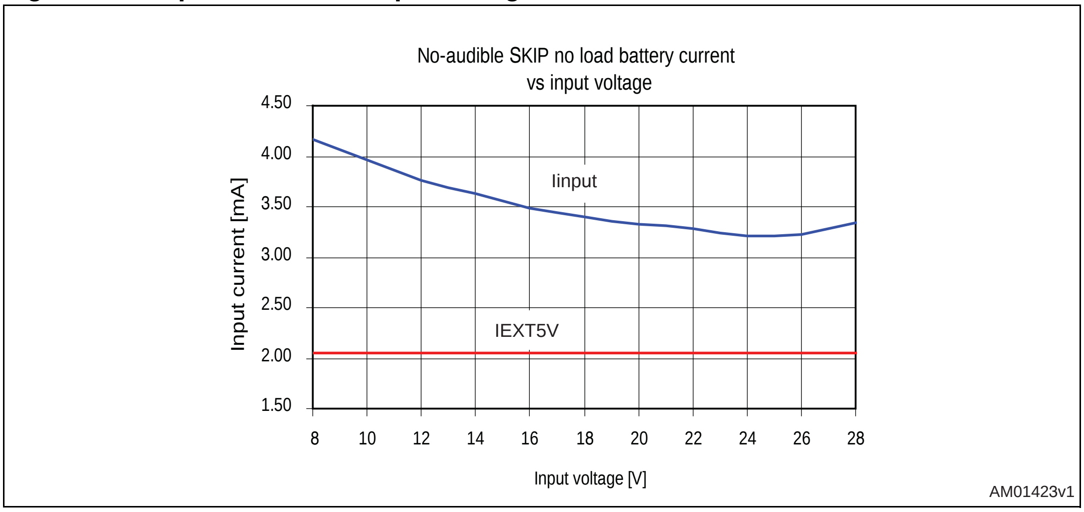


Figure 17 shows the input current consumption measured at V_{IN}+. Both switching sections work in no audible skip mode. No load is applied on the outputs.

Figure 17. Input current vs. input voltage



In the following figures, the device current consumption is measured in shutdown mode. In shutdown mode all outputs are off (SHDN pin low). In standby mode only the linear regulators output are on (V5SW=SGND; SHDN pin high; EN5, EN3 pins low).

Figure 18. Device current consumption vs. input voltage

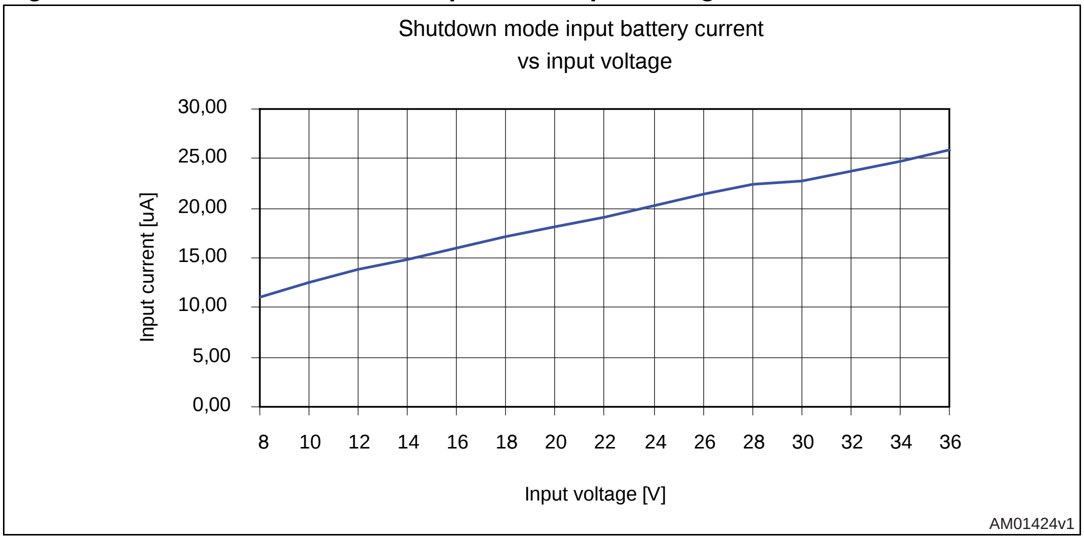
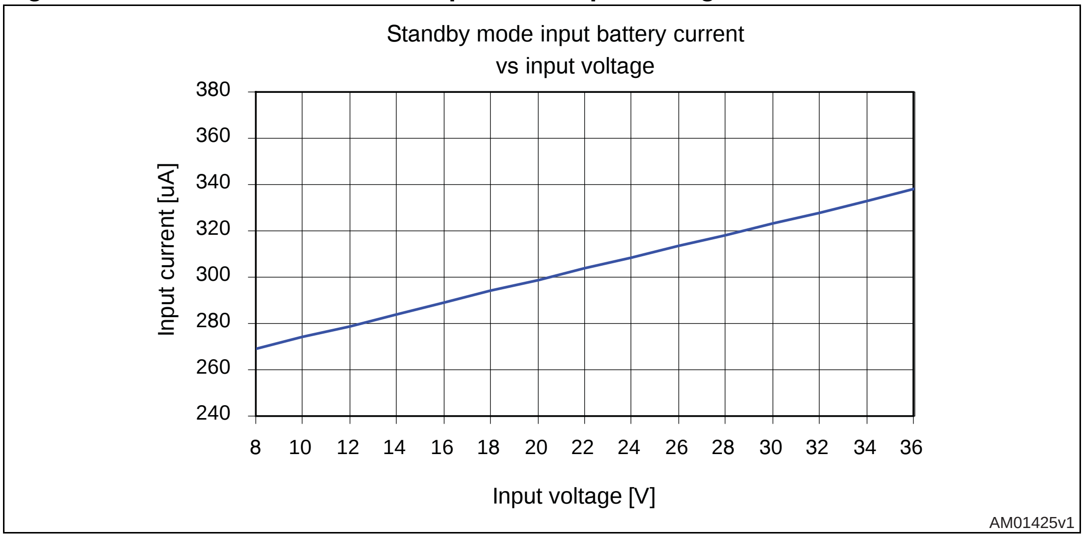


Figure 19. Device current consumption vs. input voltage



11.6 Switching frequency vs. load current

Figure 20 and *21* show the switching frequency variation with the load current in PWM mode, skip mode and no audible skip mode. 12 V is applied at the V_{IN}+ and V_{IN}- test points.

Figure 20. 1.5 V output switching frequency vs. load current

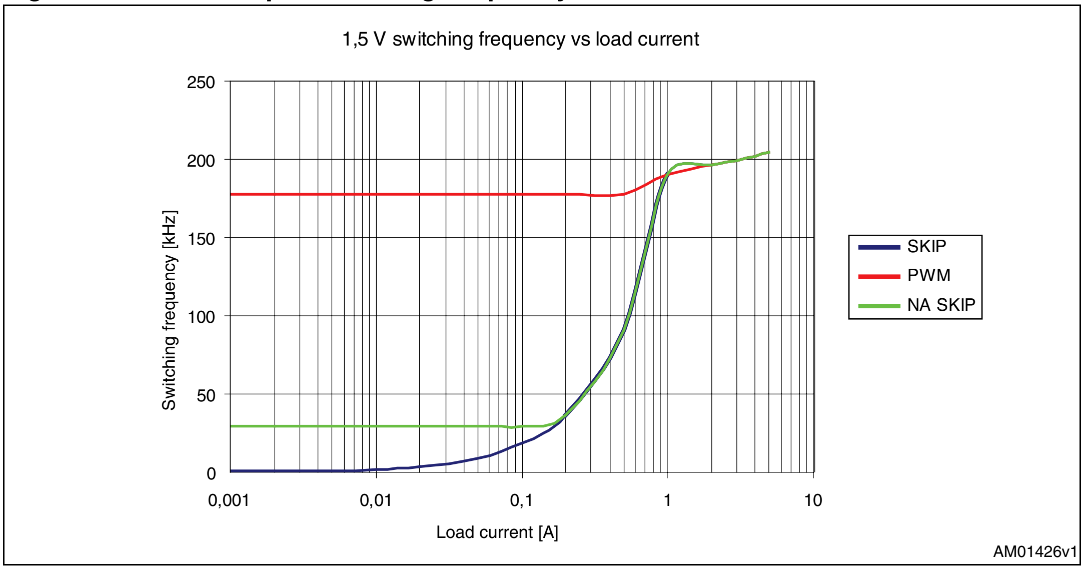
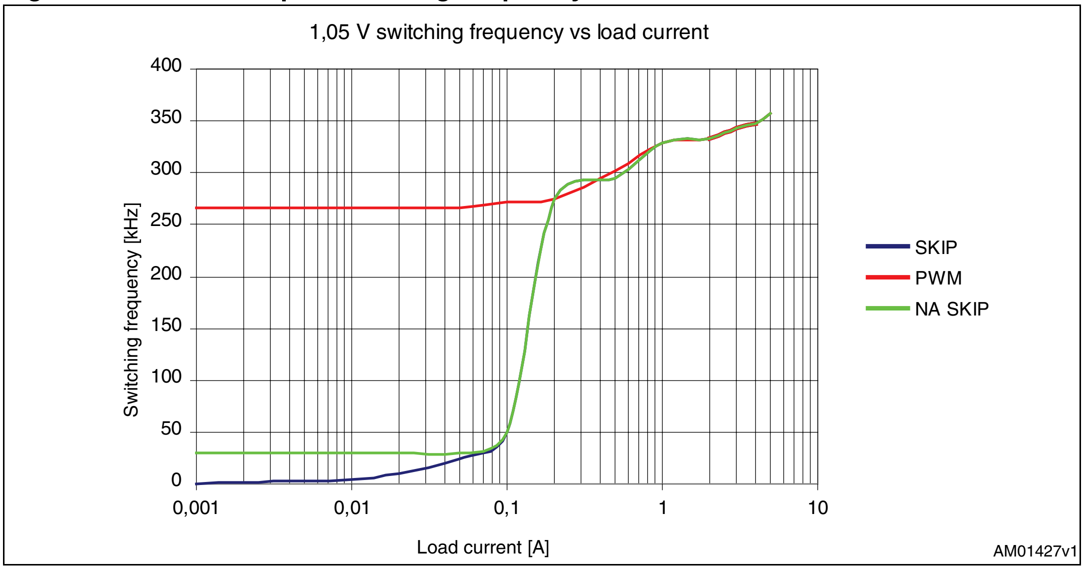


Figure 21. 1.05 V output switching frequency vs. load current



11.7 Linear regulator output voltages vs. output current

Figure 22 and *23* show the load regulation respectively for the internal linear regulators LDO5 and the adjustable linear regulator LDO_ADJ. Both switching sections are disabled. 12 V is applied at the V_{IN}+ and V_{IN}- test points.

Figure 22. LDO5 output vs. load current

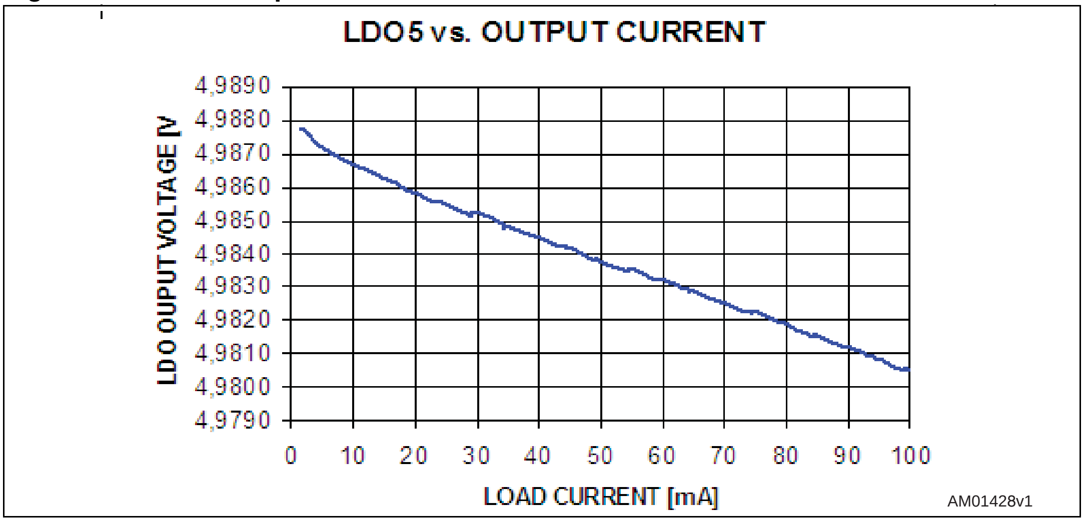
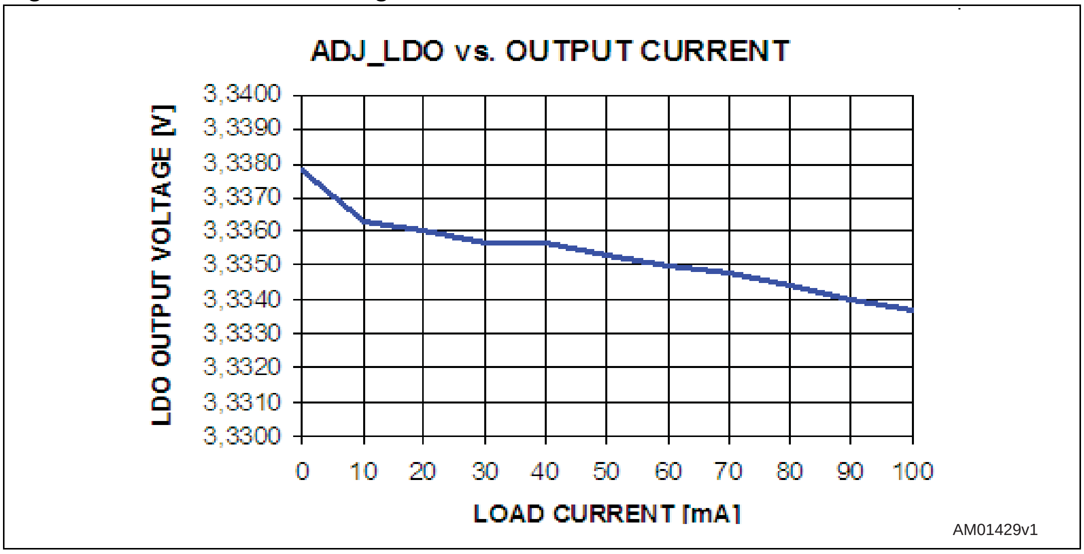


Figure 23. ADJ_LDO load regulation



11.8 Load transient response

The following figures show the load transient response from 1 A to 4 A for both switching outputs. In both cases the PM6681A works in forced PWM mode (the SKIP pin is high).

Figure 24. SMPS 1.5 V load transient response

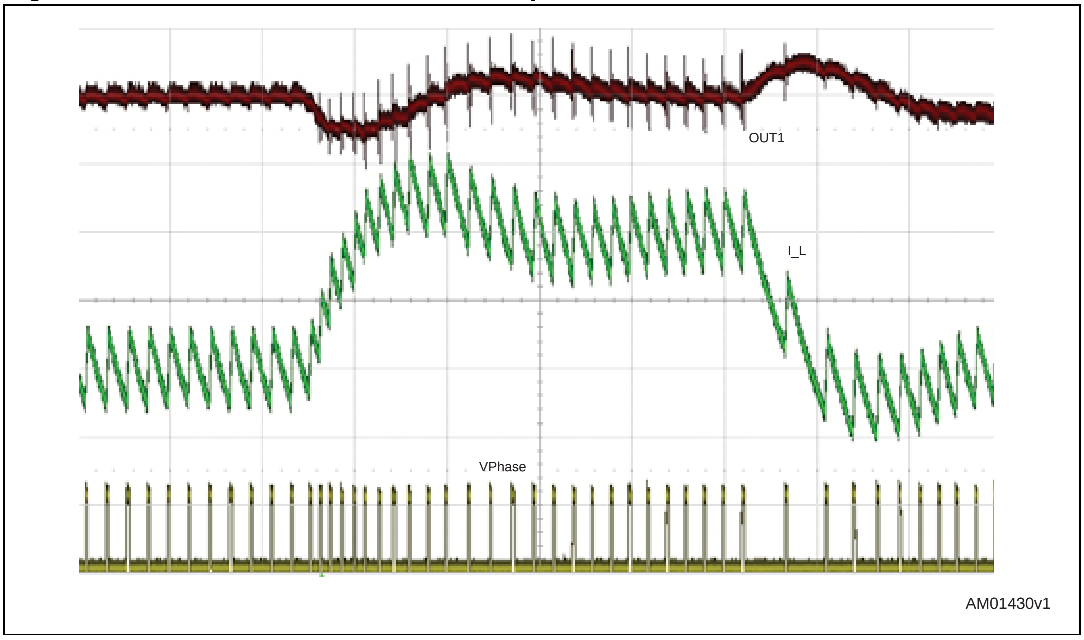
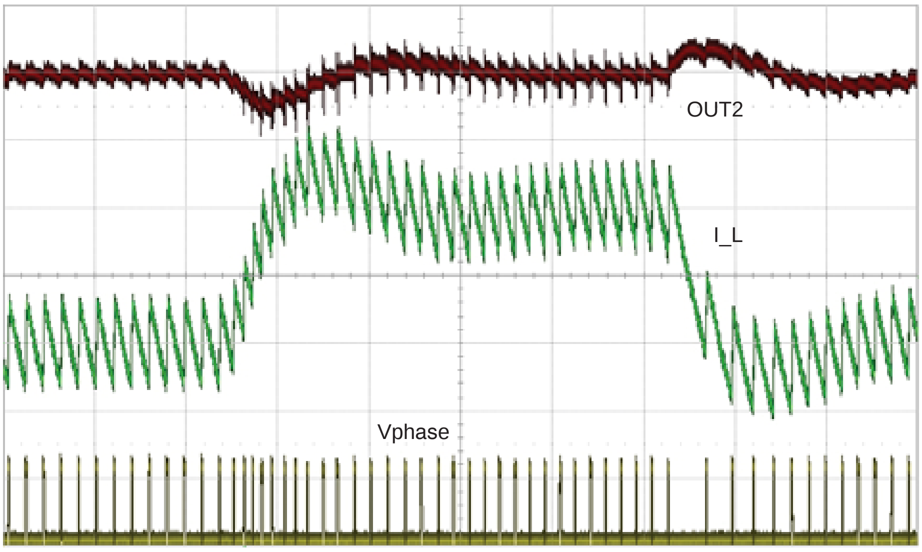


Figure 25. SMPS 1.05 V load transient response



12 Representative waveforms

The following figures show the relevant waveforms of a switching section, to underline the behavior of the device in different working conditions: pulse skip mode, no-audible skip mode and forced PWM mode.

Figure 26. SMPS pulse skip mode

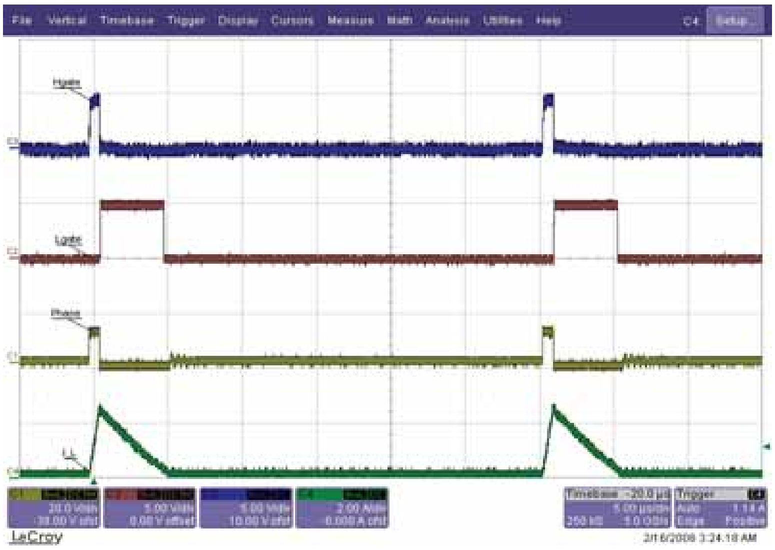


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Figure 27. SMPS no-audible skip mode

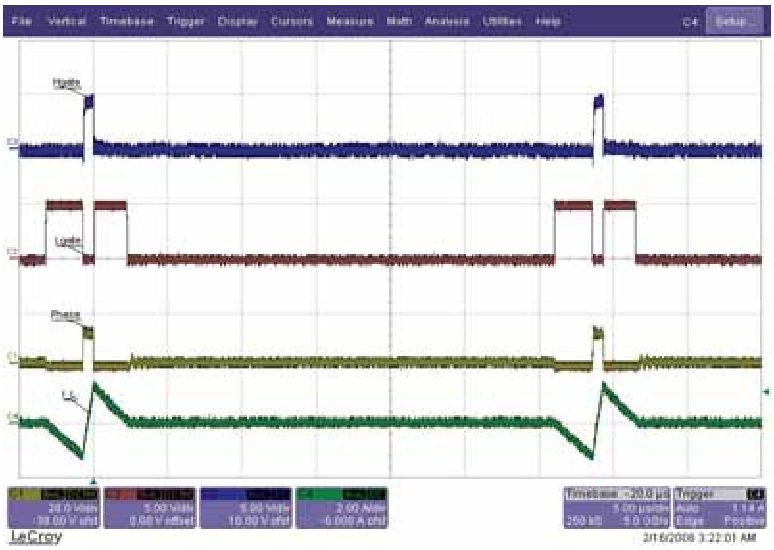

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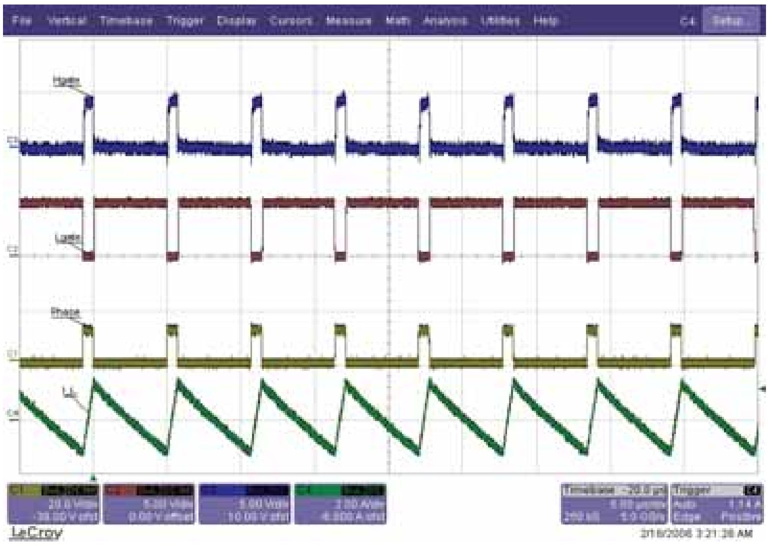
Figure 28. SMPS PWM mode



13 Revision history

Table 10. Document revision history

Date	Revision	Changes
25-Feb-2009	1	Initial release