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April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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HAT2200R

Silicon N Channel Power MOS FET
Power Switching

REJ03G0232-0200Z

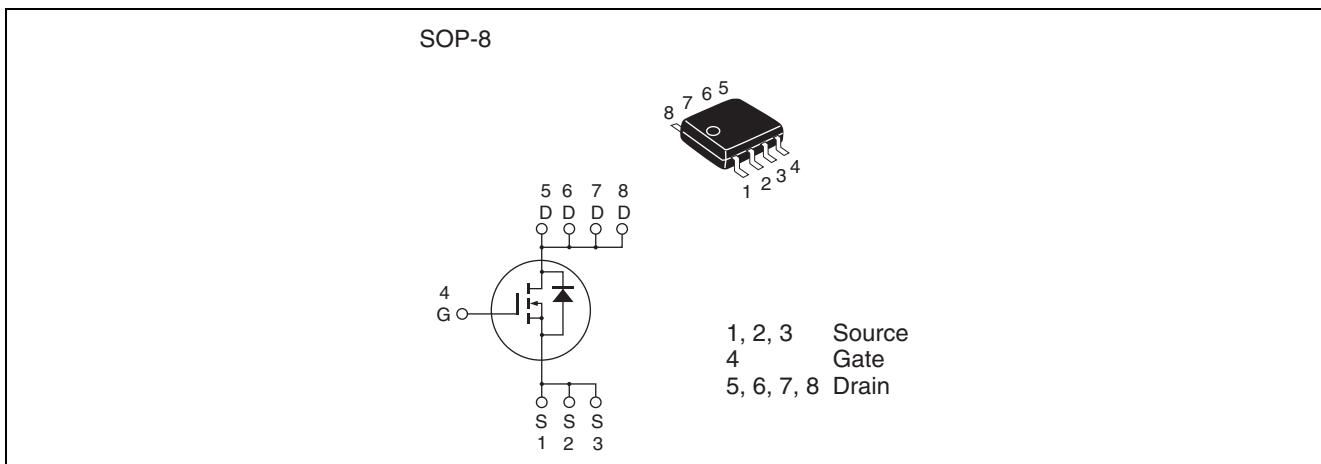
Rev.2.00

Apr.05.2004

Features

- Capable of 8 V gate drive
- Low drive current
- High density mounting
- Low on-resistance
 $R_{DS(on)} = 22 \text{ m}\Omega$ typ. (at $V_{GS} = 10 \text{ V}$)

Outline



Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V _{DSS}	100	V
Gate to source voltage	V _{GSS}	±20	V
Drain current	I _D	8	A
Drain peak current	I _{D(pulse)} ^{Note1}	64	A
Body-drain diode reverse drain current	I _{DR}	8	A
Avalanche current	I _{AP} ^{Note2}	8	A
Avalanche energy	E _{AR} ^{Note2}	6.4	mJ
Channel dissipation	P _{ch} ^{Note3}	2.5	W
Channel to Ambient Thermal Impedance	θ _{ch-a} ^{Note3}	50	°C/W
Channel temperature	T _{ch}	150	°C
Storage temperature	T _{stg}	-55 to +150	°C

- Notes: 1. PW ≤ 10 μs, duty cycle ≤ 1%
 2. Value at T_{ch} = 25°C, R_g ≥ 50 Ω
 3. When using the glass epoxy board (FR4 40 x 40 x 1.6 mm), PW ≤ 10s

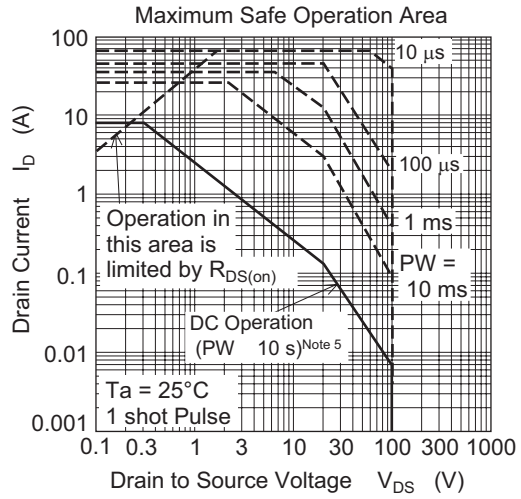
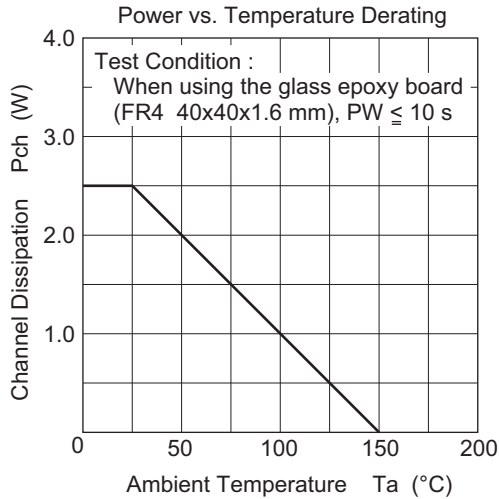
Electrical Characteristics

(Ta = 25°C)

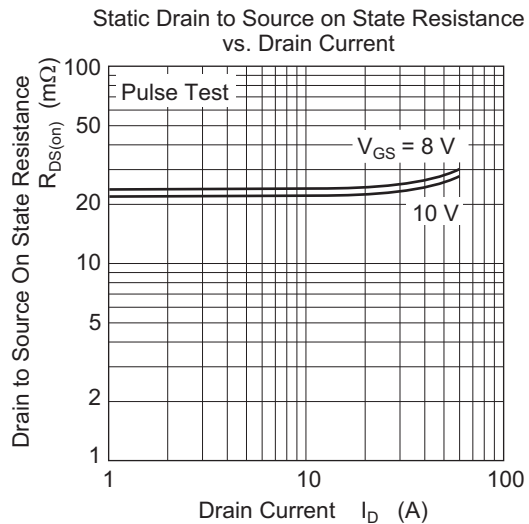
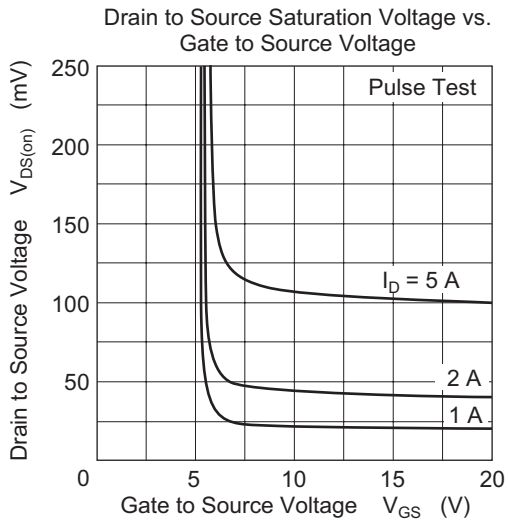
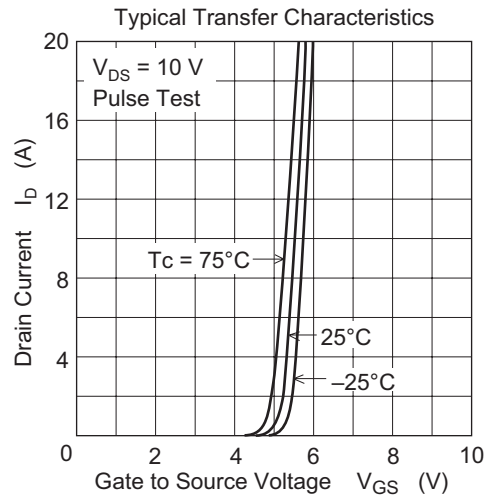
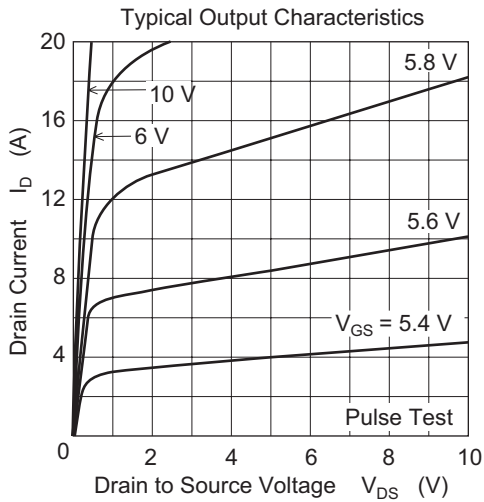
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	V _{(BR)DSS}	100	—	—	V	I _D = 10 mA, V _{GS} = 0
Gate to source leak current	I _{GSS}	—	—	± 0.1	μA	V _{GS} = ±20 V, V _{DS} = 0
Zero gate voltage drain current	I _{DSS}	—	—	1	μA	V _{DS} = 100 V, V _{GS} = 0
Gate to source cutoff voltage	V _{GS(off)}	3.5	—	5.0	V	V _{DS} = 10 V, I _D = 1 mA
Static drain to source on state resistance	R _{DS(on)}	—	22	28	mΩ	I _D = 4 A, V _{GS} = 10 V ^{Note4}
	R _{DS(on)}	—	23	33	mΩ	I _D = 4 A, V _{GS} = 8 V ^{Note4}
Forward transfer admittance	y _{fs}	8	14	—	S	I _D = 4 A, V _{DS} = 10 V ^{Note4}
Input capacitance	C _{iss}	—	2300	—	pF	V _{DS} = 10 V
Output capacitance	C _{oss}	—	280	—	pF	V _{GS} = 0
Reverse transfer capacitance	C _{rss}	—	90	—	pF	f = 1 MHz
Gate Resistance	R _g	—	1.3	—	Ω	
Total gate charge	Q _g	—	32	—	nC	V _{DD} = 50 V
Gate to source charge	Q _{gs}	—	12	—	nC	V _{GS} = 10 V
Gate to drain charge	Q _{gd}	—	8	—	nC	I _D = 8 A
Turn-on delay time	t _{d(on)}	—	16	—	ns	V _{GS} = 10 V, I _D = 4 A
Rise time	t _r	—	4	—	ns	V _{DD} ≅ 30 V
Turn-off delay time	t _{d(off)}	—	32	—	ns	R _L = 7.5 Ω
Fall time	t _f	—	4.5	—	ns	R _g = 4.7 Ω
Body–drain diode forward voltage	V _{DF}	—	0.79	1.03	V	I _F = 8 A, V _{GS} = 0 ^{Note4}
Body–drain diode reverse recovery time	t _{rr}	—	45	—	ns	I _F = 8 A, V _{GS} = 0 diF/ dt = 100 A/ μs

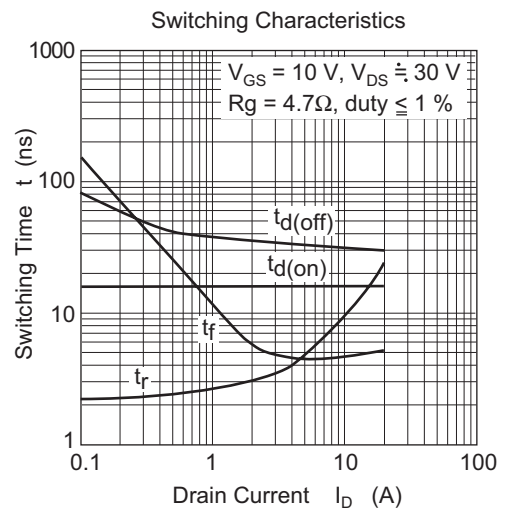
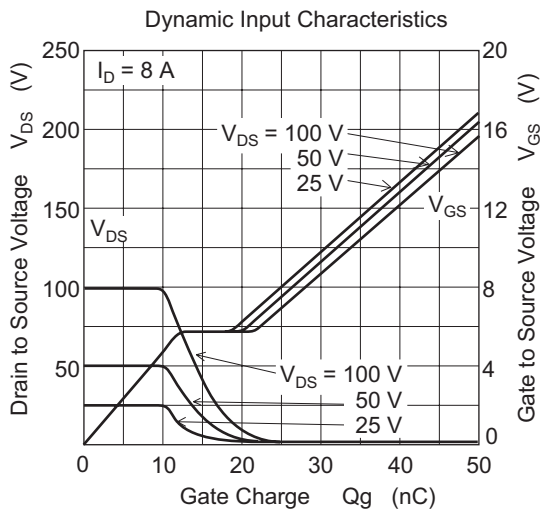
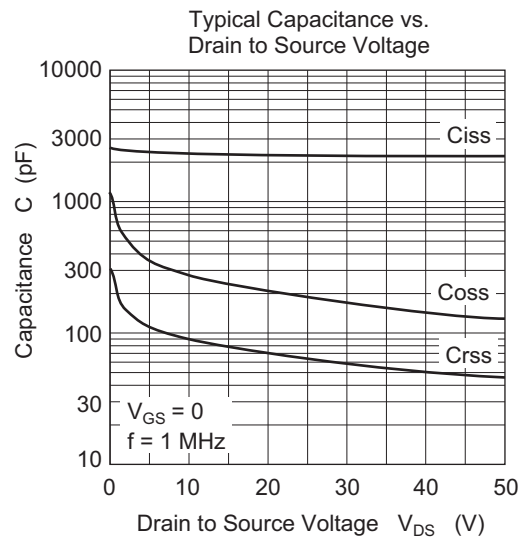
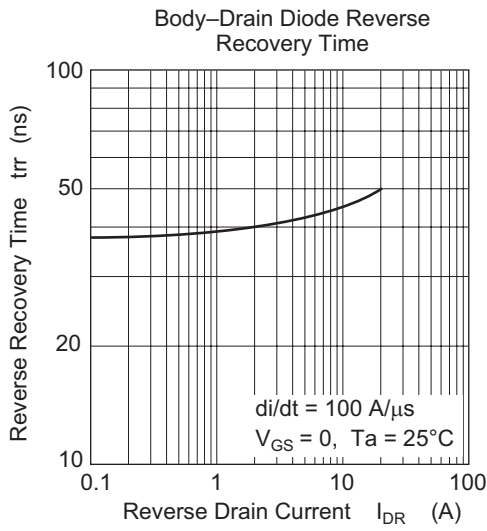
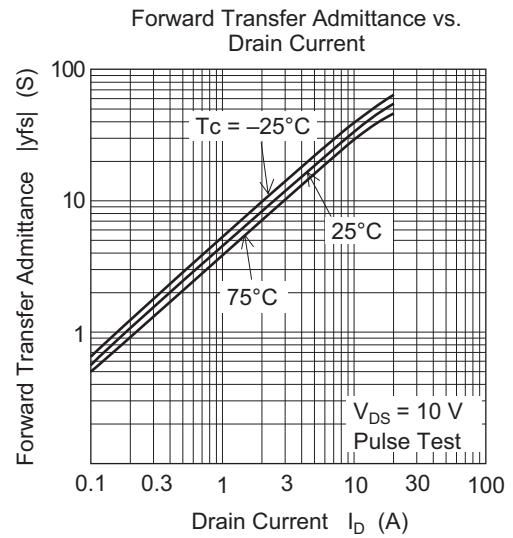
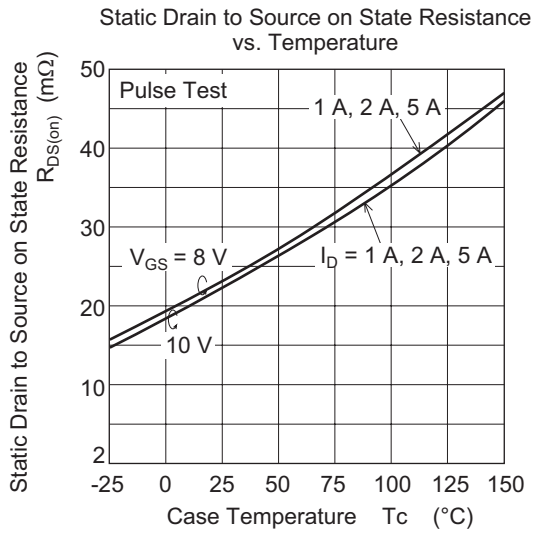
- Notes: 4. Pulse test

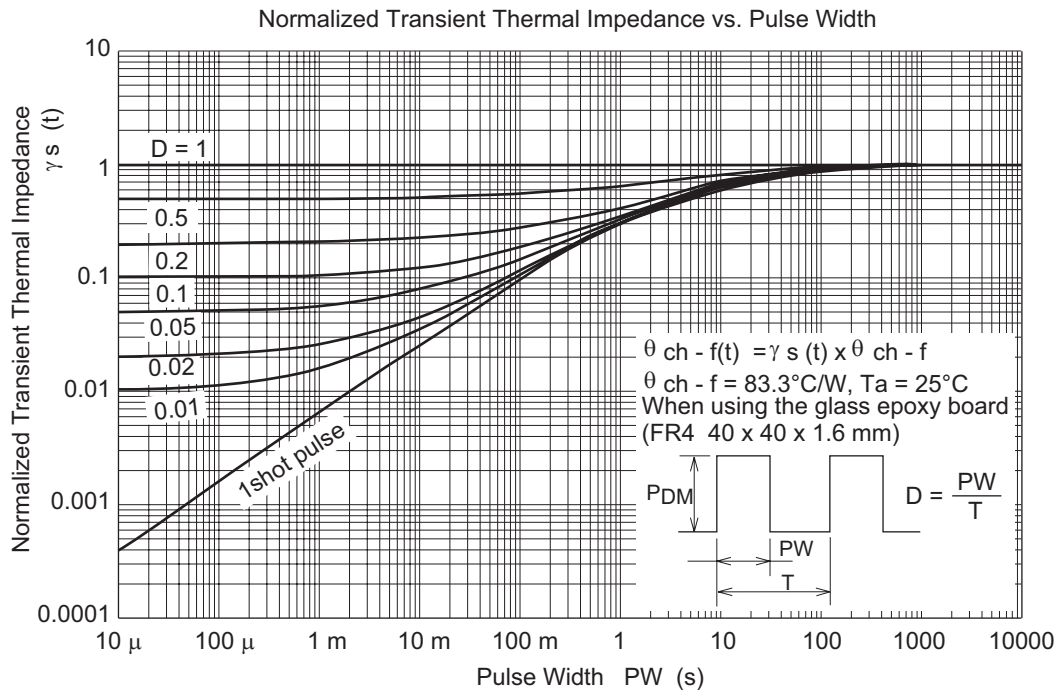
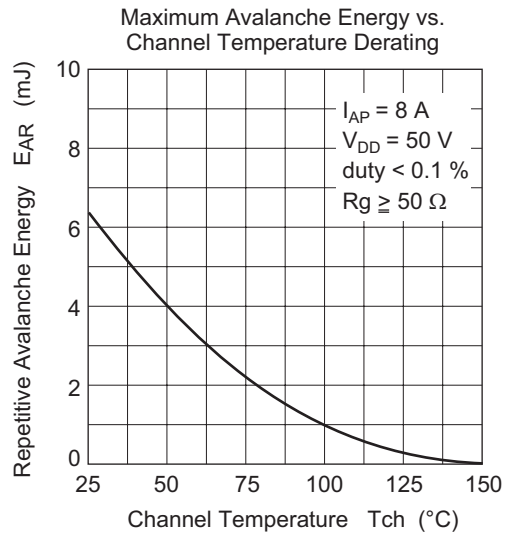
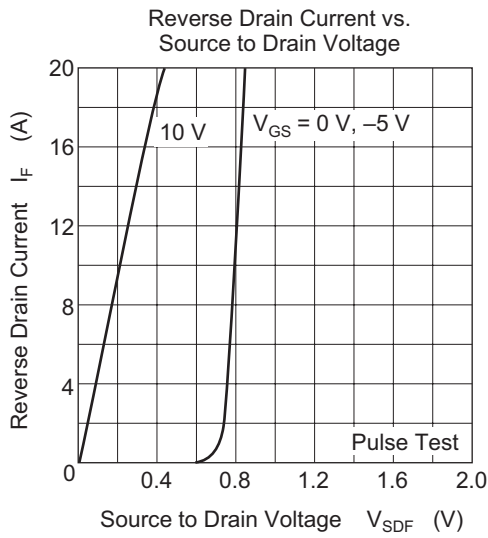
Main Characteristics



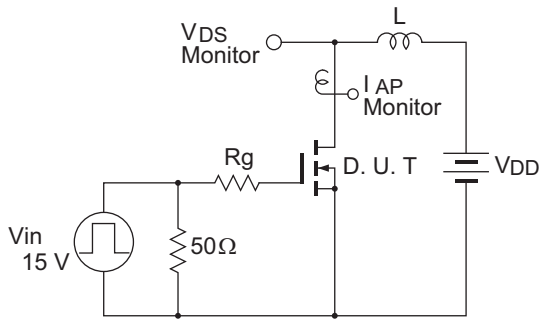
Note 5 :
When using the glass epoxy board
(FR4 40x40x1.6 mm)





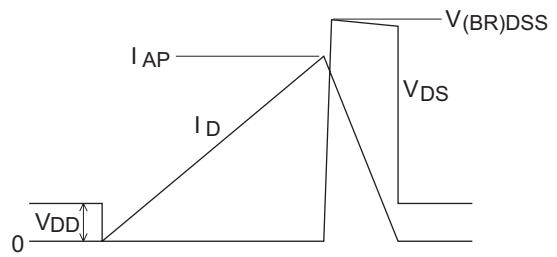


Avalanche Test Circuit

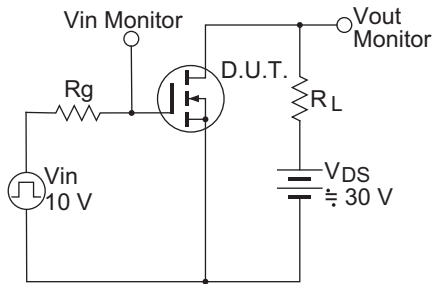


Avalanche Waveform

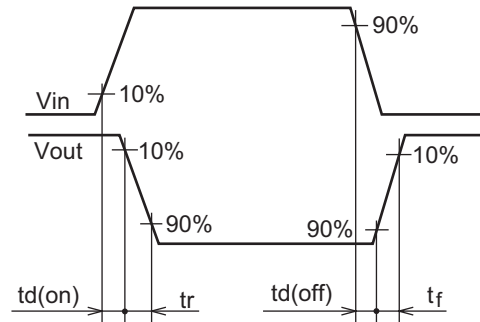
$$E_{AR} = \frac{1}{2} L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



Switching Time Test Circuit

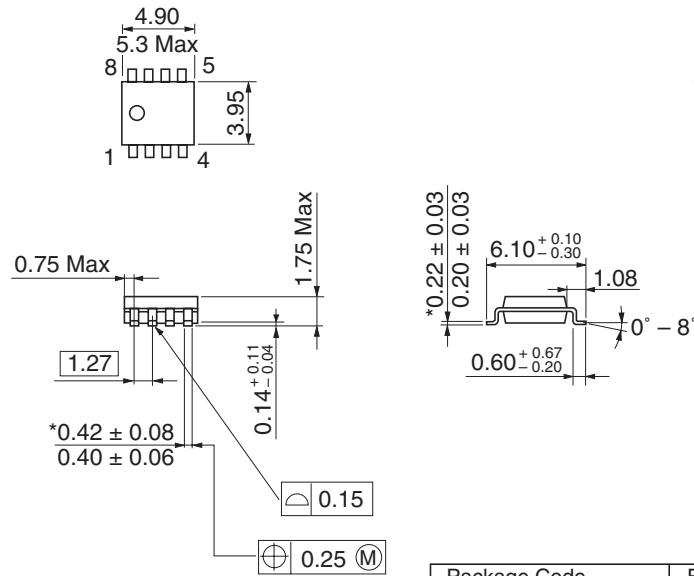


Switching Time Waveform



Package Dimensions

As of January, 2003
Unit: mm



*Dimension including the plating thickness
Base material dimension

Package Code	FP-8DA
JEDEC	Conforms
JEITA	—
Mass (reference value)	0.085 g

Ordering Information

Part Name	Quantity	Shipping Container
HAT2200R-EL-E	2500pcs	Taping

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