C9630

PC133 Clock Generator for SiS630/Pentium®III & SiS540/Socket7 Applications

Product Features

- Supports Pentium®III, K6, and Socket 7 CPU's
- Designed to SiS630 & SiS540 Chipset requirements
- 3 copies of CPU Clock (CPU[0:2])
- 14 copies of SDRAM Clock (SDRAM[0:13]
- 7 copies of PCI Clock
- 2 REF(0:1) Clock outputs
- 1 USB Clock (Non SSC), 48MHz
- 1 programmable SIO (Non SSC), 24/48MHz
- 133 MHz SDRAM support
- Cypress Spread Spectrum for best EMI reduction
- SMBus Support with read back capabilities.
- Dial-a-Frequency™ Feature
- 48 Pin SSOP package.

Block Diagram

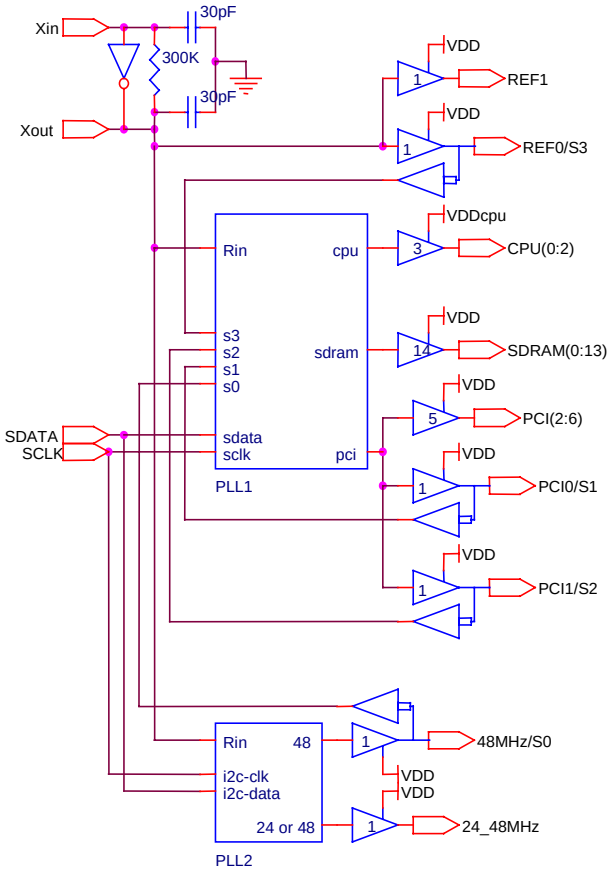


Fig.1

Frequency Table (MHz)

FS3	FS2	FS1	FS0	CPU	SDRAM	PCICLK
0	0	0	0	66.6	100.0	33.3
0	0	0	1	100.0	100.0	33.3
0	0	1	0	150.0	100.0	37.5
0	0	1	1	133.3	100.0	33.3
0	1	0	0	66.8	133.6	33.4
0	1	0	1	100.0	133.3	33.3
0	1	1	0	100.0	150.0	37.5
0	1	1	1	133.3	133.3	33.3
1	0	0	0	66.9	66.9	33.4
1	0	0	1	97.2	97.2	32.4
1	0	1	0	70.0	105.0	35.0
1	0	1	1	95.0	95.0	31.6
1	1	0	0	95.0	126.7	31.6
1	1	0	1	112.0	112.0	37.3
1	1	1	0	97.0	129.3	32.4
1	1	1	1	96.0	96.0	32.0

Table 1

Note: *Programmable to 48 MHz via SMBus

Pin Configuration

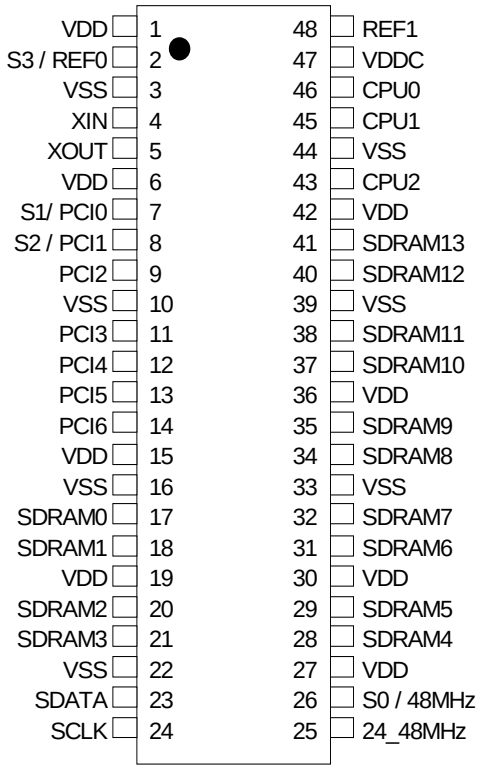


Fig.2

Pin Description

PIN No.	Pin Name	PWR	I/O	Description
2	**S3/ REF0**	VDD	I/O	3.3V 14.318 MHz clock output. This Is a power on bi-directional pin. During power up, this pin is an input “S3” for setting the CPU frequency (see table1, page 1) (see app note, page 5). When the power reaches the rail, this pin becomes a buffered output of the signal applied at Xin (typically 14.318 MHz).
48	**REF1**	VDD	O	This pin is a buffered output of the signal applied at Xin (typically 14.318)
4	**XIN**	VDD	I	14.318MHz Crystal input
5	**XOUT**	VDD	O	14.318MHz Crystal output
7	**S1/ PCI0***	VDD	I/O	This is a power on bi-directional pin. During power up, this pin is an input “S1” for setting the CPU frequency (see table1, page 1) (see app not, page 5). When the power reaches the rail, this pin becomes a PCI0 clock output.
8	**S2/ PCI1***	VDD	I/O	This is a power on bi-directional pin. During power up, this pin is an input “S2” for setting the CPU frequency (see table1, page 1) (see app not, page 5). When the power reaches the rail, this pin becomes a PCI1 clock output.
9,11,12,13, 14	**PCI(2:6)**	VDD	O	3.3V PCI clock outputs.
25	**24/48MHz**	VDD	O	This pin is programmable to 24MHz or 48 MHz clock output through SMBus. It defaults to 24MHz at power up.
26	**S0 / 48MHz***	VDD	I/O	This is a power on bi-directional pin. During power up, this pin is an input “S0” for setting the CPU frequency (see table1, page 1) (see app note, page 5). When the power reaches the rail, this pin becomes a 48MHz clock output. This clock conforms to the USB spec. of +167ppm.
28	**SDATA**	VDD	I	SMBus compatible SDATA input. Has an internal pull-up (>100KΩ)
29	**SCLK**	VDD	I	SMBus compatible SCLK input. Has an internal pull-up (>100KΩ)
17,18,20,21, 28,29,31,32, 34,35,37,38, 40,41	**SDRAM(0:13)**	VDD	O	3.3V SDRAM clock outputs. See table1, p.1 for frequency selection.
43,45,46	**CPU(0:2)**	VDDC	O	2.5V or 3.3V Host bus clock outputs. See table 1, page 1 for frequency selection.
1,6,15,19, 27, 30,36,42	**VDD**	-		3.3V Common Power Supply
47	**VDDC**	-		2.5V or 3.3V Power Supply’s for CPU (0:2) clock outputs.
3,10,16,22, 33,39,44	**VSS**	-		Common Ground pin.

A bypass capacitor (0.1µF) should be placed as close as possible to each positive power pin. If these bypass capacitors are not close to the pins their high frequency filtering characteristic will be cancelled by the lead inductance of the traces.

*Note: These pins have pulldown resistors, typical value 250 Ω.

Device Clock Phase Relationships

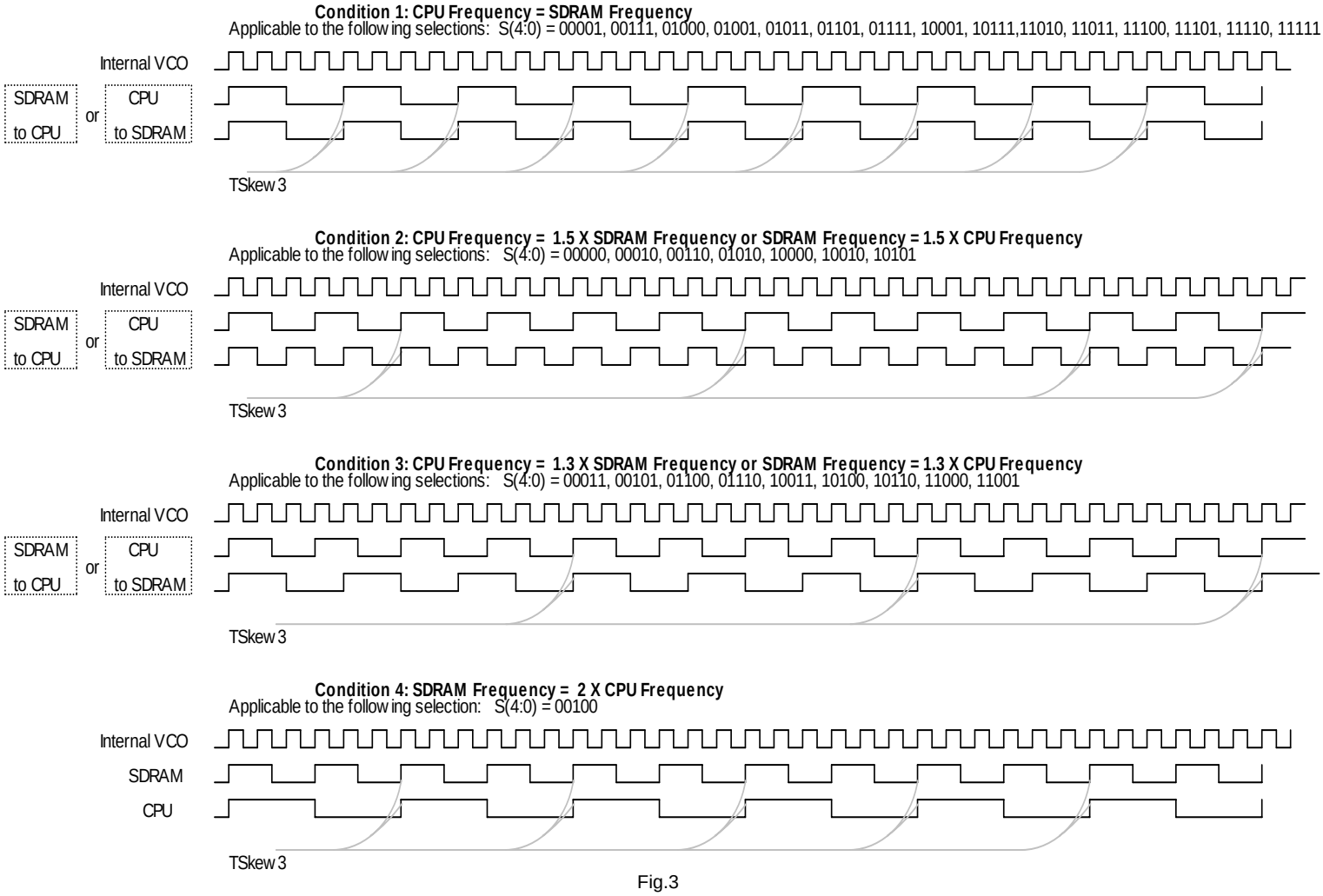


Fig.3

Frequency Smooth Switching Groups

Group	S(4:0)
1	00001, 00010, 00111, 01101, 10001, 10010, 10111, 11010, 11011, 11100, 11101, 11110, 11111
2	00000, 00011, 00110, 01010, 10000, 10101
3	00100, 00101, 01000, 01001, 01011, 01100, 01110, 01111, 10011, 10100, 10110, 11000, 11001

Table 2

Table 2 above describes 3 different groups of frequencies. Within the same group, frequency may be switched through SMBus byte 0 without causing any glitching or clock discontinuity at the CPU(0:2) outputs, therefore allowing frequency smooth switching of the clock.

Switching frequency from one group to another is permitted but will cause the CPU(0:2) clocks to jump immediately to the next frequency. (non smooth switching.).

Power on Bi-Directional Pins

Power Up Condition:

Pins 2,7,8,and 26 are Power up bi-directional pins used for selecting the host frequency in page 1, table 1. During power-up of the device, these pins are in input mode (see Fig 4, below), therefore; they are considered input select pins internal to the IC. After a settling time, the selection data is latch into the internal control register and these pins become a clock outputs.

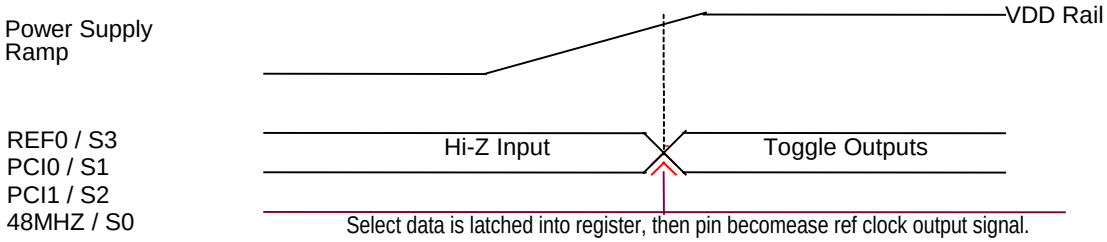


Fig.4

Strapping Resistor Options:

The power up bi-directional pins have a large value pull-down each (250KΩ), therefore, a selection "0" is the default. If the system uses a slow power supply (over 5mS settling time), then **it is recommended** to use an external Pull-Down (Rdn) in order to insure a Low selection. In this case, the designer may choose one of two configurations, see Fig.5A and B.

Fig. 5A represents an additional pull down resistor Rdn = 50KΩ connected from the pin to the ground plane, which allows a faster pull to a low level.
If a selection "1" is desired, then a jumper is placed on JP1 to a Rup = 10KΩ resistor as implemented as shown in Fig.5A. Please note the selection resistors (Rup and Rdn) are placed before the Damping resistor (Rd) close to the pin.

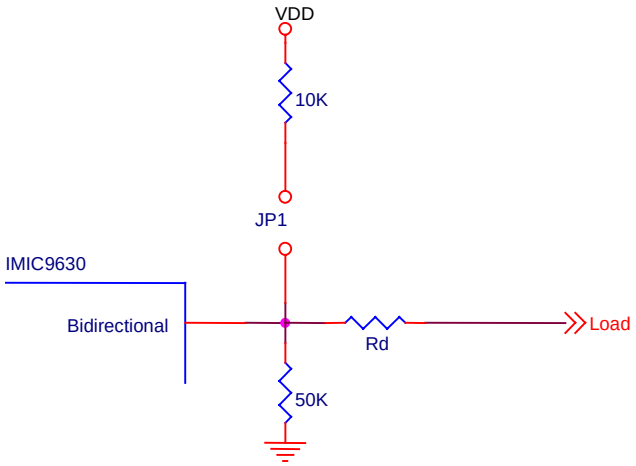


Fig.5A

Fig. 5B represent a single resistor 10KΩ connected to a 3-way jumper, JP2. When a "1" selection is desired, a jumper is placed between leads1 and 3. When a "0" selection is desired, a jumper is placed between leads 3 and 2.

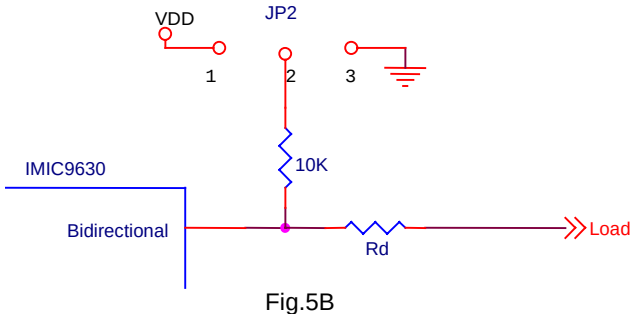


Fig.5B

2-Wire SMBus Control Interface

The 2-wire control interface implements a read/write slave only interface according to SMBus specification (IC12, 1996). The device can be read back by using standard SMBus command bytes. Sub addressing is not supported, thus all preceding bytes must be sent in order to change one of the control bytes. The 2-wire control interface allows each clock output to be individually enabled or disabled. 100 Kbits/second (standard mode) data transfer is supported.

During normal data transfer, the SDATA signal only changes when the SCLK signal is low, and is stable when SCLK is high. There are two exceptions to this. A high to low transition on SDATA while SCLK is high is used to indicate the start of a data transfer cycle. A low to high transition on SDATA while SCLK is high indicates the end of a data transfer cycle. Data is always sent as complete 8-bit bytes, after which an acknowledge is generated. The first byte of a transfer cycle is a 7-bit address with a Read/Write bit (R/W#) as the LSB. R/W# = 1 in read mode. R/W# = 0 in write mode.

A maximum of 10 bytes of data may be written/Read Data is transferred MSB first at a max rate of 100kbits/S.The device will not respond to any other control interface conditions.

In the Write mode (See fig6A, p.9), the clock gen. acknowledges Address Byte, D2, then receives two additional bytes:
1) "**Command Code** " byte, and
2) "**Byte Count**" byte. Must be programmed to FF for correct operation.
Although the data (bits) in these two bytes are considered "don't care"; they must be sent and will be acknowledged.
Subsequently, the below-described sequence (Byte 0, Byte 1, Byte2,) will be valid and acknowledged.

In the Read Mode (See fig6B, p.9), the clock gen. acknowledges Address D3, and immediately transmits data starting with Byte count, then Byte 0, 1, 2, ... After each transmitted byte, this device waits for an acknowledge before transmitting the next byte.

Serial Control Registers

NOTE: Power up conditions for each bit are listed in the "@Pup" column.

Byte 0: Frequency, Function Select Register

Bit	@Pup	Pin#	Description, see page 8 for SSCG description.	
7	0	n/a	S4 (for frequency table 3, selection by software via SMBus), selection valid if bit3 = 1	
6	0	n/a	S2 (for frequency table 3, selection by software via SMBus), selection valid if bit3 = 1	
5	0	n/a	S1 (for frequency table 3, selection by software via SMBus), selection valid if bit3 = 1	
4	0	n/a	S0 (for frequency table 3, selection by software via SMBus), selection valid if bit3 = 1	
3	0	n/a	0 = frequency selected by hardware, pins 2,7,8,26	1 = frequency selection via SMBus byte0. bits 4,5,6,2,7
2	0	n/a	S3 (for frequency table 3, selection by software via SMBus), selection valid if bit3 = 1	
1	0	n/a	0 = Spread Spectrum disabled	1 = Spread spectrum enabled
0	0	n/a	0 = Running	1 = Test mode.

Serial Configuration Command Bitmap

Byte0: Functionality and Frequency Select Register (default = 0)

S4	S3	S2	S1	S0	Description			
Bit7	Bit2	Bit6	Bit5	Bit4	CPU	SDRAM	PCI	Spread Spectrum, MBS0 = MBS1 = 1, SSTS = 1
0	0	0	0	0	66.6	100.0	33.3	0 to –0.5%
0	0	0	0	1	100.0	100.0	33.3	0 to –0.5%
0	0	0	1	0	150.0	100.0	37.5	+/- 0.25%
0	0	0	1	1	133.3	100.0	33.3	0 to –0.5%
0	0	1	0	0	66.8	133.6	33.4	0 to –0.5%
0	0	1	0	1	100.0	133.3	33.3	0 to –0.5%
0	0	1	1	0	100.0	150.0	37.5	+/- 0.25%
0	0	1	1	1	133.3	133.3	33.3	0 to –0.5%
0	1	0	0	0	66.8	66.8	33.4	+/- 0.25%
0	1	0	0	1	97.0	97.0	32.3	0 to –0.5%
0	1	0	1	0	70.0	105.0	35.0	+/- 0.25%
0	1	0	1	1	95.0	95.0	31.7	+/- 0.25%
0	1	1	0	0	95.0	126.7	31.7	+/- 0.25%
0	1	1	0	1	112.0	112.0	37.3	+/- 0.25%
0	1	1	1	0	97.0	129.3	32.3	0 to –0.5%
0	1	1	1	1	96.2	96.2	32.1	0 to –0.5%
1	0	0	0	0	66.8	100.2	33.4	+/- 0.25%
1	0	0	0	1	100.2	100.2	33.4	+/- 0.25%
1	0	0	1	0	166.0	110.7	33.3	+/- 0.25%
1	0	0	1	1	100.2	133.6	33.4	+/- 0.25%
1	0	1	0	0	75.0	100.0	37.5	+/- 0.25%
1	0	1	0	1	83.3	125.0	31.3	+/- 0.25%
1	0	1	1	0	105.0	140.0	35.0	+/- 0.25%
1	0	1	1	1	133.6	133.6	33.4	+/- 0.25%
1	1	0	0	0	110.3	147.0	36.8	+/- 0.25%
1	1	0	0	1	115.0	153.3	38.3	+/- 0.25%
1	1	0	1	0	120.0	120.0	30.0	+/- 0.25%
1	1	0	1	1	138.0	138.0	34.5	+/- 0.25%
1	1	1	0	0	140.0	140.0	35.0	+/- 0.25%
1	1	1	0	1	145.0	145.0	36.3	+/- 0.25%
1	1	1	1	0	147.5	147.5	29.5	+/- 0.25%
1	1	1	1	1	160.0	160.0	32	+/- 0.25%

Table 3.

TEST Function Table: Applicable only when bit0=1 in Byte0.

CPU (0:2)	PCI (0:6)	SDRAM (0:13)	REF(0,1)	48MHz	24_48MHz
= Xin / 3	= Xin / 6	= Xin / 2	= Xin	= Xin	= Xin / 2

Test Clock should be applied at Xin pin.

Serial Control Registers (Cont.)

Byte 1: CPU Clock Register (1 = enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7	1	-	Selects Frequency at pin 25 1 = selects 24MHz (default) 0 = selects 48MHz
6	1	-	SSTS, See Table 4, p 11
5	1	-	Reserved for IMI test^
4	1	-	Reserved for IMI test^
3	1	43	CPU2 enable/Stopped
2	1	45	CPU1 enable/Stopped
1	1	46	CPU0 enable/Stopped
0	1	-	Reserved for IMI test^

Byte 2: PCI Clock Register (1 = enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7	1	-	Reserved
6	1	14	PCI6 enable/Stopped
5	1	13	PCI5 enable/Stopped
4	1	12	PCI4 enable/Stopped
3	1	11	PCI3 enable/Stopped
2	1	9	PCI2 enable/Stopped
1	1	8	PCI1 enable/Stopped
0	1	7	PCI0 enable/Stopped

Byte 3: SDRAM Clock Register (1 = enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7	1	32	SDRAM7 enable/Stopped
6	1	31	SDRAM6 enable/Stopped
5	1	29	SDRAM5 enable/Stopped
4	1	28	SDRAM4 enable/Stopped
3	1	21	SDRAM3 enable/Stopped
2	1	20	SDRAM2 enable/Stopped
1	1	18	SDRAM1 enable/Stopped
0	1	17	SDRAM0 enable/Stopped

Byte 4: Additional SDRAM Clock Register (1=enable, 0=Stopped)

Bit	@Pup	Pin#	Description
7	1	25	24_48MHz enable/Stopped
6	1	26	48 MHz enable/Stopped
5	1	41	SDRAM13 enable/Stopped
4	1	40	SDRAM12 enable/Stopped
3	1	38	SDRAM11 enable/Stopped
2	1	37	SDRAM10 enable/Stopped
1	1	35	SDRAM9 enable/Stopped
0	1	34	SDRAM8 enable/Stopped

Byte 5: Peripheral Control (1 = enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7	1	-	**MBS1**, See table 4, p. 11 for Spread Spectrum
6	1	-	**MBS0**, See table 4, p.11 for Spread Spectrum
5	1	-	S3# *
4	1	-	S2# *
3	1	-	S1# *
2	1	-	S0# *
1	1	48	REF1 enable/Stopped
0	1	2	REF0 enable/Stopped

***Inverted read back of hardware settings.

Byte 6: Reserved Register (1 = enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7	0	-	Reserved for IMI test^
6	0	-	
5	0	-	
4	0	-	Reserved for IMI test^
3	0	-	Reserved for IMI test
2	1	-	Reserved for IMI test
1	0	-	N9, MSB
0	0	-	N8

Byte 7: Dial-a-Frequency® N Register (1 = enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7	0	-	N7
6	0	-	N6
5	0	-	N5
4	0	-	N4
3	0	-	N3
2	0	-	N2
1	0	-	N1
0	0	-	N0, LSB

Byte 8: Dial-a-Frequency® R Register (1 = enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7	0	-	R6, MSB
6	0	-	R5
5	0	-	R4
4	0	-	R3
3	0	-	R2
2	0	-	R1
1	0	-	R0, LSB
0	0	-	1 = Enable SMBus N and R

Dial-a-Frequency™ Feature

SMBus Dial-a-frequency™ feature is available in this device via byte7, and byte 8
These bytes allow the user to enter the N and R values that will allow them to program any CPU frequency desired following the formula:

$$Fcpu = \frac{P \times N}{R}$$

Where N and R values are programmed in binary into byte 7 for N and byte 8 for R. See table below for min and max allowed values.

R	Min N	Max N
42	44	87
43	45	90
44	46	92
45	47	94
46	48	96
47	49	98
48	50	100
49	51	102
50	52	104
51	53	107

P is a large value PLL constant that depends on the last frequency selection achieved through the hardware selectors (S3, S2, S1, S0) or through the software selectors (byte0 , bits 7,6,5,4,2). P value may be determined from the following table:

S(4:0)	P
00001, 00010, 00111, 01101, 10001, 10010, 10111, 11010, 11011, 11100, 11101, 11110, 11111	96016000
00000, 00011, 00110, 01010, 10000, 10101	64010667
00100, 00101, 01000, 01001, 01011, 01100, 01110, 01111, 10011, 10100, 10110, 11000, 11001	48008000

Therefore, if a 145MHz (use $145x10^6$)value is desired, then we should apply 145 into equation 1, and start by choosing R to be 47 (assume the last frequency selection has the value P = 96016000):

$$145X10^6 = \frac{96016000 \times N}{47} \quad \Rightarrow \quad N = 70.97775371$$

Dial-a-Frequency™ Feature (Cont.)

Since this N number must be entered in Binary, it can only be an integer, so it must be rounded up or down. Here we can rounded it up to 71, which will give us an exact CPU frequency of:

$$Fcpu = \frac{96016000 \times N}{47} = 145.045 \text{ MHz (accuracy + 310 ppm)}$$

If the above frequency is not accurate enough, then you must choose another R value and start from the beginning. For example choose R = 49 and this will yield an N = 73.99808365, which is rounded to 74. If the 74 is applied in the formula 1, then Fcpu = 145.0038 MHz (accuracy + 26 ppm).

Other R values within the above limits may also be evaluated.

SMBus Communication Waveform

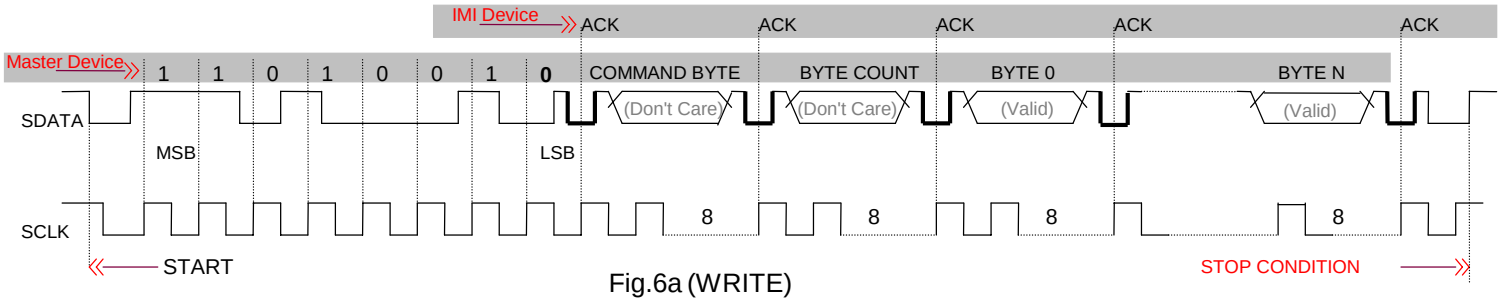


Fig.6a (WRITE)

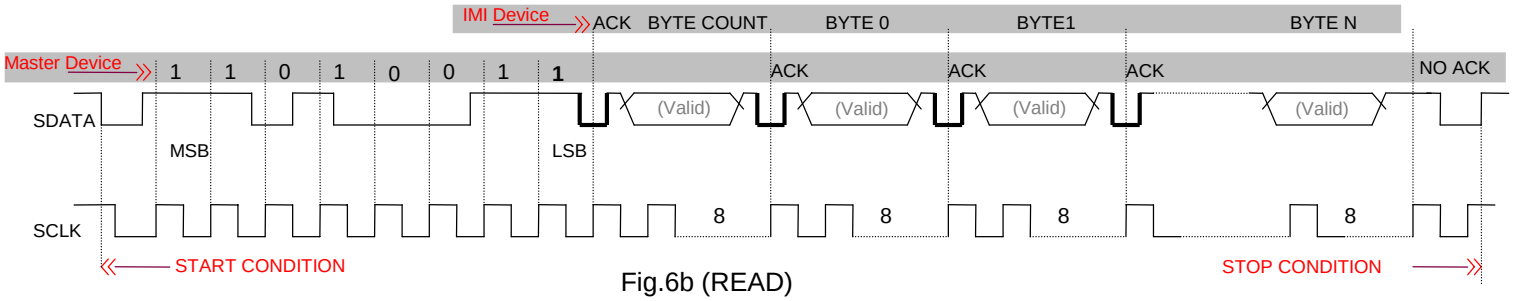


Fig.6b (READ)

SMBus Test Circuitry

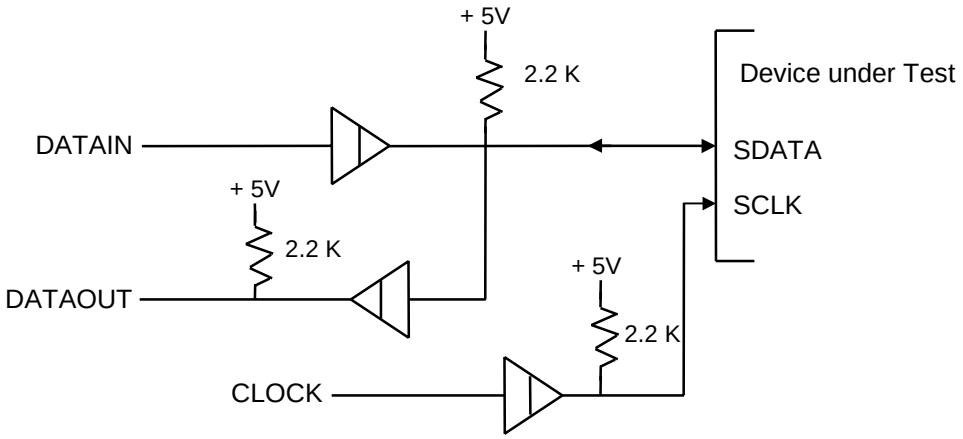


Fig.7

Note: Buffer is 7407 with VCC @ 5.0 V

Spread Spectrum Clock Generation (SSCG)

Spread Spectrum is a modulation technique applied here for maximum efficiency in minimizing Electro-Magnetic Interference radiation generated from repetitive digital signals mainly clocks. A clock accumulates EM energy at the center frequency it is generating. Spread Spectrum distributes this energy over a small frequency bandwidth therefore spreading the same amount of energy over a spectrum. This technique is achieved by modulating the clock down from (Fig.8A) or around the center (Fig.8B) of its resting frequency by a certain percentage (which also determines the energy distribution bandwidth). In this device, Spread Spectrum is enabled by setting I²C byte0, bit1 = 1. The default of the device at power up keeps the Spread Spectrum disabled, it is therefore, important to have I²C accessibility to turn-on the Spread Spectrum function. Once the Spread Spectrum is enabled, the spread bandwidth option is selected by MBS(0:1) in I²C byte 5, bit6 and bit 7, and SSTS Byte1, Bit6 following table 4 below.

In Down Spread mode the center frequency is shifted down from its rested (non-spread) value by ½ of the total spread %. (eg.: assuming the center frequency is 100MHz in non-spread mode; when down spread of –0.5% is enabled, the center frequency shifts to 99.75MHz.).

Spread Spectrum Clock Generation (SSCG) (Cont.)

In Center Spread mode, the Center frequency remains the same as in the non-spread mode.

Down Spread

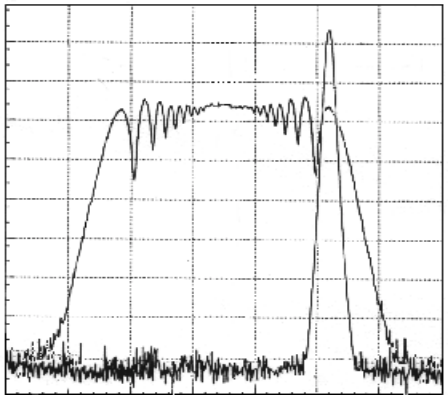


Fig.8A

Center Spread

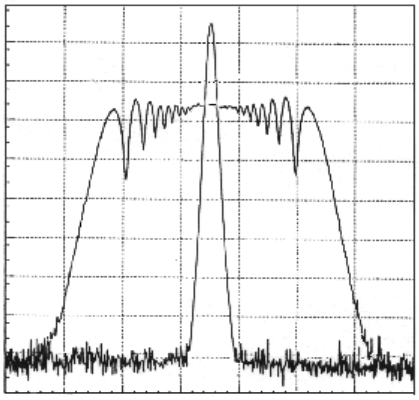


Fig.8B

Spread Spectrum Selection Table

SSTS	MBS 1	MBS 0	Spread%
0	0	0	- 0.5
0	0	1	+/- 0.125
0	1	0	+/- 0.5
0	1	1	+/- 0.25
1	0	0	-0.5
1	0	1	+/- 0.125
1	1	0	+/- 0.5
1	1	1	See table 3, (default)

Table 4

Maximum Ratings[1]

Maximum Input Voltage Relative to VSS: VSS - 0.3V

Maximum Input Voltage Relative to VDD: VDD + 0.3V

Storage Temperature: -65ºC to + 150ºC

Operating Temperature: 0ºC to +70ºC

Maximum ESD protection 2KV

Maximum Power Supply: 5.5V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, Vin and Vout should be constrained to the range:

VSS<(Vin or Vout)<VDD

Unused inputs must always be tied to an appropriate logic voltage level (either VSS or VDD).

[1] Multiple Supplies: The voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.

DC Parameters

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Input Low Voltage	VIL2	-	-	1.0	Vdc	Note 2
Input High Voltage	VIH2	2.2	-	-	Vdc	
Input Low Current (@VIL = VSS)	IIL			-5	µA	For internal Pull down resistors, Notes 1,3
Input High Current (@VIL =VDD)	IIH	66		5	µA	
Tri-State leakage Current	Ioz	-	-	10	µA	
Dynamic Supply Current	Idd3.3V	-	-	400	mA	S(3:0) = 0101, Note 4
Dynamic Supply Current	Idd2.5V	-	-	100	mA	S(3:0) = 0111, Note 4
Input pin capacitance	Cin	-	-	5	pF	
Output pin capacitance	Cout	-	-	6	pF	
Pin inductance	Lpin	-	-	7	nH	
Crystal pin capacitance	Xin/Xout	30	32	34	pF	Measured from Pin to Ground. Note 5
Crystal DC Bias Voltage	V_{BIAS}	0.3Vdd	Vdd/2	0.7Vdd	V	
Crystal Startup time	Txs	-	-	40	µS	From Stable 3.3V power supply.
VDD = 3.3V ±5%, VDDC = 2.5 ± 5%, TA = 0º to +70ºC						

Note1: Applicable to S(0:3).
Note2: Applicable to Sdata, and Sclk.
Note3: Although internal pull-down resistors have a typical value of 250K, this value may vary between 200K and 500K.
Note4: All outputs loaded as per table 5 below.
Note5: Although the device will reliably interface with crystals of a 15pF – 20pF C_L range, it is optimized to interface with a typical C_L = 16pF crystal specifications.

Clock Name	Max Load (in pF)
CPU, REF	20
PCI, SDRAM	30
24MHz, 48MHz	15

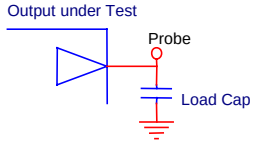
Table 5

AC Parameters

Symbol	Parameter	133 MHz Host		100 MHz Host		Units	Notes
		Min	Max	Min	Max		
TPeriod	CPU(0:2) period	7.45	8.0	9.98	10.5	nS	5, 6, 8
THIGH	CPU(0:2) high time	1.87	-	3.0	-	nS	6,10
TLOW	CPU(0:2) low time	1.67	-	2.8	-	nS	6, 11
Tr / Tf	CPU(0:2) rise and fall times	0.4	1.9	0.4	2.1	nS	6, 7
TSKEW0	Any CPU to Any CPU Skew time	-	175	-	175	pS	6, 8, 9
TCCJ	CPU(0:2) Cycle to Cycle Jitter	-	250	-	250	pS	6,8,9,14
TPeriod	SDRAM[0:13] period	7.46	8.0	9.89	10.5	nS	5, 6, 8
THIGH	SDRAM[0:13] high time	1.87	-	3.0	-	nS	6,10
TLOW	SDRAM[0:13] low time	1.67	-	2.63	-	nS	6, 11
Tr / Tf	SDRAM[0:13] rise and fall times	0.4	1.69	0.4	1.88	nS	6, 7
TSKEW1	Any SDRAM to Any SDRAM	-	500	-	500	pS	6, 8, 9
TCCJ	SDRAM[0:13] Cycle to Cycle Jitter	-	250	-	250	pS	6,8,9,14
TPeriod	PCI(0:6) period	29.93	-	29.94	-	nS	5, 6, 8
THIGH	PCI(0:6) period	12.0	-	12.0	-	nS	6,10
TLOW	PCI(0:6) low time	12.0	-	12.0	-	nS	6, 11
Tr / Tf	PCI(0:6) rise and fall times	0.5	2.9	0.5	2.9	nS	6, 7
TSKEW2	(Any PCI clock) to (Any PCI clock)	-	500	-	500	pS	6, 8, 9
TCCJ	PCI(0:6) Cycle to Cycle Jitter	-	500	-	500	pS	6, 8, 9
TPeriod	48MHz period (conforms to +167ppm max)	20.8212	20.8333	20.8299	20.8442	nS	5, 6, 8
Tr / Tf	48MHz rise and fall times	1.0	4.0	1.0	4.0	nS	6, 7
TCCJ	48MHz Cycle to Cycle Jitter	-	500	-	500	pS	6, 8, 9
TPeriod	24MHz period	41.6087	41.6666	41.6026	41.6666	nS	5, 6, 8
Tr / Tf	24MHz rise and fall times	1.0	4.0	1.0	4.0	nS	6, 7
TCCJ	24 MHz Cycle to Cycle Jitter	-	500	-	500	pS	6, 8, 9
TPeriod	REF(0:1) period	69.8167	71.0	69.8017	71.0	nS	5, 6, 8
Tr / Tf	REF0 rise and fall times	1.0	4.0	1.0	4.0	nS	6, 7
Tr / Tf	REF1 rise and fall times	1.0	4.0	1.0	4.0	nS	6, 7
TCCJ	REF(0:1) Cycle to Cycle Jitter	-	1000	-	1000	pS	6, 8
tpZL, tpZH	Output enable delay (all outputs)	1.0	10.0	1.0	10.0	nS	13
tpLZ, tpHZ	Output disable delay (all outputs)	1.0	10.0	1.0	10.0	nS	13
tstable	All clock Stabilization from power-up		3		3	mS	12
TSKEW3	CPU to SDRAM (see fig.3, p.3)	0	340	0	354	pS	5, 6, 8

Note 5: This parameter is measured as an average over 1uS duration, with a crystal center frequency of 14.31818MHz
Note 6: All outputs loaded as per table 5.
Note 7: Probes are placed on the pins, and measurements are acquired between 0.4V and 2.4V for 3.3V signals and between 0.4V and 2.0V for 2.5V signals (see Fig.9A and Fig.9B)
Note 8: Probes are placed on the pins, and measurements are acquired at 1.5V for 3.3V signals and at 1.25V for 2.5V signals. (see Figs.9A & 9B)
Note 9: This measurement is applicable with Spread ON or Spread OFF.
Note 10: Probes are placed on the pins, and measurements are acquired at 2.4V for 3.3V signals and at 2.0V for 2.5V signals, (see Figs. 9A & 9B)
Note 11: Probes are placed on the pins, and measurements are acquired at 0.4V.
Note 12: The time specified is measured from when all VDD's reach their respective supply rail (3.3V and 2.5V) till the frequency output is stable and operating within the specifications
Note 13: Measured from when both SEL1 and SEL0 are low
Note 14: Guaranteed by design in system Application (CPU frequency = SDRAM frequency)

Test and Measurement Condition



3.3V signals

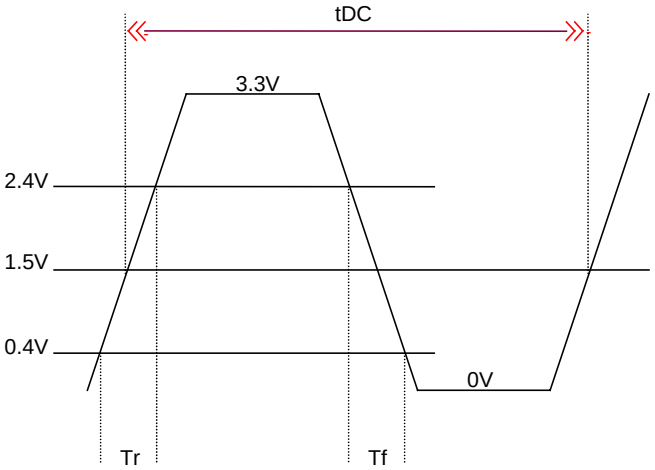


Fig. 9A

2.5V signals

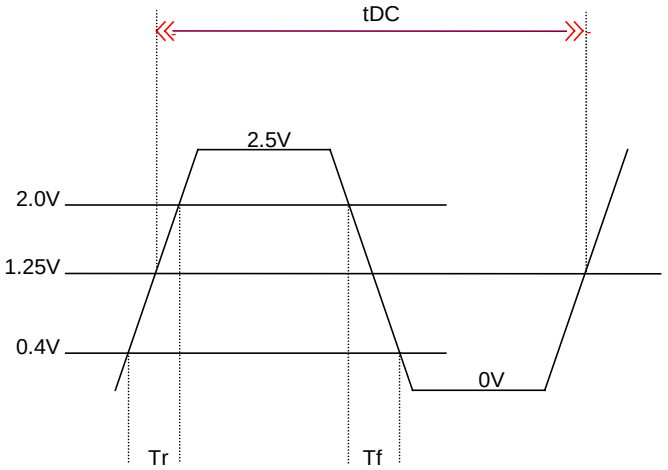


Fig. 9B

Output Buffer Characteristics

CPU(0:2), VDDC = 2.5V +/-5%

Characteristic	Symbol	Min	Typ	Max	Units	Conditions, VDDC = 2.5V
Pull-Up Current	IOH_1	-14.8	-25	-35.5	mA	Vout =VDDC - 0.5V
Pull-Up Current	IOH_2	-28.4	-58	-79.5	mA	Vout = 1.25 V
Pull-Down Current	IOL_1	11.7	20	29.3	mA	Vout = 0.4 V
Pull-Down Current	IOL_2	27	56	67.6	mA	Vout = 1.2 V
Dynamic Output Impedance	Z0	13.5		45	Ω	

CPU(0:2), VDDC = 3.3V +/-5%

Characteristic	Symbol	Min	Typ	Max	Units	Conditions, VDDC= 3.3V
Pull-Up Current	IOH_1	17	28	40	mA	Vout =VDDC - 0.5V
Pull-Up Current	IOH_2	53	100	138	mA	Vout = 1.25 V
Pull-Down Current	IOL_1	13	22	32	mA	Vout = 0.4 V
Pull-Down Current	IOL_2	35	68	83	mA	Vout = 1.2 V
Dynamic Output Impedance	Z0	10.4		37	Ω	

PCI(0:6), and REF0

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Pull-Up Current	IOH_1	-33	-58	-194	mA	Vout =VDD - 1.0 V
Pull-Up Current	IOH_2	-30	-54	-184	mA	Vout = 1. 5 V
Pull-Down Current	IOL_1	9.4	18	38	mA	Vout = 0.4 V
Pull-Down Current	IOL_2	28	55	148	mA	Vout = 1.5 V
Dynamic Output Impedance	Z0	12		55	Ω	

24MHz, 48MHz, and REF1

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Pull-Up Current	IOH_1	-29	-46	-99	mA	Vout =VDD - 1.0 V
Pull-Up Current	IOH_2	-27	-43	-92	mA	Vout = 1. 5 V
Pull-Down Current	IOL_1	9	13	27	mA	Vout = 0.4 V
Pull-Down Current	IOL_2	26	39	79	mA	Vout = 1.5 V
Dynamic Output Impedance	Z0	20		60	Ω	

Buffer Characteristics for SDRAM(0:13)

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Pull-Up Current	IOH_1	-72	-116	-198	mA	Vout =VDD - 1. 0 V
Pull-Up Current	IOH_2	-68	-110	-188	mA	Vout = 1. 4 V
Pull-Down Current	IOL_1	23	34	53	mA	Vout = 0.4 V
Pull-Down Current	IOL_1	64	98	159	mA	Vout = 1.5 V
Dynamic Output Impedance	Z0	10		24	Ω	
VDD=3.3V ±5%, TA=0 to 70ºC						

Suggested Oscillator Crystal Parameters

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Frequency	F_o	12.00	14.31818	16.00	MHz	
Tolerance	T_C	-	-	+/-100	PPM	Note 1
	T_S	-	-	+/- 100	PPM	Stability (T_A -10 to +60C) Note 1
	T_A	-	-	5	PPM	Aging (first year @ 25C) Note 1
Operating Mode	-	-	-	-		Parallel Resonant, Note 1
Load Capacitance	C_{XTAL}	-	16	-	pF	The crystal's rated load. Note 1
Effective Series Resistance (ESR)	R_{ESR}	-	40	-	Ohms	Note 2

Note1: For best performance and accurate frequencies from this device, It is recommended but not mandatory that the chosen crystal meets or exceeds these specifications

Note 2: Larger values may cause this device to exhibit oscillator startup problems

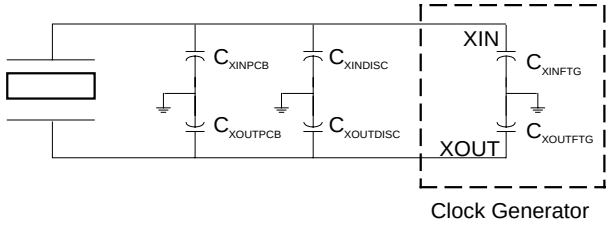
To obtain the maximum accuracy, the total circuit loading capacitance should be equal to C_{XTAL}. This loading capacitance is the effective capacitance across the crystal pins and includes the clock generating device pin capacitance (C_{FTG}), any circuit traces (C_{PCB}), and any onboard discrete load capacitors (C_{DISC}).

The following formula and schematic may be used to understand and calculate either the loading specification of a crystal for a design or the additional discrete load capacitance that must be used to provide the correct load to a known load rated crystal.

$$C_L = \frac{(C_{XINPCB} + C_{XINFTG} + C_{XINDISC}) \times (C_{XOUTPCB} + C_{XOUTFTG} + C_{XOUTDISC})}{(C_{XINPCB} + C_{XINFTG} + C_{XINDISC}) + (C_{XOUTPCB} + C_{XOUTFTG} + C_{OUTDISC})}$$

Where:

C_{XTAL} = the load rating of the crystal
$C_{XOUTFTG}$ = the clock generators XIN pin effective device internal capacitance to ground
$C_{XOUTFTG}$ = the clock generators XOUT pin effective device internal capacitance to ground
C_{XINPCB} = the effective capacitance to ground of the crystal to device PCB trace
$C_{XOUTPCB}$ = the effective capacitance to ground of the crystal to device PCB trace
$C_{XINDISC}$ = any discrete capacitance that is placed between the XIN pin and ground
$C_{XOUTDISC}$ = any discrete capacitance that is placed between the XOUT pin and ground

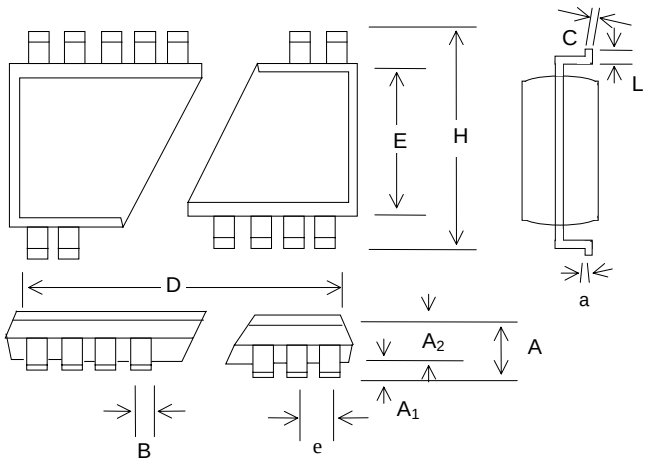


As an example, and using this formula for this datasheet's device, a design that has no discrete loading capacitors (C_{DISC}) and each of the crystal to device PCB traces has a capacitance (C_{PCB}) to ground of 2pF (typical value) would calculate as:

$$C_L = \frac{(2pF + 30pF + 0pF) \times (2pF + 30pF + 0pF)}{(2pF + 30pF + 0pF) + (2pF + 30pF + 0pF)} = \frac{32 \times 32}{32 + 32} = 16\ pF$$

Therefore to obtain output frequencies that are as close to this data sheets specified values as possible, in this design example, you should specify a parallel cut crystal, with C_L = 16pF.

Package Drawing and Dimensions



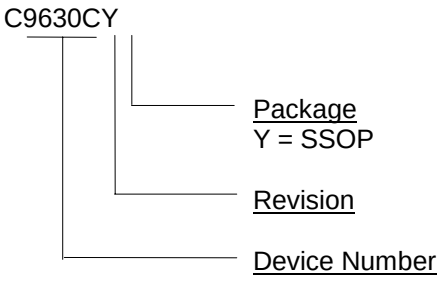
48 Pin SSOP Outline Dimensions

	INCHES			MILLIMETERS		
SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
A	0.095	0.102	0.110	2.41	2.59	2.79
A_1	0.008	0.012	0.016	0.203	0.305	0.406
A2	0.088	-	0.092	2.24	-	2.34
B	0.008	-	0.0135	0.203	-	0.343
C	0.005	-	0.010	0.127	-	0.254
D	0.620	0.625	0.630	15.75	15.88	16.00
E	0.291	0.295	0.299	7.39	7.49	7.60
e	0.025 BSC			0.635 BSC		
H	0.395	-	0.420	10.03	-	10.67
L	0.020	-	0.040	0.508	-	1.016
a	0º	-	8º	0º	-	8º

Ordering Information

Part Number	Package Type	Production Flow
C9630CY	48 PIN SSOP	Commercial, 0° to 70°C

Marking: Example: Cypress
C9630CY
Date Code, Lot #



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Document Title: C9630 PC133 Clock Generator for SiS630/Pentium®III & SiS540/Socket7 Applications **Document Number:** 38-07035				
Rev.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	106963	06/11/01	IKA	Convert from IMI to Cypress
*A	122728	12/18/02	RBI	Added power-up requirements to maximum ratings information.