

P-Channel 20-V (D-S) MOSFET

Description

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low rDS(on) and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

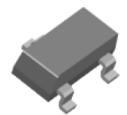
Features

Low rDS(on) provides higher efficiency and extends
battery life

- · Low thermal impedance copper lead frame
- SOT-23 saves board space
- · Fast switching speed
- · High performance trench technology
- RoHS compliant package

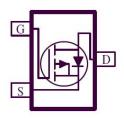
Packing & Order Information

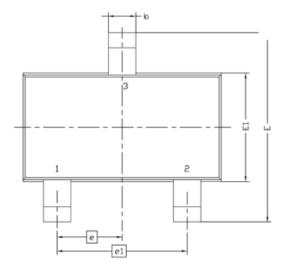
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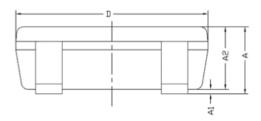


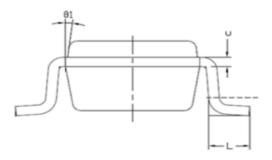


Graphic symbol









Symbol	MILLIMETERS			
Symbol	MIN	MAX		
Α	0.8	1.2		
A1	0	0.1		
A2	0.7	1.1		
b	0.3 0.5			
С	0.1 0.2			
D	2.7	3.1		
E	2.6	3		
E1	1.4	1.8		
е	0.95 BSC			
e1	1.9 BSC			
L	0.3	0.6		
θ1	7° NOM			



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MAXIMUM RATINGS AND ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (T _A =25°C unless otherwise specified)					
Symbol	Parameter Value		Unit		
V _{DS}	Drain-Source Voltage	-20	V		
V _{GS}	Gate-Source Voltage	±8	V		
L	Continuous Drain Current ^a (T _A =25°C)	-2.6	А		
ID	Continuous Drain Current ^a (T _A =70°C)	-1.5	А		
I _{DM}	Pulsed Drain Current ^b	-10	А		
I _S	Continuous Source Current (Diode Conduction) ^a	±1.6	А		
P _D	Power Dissipation ^a ($T_A = 25^{\circ}C$)	1.25	W		
	Power Dissipation ^a (T _A =70°C)	0.8	W		
TJ/T _{STG}	Operating Junction and Storage Temperature	-55 to +150	°C		

THERMAL RESISTANCE RATINGS						
Symbol	Parameter	Maximum	Units			
R _{θJA}	Maximum Junction-to-Ambient ^a (t <= 5 sec)	100	°C/W			
	Maximum Junction-to-Ambient ^a (Steady-State)	166	C/VV			

Notes:

a. Surface Mounted on 1" x 1" FR4 Board.

b. Pulse width limited by maximum junction temperature

Static						
Symbol	Parameter	Test Conditions	Min	Тур.	Max.	Units
V _{GS(th)}	Gate-Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250 \mu A$	-0.4		-1	
I _{GSS}	Gate-Body Leakage	$V_{DS} = 0 V$, $V_{GS} = \pm 8 V$			±100	nA
I _{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -16 \text{ V}$, $V_{GS} = 0 \text{ V}$ $V_{DS} = -16 \text{ V}$, $V_{GS} = 0 \text{ V}$, $T_J = 55^{\circ}\text{C}$			-1 -10	uA
I _{D(on)}	On-State Drain Current ^A	$V_{DS} = -5 V, V_{GS} = -4.5 V$	-3			A
r DS(on)	Drain-Source On-Resistance ^A	$V_{GS} = -4.5 \text{ V}, I_D = -2.6 \text{ A}$ $V_{GS} = -2.5 \text{ V}, I_D = -2.1 \text{ A}$			0.130 0.190	Ω
g _{fs}	Forward Tranconductance ^A	$V_{DS} = -5 \text{ V}, \text{ I}_{D} = -2.8 \text{ A}$		3		S
V _{SD}	Diode Forward Voltage	$I_{S} = -1.6 \text{ V}, \text{ V}_{GS} = 0 \text{ V}$		-0.70		V

Dynamic ^b						
Symbol	Parameter	Test Conditions	Min	Тур.	Max.	Units
t _{d(on)}	Turn-On Delay Time			6.5		ns
t _r	Rise Time	$V_{DD} = -5 V$, $R_L = -5 OHM$		20		ns
t _{d(off)}	Turn-Off Delay Time	V_{GEN} = -4.5 V , R_{G} = 6 OHM		31		ns
tf	Fall Time			21		ns



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Dynamic ^b						
Symbol	Parameter	Test Conditions	Min	Тур.	Max.	Units
Qg	Total Gate Charge	$V_{DS} = -5 V$, $I_D = -2.6 A$, $V_{GS} = -4.5 V$		12.2		nC
Q _{gs}	Gate-Source Charge			1.1		nC
Q_{gd}	Gate-Drain Charge			1.5		nC

Notes:

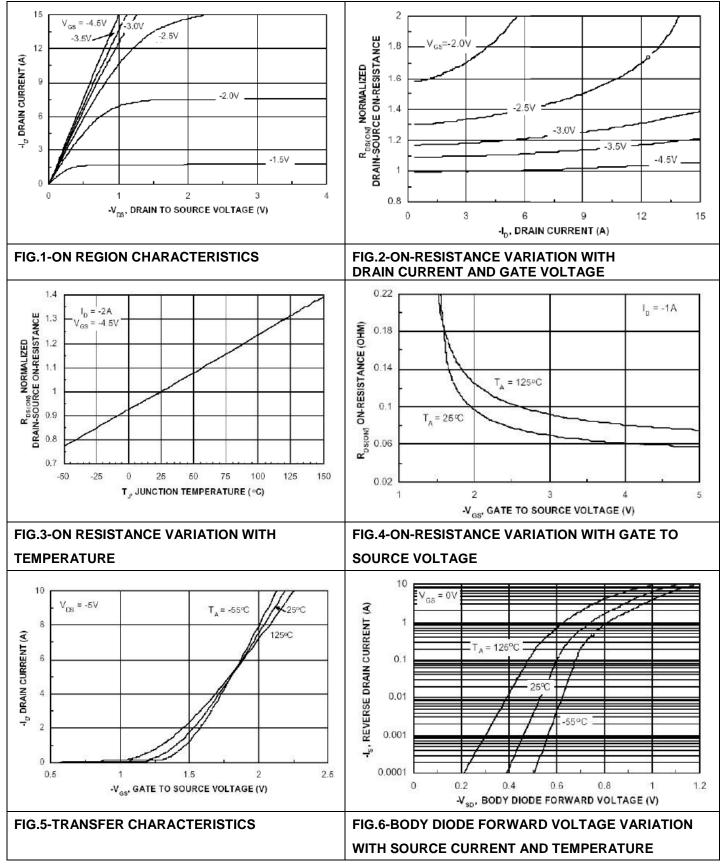
a. Pulse test: PW <= 300us duty cycle <= 2%.

b. Guaranteed by design, not subject to production testing.



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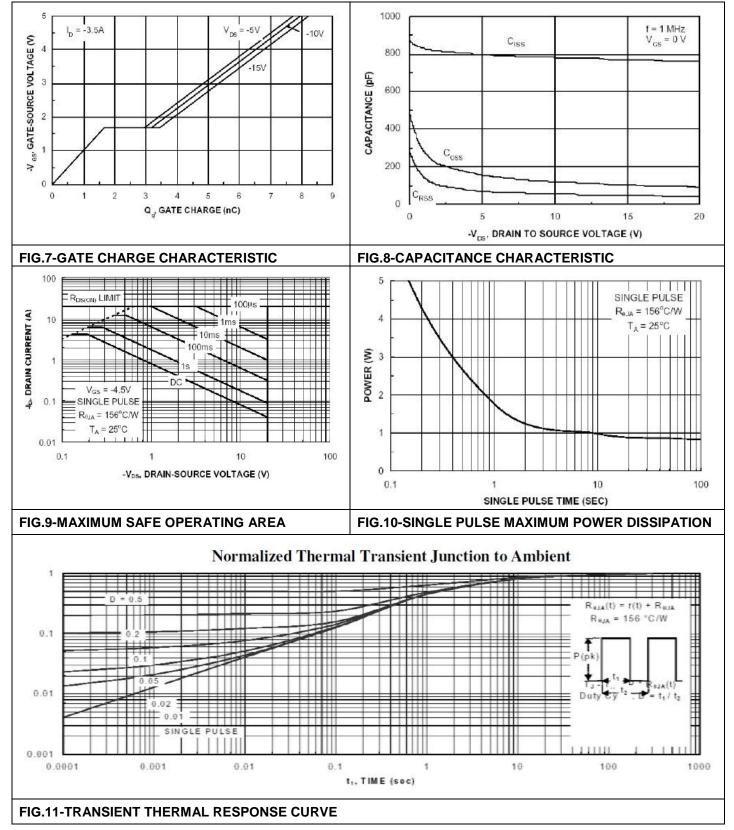
Characteristic Curves





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