

Automotive-grade N-channel 40 V, 3.0 mΩ typ., 120 A STripFET™ F6 Power MOSFET in a PowerFLAT™ 5x6 package

Datasheet - production data

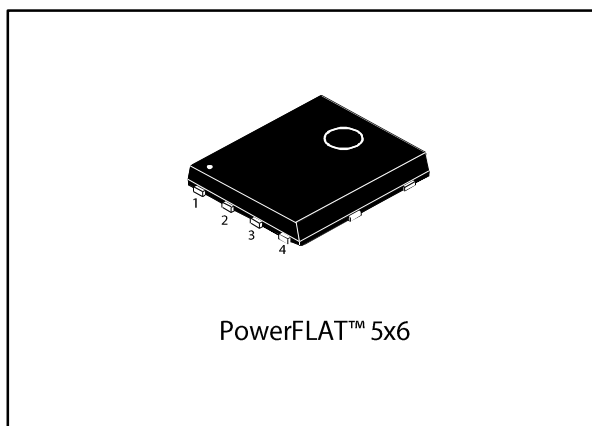
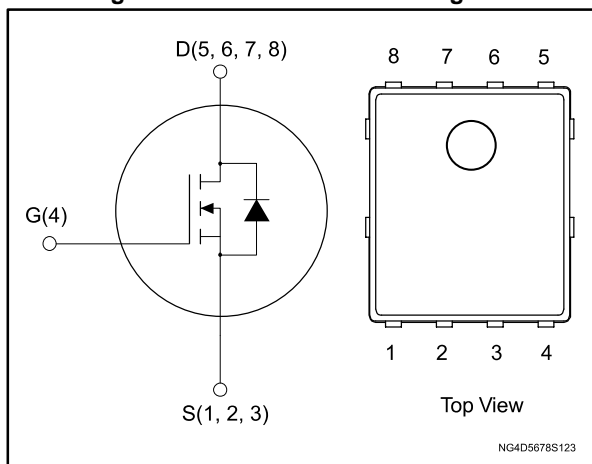


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max.	I _D	P _{TOT}
STL120N4LF6AG	40 V	3.6 mΩ	120 A	96 W

- Designed for automotive applications and AEC-Q101 qualified
- Very low on-resistance
- Very low gate charge
- High avalanche ruggedness
- Low gate drive power loss
- Wettable flanks package

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using the STripFET™ F6 technology with a new trench gate structure. The resulting Power MOSFET exhibits very low R_{DS(on)} in all packages.

Table 1: Device summary

Order code	Marking	Package	Packing
STL120N4LF6AG	120N4LF6	PowerFLAT™ 5x6	Tape and reel

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	40	V
V_{DS}	Drain-source voltage	± 20	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	120	A
$I_D^{(2)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	55	A
$I_D^{(2)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	55	A
$I_{DM}^{(3)}$	Drain current (pulsed)	220	A
$I_D^{(4)}$	Drain current (continuous) at $T_{pcb} = 25\text{ }^\circ\text{C}$	26	A
$I_D^{(4)}$	Drain current (continuous) at $T_{pcb} = 100\text{ }^\circ\text{C}$	19	A
$I_{DM}^{(3/4)}$	Drain current (pulsed)	104	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	96	W
$P_{TOT}^{(4)}$	Total dissipation at $T_{pcb} = 25\text{ }^\circ\text{C}$	4.8	W
T_{stg}	Storage temperature	-55 to 175	$^\circ\text{C}$
T_j	Operating junction temperature		

Notes:

- (1) This value is limited by the silicon
(2) This value is limited by the package
(3) Pulse width is limited by safe operating area.
(4) This value is rated according to $R_{thj-pcb}$

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	1.56	$^\circ\text{C/W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	31.3	

Notes:

- (1) When mounted on 1 inch² 2 Oz. Cu board, $t \leq 10\text{ s}$

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AV}	Avalanche current, repetitive or not repetitive (pulse width limited by maximum junction temperature)	26	A
E_{AS}	Single pulse avalanche energy ($T_j = 25\text{ }^\circ\text{C}$, $I_D = I_{AV}$, $V_{DD} = 25\text{ V}$)	200	mJ

2 Electrical characteristics

($T_C = 25\text{ °C}$ unless otherwise specified)

Table 5: Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$	40			V
I_{DSS}	Zero gate voltage Drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 40\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 40\text{ V}$, $T_j = 125\text{ °C}$			10	μA
I_{GSS}	Gate-body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 20\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	1		3	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 13\text{ A}$		3.0	3.6	m Ω
		$V_{GS} = 5\text{ V}$, $I_D = 13\text{ A}$		3.2	4.5	

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	4260	-	pF
C_{oss}	Output capacitance		-	647	-	
C_{rss}	Reverse transfer capacitance		-	373	-	
Q_g	Total gate charge	$V_{DD} = 20\text{ V}$, $I_D = 26\text{ A}$, $V_{GS} = 10\text{ V}$ (see Figure 14: "Test circuit for gate charge behavior")	-	80	-	nC
Q_{gs}	Gate-source charge		-	15	-	
Q_{gd}	Gate-drain charge		-	15	-	
R_G	Intrinsic gate resistance	$f = 1\text{ MHz}$, $I_D = 0\text{ A}$	-	1.5	-	Ω

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 20\text{ V}$, $I_D = 13\text{ A}$ $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$ (see Figure 13: "Test circuit for resistive load switching times" and Figure 18: "Switching time waveform")	-	20	-	ns
t_r	Rise time		-	70	-	
$t_{d(off)}$	Turn-off-delay time		-	40	-	
t_f	Fall time		-	20	-	

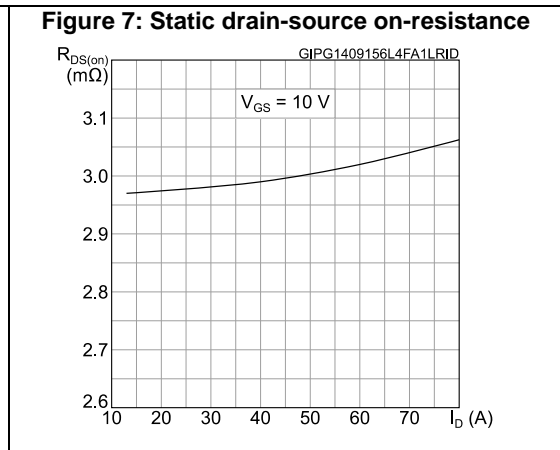
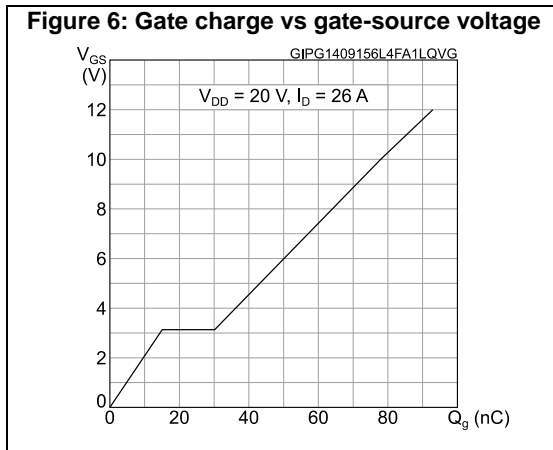
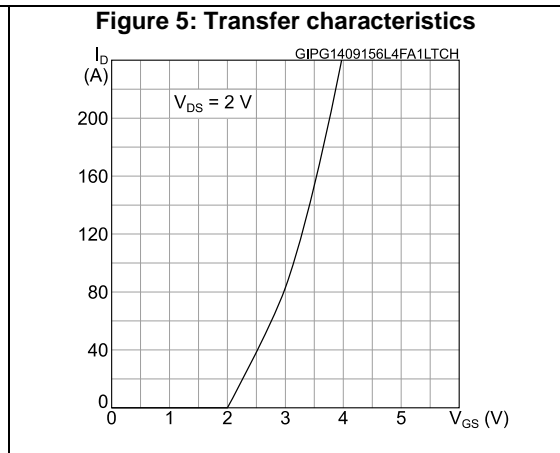
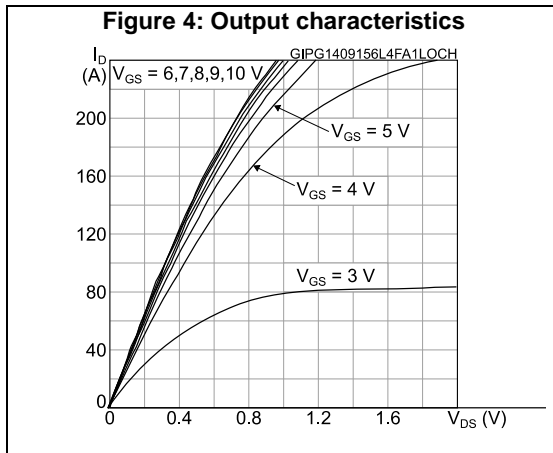
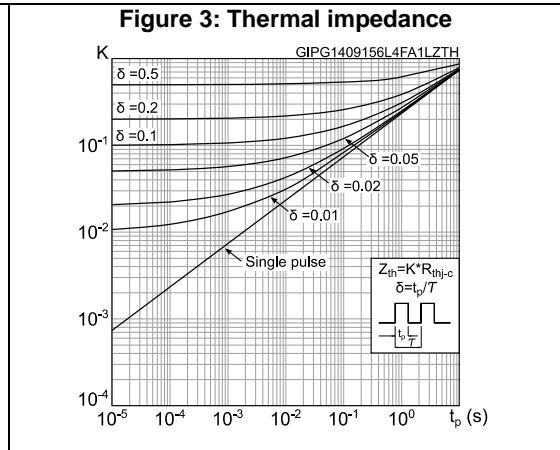
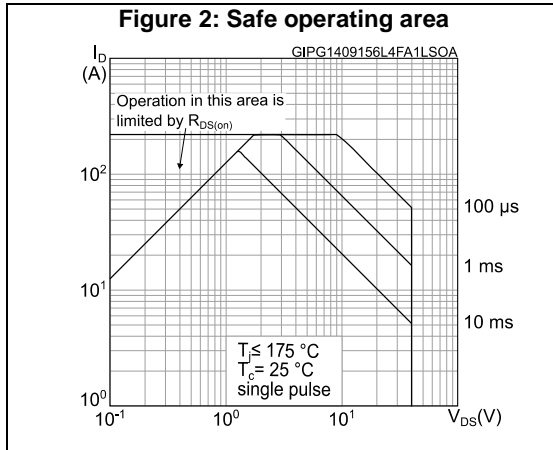
Table 8: Source drain diode

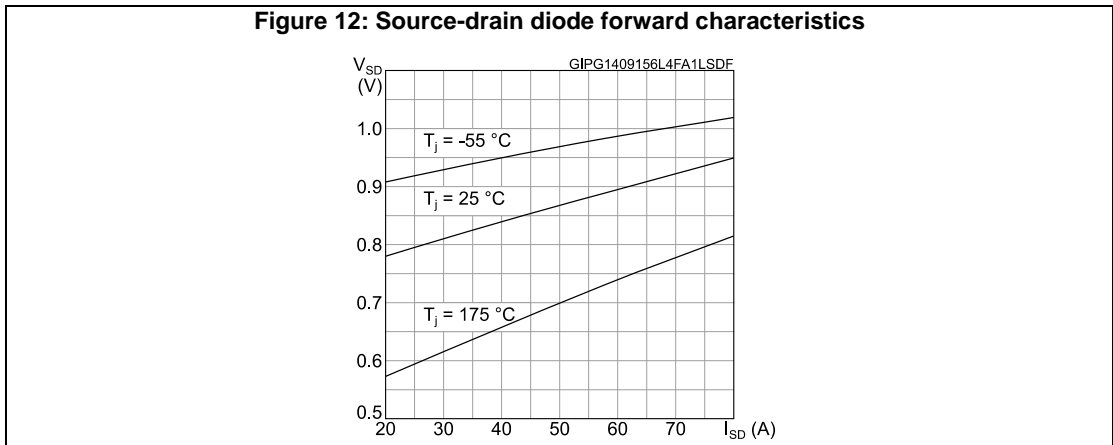
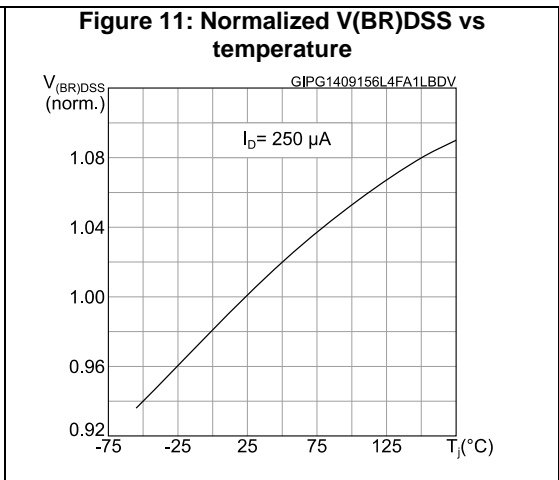
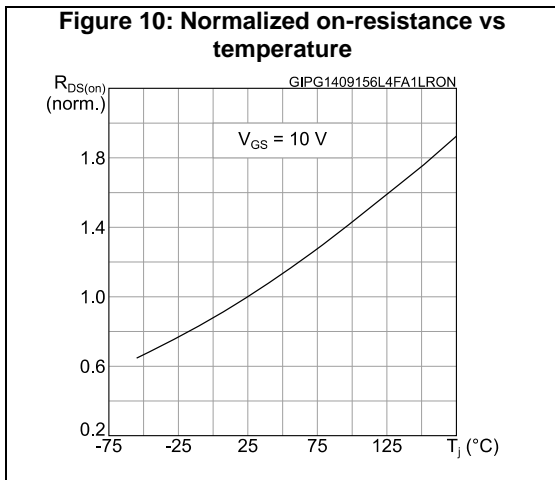
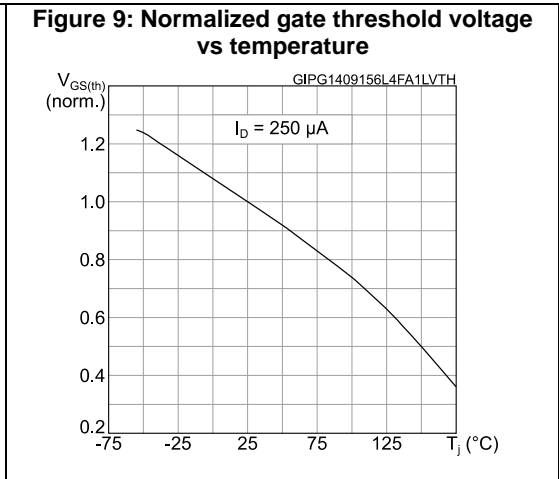
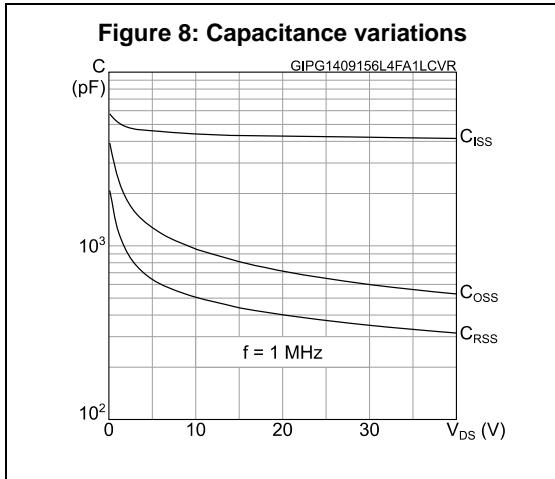
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}^{(1)}$	Source-drain current		-		26	A
$I_{SDM}^{(2)}$	Source-drain current (pulsed)		-		104	A
$V_{SD}^{(3)}$	Forward on voltage	$V_{GS} = 0\text{ V}$, $I_{SD} = 13\text{ A}$	-		1.1	V
t_{rr}	Reverse recovery time	$I_{SD} = 26\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 25\text{ V}$ (see Figure 15 : "Test circuit for inductive load switching and diode recovery times")	-	40		ns
Q_{rr}	Reverse recovery charge		-	5.6		nC
I_{RRM}	Reverse recovery current		-	2.8		A

Notes:

- (1) This value is rated according to $R_{thj-pcb}$
- (2) Pulse width is limited by safe operating area
- (3) Pulse test: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)





3 Test circuits

Figure 13: Test circuit for resistive load switching times



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Figure 14: Test circuit for gate charge behavior



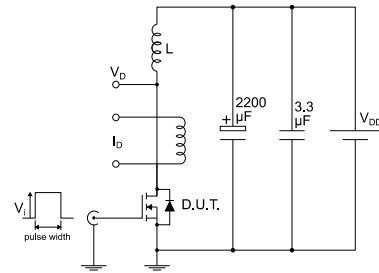
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Figure 15: Test circuit for inductive load switching and diode recovery times



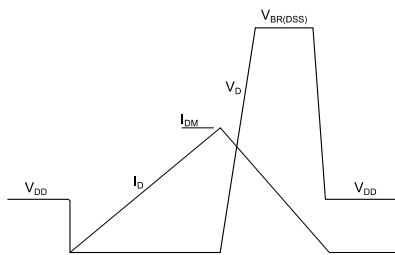
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Figure 16: Unclamped inductive load test circuit



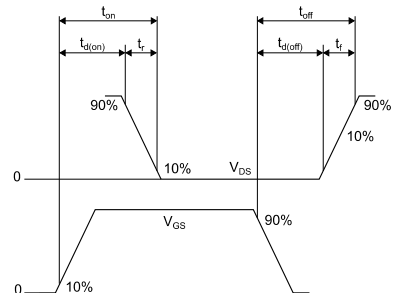
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Figure 17: Unclamped inductive waveform



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Figure 18: Switching time waveform



AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 PowerFLAT™ 5x6 WF type R package information

Figure 19: PowerFLAT™ 5x6 WF type R package outline

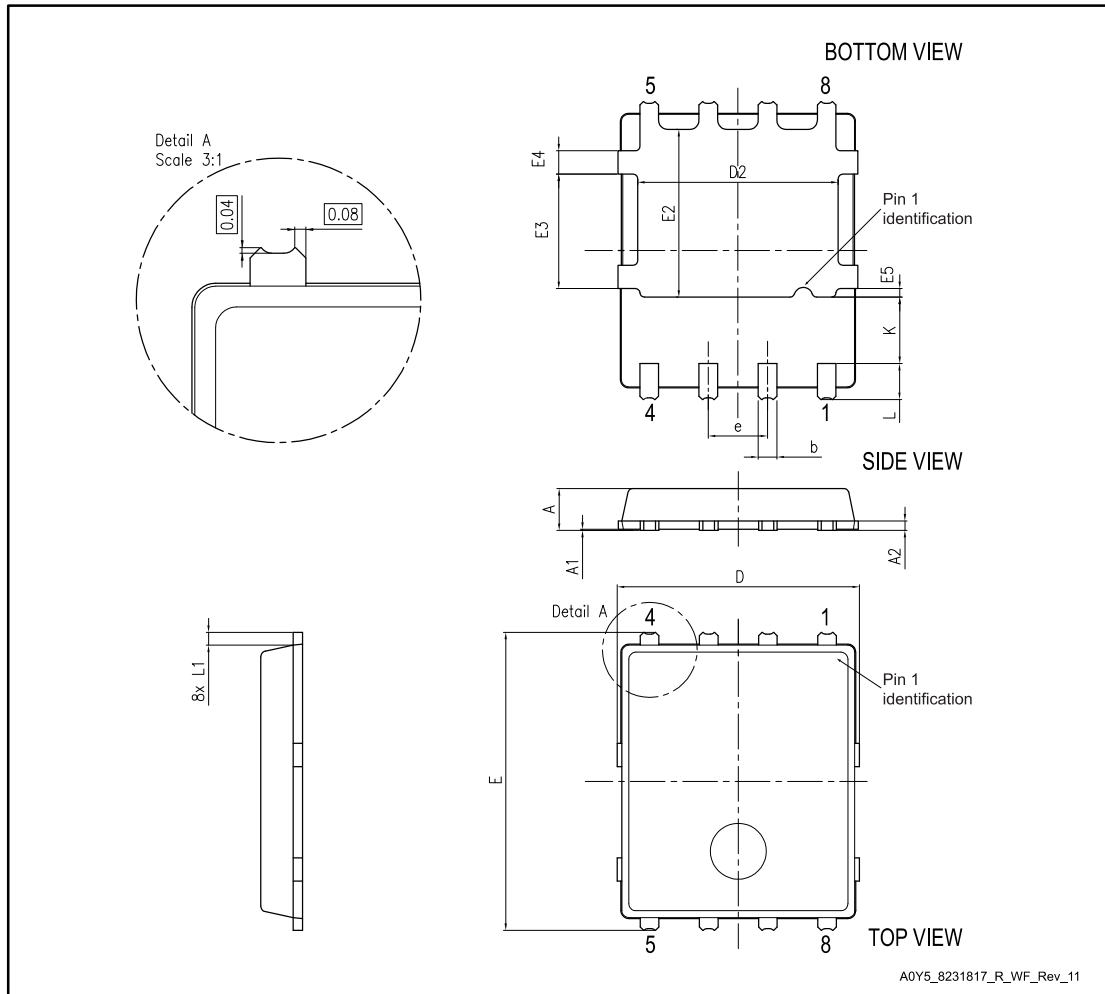
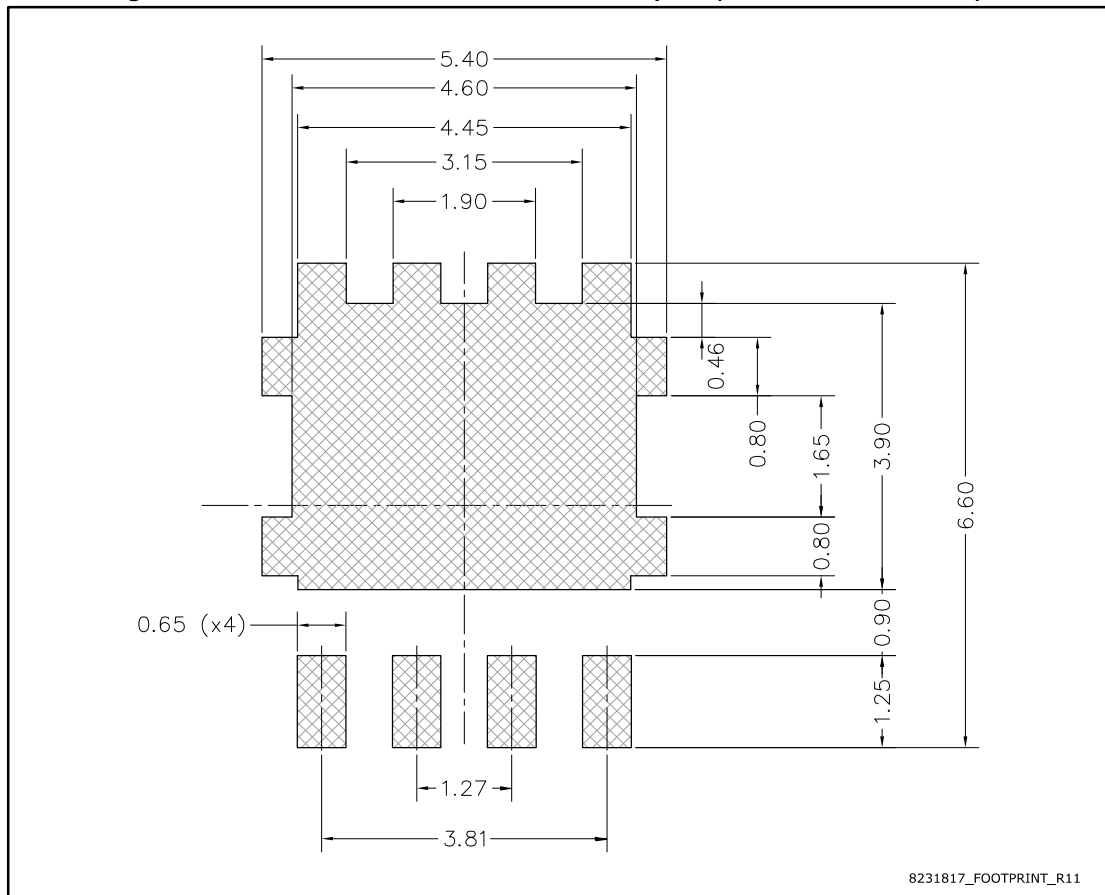


Table 9: PowerFLAT™ 5x6 WF type R mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
D	5.00	5.20	5.40
E	6.20	6.40	6.60
D2	4.15		4.45
E2	3.50		3.70
e		1.27	
L	0.70		0.90
L1		0.275	
K	1.275		1.575
E3	2.35		2.55
E4	0.40		0.60
E5	0.08		0.28

Figure 20: PowerFLAT™ 5x6 recommended footprint (dimensions are in mm)



4.2 PowerFLAT™ 5x6 WF packing information

Figure 21: PowerFLAT™ 5x6 WF tape

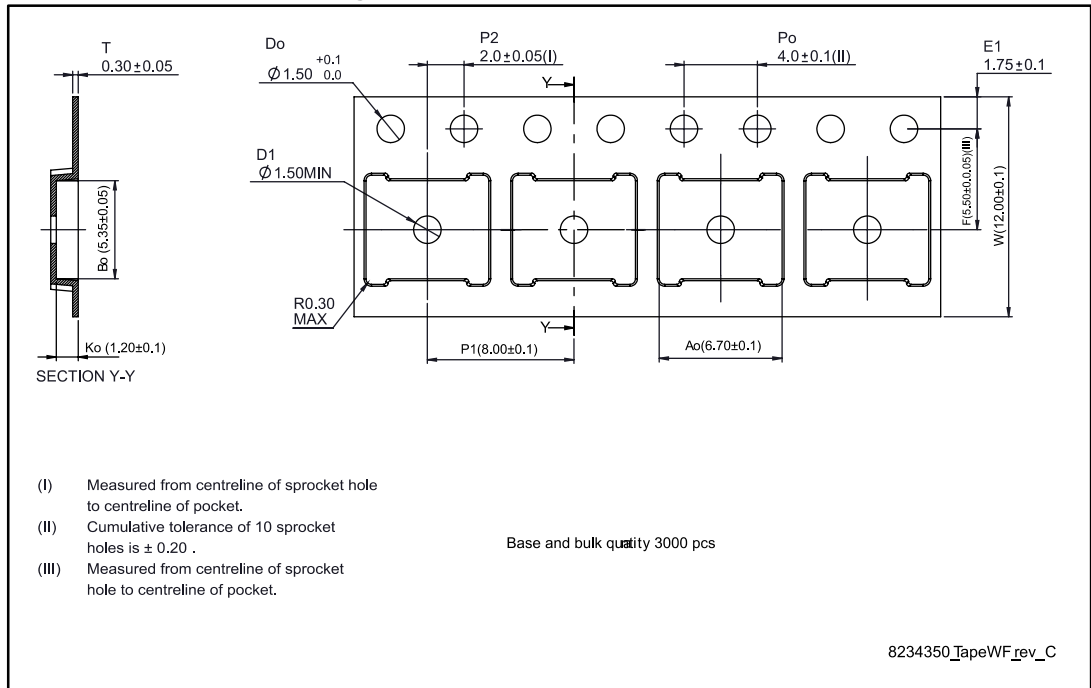


Figure 22: PowerFLAT™ 5x6 package orientation in carrier tape

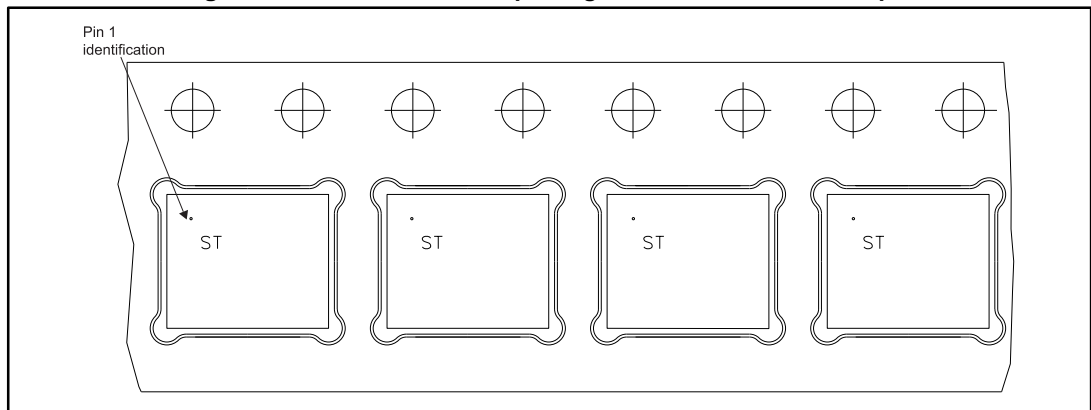
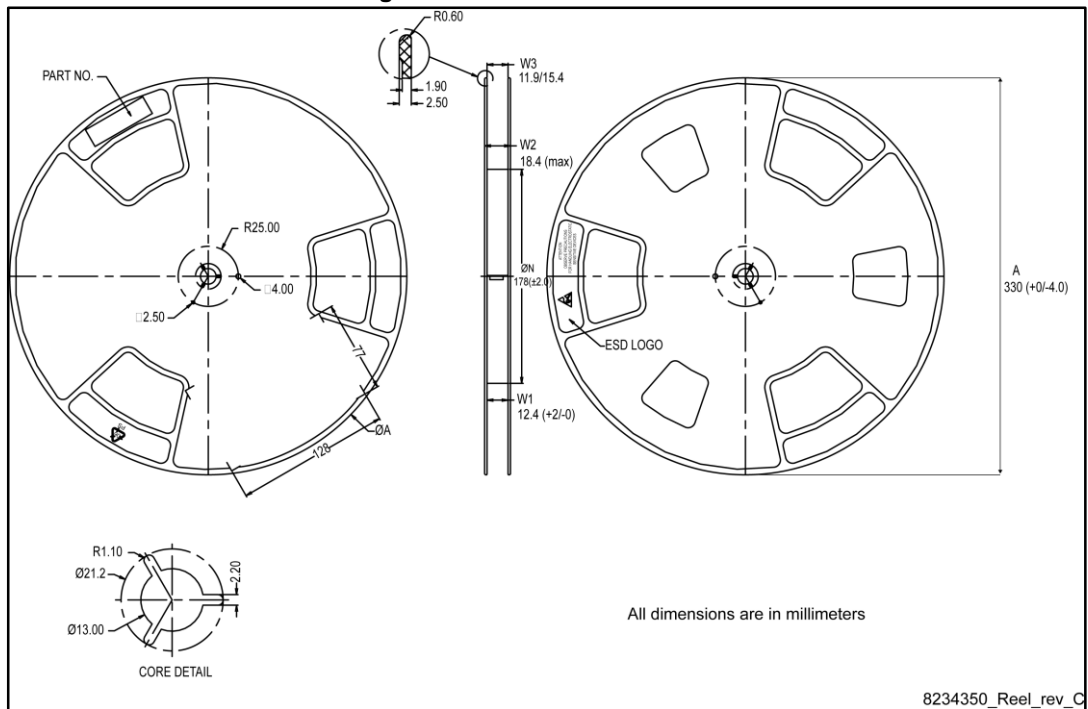


Figure 23: PowerFLAT™ 5x6 reel



5 Revision history

Table 10: Document revision history

Date	Revision	Changes
25-Sep-2015	1	First release.

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