BLF8G09LS-270W; BLF8G09LS-270GW

Power LDMOS transistor

Rev. 2 — 17 January 2014 Product data sheet

1. Product profile

1.1 General description

270 W LDMOS power transistor with improved video bandwidth for base station applications at frequencies from 716 MHz to 960 MHz.

Table 1. Typical performance

Typical RF performance at T_{case} = 25 °C in a common source class-AB production test circuit, tested on straight lead device.

Test signal	f	V_{DS}	$P_{L(AV)}$	G_p	η_D	$ACPR_{5M}$
	(MHz)	(V)	(W)	(dB)	(%)	(dBc)
2-carrier W-CDMA	716 to 728	28	67	20	33	–35[1]

[1] Test signal: 3GPP test model 1; 64 DPCH; PAR = 8.4 dB at 0.01 % probability on CCDF; carrier spacing 5 MHz.

1.2 Features and benefits

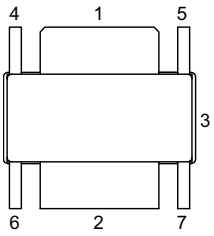
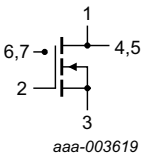
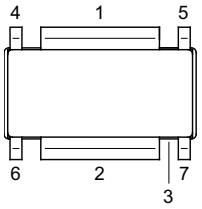
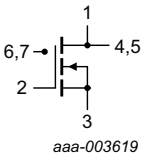
- Excellent ruggedness
- Device can operate with the supply current delivered through the video leads
- High efficiency
- Low thermal resistance providing excellent thermal stability
- Designed for broadband operation (716 MHz to 960 MHz)
- Lower output capacitance for improved performance in Doherty applications
- Decoupling leads to enable improved video bandwidth (55 MHz typical)
- Designed for low memory effects providing excellent pre-distortability
- Internally matched for ease of use
- Integrated ESD protection
- Design optimized for gull-wing and straight lead versions
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

- RF power amplifiers for W-CDMA base stations and multi carrier applications in the 716 MHz to 960 MHz frequency range

2. Pinning information

Table 2. Pinning

Pin	Description		Simplified outline	Graphic symbol
BLF8G09LS-270W (SOT1244B)				
1	drain			
2	gate			
3	source	[1]		
4	video lead	[2]		
5	video lead	[2]		
6	n.c.			
7	n.c.			
BLF8G09LS-270GW (SOT1244C)				
1	drain			
2	gate			
3	source	[1]		
4	video lead	[2]		
5	video lead	[2]		
6	n.c.			
7	n.c.			

[1] Connected to flange.

[2] Device can operate with the supply current delivered through the combined video leads.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLF8G09LS-270W	-	earless flanged ceramic package; 6 leads	SOT1244B
BLF8G09LS-270GW	-	earless flanged ceramic package; 6 leads	SOT1244C

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage			-	65	V
V_{GS}	gate-source voltage			–0.5	+13	V
T_{stg}	storage temperature			–65	+150	°C
T_j	junction temperature		[1]	-	225	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the on-line MTF calculator.

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	T_{case} = 80 °C; P_L = 67 W; V_{DS} = 28 V; I_{Dq} = 2000 mA	0.265	K/W

6. Characteristics

Table 6. DC characteristics

T_j = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 4.5 mA	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 450 mA	1.5	1.8	2.3	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 28 V	-	-	4.2	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	-	82	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	420	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 450 mA	-	3.92	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 15.75 A	-	0.04	-	Ω

Table 7. RF characteristics

Test signal: 2-carrier W-CDMA; PAR = 8.4 dB at 0.01 % probability on the CCDF; 3GPP test model 1; 1-64 DPCH; f_1 = 718.5 MHz; f_2 = 723.5 MHz; f_3 = 720.5 MHz; f_4 = 725.5 MHz; RF performance at V_{DS} = 28 V; I_{Dq} = 2000 mA; T_{case} = 25 °C; unless otherwise specified; in a class-AB production test circuit, tested on straight lead device.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	$P_{L(AV)}$ = 67 W	18.8	20	-	dB
RL_{in}	input return loss	$P_{L(AV)}$ = 67 W	-	–13	–9	dB
η_D	drain efficiency	$P_{L(AV)}$ = 67 W	28	33	-	%
$ACPR_{5M}$	adjacent channel power ratio (5 MHz)	$P_{L(AV)}$ = 67 W	-	–35	–30	dBc

7. Test information

7.1 Ruggedness in class-AB operation

The BLF8G09LS-270W and BLF8G09LS-270GW are capable of withstanding a load mismatch corresponding to VSWR = 7 : 1 through all phases under the following conditions: PAR = 8.4 dB at 0.01 % probability on CCDF; 3GPP test model 1; 64 DPCH; V_{DS} = 28 V; I_{Dq} = 2000 mA; 2-carrier W-CDMA signal; $P_{L(AV)}$ = 51.8 dBm; f = 716 MHz.

7.2 Impedance information

Table 8. Typical impedance

Measured load-pull data; I_{Dq} = 2000 mA; V_{DS} = 28 V. Typical values unless otherwise specified.

f	Z_S[1]	Z_L[1]
(MHz)	(Ω)	(Ω)
716	1.09 – j1.62	2.31 – j1.69
800	1.43 – j2.41	2.06 – j0.76
869	1.46 – j3.21	1.6 – j0.66
925	1.88 – j3.62	1.23 – j0.39
960	2.22 – j4.73	1.01 – j0.55

[1] Z_S and Z_L defined in Figure 1.

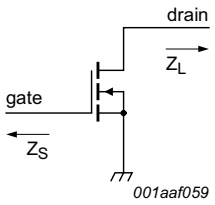
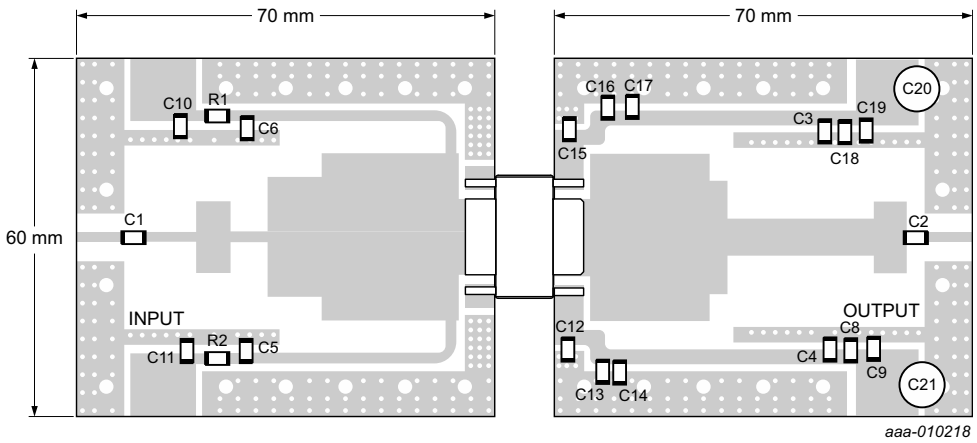


Fig 1. Definition of transistor impedance

7.3 VBW in class-AB operation

The BLF8G09LS-270W and BLF8G09LS-270GW show 55 MHz (typical) video bandwidth in class-AB test circuit in 722 MHz band at V_{DS} = 28 V and I_{Dq} = 2000 mA.

7.4 Test circuit



Printed-Circuit Board (PCB): Rogers RO4350B with a thickness of 0.762 mm.

See Table 9 for a list of components.

Fig 2. Component layout

Table 9. List of components

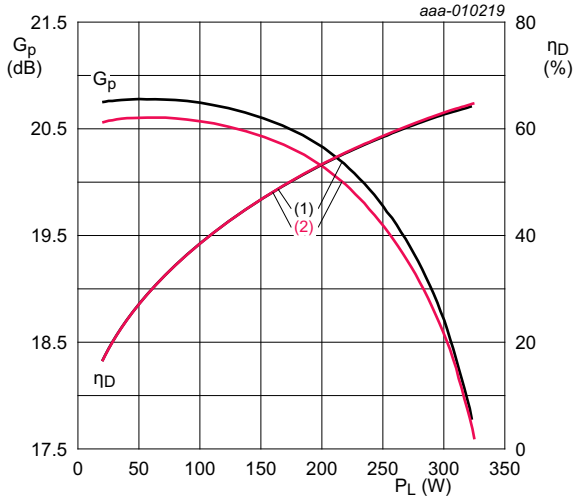
For test circuit see Figure 2.

Component	Description	Value	Remarks
C1, C2, C3, C4, C5, C6	multilayer ceramic chip capacitor	510 pF	ATC100B
C8, C9, C10, C11, C12, C13, C14, C15, C16, C17, C18, C19	multilayer ceramic chip capacitor	4.7 μF, 50 V	Murata
C20, C21	electrolytic capacitor	2200 μF, 63 V	
R1, R2	resistor	9.1 Ω	SMD 0805

7.5 Graphical data

7.5.1 Straight lead

7.5.1.1 CW



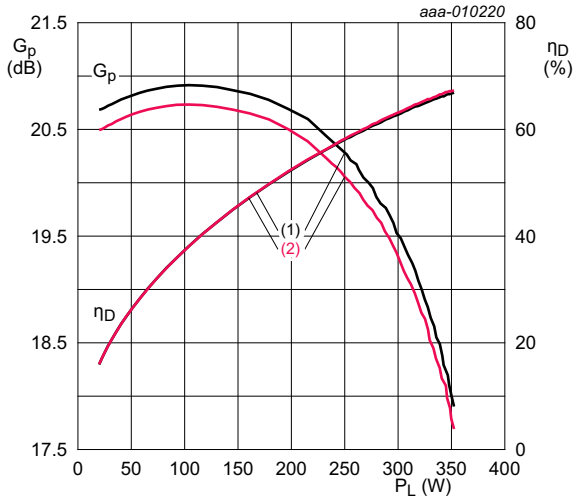
V_{DS} = 28 V; I_{Dq} = 2000 mA.

(1) f = 716 MHz

(2) f = 728 MHz

Fig 3. Power gain and drain efficiency as function of output power; typical values

7.5.1.2 CW pulsed



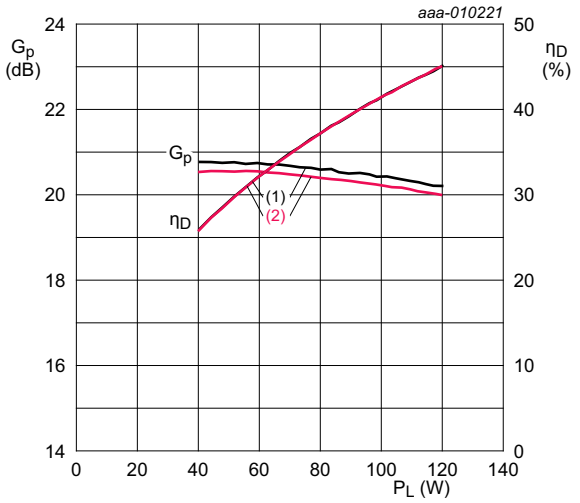
V_{DS} = 28 V; I_{Dq} = 2000 mA; t_p = 100 µs; δ = 10 %

(1) f = 716 MHz

(2) f = 728 MHz

Fig 4. Power gain and drain efficiency as function of output power; typical values

7.5.1.3 1-Carrier W-CDMA

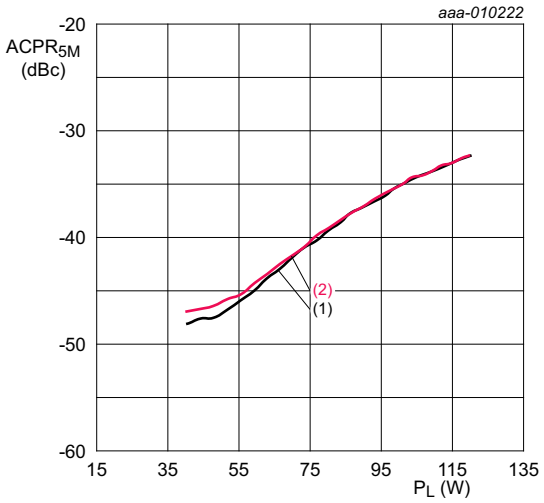


V_{DS} = 28 V; I_{Dq} = 2000 mA.

(1) f = 716 MHz

(2) f = 728 MHz

Fig 5. Power gain and drain efficiency as function of output power; typical values

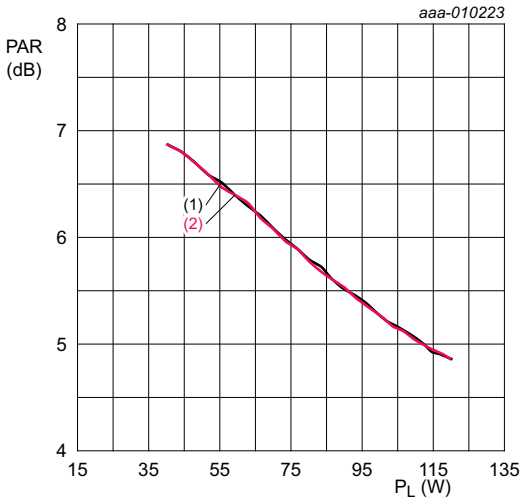


V_{DS} = 28 V; I_{Dq} = 2000 mA.

(1) f = 716 MHz

(2) f = 728 MHz

Fig 6. Adjacent channel power ratio (5 MHz) as a function of output power; typical values



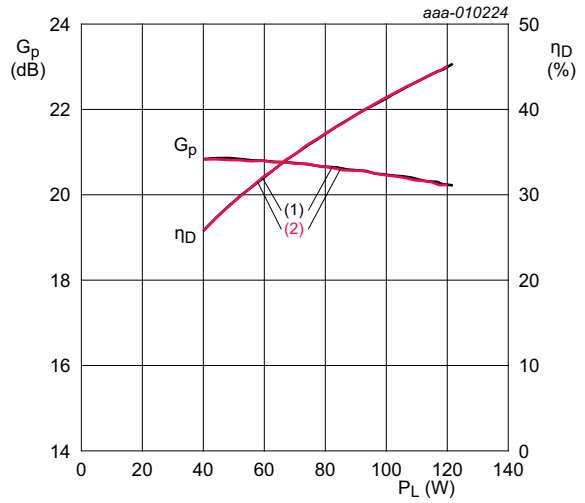
V_{DS} = 28 V; I_{Dq} = 2000 mA.

(1) f = 716 MHz

(2) f = 728 MHz

Fig 7. Peak-to-average ratio as a function of output power; typical values

7.5.1.4 2-Carrier W-CDMA

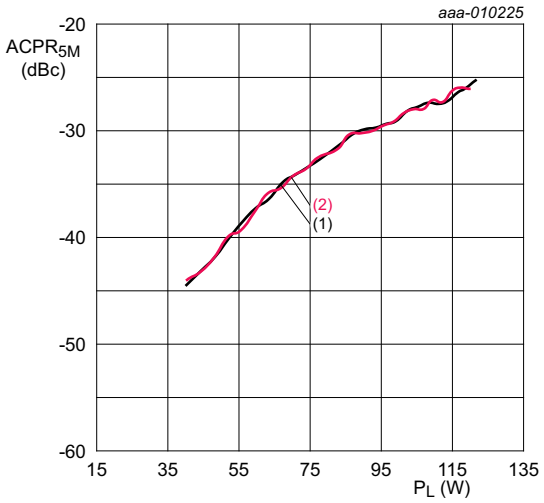


V_{DS} = 28 V; I_{Dq} = 2000 mA.

(1) f = 721 MHz

(2) f = 723 MHz

Fig 8. Power gain and drain efficiency as function of output power; typical values



V_{DS} = 28 V; I_{Dq} = 2000 mA.

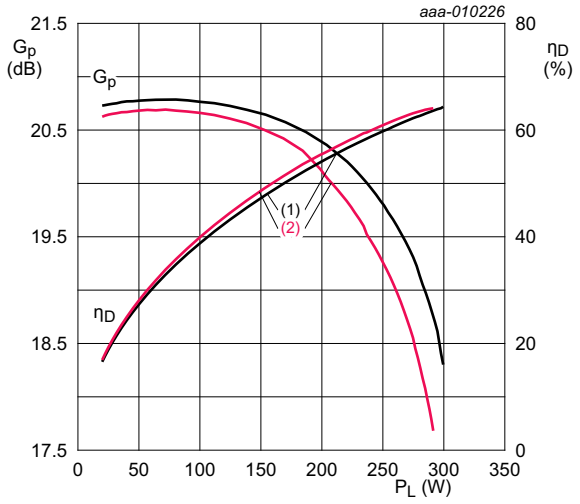
(1) f = 721 MHz

(2) f = 723 MHz

Fig 9. Adjacent channel power ratio (5 MHz) as a function of output power; typical values

7.5.2 Gull-wing

7.5.2.1 CW



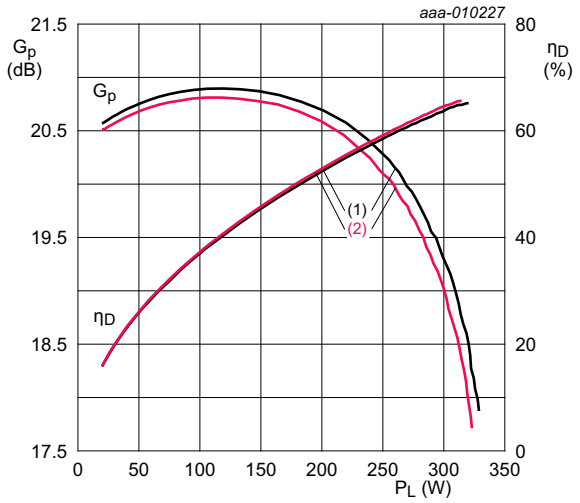
V_{DS} = 28 V; I_{Dq} = 2000 mA.

(1) f = 716 MHz

(2) f = 728 MHz

Fig 10. Power gain and drain efficiency as function of output power; typical values

7.5.2.2 CW pulsed



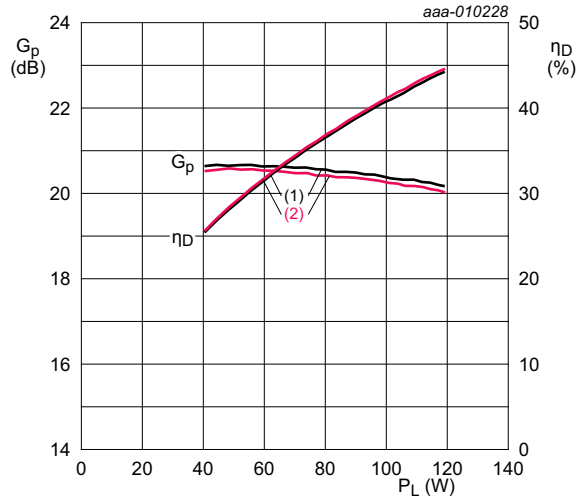
V_{DS} = 28 V; I_{Dq} = 2000 mA; t_p = 100 μs; δ = 10 %

(1) f = 716 MHz

(2) f = 728 MHz

Fig 11. Power gain and drain efficiency as function of output power; typical values

7.5.2.3 1-Carrier W-CDMA

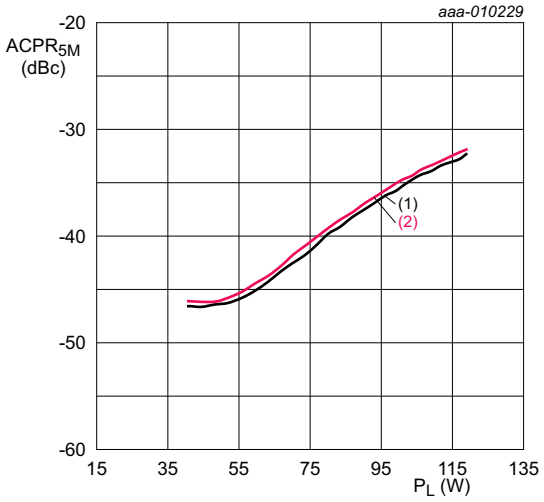


V_{DS} = 28 V; I_{Dq} = 2000 mA.

(1) f = 716 MHz

(2) f = 728 MHz

Fig 12. Power gain and drain efficiency as function of output power; typical values

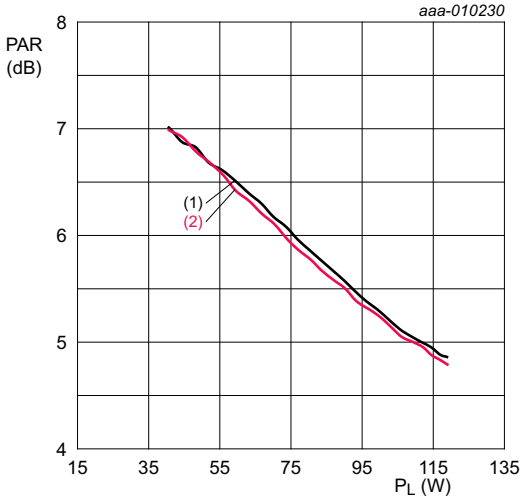


V_{DS} = 28 V; I_{Dq} = 2000 mA.

(1) f = 716 MHz

(2) f = 728 MHz

Fig 13. Adjacent channel power ratio (5 MHz) as a function of output power; typical values



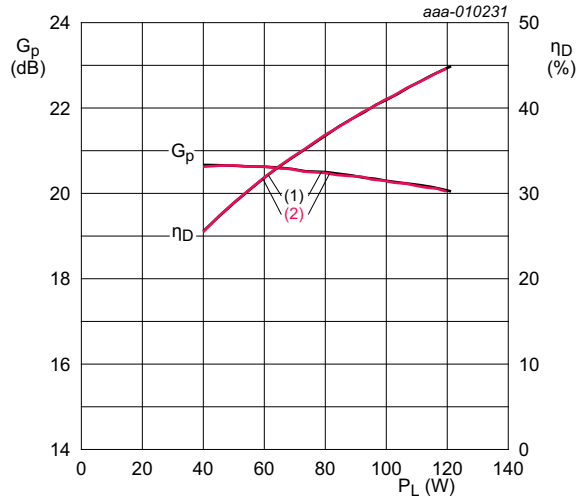
V_{DS} = 28 V; I_{Dq} = 2000 mA.

(1) f = 716 MHz

(2) f = 728 MHz

Fig 14. Peak-to-average ratio as a function of output power; typical values

7.5.2.4 2-Carrier W-CDMA

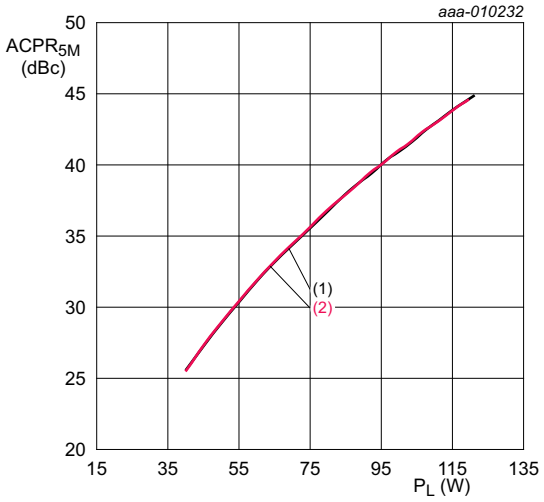


V_{DS} = 28 V; I_{Dq} = 2000 mA.

(1) f = 721 MHz

(2) f = 723 MHz

Fig 15. Power gain and drain efficiency as function of output power; typical values



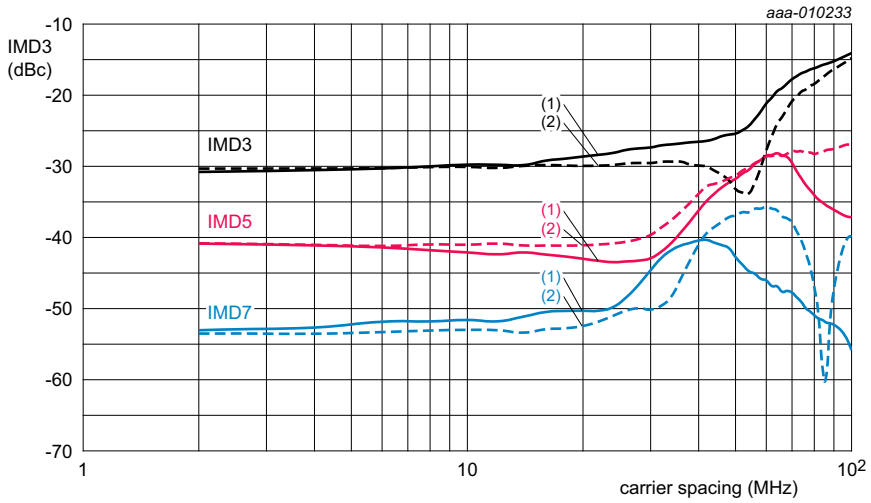
V_{DS} = 28 V; I_{Dq} = 2000 mA.

(1) f = 721 MHz

(2) f = 723 MHz

Fig 16. Adjacent channel power ratio (5 MHz) as a function of output power; typical values

7.5.2.5 2-Tone VBW



V_{DS} = 28 V; I_{Dq} = 2000 mA.

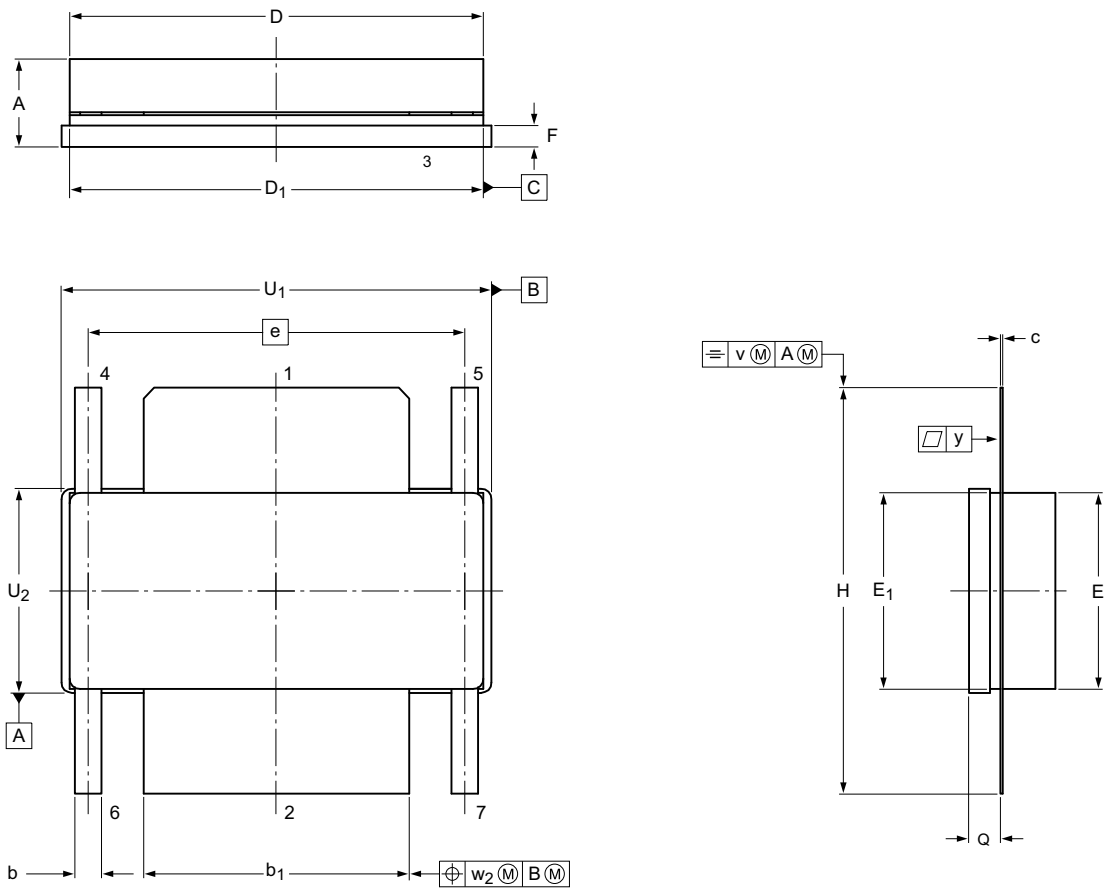
(1) IMD low

(2) IMD high

Fig 17. VBW capability in class-AB test circuit

8. Package outline

Earless flanged ceramic package; 6 leads **SOT1244B**



Dimensions

Unit[1]		A	b	b1	c	D	D1	e	E	E1	F	H	Q[2]	U1	U2	v	w2	y
mm	max	4.75	1.41	12.83	0.18	20.02	19.96		9.53	9.53	1.14	19.94	1.70	20.70	9.91	0.25	0.25	0.25
	nom							18.03										
	min	3.45	1.14	12.57	0.10	19.61	19.66		9.27	9.27	0.89	18.92	1.45	20.45	9.65			
inches	max	0.187	0.055	0.505	0.007	0.788	0.786		0.375	0.375	0.045	0.785	0.067	0.815	0.39	0.01	0.01	0.01
	nom							0.710										
	min	0.136	0.045	0.495	0.004	0.772	0.774		0.365	0.365	0.035	0.745	0.057	0.805	0.38			

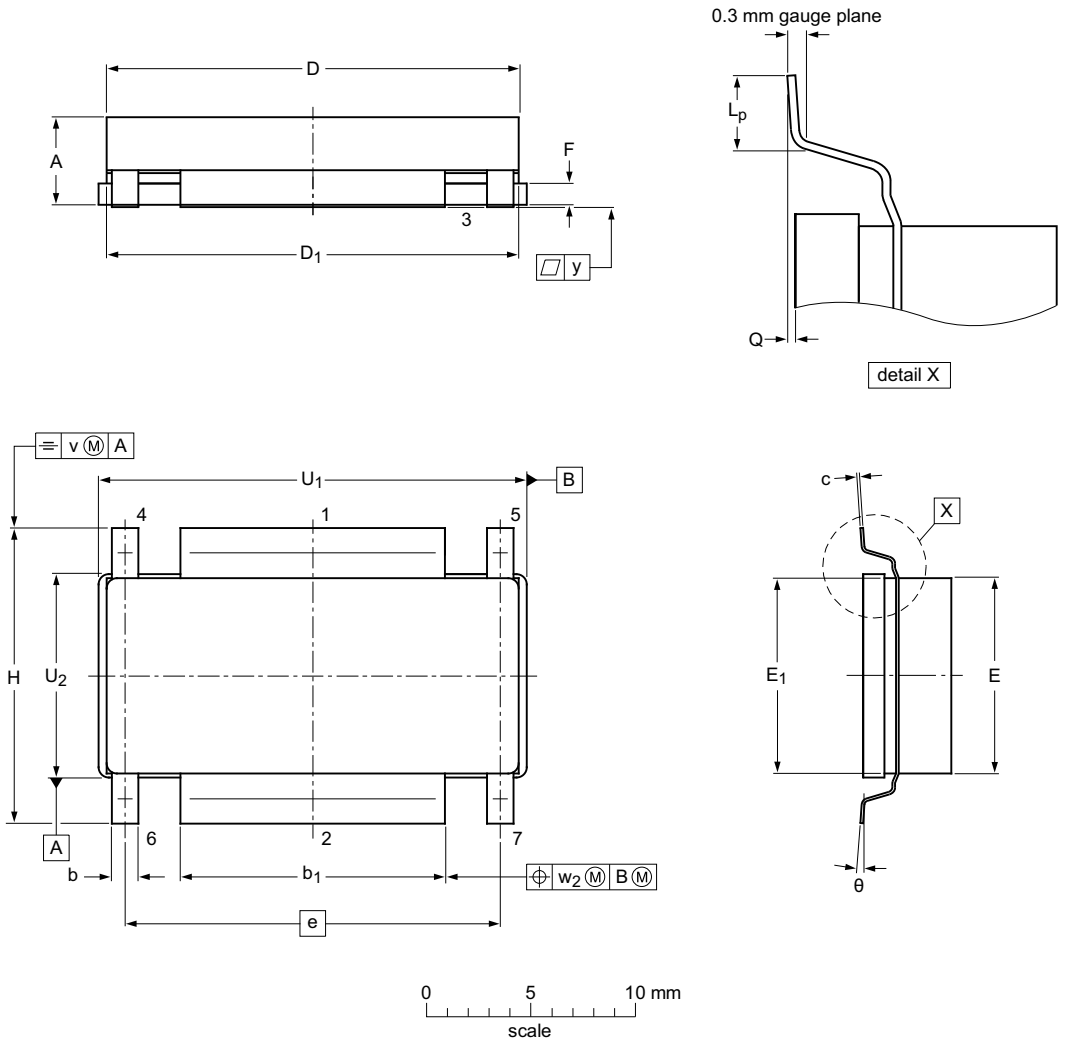
Note
1. Millimeter dimensions are derived from the original inch dimensions.
2. Dimension is measured 0.030 inch (0.76 mm) from body.

sot1244b_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1244B						~~12-04-18~~ 12-05-07

Fig 18. Package outline SOT1244B

Earless flanged ceramic package; 6 leads **SOT1244C**



Dimensions

Unit[1]		A	b	b_1	c	D	D_1	e	E	E_1	F	H	L_p	Q	U_1	U_2	v	w_2	y	θ
mm	max	4.75	1.41	12.83	0.18	20.02	19.96		9.53	9.53	1.14	14.3	1.38	0.195	20.70	9.91	0.25	0.25	0.15	7°
	nom							18.03												
	min	3.45	1.14	12.57	0.10	19.61	19.66		9.27	9.27	0.89	14.1	0.98	0.055	20.45	9.65				0°
inches	max	0.187	0.055	0.505	0.007	0.788	0.786		0.375	0.375	0.045	0.563	0.055	0.008	0.815	0.39	0.01	0.01	0.006	7°
	nom							0.710												
	min	0.136	0.045	0.495	0.004	0.772	0.774		0.365	0.365	0.035	0.555	0.039	0.002	0.805	0.38				0°

Note
1. Millimeter dimensions are derived from the original inch dimensions.

sot1244c_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1244C						~~12-05-10~~ 12-05-30

Fig 19. Package outline SOT1244C

9. Handling information

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

10. Abbreviations

Table 10. Abbreviations

Acronym	Description
3GPP	3rd Generation Partnership Project
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
DPCH	Dedicated Physical Channel
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal Oxide Semiconductor
MTF	Median Time to Failure
PAR	Peak-to-Average Ratio
SMD	Surface Mounted Device
VBW	Video Bandwidth
VSWR	Voltage Standing Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

11. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF8G09LS-270W_8G09LS-270GW v.2	20140117	Product data sheet	-	BLF8G09LS-270W_8G09LS-270GW v.1
Modifications:	• Table 1 on page 1: table updated • Table 7 on page 3: table updated • Section 7 on page 3: section added			
BLF8G09LS-270W_8G09LS-270GW v.1	20130927	Objective data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

12.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

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13. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

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