# 1. Introduction

The description of the receive mode of the MX909A given on the data sheet is based on the existence of an RF carrier detect signal that is used as a trigger to initiate the MX909A's signal acquisition process at the start of a received frame. Some systems, however, transmit a continuous carrier, which is intermittently modulated with a data stream. On these types of systems, no change in received RF carrier level will occur with the start of the frame reception. For this reason, continuous carrier systems cannot use RF 'carrier detect' as a signal acquisition trigger for the MX909A.

# 2. Baseband Data Detection

A continuous carrier system will transmit an unmodulated carrier between data packets. Therefore, differentiating between an unmodulated and modulated carrier can provide an effective means of determining the advent of a data packet. Similarly, the detection of the transition from modulated to unmodulated carrier can provide an indication of the end of a data packet.

In a continuous carrier system, the radio receiver output signal will be any of

- Wideband Noise (no RF carrier - out of range)
- Silent (unmodulated RF Carrier)
- Modulated Baseband Carrier

When no RF carrier is being received, the envelope at the discriminator output will be very wide due to the high RF gain yielding only wideband noise. It is assumed this case has been considered and so it will not be discussed further. When an unmodulated RF carrier is being received, the envelope at the discriminator output becomes very narrow (DC with low noise). As the data transmission starts, the modulated baseband carrier will appear causing the envelope to widen to the peak-to-peak amplitude of the received signal.

A signal acquisition trigger can be developed by observing the envelope of the receiver output signal to indicate when the signal undergoes a transition from 'silent' (unmodulated RF carrier before a data frame is received) to 'data modulated' (RF carrier is modulated with data). The change of the envelope from small to large amplitude indicates its transition from 'silent' to a 'modulated baseband carrier' signal and can be used as a signal acquisition trigger.

# 3. Envelope and End Of Packet Detectors

The MX909A contains circuits that can be used, with some external components, to create such a baseband data detector. In particular, it contains both positive and negative peak detectors with some holding capacitors (DOC1 and DOC2). (Note: The two capacitors represent high source impedance nodes so attached external circuits must be of very high input impedance). These two peak detectors operate with different time constants according to the configured operating mode of the MX909A. An external circuit is described to provide the following functions:

1. Use high input impedance voltage follower buffers to condition DOC1 and DOC2 signal voltages.
2. Develop a 'peak envelope threshold signal' by adding a fixed offset voltage to the actual 'valley' DOC2 capacitor voltage.
3. With hysteresis, compare the actual 'peak' DOC1 capacitor voltage with the 'peak envelope threshold signal' developed above. When the comparator trips then Envelope Detect goes high to indicate that the signal acquisition process should be triggered.

Where a signal acquisition trigger is important at the start of frame reception, an End of Packet detector is similarly helpful to force an ongoing frame reception process to abort due to lack of a data envelope. It is also useful to clearly demark the end of a packet so reliable detection of a new packet can occur. End of packet detection must respond slowly enough to ride through short signal fades.

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A schematic diagram for both Envelope Detect and End of Packet circuits is shown in Figure 1. Alternate circuit sections may be substituted so long as they provide an equivalent function. Note that the forward bias drop of the choice of Silicon or Germanium diodes directly sets the magnitude of the 'peak envelope threshold level.' Also note that the logic described with a truth table requires its input to continuously remain at a '1' state for 3 bit times, nominal, before the EndOfPacket output will go to '1'.

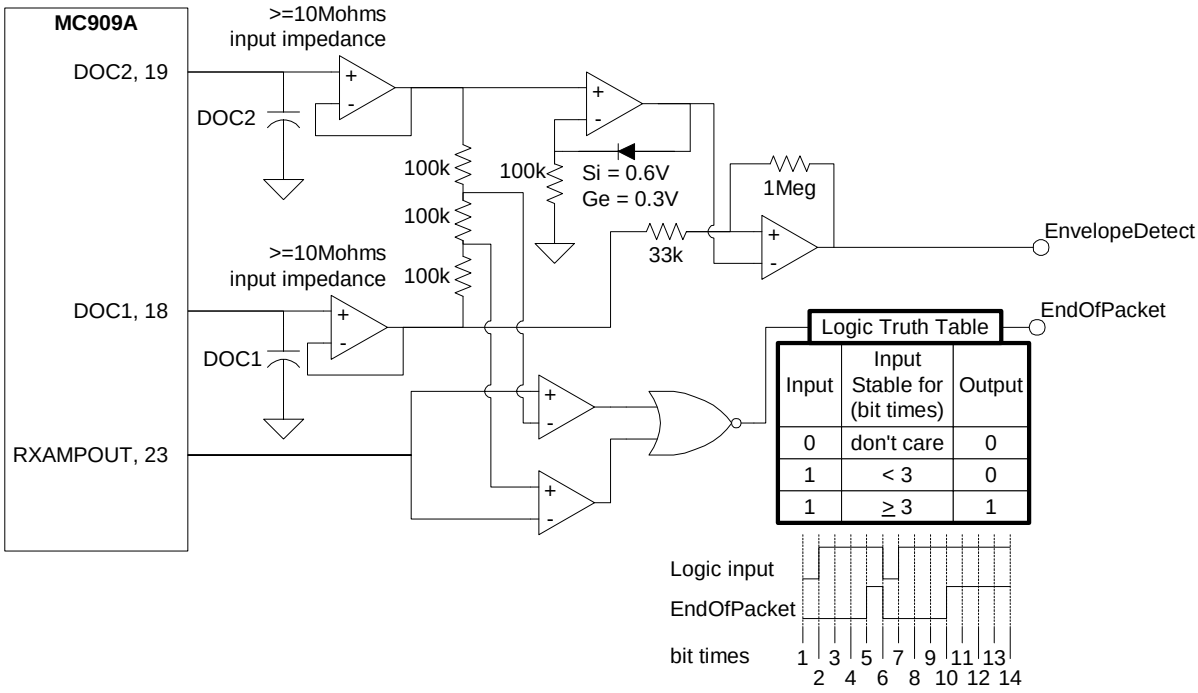


**Figure 1: Envelope and End of Packet Detector Circuit**

During its normal training process, the MX909A dynamically changes the time constant of the DOC1 and DOC2 capacitor voltages. Different time constants are required when these node voltages are used in the described training trigger circuit. Accordingly, the DOC1 and DOC2 time constants must be altered between two values when this training trigger is used; namely, (1) training trigger values and (2) normal MX909A training values. During an idle signal phase (unmodulated carrier), the training trigger time constant values are used to detect the start of carrier modulation using the described circuit. When a training trigger event occurs then the MX909A must be reconfigured with normal training time constants and then issue a training task e.g. SFS (search for frame synch). Note that some delay may need to be inserted between the training trigger event and the time at which the training task is issued.

 

### 3.1 Sequence Actions

Table 1 describes the sequence of actions to be used immediately after reception of a data packet is completed.

| Step | Operating Phase | Action | Purpose |
|---|---|---|---|
| 1 | End of Data packet has just been received so the receiver output will become 'silent.' Configure the MX909A time constants to support the external trigger circuit. | Write the MX909A Control Register settings to configure LEVRES (B3, B2) to Lossy Peak Detect mode. | This will make the DOC1 and DOC2 dynamic response quick, as needed, even after automatic level training occurs. |
| 2 | End of Data packet has just been received so the receiver output will become 'silent.' Configure the MX909A time constants to support the external trigger circuit. | Write a Null task with the AQLEV bit set to 1. | Its execution causes the DOC1 and DOC2 capacitors' differential voltage to be clamped to effectively reset the training trigger circuit. It also configures the MX909A DOC1 and DOC2 voltage time constants to the best values for training trigger circuit operation. |
| 3 | Wait for ENV signal to rise. | Wait for the training trigger signal to rise. | This event indicates MX909A signal acquisition should be started. |
| 4 | Initiate MX909A signal acquisition. | Write the MX909A Control Register settings to configure LEVRES (B3, B2) to Peak Averaging mode. | When a subsequent related task is written to the MX909A this will configure it with time constant values usually appropriate for normal Mobitex system operation. |
| 5 | Initiate MX909A signal acquisition. | Write a Null task to the MX909A with AQLEV and AQBC set | This is the "subsequent related task" mentioned above. Its execution is the first part of the normal MX909A training process described in the Data Sheet. |
| 6 | 11-bit time delay | Start a timer that will indicate when 11bit times have elapsed from the moment the previous task was issued. | Error rate is higher immediately after an AQBC and AQLEV sequence is triggered. These erroneous bits could trigger the frame sync detection circuits. It is suggested that a SFH or SFS task is set ~ 12 bits after setting the AQLEV and AQBC sequence. |
| 7 | Search for Frame Sync | Write a SFH or SFS task to the MX909A | Cause the modem to search the received signal for a 16-bit sequence that matches the frame synchronization pattern. IRQ and BFREE will be set when the frame sync has been found. |
| 8 | Receive Data | Issue a RDB task to the MX909A | Causes the modem to read the next 240 bits as a Mobitex data block. The 18 bytes are placed in the data buffer and an indication is issued for the micro to read the data from the data buffer. |
| 9 | Receive Data | Repeat RDB task N times. | N is the number of data blocks contained in the packet. |
| 10 | Loss of Signal | Continue RDB task<br>Start a timer | If at any time in the middle of a RDB task EOP equals 1, this may be may be an indication of a temporary loss of signal. The controlling device could 'ride out' the EOP signal for up to 17 bit times before aborting |

| Step | Operating Phase | Action | Purpose |
|---|---|---|---|
| 11 | End of Packet | Last block received<br>Write a Null task to MX909A with AQBC set | When the IRQ and BFREE are set from the reception of the Nth block (last data block of packet), there is the possibility of a concatenated packet coming in. The signal levels and DC offset are expected to match that of the previous packet. Only AQBC is issued to make sure that the MX909A acquires proper clock synchronization. |
| 12 | Read data from Buffer | To collect last block's data from buffer | |
| 13 | 11-bit time delay<br>(Same as Step 6) | Start a timer that will indicate when 11bit times have elapsed from the moment the previous task was issued. | Error rate is higher immediately after an AQBC and AQLEV sequence is triggered. These erroneous bits could trigger the frame sync detection circuits. It is suggested that a SFH or SFS task is set ~ 12 bits after setting the AQLEV and AQBC sequence. |
| 14 | Abort | Write a Reset task to command Register | If at any time in steps 4 through 10 EOP equals 1 for longer than 17 bit times, the current task should be aborted and return to step 1 (see Note 1) |
| 15 | End of Data packet has just been received so the receiver output will become ‘silent.’ Configure the MX909A time constants to support the external trigger circuit. (Same as Step 1) | Write the MX909A Control Register settings to configure LEVRES (B3, B2) to Lossy Peak Detect mode. | This will make the DOC1 and DOC2 dynamic response quick, as needed, even after automatic level training occurs. |

**Table 1: Description of Sequence Actions to be used immediately after reception of a data packet is completed**

**Notes**

1. The correct use of the EOP signal depends on what the controller / MX909A are doing at the time. At the end of a frame, use it to enact thorough reacquisition. During a frame, it may be used to indicate possible poor blocks or total loss of signal. If halfway through a frame, the controlling device could 'ride out' the EOP signal for up to 17 bit times, which is (the maximum number of bits in error that can be corrected by the FEC bits) - (EOP delay).

### 3.2 Signal Acquisition

The signal acquisition process is represented on the State Flow Diagram shown in Figure 2.

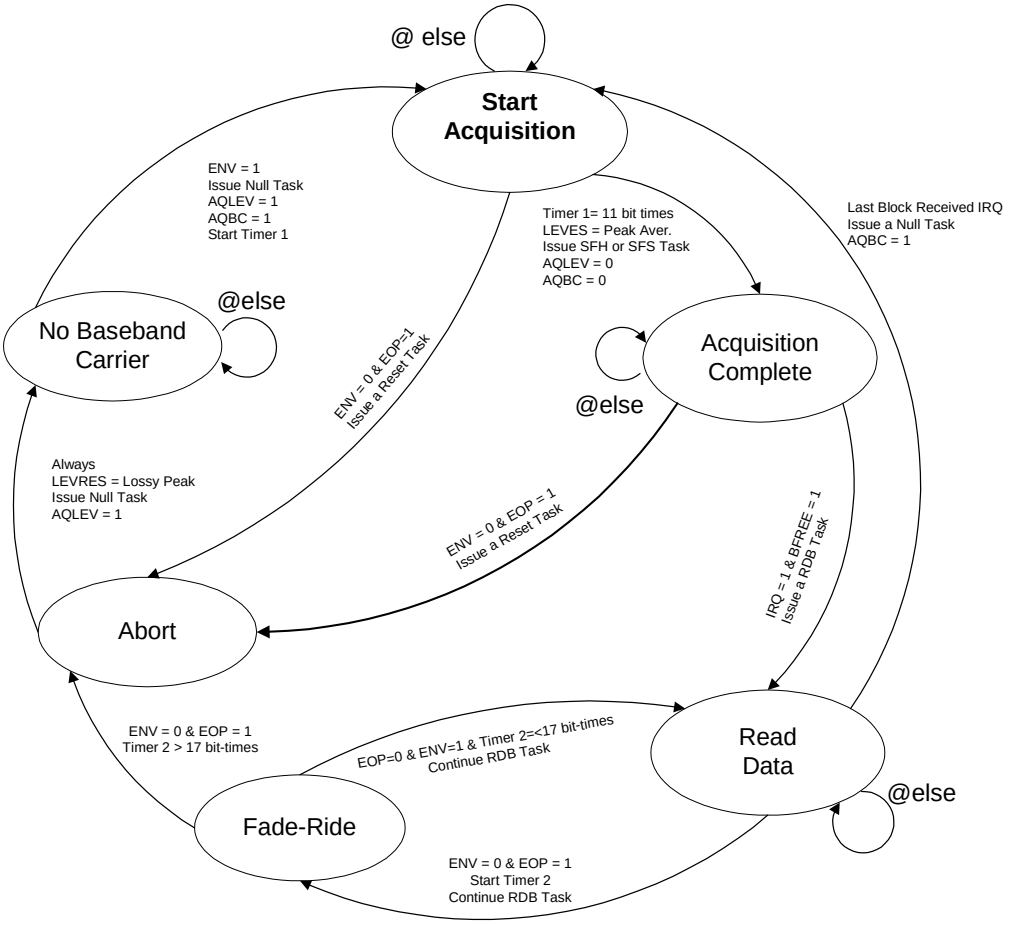


**Figure 2: Signal Acquisition Process State Flow Diagram**

# 4. Conclusion

This document describes the implementation of a simple Envelope and End of Packet Detector external circuit using the voltages produced by the level acquisition and tracking circuits inherent in the MX909A. The circuit observes the DOC1 and DOC2 voltages with a high impedance circuit to determine when the envelope of the received signal exceeds a pre-determined threshold level. This is used to trigger the signal acquisition procedure. The reduction of the incoming signal amplitude below a certain level with respect to the DOC voltages provides an indication of the End of Packet (it may also be caused by a temporary loss of signal). The detection of an End of Packet is also useful to abort an ongoing frame reception process due to the lack of signal. It may also help to clearly de-mark the end of a packet so reliable detection of a new packet can occur.

The outputs of the Envelope and End of Packet Detector Circuit will almost certainly directly drive pins on a microcontroller where they will affect system state transitions. It is possible to integrate some or all of the preceding functions into the microcontroller. The logic and monostable functions can be easily implemented in software. It is also relatively simple to sample DOC1, DOC2, and RXAMPOUT using ADC with multiplexed input, as available in most processors. The entire decision making process can then be implemented using fuzzy decision software saving considerable external hardware.