High Performance Industry Standard Single-Ended Current Mode PWM Controller

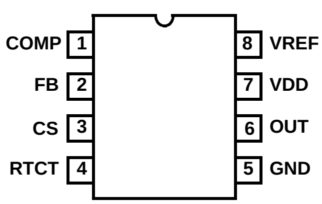
The ISL884xAMBEPZ is a high performance drop-in replacement for the popular 28C4x and 18C4x PWM controllers suitable for a wide range of power conversion applications including boost, flyback, and isolated output configurations. Its fast signal propagation and output switching characteristics make this an ideal product for existing and new designs.

Features include 30V operation, low operating current, 90µA start-up current, adjustable operating frequency to 2MHz, and high peak current drive capability with 20ns rise and fall times.

PART NUMBER	RISING UVLO (V)	MAX. DUTY CYCLE (%)
ISL8840AMBEPZ	7.0	100
ISL8841AMBEPZ	7.0	50
ISL8842AMBEPZ	14.4	100
ISL8843AMBEPZ	8.4	100
ISL8844AMBEPZ	14.4	50
ISL8845AMBEPZ	8.4	50

Pinout

ISL884XAMBEPZ
(8 LD SOIC)
TOP VIEW



Features

- Full Mil-Temp Electrical Performance from -55°C to +125°C
- Controlled Baseline with One Wafer Fabrication Site and One Assembly/Test Site
- Full Homogenous Lot Processing in Wafer Fab
- No Combination of Wafer Fabrication Lots in Assembly
- Full Traceability Through Assembly and Test by Date/Trace Code Assignment
- Enhanced Process Change Notification
- Enhanced Obsolescence Management
- Eliminates Need for Up-Screening a COTS Component
- 1A MOSFET Gate Driver
- 90µA Start-up Current, 125µA Maximum
- 35ns Propagation Delay Current Sense to Output
- Fast Transient Response with Peak Current Mode Control
- 30V Operation
- Adjustable Switching Frequency to 2MHz
- 20ns Rise and Fall Times with 1nF Output Load
- Trimmed Timing Capacitor Discharge Current for Accurate Deadtime/Maximum Duty Cycle Control
- 1.5MHz Bandwidth Error Amplifier
- Tight Tolerance Voltage Reference Over Line, Load and Temperature
- ±3% Current Limit Threshold
- Pb-Free (RoHS compliant)

Applications

- Isolated Flyback and Forward Regulators
- Boost Regulators

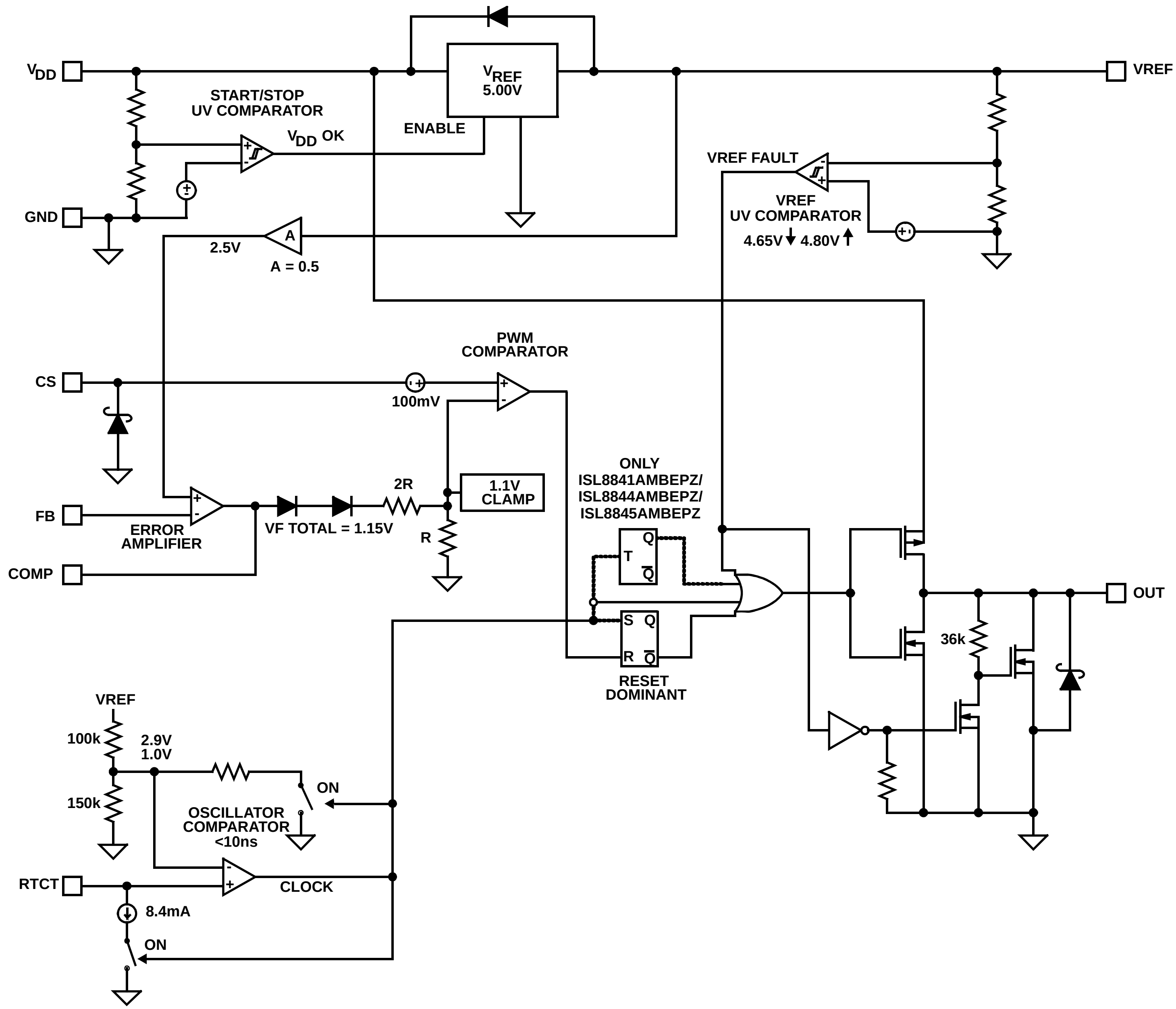
Ordering Information

PART NUMBER (Notes 1, 2)	PART MARKING	TEMP RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL8840AMBEPZ	8840A MBEPZ	-55 to +125	8 Ld SOIC	M8.15
ISL8841AMBEPZ	8841A MBEPZ	-55 to +125	8 Ld SOIC	M8.15
ISL8842AMBEPZ	8842A MBEPZ	-55 to +125	8 Ld SOIC	M8.15
ISL8843AMBEPZ	8843A MBEPZ	-55 to +125	8 Ld SOIC	M8.15
ISL8844AMBEPZ	8844A MBEPZ	-55 to +125	8 Ld SOIC	M8.15
ISL8845AMBEPZ	8845A MBEPZ	-55 to +125	8 Ld SOIC	M8.15

NOTES:

1. Add “-TK” suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Functional Block Diagram



Absolute Maximum Ratings

Supply Voltage, V_{DD} . . . . GND -0.3V to +30V
OUT . . . . GND -0.3V to V_{DD} + 0.3V
Signal Pins . . . . GND -0.3V to 6.0V
Peak GATE Current 1A

Thermal Information

Thermal Resistance (Note 4) θ_{JA} (°C/W)
SOIC Package 100
Maximum Junction Temperature . . . . +150°C
Maximum Storage Temperature Range . . . . -65°C to +150°C
Pb-Free Reflow Profile. . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Operating Conditions

Supply Voltage Range (Note 3) . . . . 9V to 30V
Temperature Range . . . .-55°C to +125°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

3. All voltages are with respect to GND.
4. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Technical Brief TB379 for details.

Electrical Specifications

Recommended operating conditions unless otherwise noted. Refer to “Functional Block Diagram” on page 3. V_{DD} = 15V, R_t = 10kΩ, C_t = 3.3nF, **T_A = -55 to +125°C,** Typical values are at T_A = +25°C. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
UNDERVOLTAGE LOCKOUT					
START Threshold (ISL8840AMBEPZ, ISL8841AMBEPZ)		6.5	7.0	7.5	V
START Threshold (ISL8843AMBEPZ, ISL8845AMBEPZ)		8.0	8.4	9.0	V
START Threshold (ISL8842AMBEPZ, ISL8844AMBEPZ)	(Note 7)	13.3	14.3	15.3	V
STOP Threshold (ISL8840AMBEPZ, ISL8841AMBEPZ)		6.1	6.6	6.9	V
STOP Threshold (ISL8843AMBEPZ, ISL8845AMBEPZ)		7.3	7.6	8.0	V
STOP Threshold (ISL8842AMBEPZ, ISL8844AMBEPZ)		8.0	8.8	9.6	V
Hysteresis (ISL8840AMBEPZ, ISL8841AMBEPZ)		-	0.4	-	V
Hysteresis (ISL8843AMBEPZ, ISL8845AMBEPZ)		-	0.8	-	V
Hysteresis (ISL8842AMBEPZ, ISL8844AMBEPZ)		-	5.4	-	V
Start-up Current, I_{DD}	V_{DD} < START Threshold	-	90	125	µA
Operating Current, I_{DD}	(Note 5)	-	2.9	4.0	mA
Operating Supply Current, I_D	Includes 1nF GATE loading	-	4.75	5.5	mA
REFERENCE VOLTAGE					
Overall Accuracy	Over line (V_{DD} = 12V to 30V), load, temperature	4.900	5.000	5.050	V
Long Term Stability	T_A = +125°C, 1000 hours (Note 6)	-	5	-	mV
Current Limit, Sourcing		-20	-	-	mA
Current Limit, Sinking		5	-	-	mA
CURRENT SENSE					
Input Bias Current	V_{CS} = 1V	-1.0	-	1.0	µA
CS Offset Voltage	V_{CS} = 0V (Note 6)	95	100	105	mV
COMP to PWM Comparator Offset Voltage	V_{CS} = 0V (Note 6)	0.80	1.15	1.30	V
Input Signal, Maximum		0.97	1.00	1.03	V

Electrical Specifications

Recommended operating conditions unless otherwise noted. Refer to “Functional Block Diagram” on page 3. V_{DD} = 15V, R_t = 10kΩ, C_t = 3.3nF, **T_A = -55 to +125°C,** Typical values are at T_A = +25°C. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Gain, $A_{CS} = \Delta V_{COMP}/\Delta V_{CS}$	0 < V_{CS} < 910mV, V_{FB} = 0V	2.5	3.0	3.5	V/V
CS to OUT Delay		-	35	60	ns
ERROR AMPLIFIER					
Open Loop Voltage Gain	(Note 6)	60	90	-	dB
Unity Gain Bandwidth	(Note 6)	1.0	1.5	-	MHz
Reference Voltage	$V_{FB} = V_{COMP}$	2.460	2.500	2.535	V
FB Input Bias Current	V_{FB} = 0V	-1.0	-0.2	1.0	µA
COMP Sink Current	V_{COMP} = 1.5V, V_{FB} = 2.7V	1.0	-	-	mA
COMP Source Current	V_{COMP} = 1.5V, V_{FB} = 2.3V	-0.4	-	-	mA
COMP VOH	V_{FB} = 2.3V	4.80	-	VREF	V
COMP VOL	V_{FB} = 2.7V	0.4	-	1.0	V
PSRR	Frequency = 120Hz, V_{DD} = 12V to 30V (Note 6)	60	80	-	dB
OSCILLATOR					
Frequency Accuracy	Initial, T_A = +25°C	48	51	53	kHz
Frequency Variation with V_{DD}	T_A = +25°C, $(f_{30V} - f_{10V})/f_{30V}$	-	0.2	1.0	%
Temperature Stability	(Note 6)	-	-	5	%
Amplitude, Peak-to-Peak	Static Test	-	1.75	-	V
RTCT Discharge Voltage (Valley Voltage)	Static Test	-	1.0	-	V
Discharge Current	RTCT = 2.0V	6.2	8.0	8.5	mA
OUTPUT					
Gate VOH	V_{DD} - OUT, I_{OUT} = -200mA	-	1.0	2.0	V
Gate VOL	OUT - GND, I_{OUT} = 200mA	-	1.0	2.0	V
Peak Output Current	C_{OUT} = 1nF (Note 6)	-	1.0	-	A
Rise Time	C_{OUT} = 1nF (Note 6)	-	20	40	ns
Fall Time	C_{OUT} = 1nF (Note 6)	-	20	40	ns
GATE VOL UVLO Clamp Voltage	V_{DD} = 5V, I_{LOAD} = 1mA	-	-	1.2	V
PWM					
Maximum Duty Cycle (ISL8840AMBEPZ, ISL8842AMBEPZ, ISL8843AMBEPZ)	COMP = VREF	94.0	96.0	-	%
Maximum Duty Cycle (ISL8841AMBEPZ, ISL8844AMBEPZ, ISL8845AMBEPZ)	COMP = VREF	47.0	48.0	-	%
Minimum Duty Cycle	COMP = GND	-	-	0	%

NOTES:

5. This is the V_{DD} current consumed when the device is active but not switching. Does not include gate drive current.
6. Limits established by characterization and are not production tested.
7. Adjust V_{DD} above the start threshold and then lower to 15V.

Typical Performance Curves

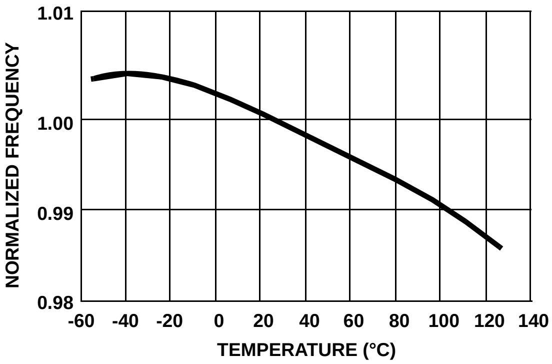


FIGURE 1. FREQUENCY vs TEMPERATURE

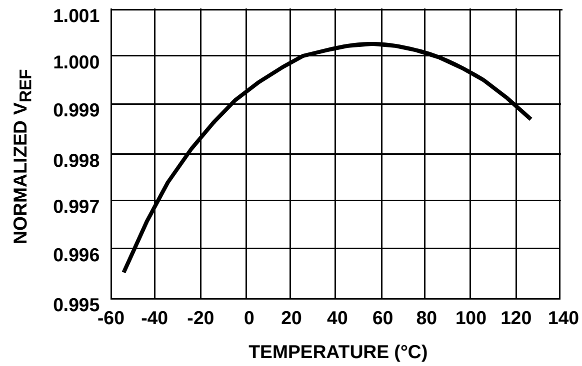


FIGURE 2. REFERENCE VOLTAGE vs TEMPERATURE

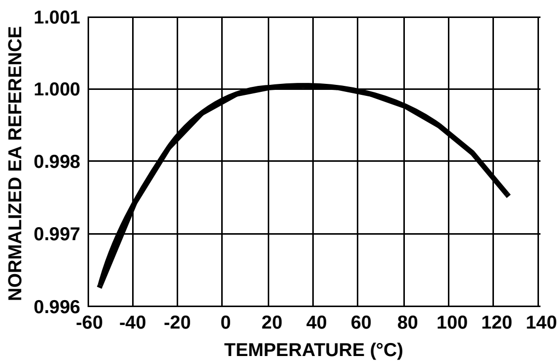


FIGURE 3. EA REFERENCE vs TEMPERATURE

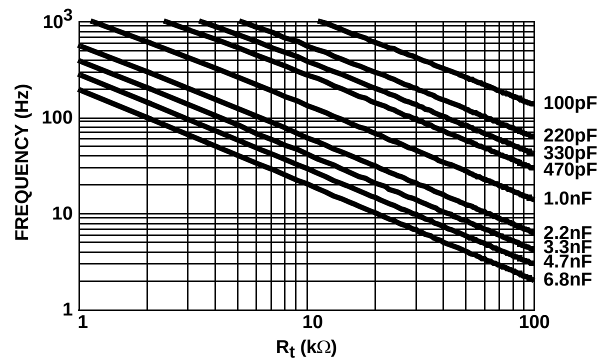


FIGURE 4. RESISTANCE FOR CT CAPACITOR VALUES GIVEN

Pin Descriptions

RTCT - This is the oscillator timing control pin. The operational frequency and maximum duty cycle are set by connecting a resistor, R_t, between V_{REF} and this pin and a timing capacitor, C_t, from this pin to GND. The oscillator produces a sawtooth waveform with a programmable frequency range up to 2.0MHz. The charge time, t_C, the discharge time, t_D, the switching frequency, f, and the maximum duty cycle, D_{MAX}, can be approximated from the following equations:

$$t_C \approx 0.533 \cdot R_t \cdot C_t \quad \text{(EQ. 1)}$$

$$t_D \approx -R_t \cdot C_t \cdot \ln\left(\frac{0.008 \cdot R_t - 3.83}{0.008 \cdot R_t - 1.71}\right) \quad \text{(EQ. 2)}$$

$$f = 1/(t_C + t_D) \quad \text{(EQ. 3)}$$

$$D = t_C \cdot f \quad \text{(EQ. 4)}$$

The formulae have increased error at higher frequencies due to propagation delays. Figure 4 may be used as a guideline in selecting the capacitor and resistor values required for a given frequency.

COMP - COMP is the output of the error amplifier and the input of the PWM comparator. The control loop frequency compensation network is connected between the COMP and FB pins.

FB - The output voltage feedback is connected to the inverting input of the error amplifier through this pin. The non-inverting input of the error amplifier is internally tied to a reference voltage.

CS - This is the current sense input to the PWM comparator. The range of the input signal is nominally 0V to 1.0V and has an internal offset of 100mV.

GND - GND is the power and small signal reference ground for all functions.

OUT - This is the drive output to the power switching device. It is a high current output capable of driving the gate of a power MOSFET with peak currents of 1.0A. This GATE output is actively held low when V_{DD} is below the UVLO threshold.

V_{DD} - V_{DD} is the power connection for the device. The total supply current will depend on the load applied to OUT. Total I_{DD} current is the sum of the operating current and the average output current. Knowing the operating frequency, f, and the MOSFET gate charge, Qg, the average output current can be calculated from Equation 5:

$$I_{OUT} = Qg \times f \quad \text{(EQ. 5)}$$

To optimize noise immunity, bypass V_{DD} to GND with a ceramic capacitor as close to the V_{DD} and GND pins as possible.

VREF - The 5.00V reference voltage output. +1.0/-1.5% tolerance over line, load and operating temperature. Bypass to GND with a 0.1µF to 3.3µF capacitor to filter this output as needed.

Functional Description

Features

The ISL884xAMBEPZ current mode PWM makes an ideal choice for low-cost flyback and forward topology applications. With its greatly improved performance over industry standard parts, it is the obvious choice for new designs or existing designs which require updating.

Oscillator

The ISL884xAMBEPZ has a sawtooth oscillator with a programmable frequency range to 2MHz, which can be programmed with a resistor from V_{REF} and a capacitor to GND on the RTCT pin. (Please refer to Figure 4 for the resistor and capacitance required for a given frequency.)

Soft-Start Operation

Soft-start must be implemented externally. One method, illustrated in Figure 5, clamps the voltage on COMP.

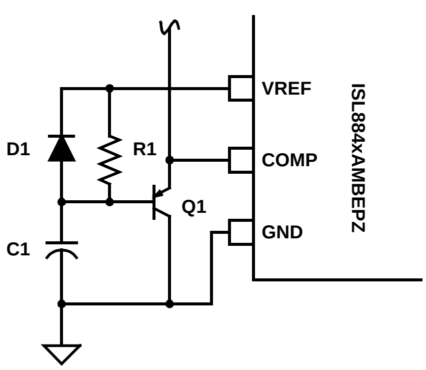


FIGURE 5. SOFT-START

The COMP pin is clamped to the voltage on capacitor C_1 plus a base-emitter junction by transistor Q_1. C_1 is charged from VREF through resistor R_1 and the base current of Q1. At power-up C_1 is fully discharged, COMP is at ~0.7V, and the duty cycle is zero. As C_1 charges, the voltage on COMP increases, and the duty cycle increases in proportion to the voltage on C_1. When COMP reaches the steady state operating point, the control loop takes over and soft-start is complete. C_1 continues to charge up to V_{REF} and no longer affects COMP. During power-down, diode D_1 quickly discharges C_1 so that the soft-start circuit is properly initialized prior to the next power-on sequence.

Gate Drive

The ISL884xAMBEPZ is capable of sourcing and sinking 1A peak current. To limit the peak current through the IC, an optional external resistor may be placed between the totem-pole output of the IC (OUT pin) and the gate of the MOSFET. This small series resistor also damps any oscillations caused by the resonant tank of the parasitic inductances in the traces of the board and the FET's input capacitance.

Slope Compensation

For applications where the maximum duty cycle is less than 50%, slope compensation may be used to improve noise immunity, particularly at lighter loads. The amount of slope compensation required for noise immunity is determined empirically, but is generally about 10% of the full scale current feedback signal. For applications where the duty cycle is greater than 50%, slope compensation is required to prevent instability.

Slope compensation may be accomplished by summing an external ramp with the current feedback signal or by subtracting the external ramp from the voltage feedback error signal. Adding the external ramp to the current feedback signal is the more popular method.

From the small signal current-mode model [1] it can be shown that the naturally-sampled modulator gain, Fm, without slope compensation, is in Equation 6.

$$Fm = \frac{1}{S_n t_{SW}} \quad \text{(EQ. 6)}$$

where S_n is the slope of the sawtooth signal and t_{sw} is the duration of the half-cycle. When an external ramp is added, the modulator gain becomes Equation 7:

$$Fm = \frac{1}{(S_n + S_e)t_{SW}} = \frac{1}{m_c S_n t_{SW}} \quad \text{(EQ. 7)}$$

where S_e is slope of the external ramp and

$$m_c = 1 + \frac{S_e}{S_n} \quad \text{(EQ. 8)}$$

The criteria for determining the correct amount of external ramp can be determined by appropriately setting the damping factor of the double-pole located at the switching frequency. The double-pole will be critically damped if the Q-factor is set to 1, over-damped for Q < 1, and under-damped for Q > 1. An under-damped condition may result in current loop instability.

$$Q = \frac{1}{\pi(m_c(1 - D) - 0.5)} \quad \text{(EQ. 9)}$$

where D is the percent of on-time during a switching cycle. Setting Q = 1 and solving for S_e yields Equation 10:

$$S_e = S_n\left(\left(\frac{1}{\pi}+0.5\right)\frac{1}{1-D}-1\right) \quad \text{(EQ. 10)}$$

Since S_n and S_e are the on time slopes of the current ramp and the external ramp, respectively, they can be multiplied by t_{ON} to obtain the voltage change that occurs during t_{ON}.

$$V_e = V_n\left(\left(\frac{1}{\pi}+0.5\right)\frac{1}{1-D}-1\right) \quad \text{(EQ. 11)}$$

where V_n is the change in the current feedback signal (ΔI) during the on-time and V_e is the voltage that must be added by the external ramp.

For a flyback converter, V_n can be solved for in terms of input voltage, current transducer components, and primary inductance, yielding

$$V_e = \frac{D \cdot t_{SW} \cdot V_{IN} \cdot R_{CS}}{L_p}\left(\left(\frac{1}{\pi}+0.5\right)\frac{1}{1-D}-1\right) \quad V \quad \text{(EQ. 12)}$$

where R_{CS} is the current sense resistor, f_{SW} is the switching frequency, L_p is the primary inductance, V_{IN} is the minimum input voltage, and D is the maximum duty cycle.

The current sense signal at the end of the on-time for CCM operation is:

$$V_{CS} = \frac{N_S \cdot R_{CS}}{N_P}\left(I_O + \frac{(1-D) \cdot V_O \cdot f_{SW}}{2L_s}\right) \quad V \quad \text{(EQ. 13)}$$

where V_{CS} is the voltage across the current sense resistor, L_s is the secondary winding inductance, and I_O is the output current at current limit. Equation 13 assumes the voltage drop across the output rectifier is negligible.

Since the peak current limit threshold is 1.00V, the total current feedback signal plus the external ramp voltage must sum to this value when the output load is at the current limit threshold.

$$V_e + V_{CS} = 1 \quad \text{(EQ. 14)}$$

Substituting Equations 12 and 13 into Equation 14 and solving for R_{CS} yields Equation 15:

$$R_{CS} = \frac{1}{\frac{D \cdot f_{sw} \cdot V_{IN}}{L_p} \cdot \left(\frac{\frac{1}{\pi}+0.5}{1-D}-1\right) + \frac{N_s}{N_p} \cdot \left(I_O + \frac{(1-D) \cdot V_O \cdot f_{sw}}{2L_s}\right)} \quad \text{(EQ. 15)}$$

Adding slope compensation is accomplished in the ISL884xAMBEPZ using an external buffer transistor and the R_tC_t signal. A typical application sums the buffered R_tC_t signal with the current sense feedback and applies the result to the CS pin, as shown in Figure 6.

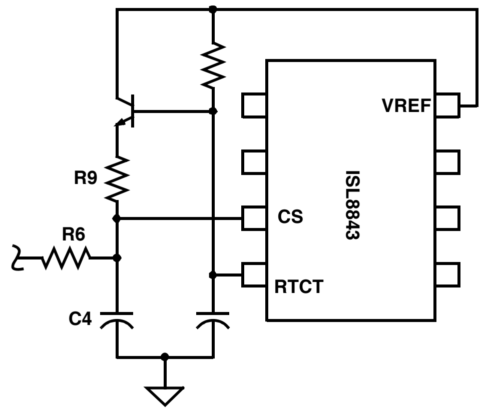


FIGURE 6. SLOPE COMPENSATION

Assuming the designer has selected values for the RC filter (R_6 and C_4) placed on the CS pin, the value of R_9 required to add the appropriate external ramp can be found by superposition.

$$V_e = \frac{2.05 D \cdot R_6}{R_6 + R_9} \quad V \quad \text{(EQ. 16)}$$

The factor of 2.05 in Equation 16 arises from the peak amplitude of the sawtooth waveform on R_tC_t minus a base-emitter junction drop. That voltage multiplied by the maximum duty cycle is the voltage source for the slope compensation. Rearranging to solve for R_9 yields:

$$R_9 = \frac{(2.05D - V_e) \cdot R_6}{V_e} \quad \Omega \quad \text{(EQ. 17)}$$

The value of R_{CS} determined in Equation 15 must be rescaled so that the current sense signal presented at the CS pin is that predicted by Equation 13. The divider created by R_6 and R_9 makes this necessary.

$$R'_{CS} = \frac{R_6 + R_9}{R_9} \cdot R_{CS} \quad \text{(EQ. 18)}$$

Example:

V_{IN} = 12V

V_O = 48V

L_S = 800µH

Ns/Np = 10

L_p = 8.0µH

I_O = 200mA

Switching Frequency, f_{SW} = 200kHz

Duty Cycle, D = 28.6%

$R_6 = 499\Omega$

Solve for the current sense resistor, R_{CS}, using Equation 15.

$R_{CS} = 295m\Omega$

Determine the amount of voltage, V_e, that must be added to the current feedback signal using Equation 12.

$V_e = 92.4mV$

Using Equation 17, solve for the summing resistor, R_9, from CT to CS.

$R_9 = 2.67k\Omega$

Determine the new value of R_{CS} (R'_{CS}) using Equation 18.

$R'_{CS} = 350m\Omega$

Additional slope compensation may be considered for design margin. The previous discussion determines the minimum external ramp that is required. The buffer transistor used to create the external ramp from R_tC_t should have a sufficiently high gain (>200) so as to minimize the required base current. Whatever base current is required reduces the charging current into R_tC_t and will reduce the oscillator frequency.

Fault Conditions

A Fault condition occurs if V_{REF} falls below 4.65V. When a Fault is detected, OUT is disabled. When V_{REF} exceeds 4.80V, the Fault condition clears, and OUT is enabled.

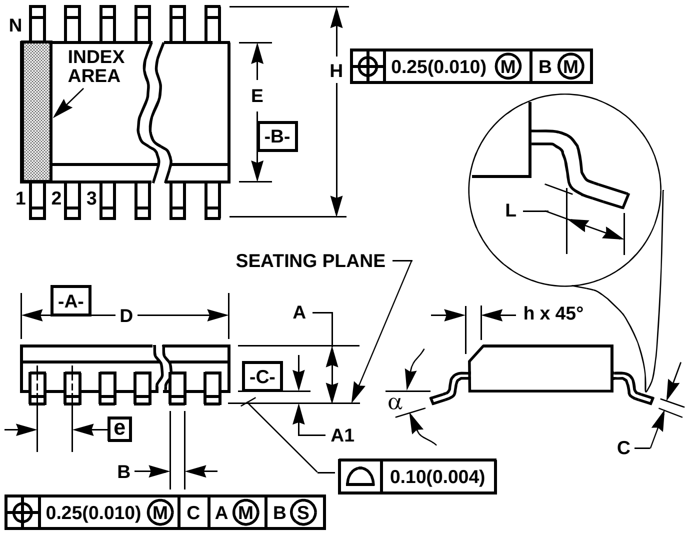
Ground Plane Requirements

Careful layout is essential for satisfactory operation of the device. A good ground plane must be employed. A unique section of the ground plane must be designated for high di/dt currents associated with the output stage. V_{DD} should be bypassed directly to GND with good high frequency capacitors.

References

[1] Ridley, R., “A New Continuous-Time Model for Current Mode Control”, IEEE Transactions on Power Electronics, Vol. 6, No. 2, April 1991.

Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M8.15 **(JEDEC MS-012-AA ISSUE C)**
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.1890	0.1968	4.80	5.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	8		8		7
α	0°	8°	0°	8°	-

Rev. 1 6/05

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Intersil Corporation's quality certifications can be viewed at www.intersil.com/design/quality

For information regarding Intersil Corporation and its products, see www.intersil.com