LXD974A Demo Board for 10/100 Applications

Development Kit Manual

January 2001

As of January 15, 2001, this document replaces the Level One document *LXD974A Demo Board for 10/100 Applications*.

Order Number: 249104-001

Contents

Figures

Tables

1.0 General Description

The LXD974A Demo Board is a four-port 10/100 Mbps Ethernet Media Access Unit (MAU) that demonstrates all of the standard MII features of the LXT974A Fast Ethernet Quad Transceiver. The LXD974A is designed to maximize return loss and EMI performance.

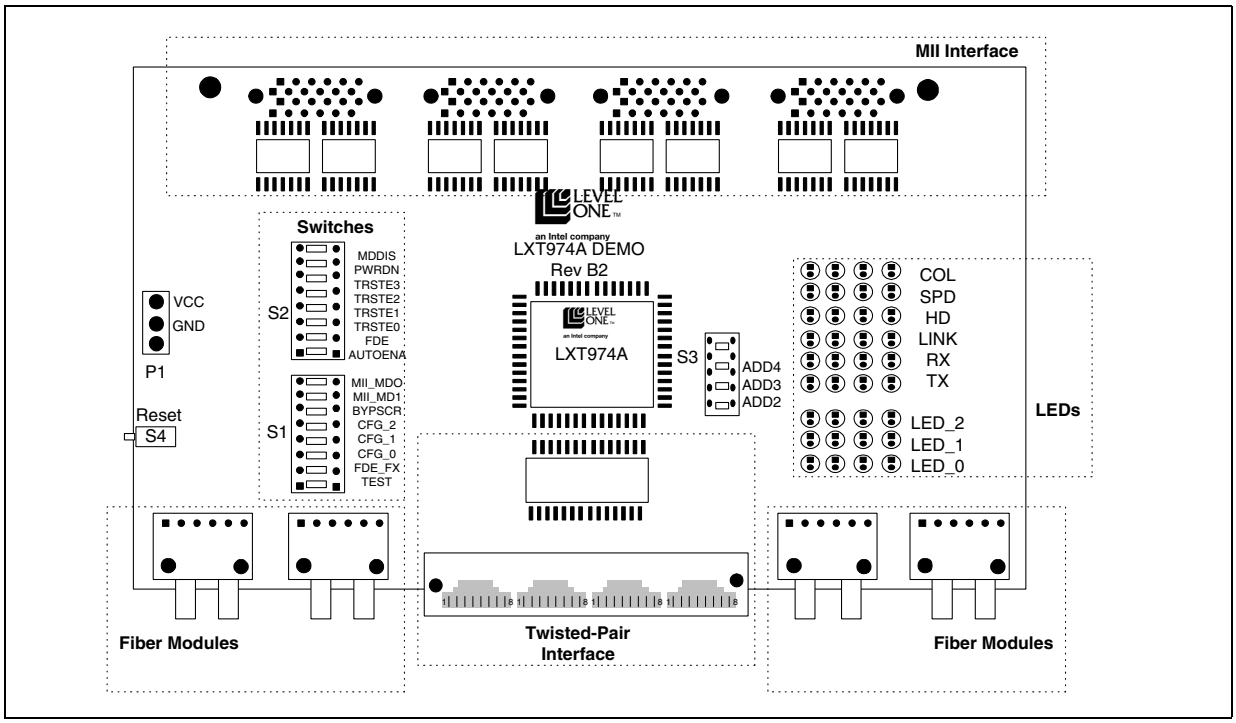
The LXD974A provides a working platform for evaluation of the LXT974A Fast Ethernet 10/100 Quad Transceiver in 10BASE-T and/or 100BASE-TX/FX applications. A pseudo-ECL (PECL) interface is provided on all four ports for fiber operation.

The LXD974A Demo Board allows system designers to test 10 Mbps and 100 Mbps link performance, auto-negotiation, and register functionality prior to board prototyping. Refer to the latest LXT974A/975A Quad Fast Ethernet Transceiver data sheet for device functionality and specifications.

1.1 Features

- Four independent IEEE 802.3-compliant 10BASE-T or 100BASE-TX ports.
- Quick setup, ease of use, and clear visibility of application settings for:
  - EMI compliant reference designs.
  - Complete system demonstration.
  - Individual circuit isolation.
- Auto-negotiation protocol compliant with legacy systems that do not support auto-negotiation.
- LED indicators for major functions.
- Configurable through MII serial port or via external control pins.
- Standard half-duplex or full-duplex operation at 10 or 100 Mbps.
- 100BASE-FX fiber-optic capable.

Figure 1. LXD974A Demo Board



2.0 Setup Procedures

This document describes typical Demo Board set-up procedures for a 10BASE-T, 100BASE-TX, or 100BASE-FX environment and provides basic hardware set-up information, Bill of Materials, and board schematics. Gerber files for board layout are available by contacting your local sales office (see the back page for listings).

The LXD974A Demo Board is populated with all of the IC components needed for twisted-pair evaluation. However, the following additional equipment is also required:

- SmartBits Advanced Multi-port Performance Test Box configured with firmware version 4.39 or newer.
- PC with Smart Windows (version 6.0 or newer) installed.
- 5V DC Power Supply.
- Four MII Cables.
- Four external NIC cards.
- Four Category 5 Unshielded Twisted-Pair (UTP) cables.
- Fiber-optic transceiver modules (HFBR-5103), fiber-optic cable, and external jumpers are required for 100BASE-FX evaluation.

2.1 Hardware Setup

2.1.1 Twisted-Pair

The following set-up procedure is recommended for standard twisted-pair evaluation.

1. Set the jumpers as shown in Table 2.
2. Set switch S1, S2, and S3 according to Table 4 through Table 6.
3. Connect a +5V DC power supply to P1 VCC. Connect ground to P1 GND.
4. Connect all four ports of the LXD974A to the SmartBits test box via MII connector/cables.
5. Connect the twisted-pair ports to external NIC cards via UTP cables. Each NIC card plugs directly into the SmartBits test box.
6. With the demo board appropriately configured, apply power to the LXD974A and press Reset switch S4.
7. Proceed with evaluation as desired.

2.1.2 Fiber Modules

There are four combination twisted-pair/fiber ports provided on the LXT974A. For 100BASE-FX evaluation, fiber-optic transceiver module (HFBR-5103) and four external blue-wire connections are required per port.

- Remove twisted-pair transformer.
- Solder fiber modules on board.

- Cut the required circuit traces and make the external blue-wire connections as shown in Table 1.
- Set the fiber module jumpers as shown in Table 3 on page 11.

2.1.2.1 External Blue-Wire Connections

Seventeen cuts and sixteen external blue-wire connections are required to set up the combination ports for fiber operation. Cut circuit traces as required to remove T1, R38, R39, R40, R41, R59, R60, R61, R62, R100, R101, R102, R103, R121, R122, R123, and R124.

Make the external blue-wire connections using 24 AWG solid wire from the LXD974A test points to the T1 transformer pads as shown in Table 1. TP236 - TP239 represent port 0, TP240 - TP243 represent port 1, TP244 - TP247 represent port 2, and TP248 - TP251 represent port 3. Refer to Figure 6 on page 21 (port 0), to Figure 7 on page 22 (port 1), to Figure 9 on page 24 (port 2), and to Figure 10 on page 25 (port 3) for schematics of the external blue-wire circuitry.

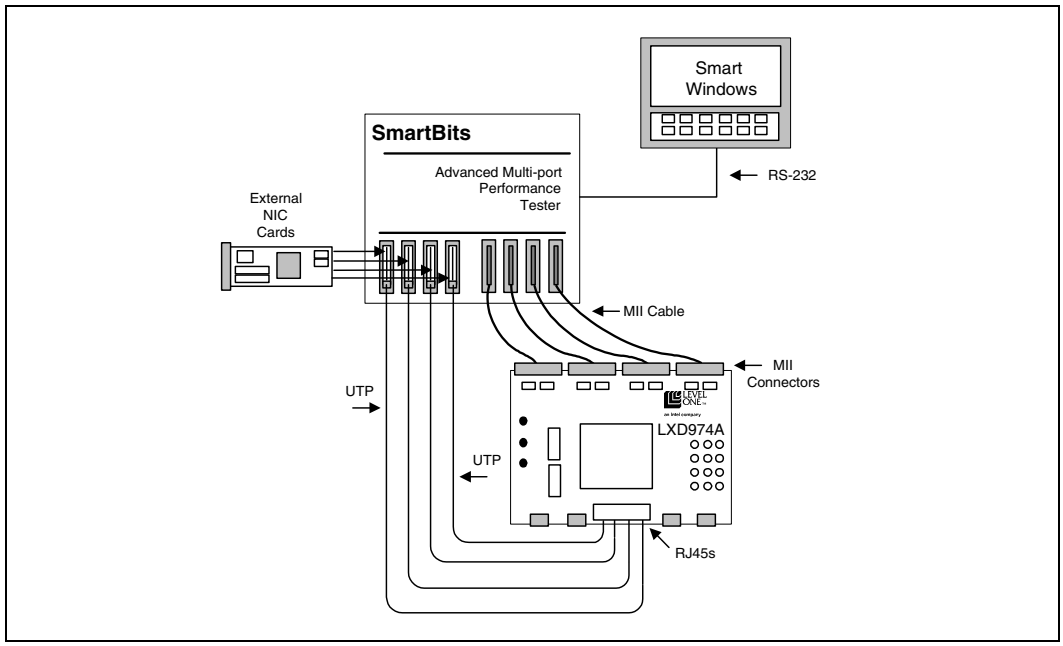
Table 1. External Blue-Wire Connections for Fiber Module Operation

LXD974A Test Points	T1 Pads
TP236	1
TP237	3
TP238	4
TP239	5
TP240	6
TP241	8
TP242	9
TP243	10
TP244	11
TP245	13
TP246	14
TP247	15
TP248	16
TP249	18
TP250	19
TP251	20

2.2 Test Setup

Figure 2 shows a typical test setup for standard operation of the LXD974A. The LXD974A plugs into a SmartBits Advanced Multi-port Performance Test Box via four standard 40-pin MII connectors, that are included on the board. The MII cables are not included. Four external NIC cards directly connect to the SmartBits test box and plug into the LXD974A through RJ45 connections. Each port's operating speed can be set individually for evaluation of 10 Mbps, 100 Mbps, and auto-negotiation capabilities using all four ports.

Figure 2. Basic Test Setup



3.0 Jumpers

3.1 Twisted-Pair Evaluation

JP50 and JP51 must be jumpered on the LXD974A for the SmartBits test box to access the MII management registers inside the LXT974A. MII registers can be accessed for each port by setting bits ADD<1:0> of the PHY address with the port number. Refer to the *LXT974A/975A Data Sheet* for specific register definitions and functions.

For standard 10BASE-T/100BASE-TX operation, leave all other jumpers open, as shown in Table 2.

Table 2. LXD974A Jumper Settings for Twisted-Pair Operation

Port	Jumper	Description	Jumper Setting
0	JP50	**MDC.** Management Data Clock . Clock for the MDIO serial channel. Maximum frequency is 2.5 MHz.	Jumpered
	JP51	**MDIO.** Management Data I/O. Bidirectional serial data channel for PHY/STA communication.	Jumpered
	JP1	**MII VCC.** Power Supply.	Open
1	JP52	**MDC.** Management Data Clock. Clock for the MDIO serial channel. Maximum frequency is 2.5 MHz.	Open
	JP53	**MDIO.** Management Data I/O. Bidirectional serial data channel for PHY/STA communication.	Open
	JP2	**MII VCC.** Power Supply.	Open
	JP8	**SD Pullup.** Signal Detect, connects an 82Ω resistor to signal detect pin.	Open
	JP69	**SD CONNECT.** Selects TP or FX Mode.	Open
2	JP54	**MDC.** Management Data Clock. Clock for the MDIO serial channel. Maximum frequency is 2.5 MHz.	Open
	JP55	**MDIO.** Management Data I/O. Bidirectional serial data channel for PHY/STA communication.	Open
	JP13	**MII VCC.** Power Supply.	Open

Table 2. LXD974A Jumper Settings for Twisted-Pair Operation

Port	Jumper	Description	Jumper Setting
3	JP56	**MDC.** Management Data Clock. Clock for the MDIO serial channel. Maximum frequency is 2.5 MHz.	Open
	JP57	**MDIO.** Management Data I/O. Bidirectional serial data channel for PHY/STA communication.	Open
	JP14	**MII VCC.** Power Supply.	Open
	JP20	**SD Pullup.** Signal Detect, connects an 82Ω resistor to signal detect pin.	Open
	JP71	**SD CONNECT.** Selects TP or FX Mode.	Open

3.2 Fiber Evaluation

For 100BASE-FX evaluation, install the fiber module jumpers as shown in Table 3.

Table 3. LXD974A Jumper Settings for Fiber Module Operation

Port	Jumper	Description	Jumper Setting
1	JP8	**SD Pullup.** Signal Detect, connects an 82Ω resistor to signal detect pin.	Jumpered
	JP69	**SD CONNECT.** Selects TP or FX Mode.	Jumpered
3	JP20	**SD Pullup.** Signal Detect, connects an 82Ω resistor to signal detect pin.	Jumpered
	JP71	**SD CONNECT.** Selects TP or FX Mode.	Jumpered

4.0 Switches

4.1 Operating Characteristics

Three switches configure operating characteristics of the LXD974A. Each switch can be set manually by toggling the switch either to 1 or 0.

Table 4 through Table 6 show the description and recommended setting for each switch. For standard operation, set switch S1, S2, and S3 according to these tables.

Table 4. S1 Switch Settings

Switch	Signal	Recommended Setting	Description
1	Test	0	Test - Test Mode, for internal use only.
2	FDE_FX	0	Full-Duplex Enable (FX Ports) - Selects full-duplex in FX Mode. 1 = Enables half-duplex operation on all ports set for FX Mode. 0 = Enables full-duplex operation on all ports set for FX Mode.
3	CFG_0	0	Configuration Control 0 - Selects operating speed. 1 = 100 Mbps. 0 = 10 Mbps.
4	CFG_1	0	Configuration Control 1 - Enables 10Mbps link test. 1 = 10 Mbps link Test Disabled. 0 = 10 Mbps Link Test Enabled.
5	CFG_2	0	Configuration Control 2 - Selects either TP or FX interface. 1 = FX operation. 0 = TP Operation.
6	BYPSCR	0	Bypass Scrambler - Enables Scrambler operation. 1 = Scrambler Bypassed. 0 = Scrambler Enabled.
7	MII_MD1	0	MII Mode Select - Selects operating mode of MII. 1 = Selects 5B Symbol Mode. 0 = Standard 4B Operating Mode.
8	MII_MD0	0	MII Mode Select - Selects operating mode of MII. 1 = Selects 5B Symbol Mode. 0 = Standard 4B Operating Mode.

Table 5. S2 Switch Settings

Switch	Signal	Recommended Setting	Description
1	AUTOENA	1	Auto-Negotiation Enable - Enables Auto-Negotiation. 1 = Enable Auto-Negotiation. 0 = Disable Auto-Negotiation.
2	FDE	0	Full Duplex Enable (All Ports) - Enables Full Duplex operation. 1 = Full-Duplex operation on all ports. 0 = Half-Duplex operation on all ports.
3	TRSTE0	0	Tristate Port 0 - Enables Tristate on Port 0. 1 = Force Tristate to isolate port. 0 = Normal operation.
4	TRSTE1	0	Tristate Port 1 - Enables Tristate on Port 1. 1 = Force Tristate to isolate port. 0 = Normal operation.
5	TRSTE2	0	Tristate Port 2 - Enables Tristate on Port 2. 1 = Force Tristate to isolate port. 0 = Normal operation.
6	TRSTE3	0	Tristate Port 3 - Enables Tristate on Port 3. 1 = Force Tristate to isolate port. 0 = Normal operation.
7	PWRDN	0	Power Down - Enables Power Down Mode. 1 = Forces Power Down Mode. 0 = Normal Operation.
8	MDDIS	0	Management Disable - Management control of the LXT974A. 1 = The Hardware Control Interface provides continual control of register bits. 0 = The Hardware Control Interface provides only initial default values of register bits.

Table 6. S3 Switch Settings

Switch	Signal	Setting	Description
1	ADD2	0	Address <4:2> - Sets upper three bits of PHY address.
2	ADD3	0	
3	ADD4	0	
4	N/C	-	N/C

4.2 Advertisement Configurations

When Auto-Negotiation is enabled, CFG_1, CFG_2, and FDE are used to configure advertising characteristics of LXD974A. Table 7 shows how to set the various configurations.

Table 7. Advertised Configurations when Auto-Negotiation Enabled

Desired Configuration	CFG_2	CFG_1	FDE
Advertise All	0	0	Ignore
Advertise 100 HD	1	0	0
Advertise 100 HD/FD	1	0	1
Advertise 10 HD	0	1	0
Advertise 10 HD/FD	0	1	1
Advertise 10/100 HD	1	1	0

5.0 LED Indicators

There are 38 status LEDs on the Demo Board. The LXT974A provides six serial LED outputs and three programmable LEDs per port. LED indicators and descriptions are listed in Table 8 and Table 9.

Note: Programmable LEDs (LED_0, LED_1, LED_2) are set in default mode and may be programmed to indicate optional conditions. Refer to LXT974A data sheet for LED programming options.

Table 8. Global LED Descriptions

Label	Ref Des	Description
MDINT	D1	**Management Data Interrupt.** Indicates status change to LXT974A.
PWR	D77	**Power.** Indicates power to LXD974A Demo Board.

Table 9. Port LED Descriptions

Label	Reference Designators				Description
	Port 0	Port 1	Port 2	Port 3	
COL	D21	D15	D9	D3	**Collision.** Indicates collision on the respective port.
SPD	D22	D16	D10	D4	**Speed.** Indicates 100 Mbps operation.
HD	D23	D17	D11	D5	**Duplex.** Indicates half-duplex on the respective port.
LINK	D24	D18	D12	D6	**Link.** Indicates connection on the respective port.
RX	D25	D19	D13	D7	**Receive.** Indicates received data on the respective port.
TX	D26	D20	D14	D8	**Transmit.** Indicates transmitted data on the respective port.
LED_0	D27	D32	D35	D38	**LED0.** Indicates transmitter is active.
LED_1	D28	D31	D34	D37	**LED1.** Indicates receiver is active.
LED_2	D27	D30	D33	D36	**LED2.** Indicates link is up.

6.0 Bill of Materials and Board Schematics

Table 10. LXT974A Bill of Materials

Item	Qty	Reference Designator	Description
1	1	C1	100 uF Tantalum
2	1	C2	1.0 uF Tantalum
3	1	C3	22 uF Tantalum
4	56	C4, C5, C10, C11, C12, C13, C14, C15, C16, C17, C41, C42, C43, C44, C45, C46, C47, C48, C49, C50, C51, C52, C53, C54, C69, C70, C72, C73, C74, C75, C76, C80, C102, C103, C105, C106, C107, C108, C109, C210, C211, C212, C213	0.1 uF
5	19	C78, C79, C89, C90, C100, C101, C111, C112, C159, C160, C161, C162, C163, C164, C165, C166, C167, C168, C169	.001 uF
6	4	C71, C82, C93, C104	10 uF
7	1	C208	.01 uF
8	1	C209	10 uF
9	2	C214, C215	47 uF
10	14	D1, D3, D8, D9, D14, D15, D20, D21, D26, D29, D32, D35, D38, D77	LED Red
11	1	D2	Diode
12	16	D4, D5, D7, D10, D11, D13, D16, D17, D19, D22, D23, D25, D28, D31, D34, D37	LED Yellow
13	8	D6, D12, D18, D24, D27, D30, D33, D36	LED Green
14	2	FB2, FB1	Ferrite Bead
15	4	FM1, FM2, FM3, FM4	HP Fiber Module
16	20	JP1, JP2, JP3, JP8, JP13, JP14, JP15, JP20, JP50, JP51, JP52, JP53, JP54, JP55, JP56, JP57, JP68, JP69, JP70, JP71	Jumpers
17	1	J1	Connector RJ45
18	1	J3	Con2
19	4	L3, L8, L11, L15	320 nH
20	8	L1, L2, L5, L6, L10, L13, L14	1 uH
21	1	P1	Termblk
22	4	P4, P5, P6, P7	MII 40-pin Connector
23	2	R1, R261	330
24	1	R2	22.1 kΩ 1%
25	77	R3, R4, R7, R8, R9, R10, R11, R12, R13, R14, R15, R16, R17, R18, R19, R20, R21, R22, R23, R24, R25, R26, R40, R41, R42, R43, R44, R45, R46, R47, R61, R62, R63, R64, R65, R66, R67, R68, R69, R70, R71, R72, R73, R74, R75, R76, R77, R78, R79, R80, R81, R82, R83, R84, R85, R86, R87, R88, R102, R103, R104, R105, R106, R107, R108, R109, R123, R124, R125, R126, R127, R128, R129, R130, R321, R322, R323	50Ω 1%

Table 10. LXT974A Bill of Materials

Item	Qty	Reference Designator	Description
26	2	R5, R6	10k Ω
27	8	R38, R39, R59, R60, R100, R101, R121, R122	200Ω 1%
28	20	R27, R29, R30, R34, R35, R48, R50, R51, R55, R56, R89, R91, R92, R96, R97, R110, R112, R113, R117, R118	82Ω
29	20	R28, R31, R32, R33, R37, R49, R52, R53, R54, R58, R111, R114, R115, R116, R120	130Ω
30	40	R262, R263, R264, R265, R266, R267, R268, R269, R270, R271, R272, R273, R274, R275, R276, R277, R278, R279, R280, R281, R282, R283, R284, R285, R286, R297, R288, R289, R290, R291, R292, R293, R294, R295, R296, R297, R298, R299, R300, R301,	22Ω
31	36	R200, R201, R202, R203, R204, R205, R206, R207, R208, R209, R210, R211, R212, R213, R214, R215, R216, R217, R218, R219, R220, R221, R222, R223, R224, R225, R226, R227, R228, R229, R230, R231, R240, R241, R242, R243	220Ω
32	19	R302, R303, R304, R305, R306, R307, R308, R309, R310, R311, R312, R313, R314, R315, R316, R317, R318, R319, R320	3.3 kΩ
33	2	S1, S2	Switch DIP-8
34	1	S3	Switch DIP-4
35	1	S4	Switch SPDT
36	1	U1	Quad Transceiver LXT974A
37	1	U4	IC - 74HCT08
38	1	U5	IC - 74HCT04
39	3	U6, U7, U8	IC - 74HCT164
40	8	U9, U10, U11, U12, U13, U14, U15, U16	IC - 74ABT244
41	1	T1	Quad Transformer HALO TG110-S460NX
42	1	Y1	Crystal Oscillator - 25 MHz

Figure 3. LXD974A

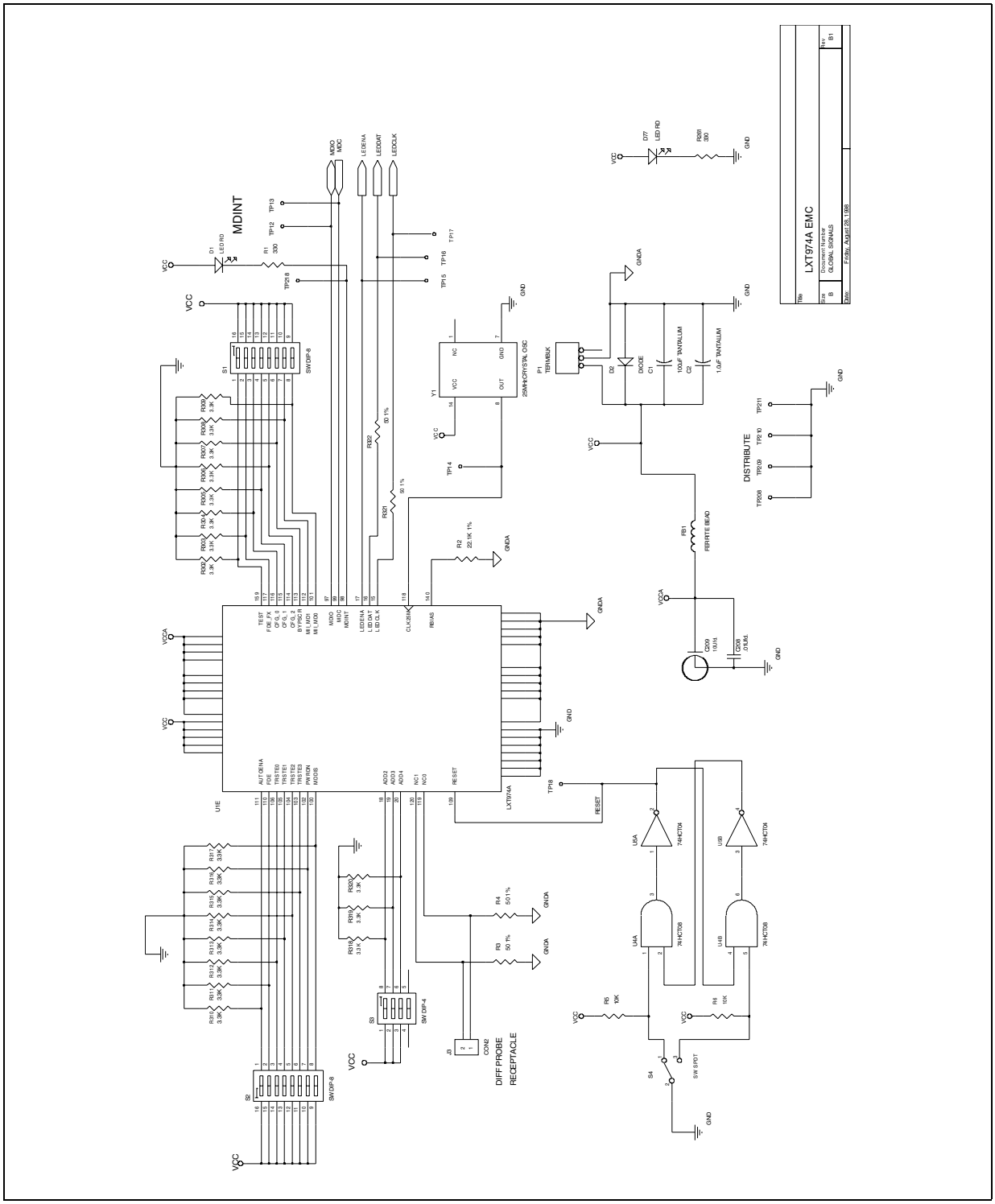


Figure 4. LEDs

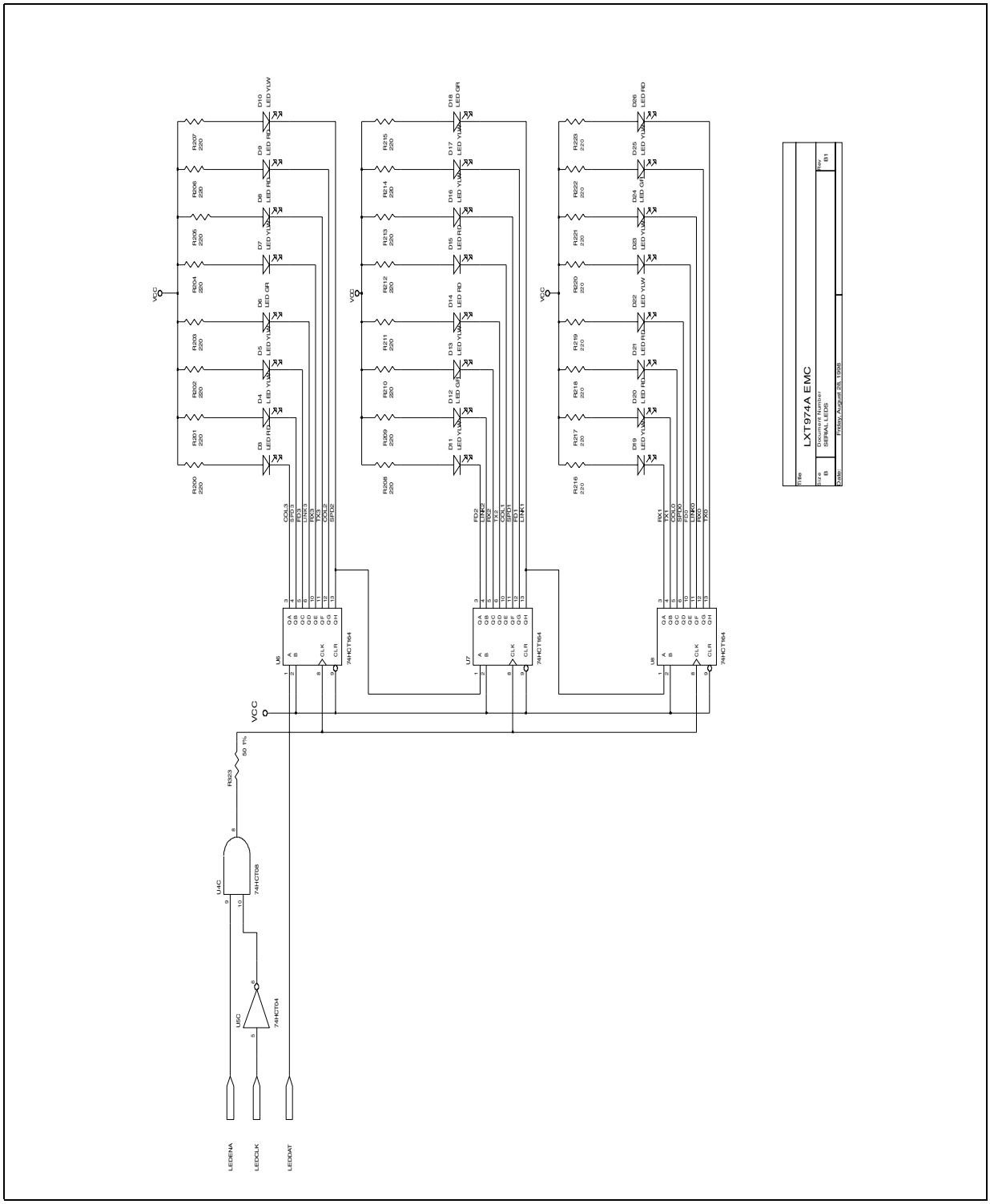


Figure 5. Ports 0 and 1

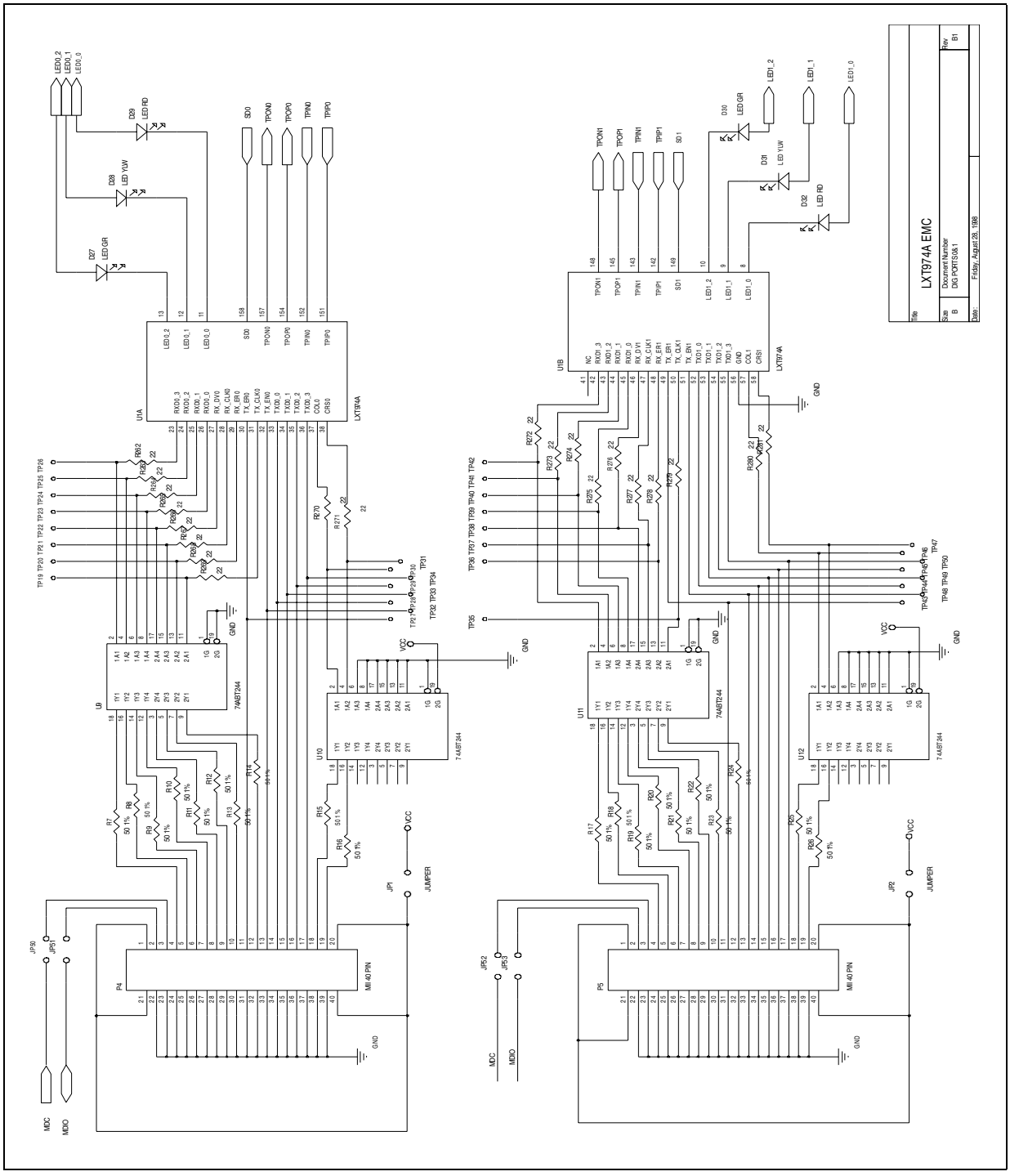


Figure 6. Port 0 Analog Circuitry

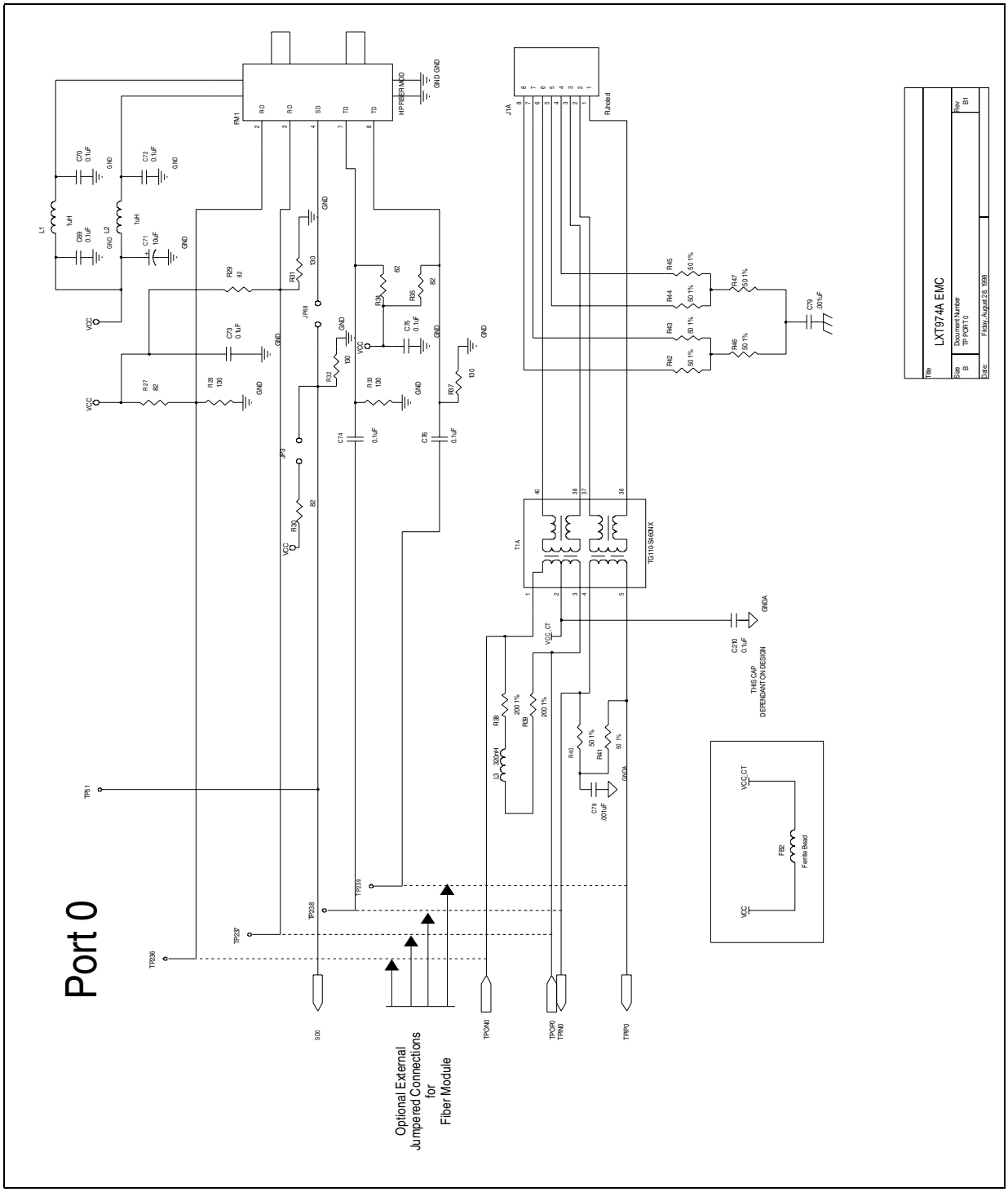


Figure 7. Port 1 Analog Circuitry

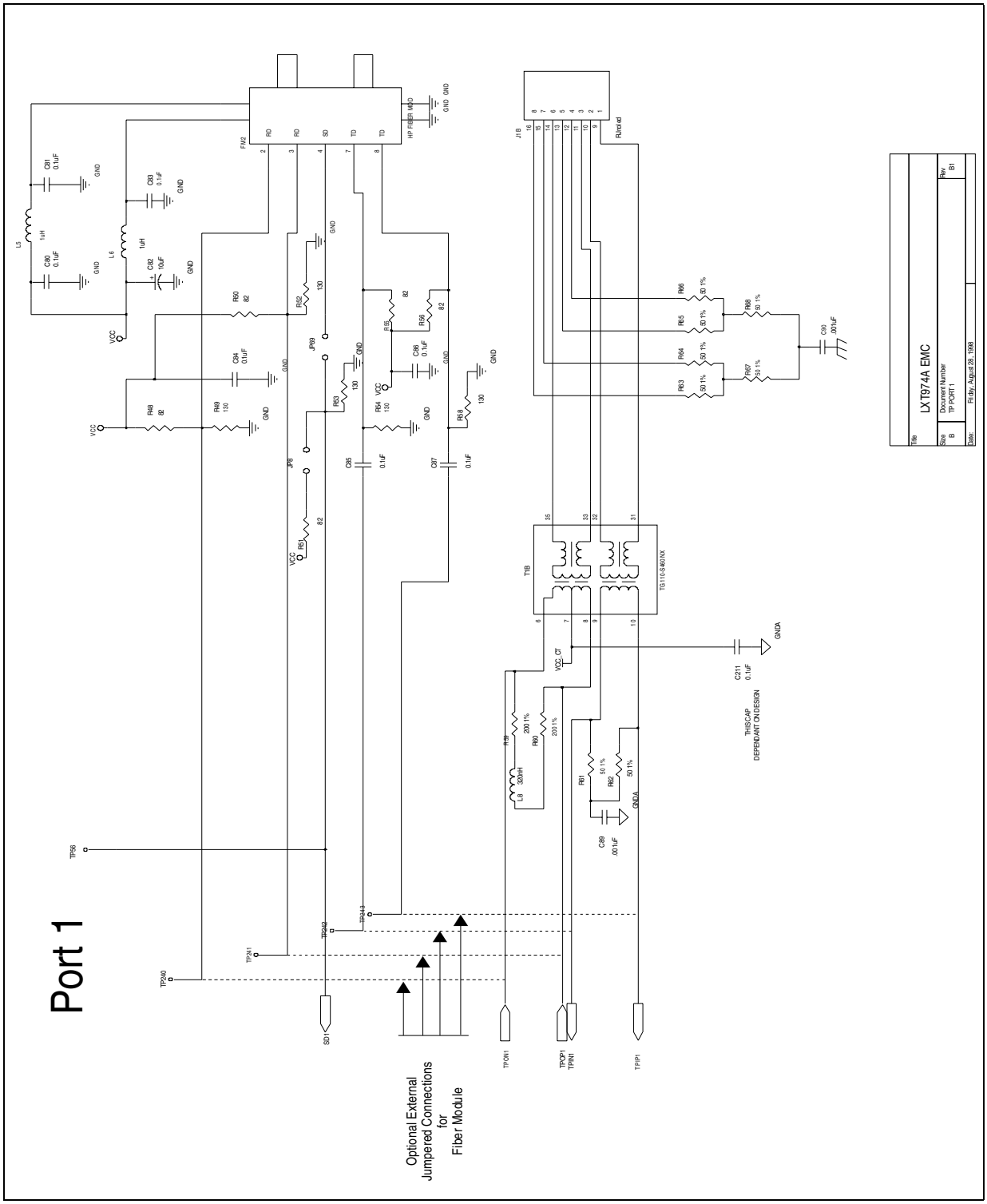


Figure 8. Ports 2 and 3

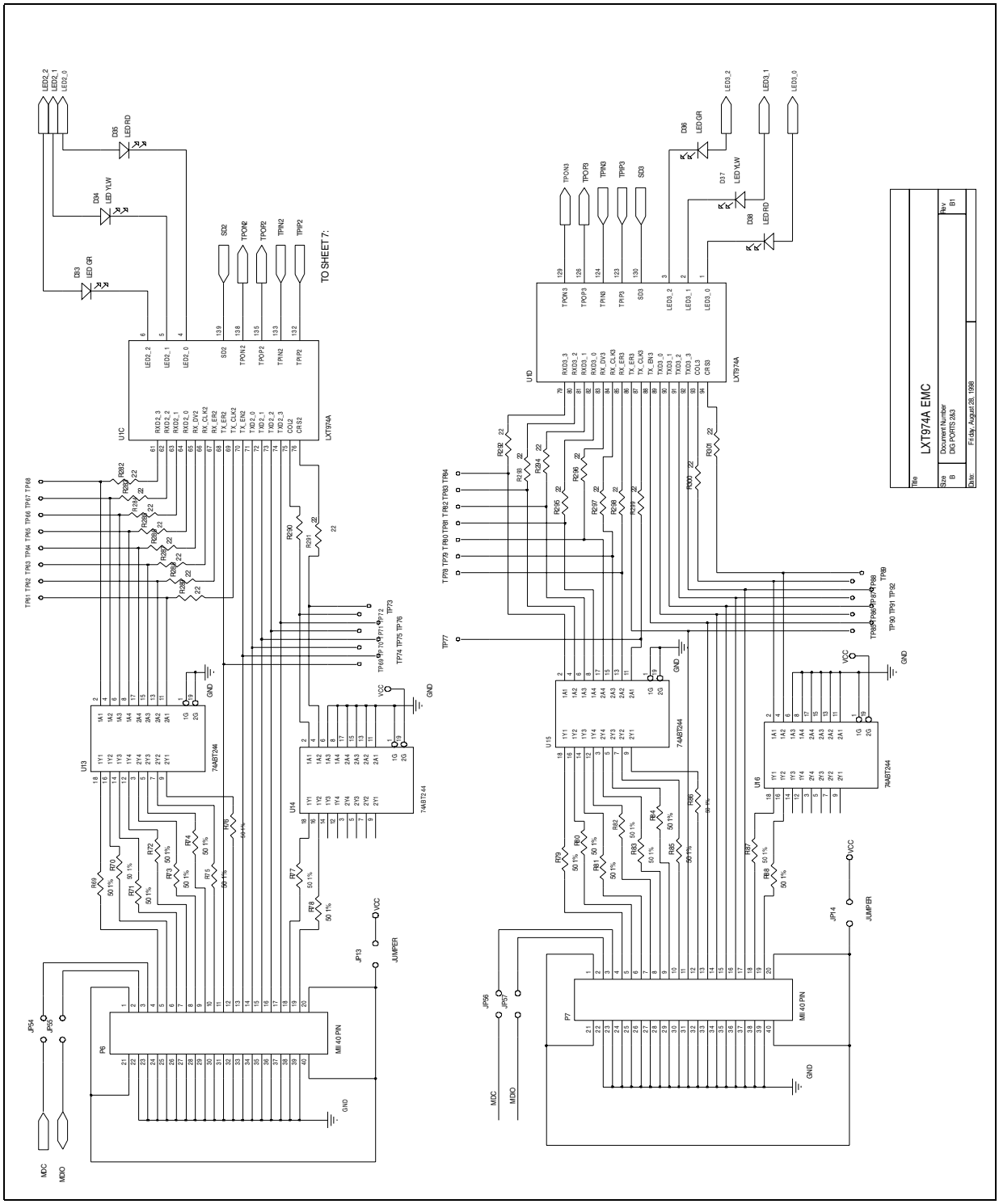


Figure 9. Port 2 Analog Circuitry

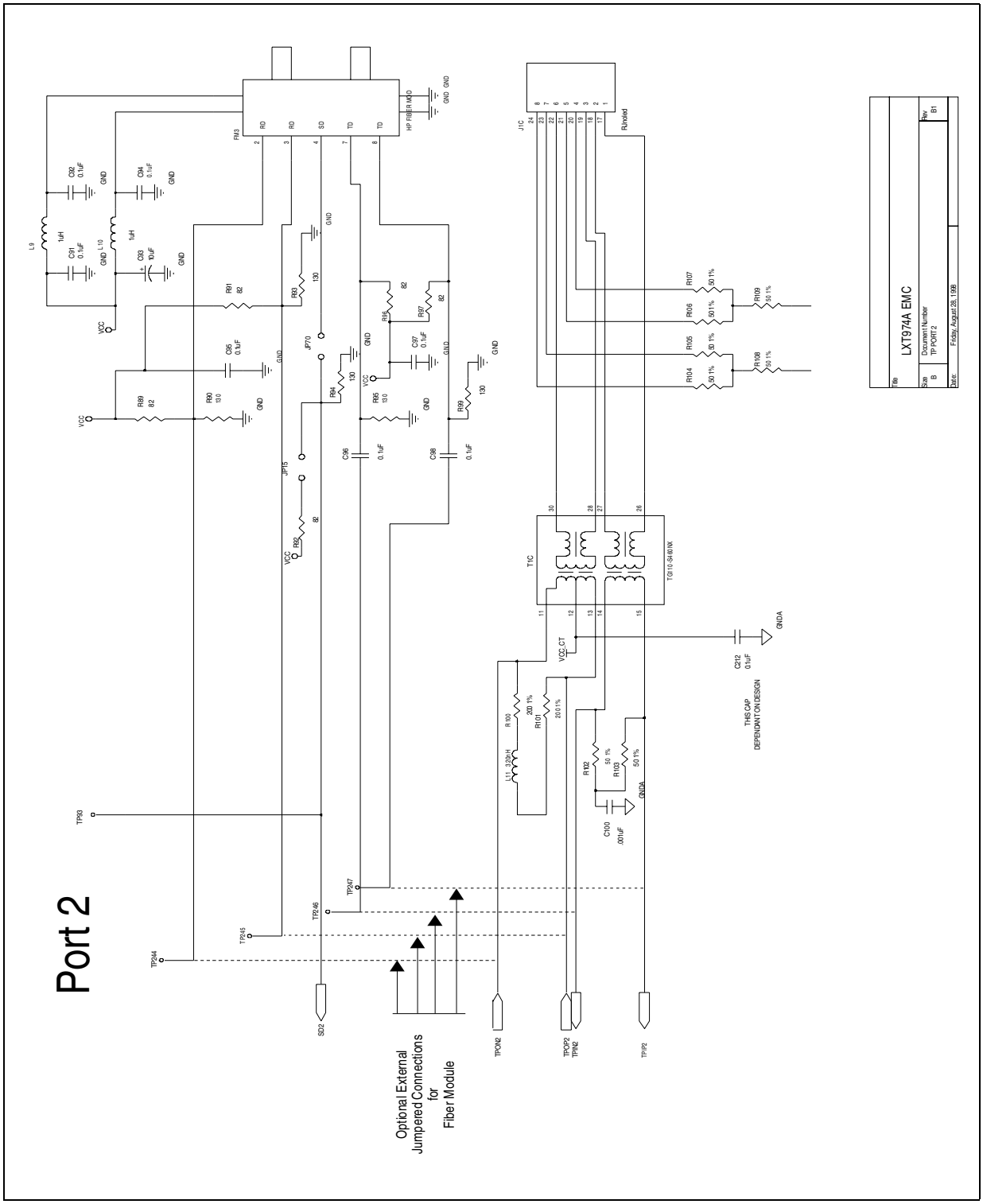


Figure 10. Port 3 Analog Circuitry

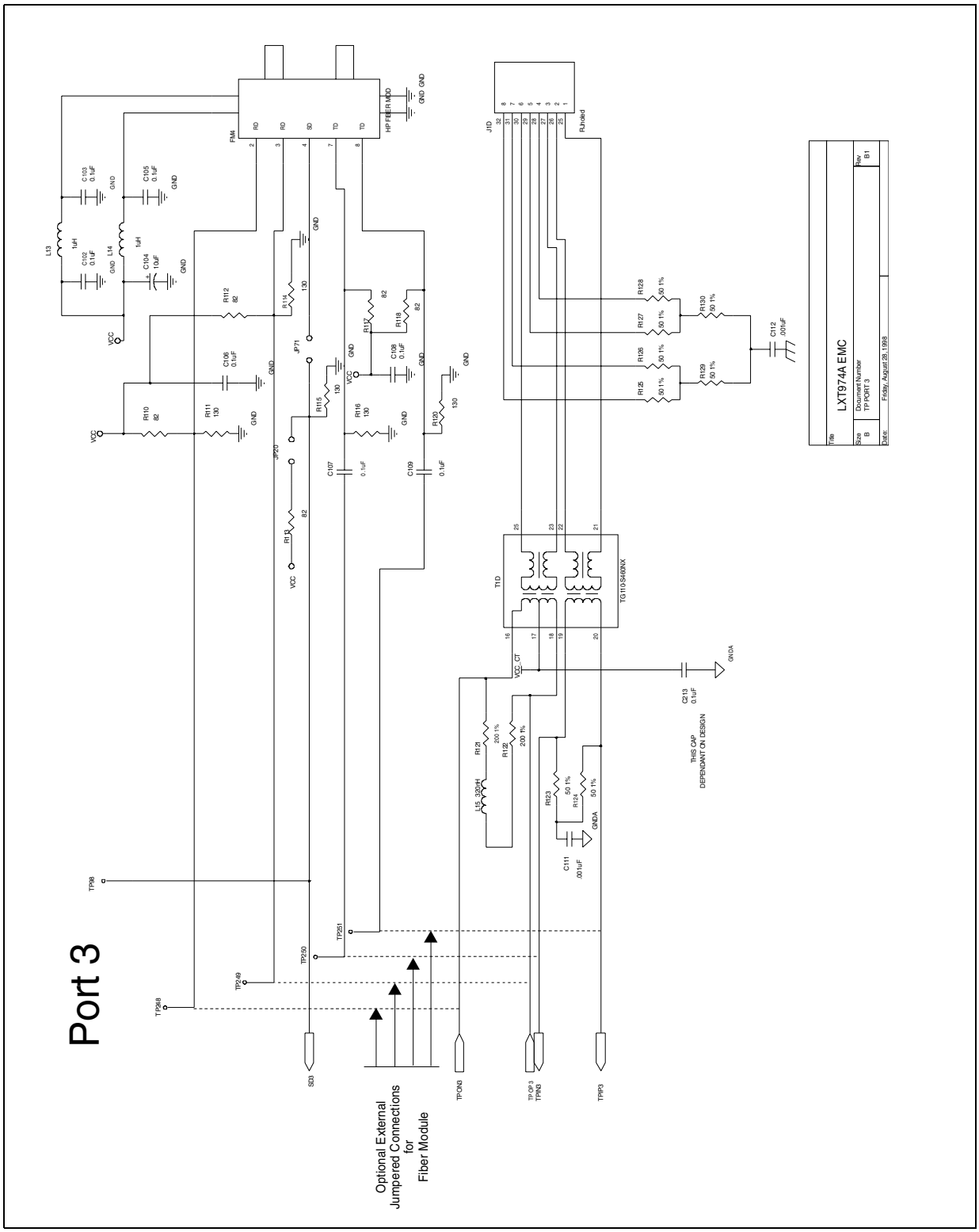


Figure 11. LED Resistor Packs