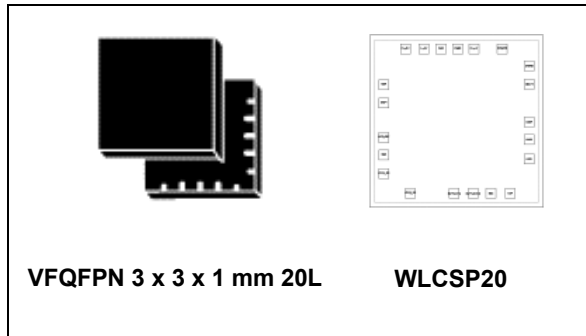


## Ultralow power energy harvester and battery charger

Datasheet - preliminary data



### Features

- Transformerless thermoelectric generators and PV modules energy harvester
- High efficiency for any harvesting source
- Up to 70 mA maximum battery charging current
- Fully integrated buck-boost DC-DC converter
- Programmable MPPT by external resistors
- 2.6 V to 5.3 V trimmable battery charge voltage level ( $\pm 1\%$  accuracy)
- 2.2 V to 3.6 V trimmable battery discharge voltage level ( $\pm 1\%$  accuracy)
- Two fully independent LDOs (1.8 V and 3.3 V output)
- Enable/disable LDO control pins
- Battery disconnect function for battery protection
- Battery connected and ongoing charge logic open drain indication pins

### Applications

- Charge any battery chemistry, including lithium based, solid state thin film and super-capacitor.
- WSN, HVAC, building and home automation, industrial control, remote metering, lighting, security, surveillance.
- Healthcare and biomedical sensors, fitness.

### Description

The SPV1050 is an ultralow power and high-efficiency energy harvester and battery charger, which implements the MPPT function and integrates the switching elements of a buck-boost converter.

The SPV1050 device allows the charge of any battery, including the thin film batteries, by tightly monitoring the end-of-charge and the minimum battery voltage in order to avoid the overdischarge and to preserve the battery life.

The power manager is suitable for both PV cells and TEG harvesting sources, as it covers the input voltage range from 75 mV up to 18 V and guarantees high efficiency in both buck-boost and boost configuration.

Furthermore the SPV1050 device shows very high flexibility thanks also to the trimming capability of the end-of-charge and undervoltage protection voltages. In such way any source and battery is matched.

The MPPT is programmable by a resistor input divider and allows maximizing the source power under any temperature and irradiance condition.

An unregulated voltage output is available (e.g. to supply a microcontroller), while two fully independent LDOs are embedded for powering sensors and RF transceivers. Both LDOs (1.8 V and 3.3 V) can be independently enabled through two dedicated pins.

# Contents

<b>1</b>	<b>Block diagram</b> .....	<b>5</b>
<b>2</b>	<b>Pin configuration</b> .....	<b>6</b>
<b>3</b>	<b>Pin description</b> .....	<b>7</b>
<b>4</b>	<b>Maximum ratings</b> .....	<b>9</b>
<b>5</b>	<b>Electrical characteristics</b> .....	<b>10</b>
<b>6</b>	<b>Functional description</b> .....	<b>13</b>
6.1	Battery charger .....	13
6.2	Boost configuration .....	15
6.3	Buck-boost configuration .....	19
6.4	MPPT setting .....	23
6.5	Power manager .....	25
<b>7</b>	<b>Package information</b> .....	<b>27</b>
<b>8</b>	<b>Ordering information</b> .....	<b>31</b>
<b>9</b>	<b>Revision history</b> .....	<b>31</b>

## List of tables

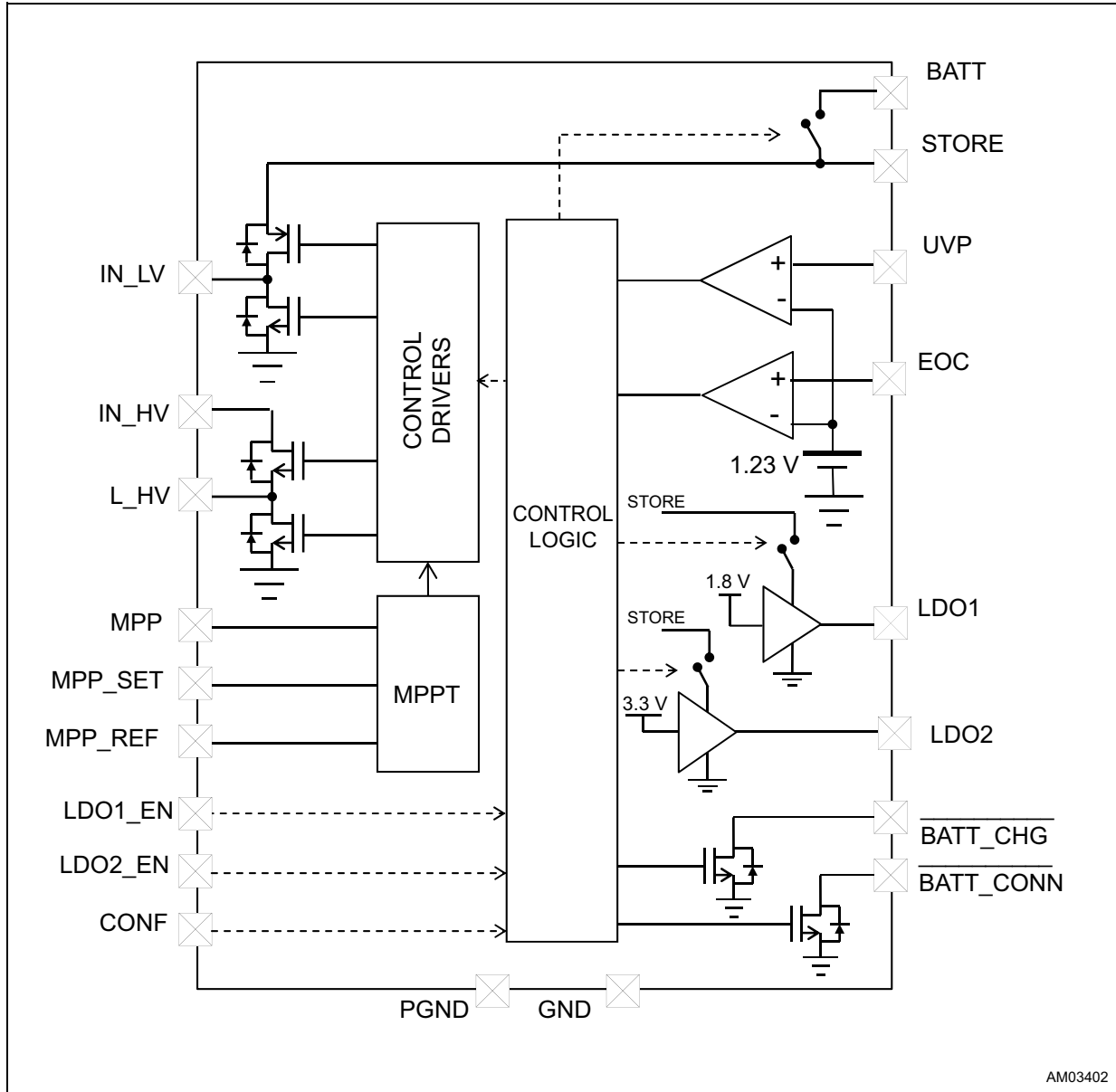
Table 1.	Pin description . . . . .	7
Table 2.	Thermal data . . . . .	9
Table 3.	Absolute maximum ratings . . . . .	9
Table 4.	Electrical characteristics . . . . .	10
Table 5.	VFQFPN20 3 x 3 x 1 mm - 20-lead pitch 0.4 package mechanical data . . . . .	28
Table 6.	WLCSP20, die pads coordinates and pads size. . . . .	30
Table 7.	Device summary . . . . .	31
Table 8.	Document revision history . . . . .	31

## List of figures

Figure 1.	Block diagram . . . . .	5
Figure 2.	Pin configuration (top through view) . . . . .	6
Figure 3.	Battery management section . . . . .	13
Figure 4.	Boost configuration . . . . .	15
Figure 5.	Boost startup . . . . .	16
Figure 6.	MPPT tracking . . . . .	17
Figure 7.	Triggering of $V_{EOC}$ (BATT pin floating) . . . . .	17
Figure 8.	Efficiency vs. input current - $V_{OC} = 1.0\text{ V}$ . . . . .	18
Figure 9.	Efficiency vs. input current - $V_{OC} = 1.5\text{ V}$ . . . . .	18
Figure 10.	Efficiency vs. input current - $V_{OC} = 2.0\text{ V}$ . . . . .	18
Figure 11.	Efficiency vs. input current - $V_{OC} = 2.5\text{ V}$ . . . . .	18
Figure 12.	Buck-boost configuration . . . . .	19
Figure 13.	Buck-boost startup ( $I_{IN} = 5\text{ }\mu\text{A}$ ) . . . . .	20
Figure 14.	MPPT tracking . . . . .	21
Figure 15.	Efficiency vs. input current - $V_{OC} = 6\text{ V}$ . . . . .	22
Figure 16.	Efficiency vs. input current - $V_{OC} = 9\text{ V}$ . . . . .	22
Figure 17.	Efficiency vs. input current - $V_{OC} = 12\text{ V}$ . . . . .	22
Figure 18.	Efficiency vs. input current - $V_{OC} = 15\text{ V}$ . . . . .	22
Figure 19.	MPPT setup circuitry . . . . .	23
Figure 20.	Energy harvester equivalent circuit . . . . .	24
Figure 21.	Voltage vs. time at different C values and fixed current . . . . .	24
Figure 22.	LDO1 turn on with 100 mA load . . . . .	25
Figure 23.	LDO2 turn on with 100 mA load . . . . .	26
Figure 24.	VFQFPN20 3 x 3 x 1 mm - 20-lead pitch 0.4 package outline(1) . . . . .	27
Figure 25.	WLCSP20, die and pads position (top view) . . . . .	29

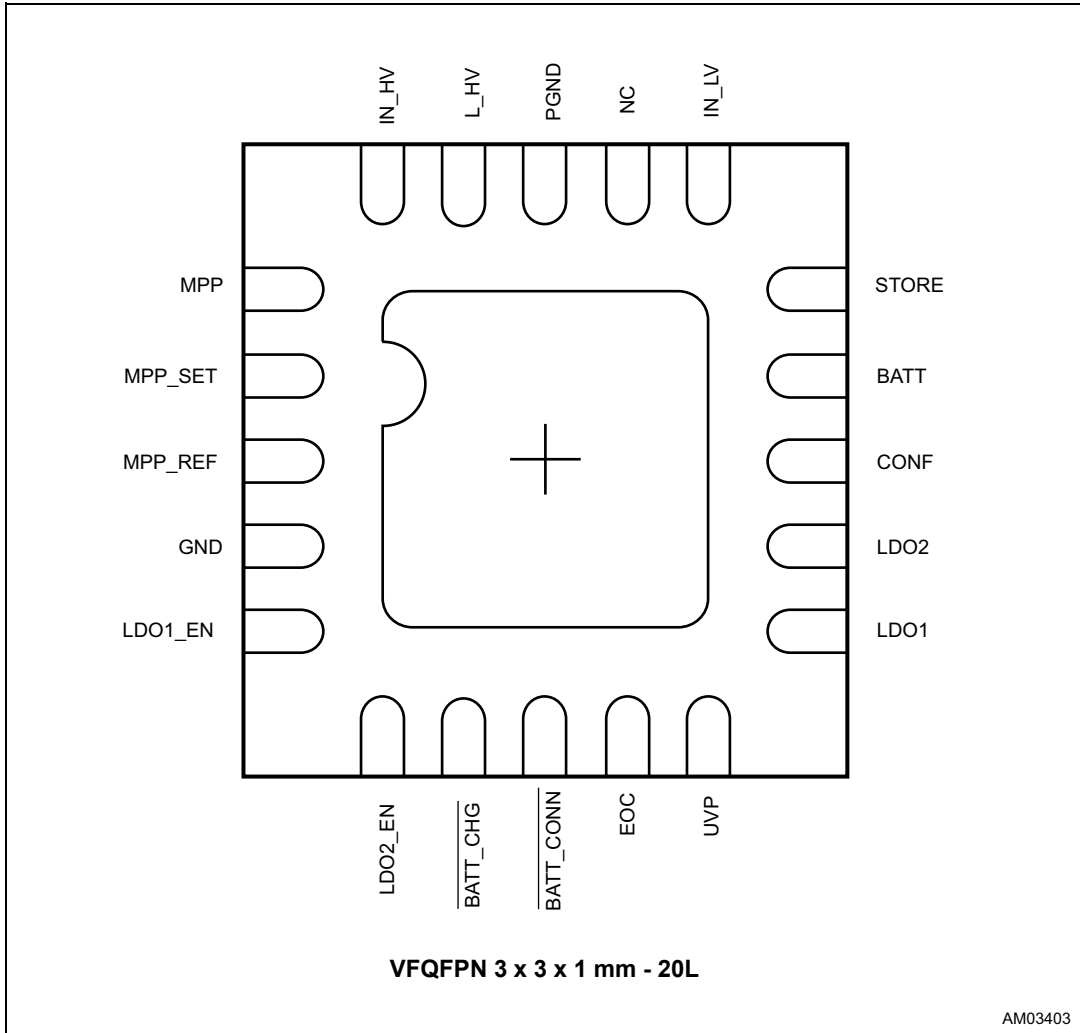
# 1 Block diagram

Figure 1. Block diagram



## 2 Pin configuration

Figure 2. Pin configuration (top through view)



### 3 Pin description

**Table 1. Pin description**

Pin no.	Name	Type	Description
1	MPP	I	Max. power point tracking voltage sense pin. To be connected to the voltage source through a ladder resistor.
2	MPP-SET	I	Max. power point setting voltage pin. To be connected to the MPP pin through a ladder resistor. Connect to STORE if MPP function is not required.
3	MPP-REF	I	Max. power point reference voltage pin. To be connected to a 10 nF capacitor. Connect to an external voltage reference if MPP function is not required.
4	GND	GND	Signal ground pin.
5	LDO1_EN	I	If high, enables LDO1.
6	LDO2_EN	I	If high, enables LDO2.
7	$\overline{\text{BATT\_CHG}}$	O	Ongoing battery charge output flag pin (open drain). If low, it indicates that the battery is on charge. If high, it indicates that the battery is not on charge.
8	$\overline{\text{BATT\_CONN}}$	O	Battery status output flag pin (open drain). If high, it indicates that the pass transistor between the STORE and BATT pins is open (battery disconnected). If low, it indicates that the pass transistor between the STORE and BATT pins is closed (battery connected).
9	EOC	I	Battery end-of-charge pin. To be connected to the STORE pin through a resistor divider between EOC and GND.
10	UVP	I	Battery undervoltage protection pin. To be connected to the STORE pin through a resistor.
11	LDO1	O	1.8 V regulated output voltage pin.
12	LDO2	O	3.3 V regulated output voltage pin.
13	CONF	I	Configuration pin. Boost configuration: to be connected to the voltage supply source. Buck-boost configuration: to be connected to ground.
14	BATT	I/O	Battery connection pin.
15	STORE	I/O	Tank capacitor connection pin.
16	IN_LV	I	Low voltage input source. It has to be connected to the inductor for both boost and buck-boost configuration.
17	NC	-	Not connected.
18	PGND	PGND	Power ground pin.

Table 1. Pin description (continued)

Pin no.	Name	Type	Description
19	L_HV	I	Input pin for buck-boost configuration. Boost configuration: to be connected to ground. Buck-boost configuration: to be connected to the inductor.
20	IN_HV	I	High voltage input source. Boost configuration: to be connected to ground. Buck-boost configuration: to be connected to the voltage supply source.



## 4 Maximum ratings

**Table 2. Thermal data**

Symbol	Parameter	Value		Unit
		Min.	Max.	
$R_{th\ j-c}$	Max. thermal resistance, junction to case		TBD	°C/W
$R_{th\ j-a}$	Max. thermal resistance, junction to ambient		TBD	°C/W
$P_{TOT}$	Maximum power dissipation at $T_{amb} = 85\text{ °C}$		1	W
$T_j$	Junction temperature range	-40 ÷ 125		°C
$T_{storage}$	Storage temperature	150		°C

**Table 3. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
IN_LV	Analog input	$V_{STORE} + 0.3$	V
IN_HV	Analog input	20	V
L_HV	Analog input	$IN\_HV + 0.3$	V
CONF	Analog input	5.5	V
MPP	Analog input	5.5	V
MPP-SET	Analog input	5.5	V
MPP-REF	Analog input	5.5	V
BATT	Analog input/output	5.5	V
STORE	Analog input/output	5.5	V
UVP	Analog input	$V_{STORE} + 0.3$	V
EOC	Analog input	$V_{STORE} + 0.3$	V
$\overline{BATT\_CONN}$	Digital output	5.5	V
$\overline{BATT\_CHG}$	Digital output	5.5	V
LDO1_EN	Digital input	$V_{STORE} + 0.3$	V
LDO2_EN	Digital input	$V_{STORE} + 0.3$	V
LDO1	Analog output	$V_{STORE} + 0.3$	V
LDO2	Analog output	$V_{STORE} + 0.3$	V
PGND	Power ground	0	V
GND	Signal ground	-0.3 to 0.3	V

## 5 Electrical characteristics

$V_{STORE} = 4\text{ V}$ ,  $T_{amb} = -40\text{ to }85\text{ }^\circ\text{C}$ , unless otherwise specified. Voltage with respect to GND unless otherwise specified.

**Table 4. Electrical characteristics**

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
<b>Battery operating range</b>						
$I_{BATT}$	Maximum battery charging current				70	mA
$V_{BATT}$	BATT pin voltage range		2.2		5.3	V
$V_{BATTACC}$	Battery voltage accuracy		-1		+1	%
$R_{BATT}$	Pass transistor resistance			7		$\Omega$
<b>Bandgap</b>						
$V_{BG}$	Internal reference voltage			1.23		V
	Accuracy		-1		+1	%
<b>UVP</b>						
$V_{UVP}$	Undervoltage protection range	$(V_{UVP} + UVP_{HYS}) < (V_{EOC} - EOC_{HYS})$	2.2		3.6	V
<b>EOC</b>						
$V_{EOC}$	Battery end-of-charge voltage	$(V_{UVP} + UVP_{HYS}) < (V_{EOC} - EOC_{HYS})$	2.6		5.3	V
$EOC_{HYS}$	EOC hysteresis	$V_{STORE}$ decreasing		-1		%
<b>Static current consumption</b>						
$I_{SD}$	Shutdown current	Shut down mode: Before first startup or $\overline{BATT\_CONN}$ high $T_{AMB} < 60\text{ }^\circ\text{C}$			1	nA
$I_{SB}$	Standby current	Standby mode: $\overline{BATT\_CONN}$ low, $\overline{BATT\_CHG}$ high and LDO1,2_EN low $T_{AMB} = 25\text{ }^\circ\text{C}$		1.0		$\mu\text{A}$
$I_{OP}$	Operating current in open load	Operating mode (LDOs in open load) $\overline{BATT\_CONN}$ low $\overline{BATT\_CHG}$ high $T_{AMB} = 25\text{ }^\circ\text{C}$	LDO1_EN = 1 or LDO2_EN = 1	1.9		$\mu\text{A}$
			LDO1,2_EN = 1	2.8		

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
<b>DC-DC converter</b>						
$V_{IN\_LV}$	Input voltage range	Boost configuration	0.15		$V_{EOC}$	V
$V_{IN\_HV}$		Buck-boost configuration	0.15		18	
$V_{IN\_MIN}$	Minimum input voltage at startup	Boost configuration $\overline{BATT\_CONN}$ high or at first startup		0.5		V
		Buck-boost configuration $\overline{BATT\_CONN}$ high or at first startup		2.6		
$I_{B\_SU}$	Startup input current	Boost configuration		30		$\mu A$
$I_{BB\_SU}$		Buck-boost configuration		5		$\mu A$
$R_{ON\_B}$	Low-side MOS resistance	Boost configuration		1.0		$\Omega$
$SR_{ON\_B}$	Synchronous rectifier MOS resistance			1.0		
$R_{ON\_BB}$	Low-side MOS resistance	Buck-boost configuration		1.5		$\Omega$
$SR_{ON\_BB}$	Synchronous rectifier MOS resistance			1.5		
$f_{SW}$	Switching frequency	Boost and buck-boost configurations			1	MHz
$UVLO_H$	Undervoltage lockout threshold ( $V_{STORE}$ increasing)	Boost and buck-boost configurations		2.6		V
$UVLO_L$	Undervoltage lockout threshold ( $V_{STORE}$ decreasing)			2.1		V
<b>MPPT</b>						
$T_{TRACKING}$	MPPT tracking period	$\overline{BATT\_CHG}$ low		16		s
$T_{SAMPLE}$	MPPT sampling time	$\overline{BATT\_CHG}$ high		0.4		s
$V_{MPP}$	MPP pin voltage range	Boost and buck-boost configurations	0.075		$V_{UVP}$	V
$MPP_{ACC}$	MPP tracking accuracy	Boost and buck-boost configurations	95			%
<b>LDO</b>						
$V_{LDO1,2}$	LDO1,2 adjusted output voltage	$LDO1\_EN = 1$		1.8		V
		$LDO2\_EN = 1$		3.3		
$\Delta V_{LDO1,2}$	LDO1 dropout	$V_{LDO1} + 200\text{ mV} < V_{BATT} \leq 5.3\text{ V}$ $I_{LDO1} = 100\text{ mA}$		0.5		%
	LDO2 dropout	$V_{LDO2} + 200\text{ mV} < V_{BATT} \leq 5.3\text{ V}$ $I_{LDO2} = 100\text{ mA}$		1.3		
$t_{LDO}$	LDO1,2 startup time	$\overline{BATT\_DIS}$ low $C_{LDO1,2} = 100\text{ nF}$			1	ms
$V_{LDO1,2\_EN\_H}$	LDO1,2 enable input HIGH			1		V
$V_{LDO1,2\_EN\_L}$	LDO1,2 enable input LOW			0.5		V

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
<b>Digital output</b>						
$V_{\overline{\text{BATT\_CONN\_L}}}$	$V_{\text{BATT\_DIS}} \text{ LOW}$	1 mA sink current		50		mV
$V_{\overline{\text{BATT\_CHG\_L}}}$	$V_{\text{XBATT\_CHG}} \text{ LOW}$	1 mA sink current		50		mV

## 6 Functional description

The SPV1050 is an ultralow power energy harvester with an embedded MPPT algorithm, a battery charger and power manager designed for applications up to about 400 mW.

The SPV1050 device integrates a DC-DC converter stage that can be configured as boost or buck-boost by tying the CONF pin to PV+/TEG+ or to ground respectively as shown in [Figure 4](#) and [Figure 12 on page 19](#).

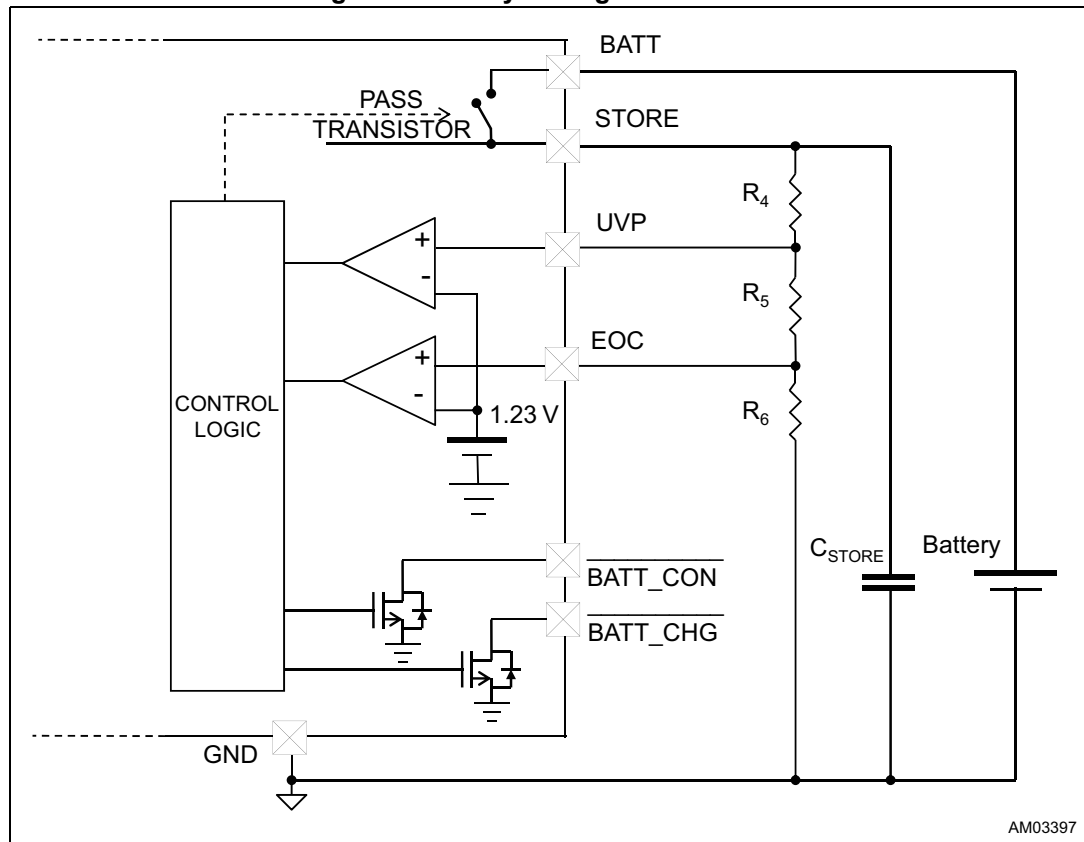
If the embedded MPPT algorithm is enabled, the device regulates the working point of the DC-DC converter in order to maximize the power extracted from the source by tracking its output voltage. See further details in [Section 6.2: Boost configuration on page 15](#) and [Section 6.3: Buck-boost configuration on page 19](#).

The MPPT algorithm can be disabled by shorting the MPP-SET pin to the STORE pin, and by providing an external voltage to the MPP-REF pin. The reference voltage on the MPP-REF pin must be  $< (V_{STORE} - 200 \text{ mV})$ .

### 6.1 Battery charger

In order to guarantee the lifetime and safety of the battery, the SPV1050 device controls an integrated pass transistor between the STORE and BATT pins and implements both the undervoltage (UVP) and the end-of-charge (EOC) protection thresholds.

Figure 3. Battery management section



Before the first startup the pass transistor is open, so that the leakage from the battery is lower than 1 nA. The pass transistor will be closed once the voltage on the STORE pin will rise such that the EOC threshold  $V_{EOC}$  is triggered. If the battery is full, and until  $V_{STORE} > V_{EOC} - EOC_{HYS}$ , the DC-DC converter will stop switching to avoid battery overcharge.

On the contrary, in order to avoid the overdischarge of the battery, the pass transistor will be opened once the voltage on the STORE pin will decrease down to UVP threshold  $V_{UVP}$ .

These functions are simply implemented by the control of two voltage thresholds,  $V_{UVP}$  and  $V_{EOC}$ , which can be regulated by a resistor partitioning (R4, R5, R6) between STORE, UVP and EOC pins.

The scaled voltages on the UVP and EOC pins will be compared with the internal bandgap voltage reference  $V_{BG}$  set at 1.23 V.

The design rules to setup the R4, R5 and R6 are the following:

#### Equation 1

$$V_{BG} = V_{UVP} \cdot (R5 + R6) / (R4 + R5 + R6)$$

#### Equation 2

$$V_{BG} = V_{EOC} \cdot R6 / (R4 + R5 + R6)$$

In order to minimize the leakage due to the output resistor partitioning it has to be typically:

#### Equation 3

$$10 \text{ M}\Omega \leq R4 + R5 + R6 \leq 20 \text{ M}\Omega$$

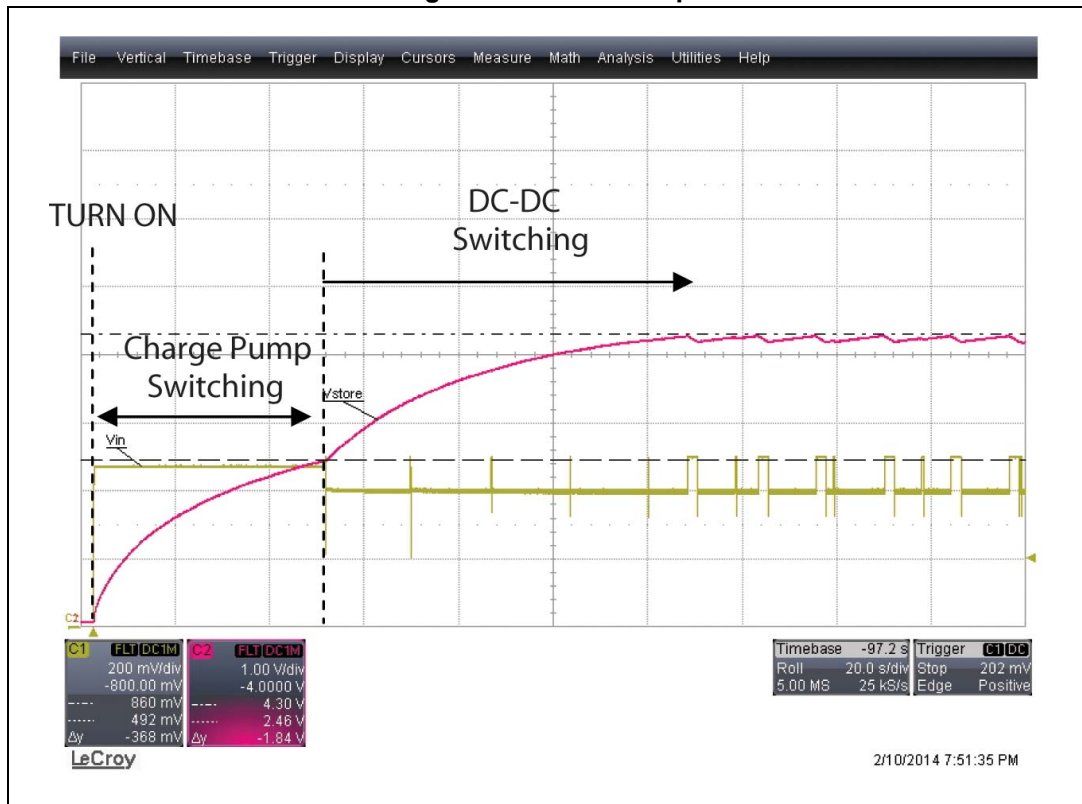
Further, the SPV1050 device provides two open drain digital outputs to an external microcontroller:

- **BATT\_CONN**  
This pin is pulled down when the pass transistor is closed. It will be released once the pass transistor will be opened (e.g. triggering of  $V_{UVP}$ ). If used, this pin must be pulled-up to the STORE by a 10 M $\Omega$  (typical) resistor.
- **BATT\_CHG**  
This pin is pulled down when the DC-DC converter is switching, while it's released when it is not switching, i.e. when the EOC threshold is triggered until the voltage on the STORE pin drops at  $V_{EOC} - EOC_{HYS}$ , when the UVLO threshold is triggered or during the  $T_{SAMPLE}$  of the MPPT algorithm. If used, this pin must be pulled-up to the STORE by a 10 M $\Omega$  (typical) resistor.



Figure 5 shows the behavior of input voltage  $V_{IN}$  and  $V_{STORE}$  at the startup.

Figure 5. Boost startup



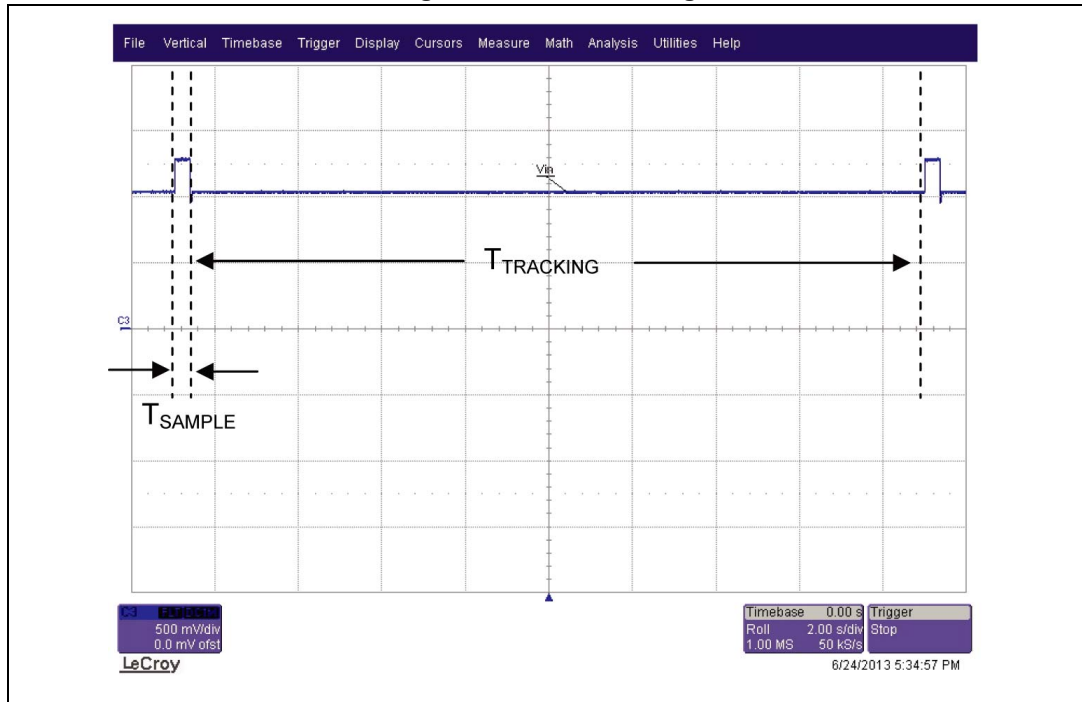
In the range  $2.6\text{ V} \leq V_{STORE} < V_{EOC}$  the voltage is boosted by the DC-DC converter. In this voltage range the SPV1050 device sets its internal impedance according to the integrated MPPT algorithm (the MPPT mode is active). The SPV1050 device will stop switching for 400 ms ( $T_{SAMPLE}$ ) every 16 seconds ( $T_{TRACKING}$ ). During the  $T_{SAMPLE}$ , the input open circuit voltage  $V_{OC}$  is sampled by charging the capacitor on the MPP-REF pin. Once the  $T_{SAMPLE}$  is elapsed, the DC-DC converter will start switching back by setting its own impedance such that  $V_{IN}$  stays as close as possible to  $V_{MPP}$  of the source. A resistor partitioning connected between the source and the pins MPP and MPP-SET has to be properly selected, in order to match the manufacturer's specs. Please refer to [Section 6.4: MPPT setting on page 23](#) for further details.

The periodic sampling of  $V_{OC}$  guarantees the best MPPT in case of source condition variations (e.g. irradiation/thermal gradient and/or temperature changes).



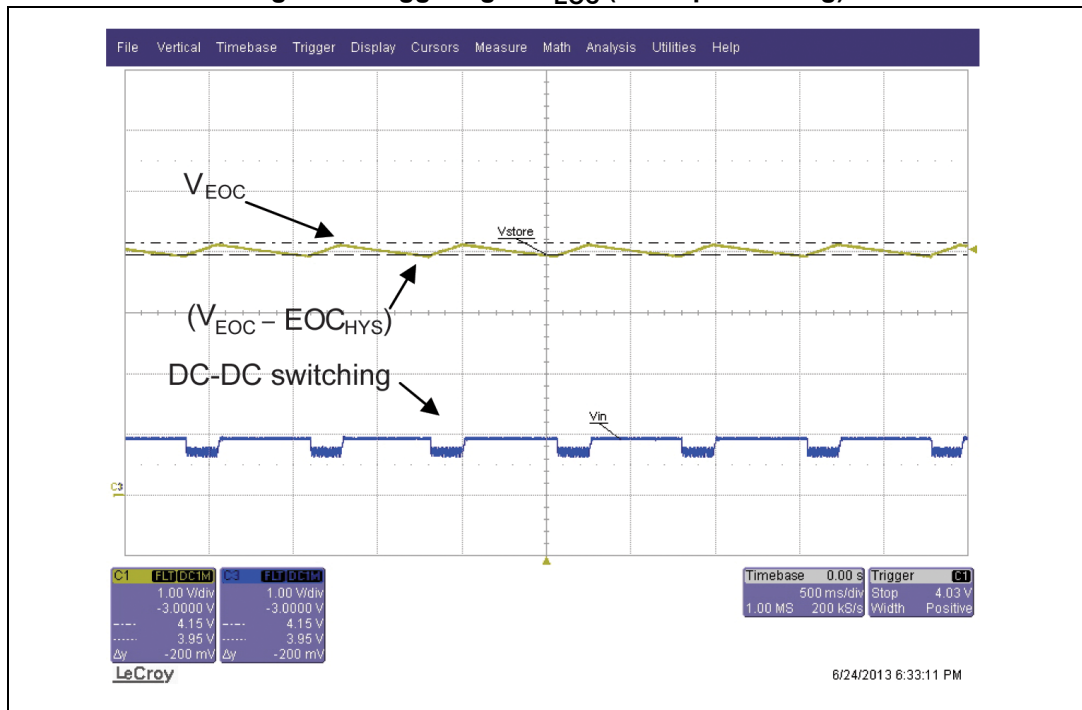
Figure 6 shows the input voltage waveform of a PV panel supplying  $V_{OC} = 1.25\text{ V}$  and  $V_{MPP} = 1.05\text{ V}$ .

Figure 6. MPPT tracking

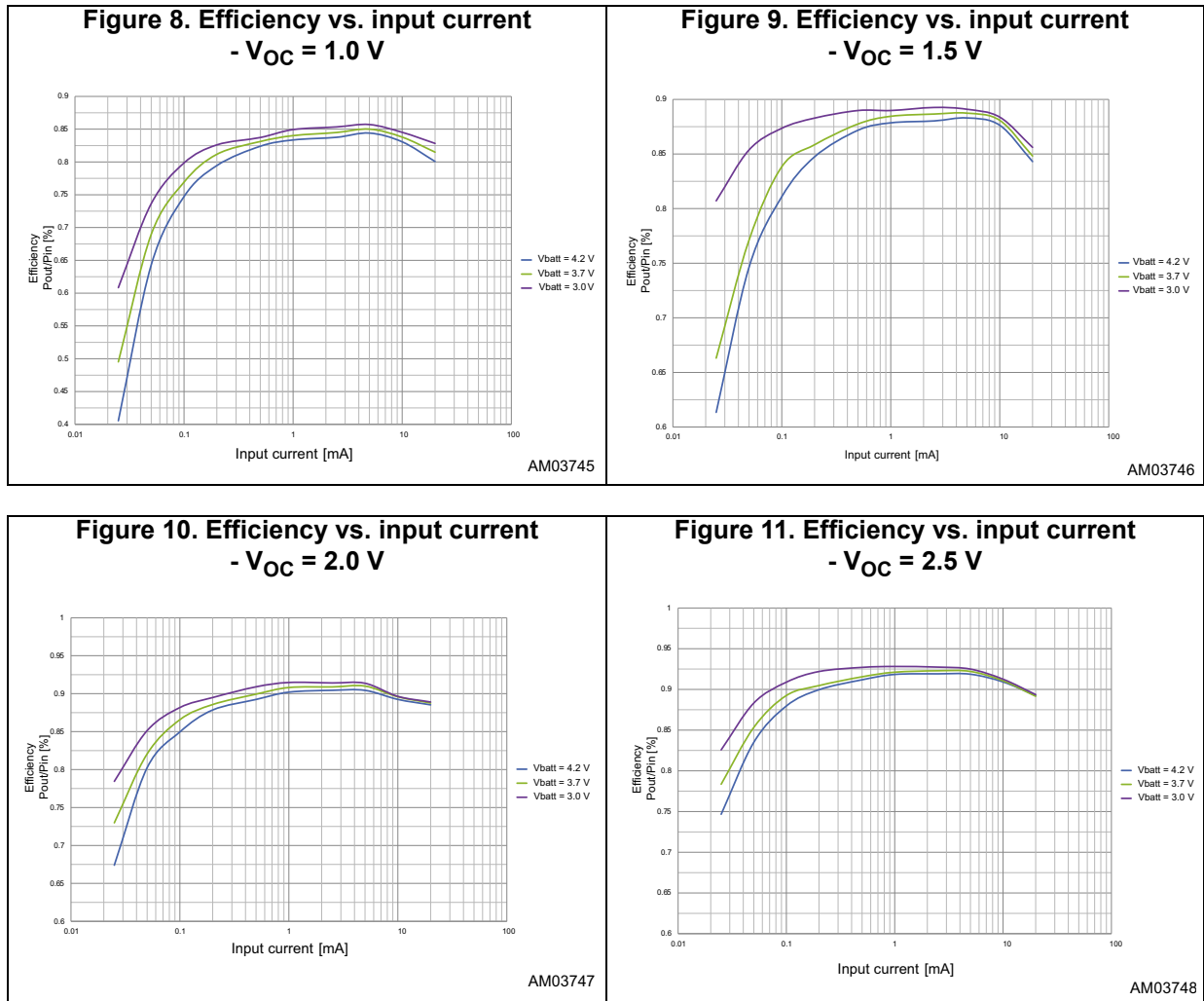


Once the  $V_{EOC}$  threshold is triggered, the switching of the DC-DC converter is stopped until  $V_{STORE}$  will decrease to  $V_{EOC} - EOC_{HYS}$ .

Figure 7. Triggering of  $V_{EOC}$  (BATT pin floating)



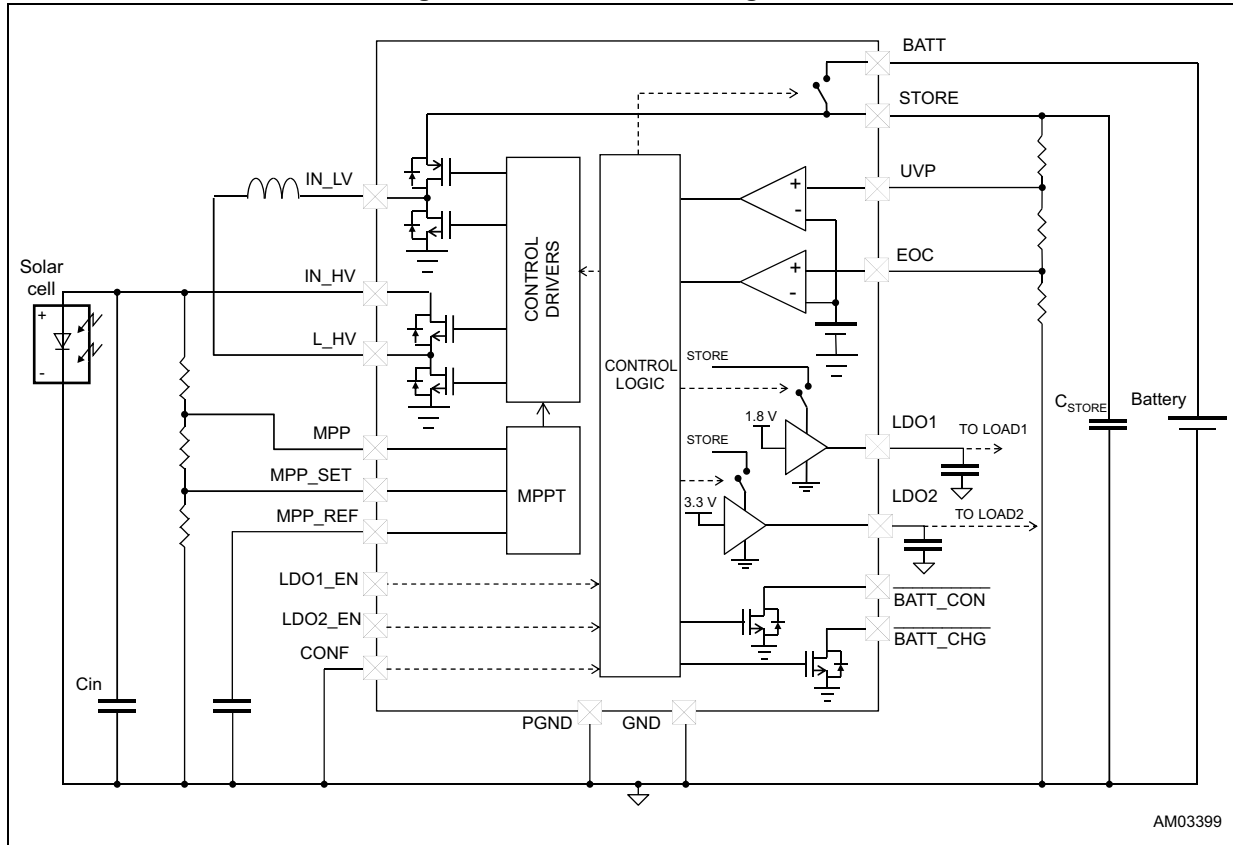
The following plots from *Figure 8* to *Figure 11* show the power efficiency of the DC-DC converter configured in boost mode at  $T_{amb} = 25\text{ }^{\circ}\text{C}$  in some typical use cases at different open circuit voltages:



### 6.3 Buck-boost configuration

Figure 12 shows the buck-boost application circuit.

Figure 12. Buck-boost configuration



In case of buck-boost configuration, once the harvested source is connected, the IN\_HV and STORE pins will be internally shorted until  $V_{STORE} < 2.6\text{ V}$ . *Figure 13* shows the behavior of the input voltage  $V_{IN\_HV}$  and  $V_{STORE}$  at the startup.

**Figure 13. Buck-boost startup ( $I_{IN} = 5\ \mu\text{A}$ )**

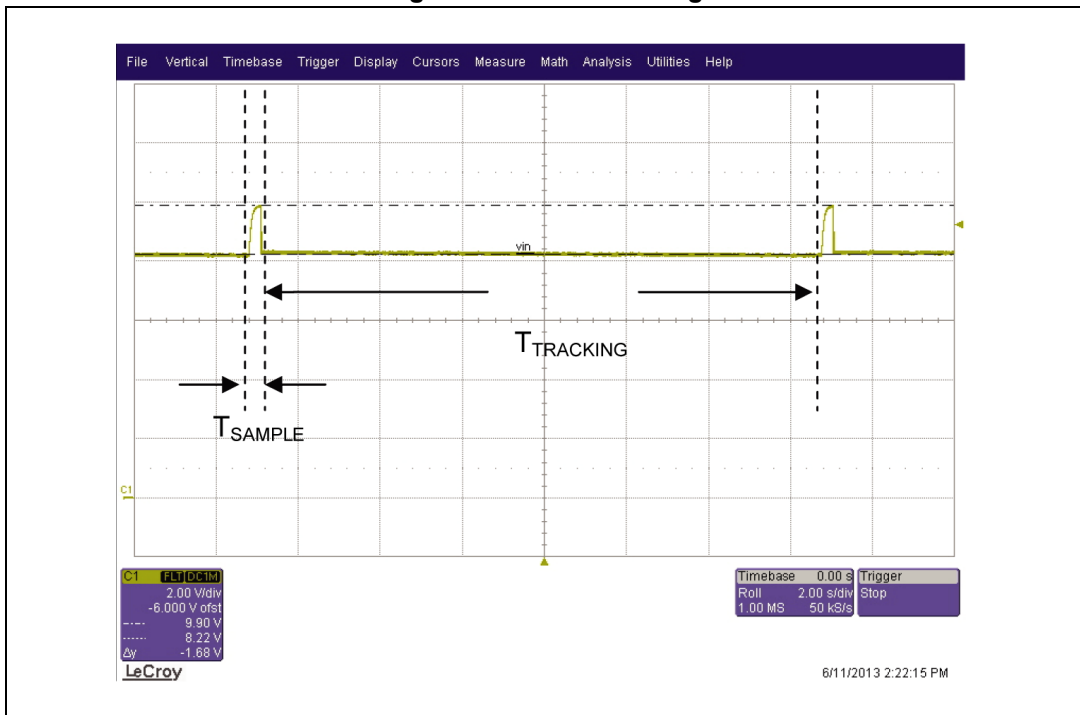


In the range  $2.6\text{ V} \leq V_{STORE} < V_{EOC}$  the integrated DC-DC converter will start switching. In this operating range the SPV1050 input impedance is set by the embedded MPPT algorithm (the MPPT mode is active). The SPV1050 device will stop switching for 400ms ( $T_{SAMPLE}$ ) every 16 seconds ( $T_{TRACKING}$ ). During the  $T_{SAMPLE}$ , the input open circuit voltage  $V_{OC}$  is sampled by charging the capacitor on the MPP-REF pin. Once the  $T_{SAMPLE}$  is elapsed, the DC-DC converter will start switching back by setting its own impedance such that  $V_{IN}$  stays as close as possible to  $V_{MPP}$  of the source. A resistor partitioning connected between the source and the pins MPP and MPP-SET has to be properly selected in order to match the  $V_{MPP}$  given by the source manufacturer. Please refer to [Section 6.4: MPPT setting](#) for further details.

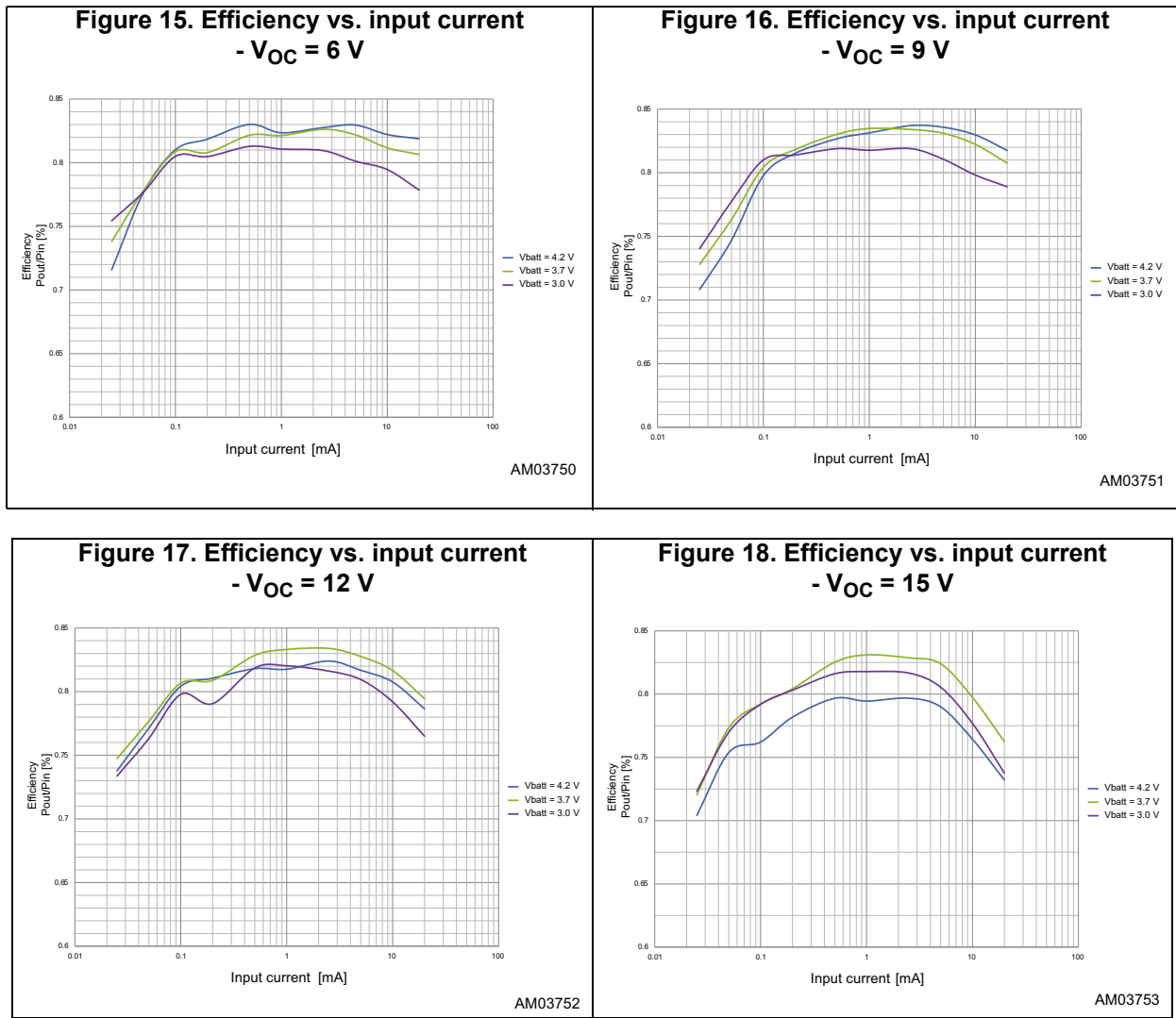
The periodic sampling of  $V_{OC}$  guarantees the best MPPT in case of source condition variations (e.g. irradiation and/or temperature changes).

Figure 14 shows the MPPT tracking form in case of  $V_{OC} = 9.9\text{ V}$  and  $V_{MPP} = 8.2\text{ V}$ .

Figure 14. MPPT tracking



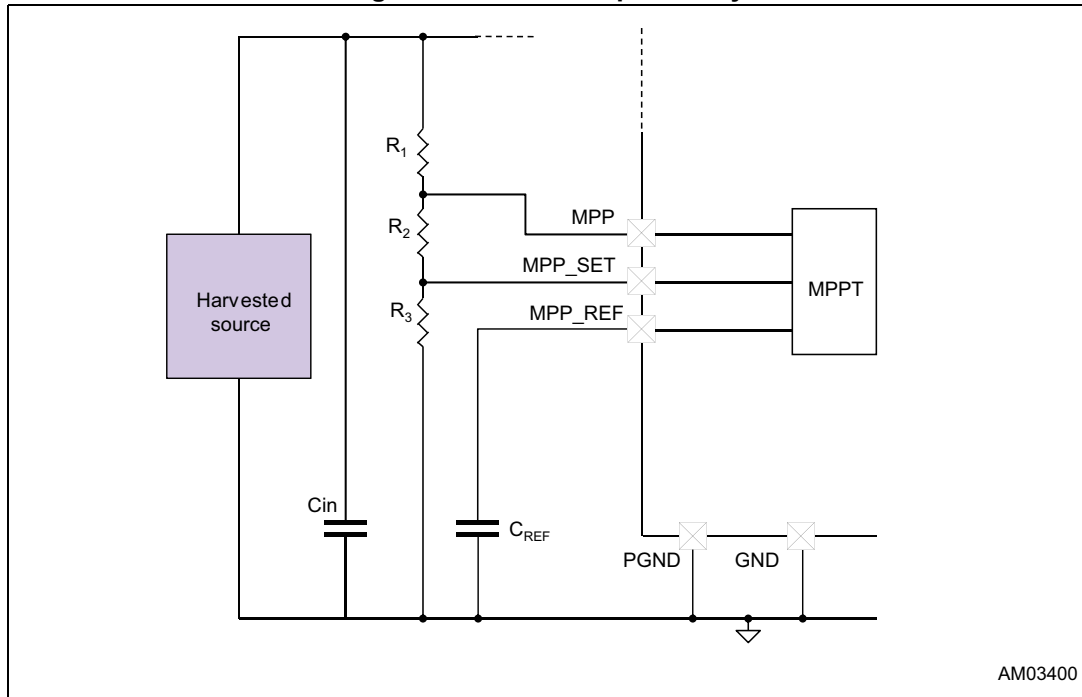
The following plots from *Figure 15* to *Figure 18* show the power efficiency of the DC-DC converter configured in buck-boost mode at  $T_{amb} = 25\text{ }^{\circ}\text{C}$  in some typical use cases:



## 6.4 MPPT setting

The SPV1050 device sets its working point such that  $V_{IN} = V_{MPP}$ . In fact  $V_{MPP}$  is a fraction of the open circuit voltage  $V_{OC}$  of the harvesting source.

Figure 19. MPPT setup circuitry



The maximum power point is set through the input resistor partitioning R1, R2 and R3.

First of all, set the total input resistance ( $R1 + R2 + R3$ ) considering the maximum acceptable leakage current ( $I_{LEAKAGE}$ ):

### Equation 4

$$I_{LEAKAGE} = V_{OC} / (R1 + R2 + R3)$$

Typically, assuming  $10\text{ M}\Omega \leq R1 + R2 + R3 \leq 20\text{ M}\Omega$ , the leakage on the input resistor partitioning can be considered as negligible.

Then set the R2 + R3 considering that the voltage on the MPP pin must be lower than the minimum  $V_{UVP}$  ( $V_{UVP(min)} = 2.2\text{ V}$ ):

### Equation 5

$$R2 + R3 \leq (R1 + R2 + R3) * V_{UVP(min)} / V_{OC}$$

Finally, set the R3 considering the  $MPP_{RATIO}$  (in case of PV panels  $MPP_{RATIO} = V_{MP} / V_{OC}$ ):

### Equation 6

$$MPP_{RATIO} = R3 / (R2 + R3)$$

In boost mode if the electrical characteristics of the selected source and battery are such that  $V_{OC-MAX} \leq V_{UVP(min)}$ , then the resistor R1 can be replaced by a short-circuit. Consequently, only R2 and R3 have to be selected for a proper setting of  $MPP_{RATIO}$ .

In a PV panel the  $V_{MPP}$  is typically within 70% ÷ 80% of  $V_{OC}$ .

In a TEG the  $V_{MPP\_SET}$  is typically about 50% of  $V_{OC}$ , so the proper partitioning is:  $R1 = 0$  and  $R2 = R3$ .

The MPPT accuracy can be strongly affected by an improper selection of the input capacitor. The input capacitance  $C_{IN} = 4.7 \mu F$  generally covers the most typical use cases.

The energy extracted from the harvested source, and stored in the input capacitance, is transferred to the load by the DC-DC converter through the inductor. The energy extracted by the inductor depends by the sink current: the higher input currents cause higher voltage drop on the input capacitance and this may result a problem for low voltage (< 1 V) and high energy (> 20 mA) sources. In such application cases the input capacitance has to be increased or, alternatively the L1 inductance has to be reduced.

During the  $T_{SAMPLE}$  time frame the input capacitor  $C_{IN}$  is charged up to  $V_{OC}$  by the source with a T1 time constant resulting from the capacitance and the equivalent resistance  $R_{EQ}$  of the source.

In case of the PV source, assuming  $I_{MPP}$  the minimum current at which the MPP must be guaranteed, the  $R_{EQ}$  can be calculated as following:

**Equation 7**

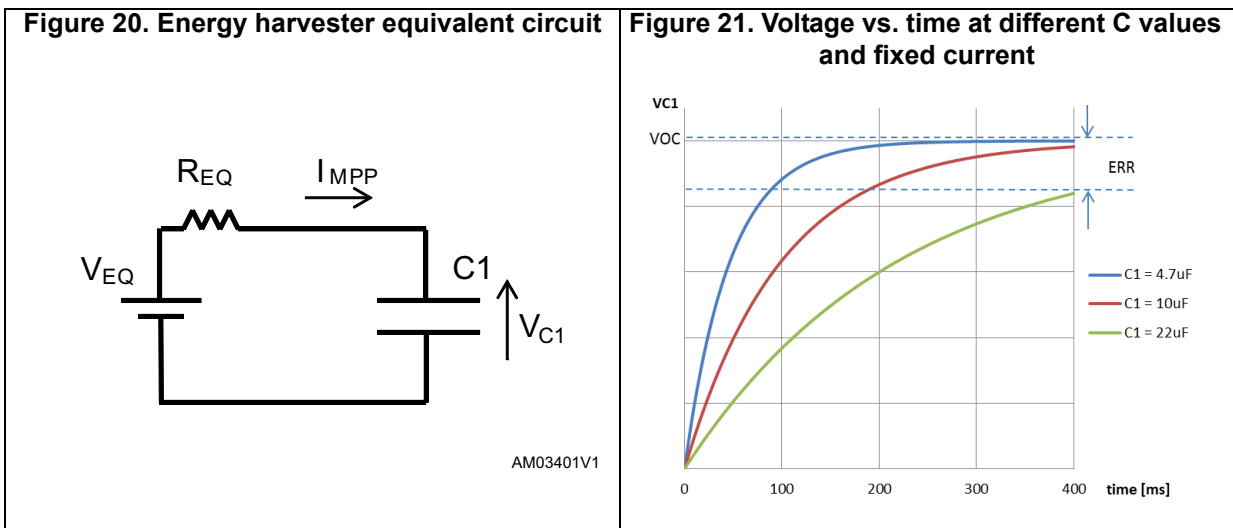
$$R_{EQ} = (V_{OC} - V_{MPP}) / I_{MPP} = V_{OC} \cdot (1 - MPP_{RATIO}) / I_{MPP}$$

Thus  $C_{IN}$  is calculated by the following formula:

**Equation 8**

$$C_{IN} \leq T1 / R_{EQ}$$

The following plots in [Figure 20](#) and [Figure 21](#) show the effect of different  $C_{IN}$  values on the time constant. If the capacitance is too high, the capacitor may not be charged within the  $T_{SAMPLE} = 400 \text{ ms}$  time window, thus affecting the MPPT accuracy.





## 6.5 Power manager

The SPV1050 device works as a power manager also by providing one unregulated output voltage on the STORE pin and two regulated voltages on the LDO1 (1.8 V) and LDO2 (3.3 V) pins.

Each LDO can be selectively enabled or disabled by driving the related enable/disable pins LDO1\_EN and LDO2\_EN.

The performances of the LDOs can be optimized by selecting a proper capacitor between the LDO output pin and ground. A 100 nF for each LDO pin is suitable for the most typical use cases. *Figure 22* and *Figure 23* show the behavior of the LDOs when a 100 mA load is connected.

Figure 22. LDO1 turn on with 100 mA load

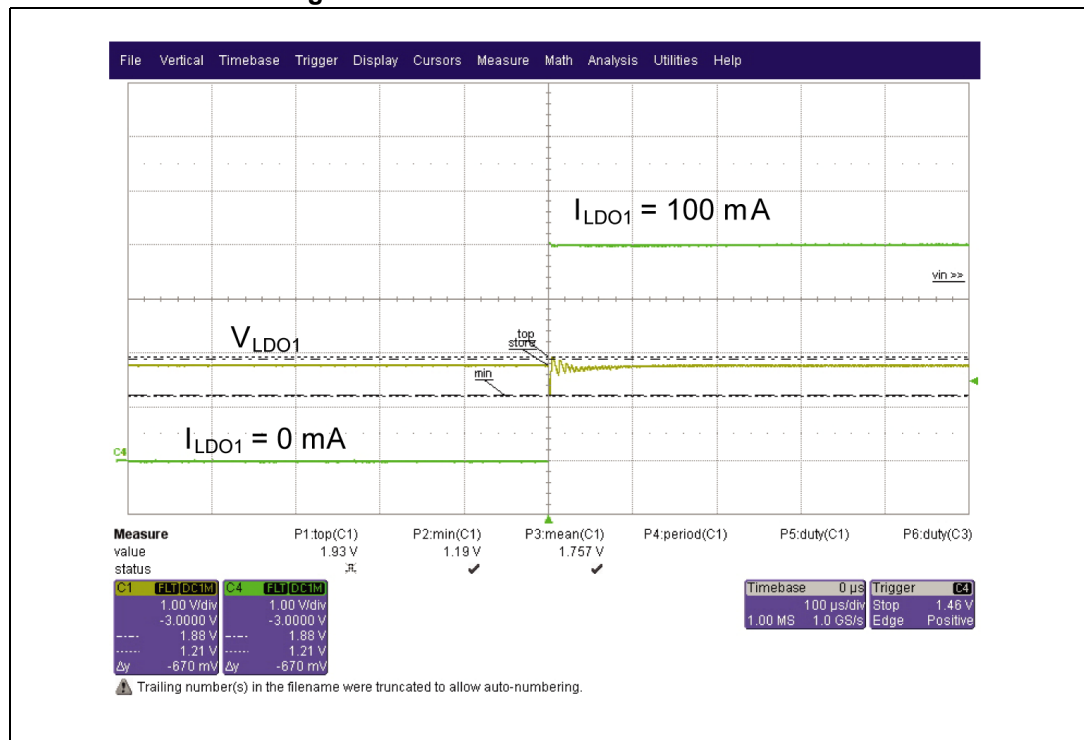
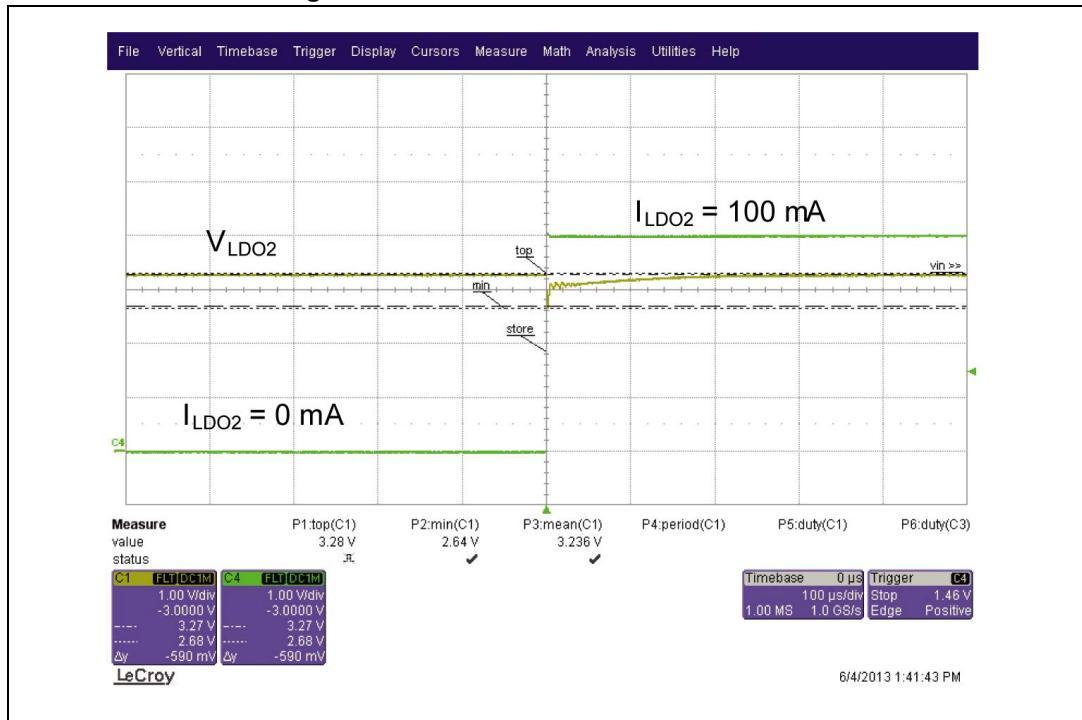


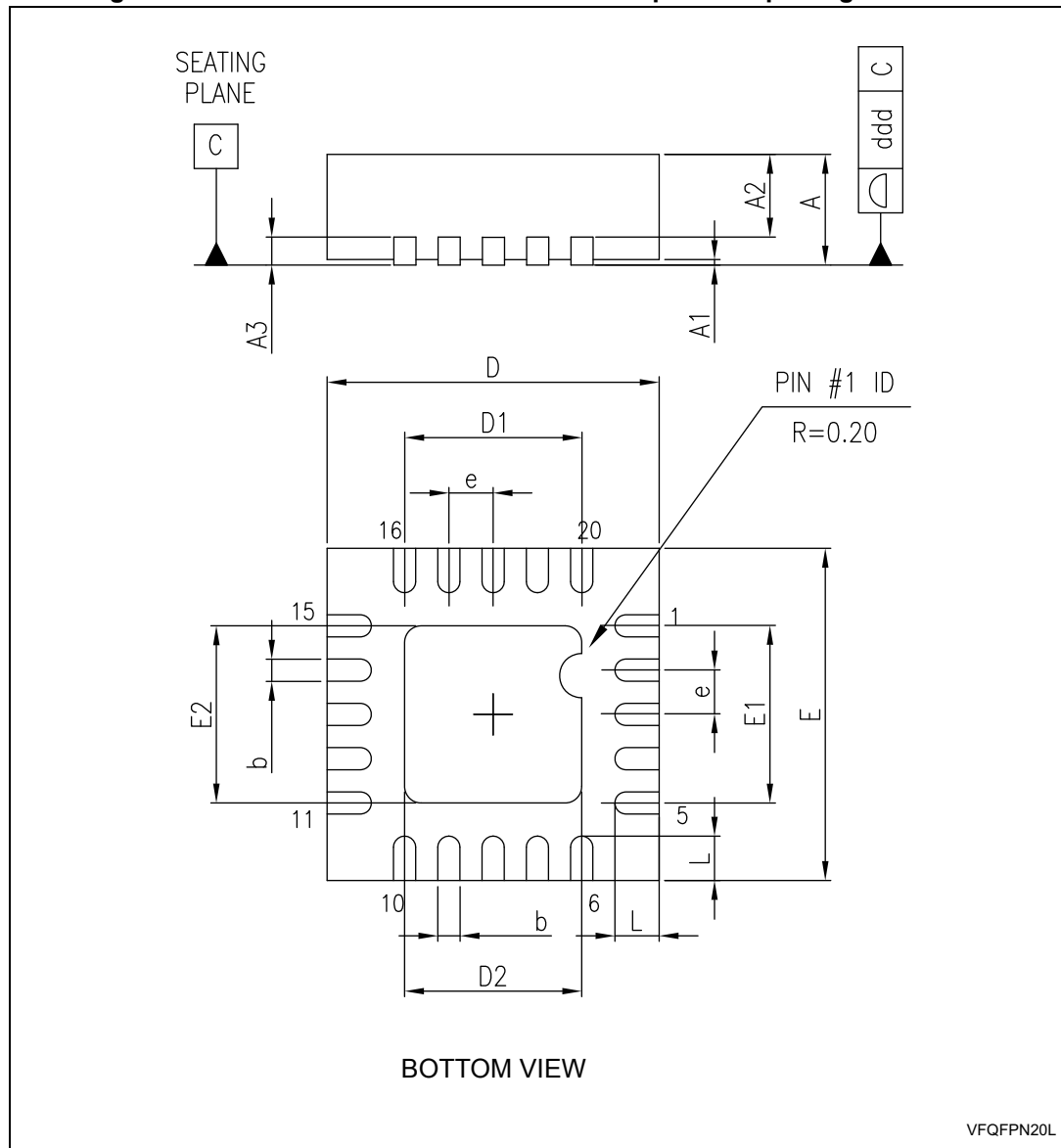
Figure 23. LDO2 turn on with 100 mA load



# 7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

Figure 24. VFQFPN20 3 x 3 x 1 mm - 20-lead pitch 0.4 package outline<sup>(1)</sup>



1. The pin #1 identifier must exist on the top surface of the package by using an indentation mark or another feature of the package body. Exact shape and size of this feature is optional.

Table 5. VFQFPN20 3 x 3 x 1 mm - 20-lead pitch 0.4 package mechanical data

Symbol	Dimensions (mm)			Note
	Min.	Typ.	Max.	
A	0.80	0.90	1.00	(1)
A1		0.02	0.05	
A2		0.65	1.00	
A3		0.20		
b	0.15	0.20	0.25	
D	2.85	3.00	3.15	
D1		1.60		
D2	1.50	1.60	1.70	
E	2.85	3.00	3.15	
E1		1.60		
E2	1.50	1.60	1.70	
e	0.35	0.40	0.45	
L	0.30	0.40	0.50	
ddd			0.07	

1. "VFQFPN" stands for "Thermally Enhanced Very thin Fine pitch Quad Packages No lead".  
Very thin:  $0.80 < A \leq 1.00$  mm / fine pitch:  $e < 1.00$  mm.

Figure 25. WLCSP20, die and pads position (top view)

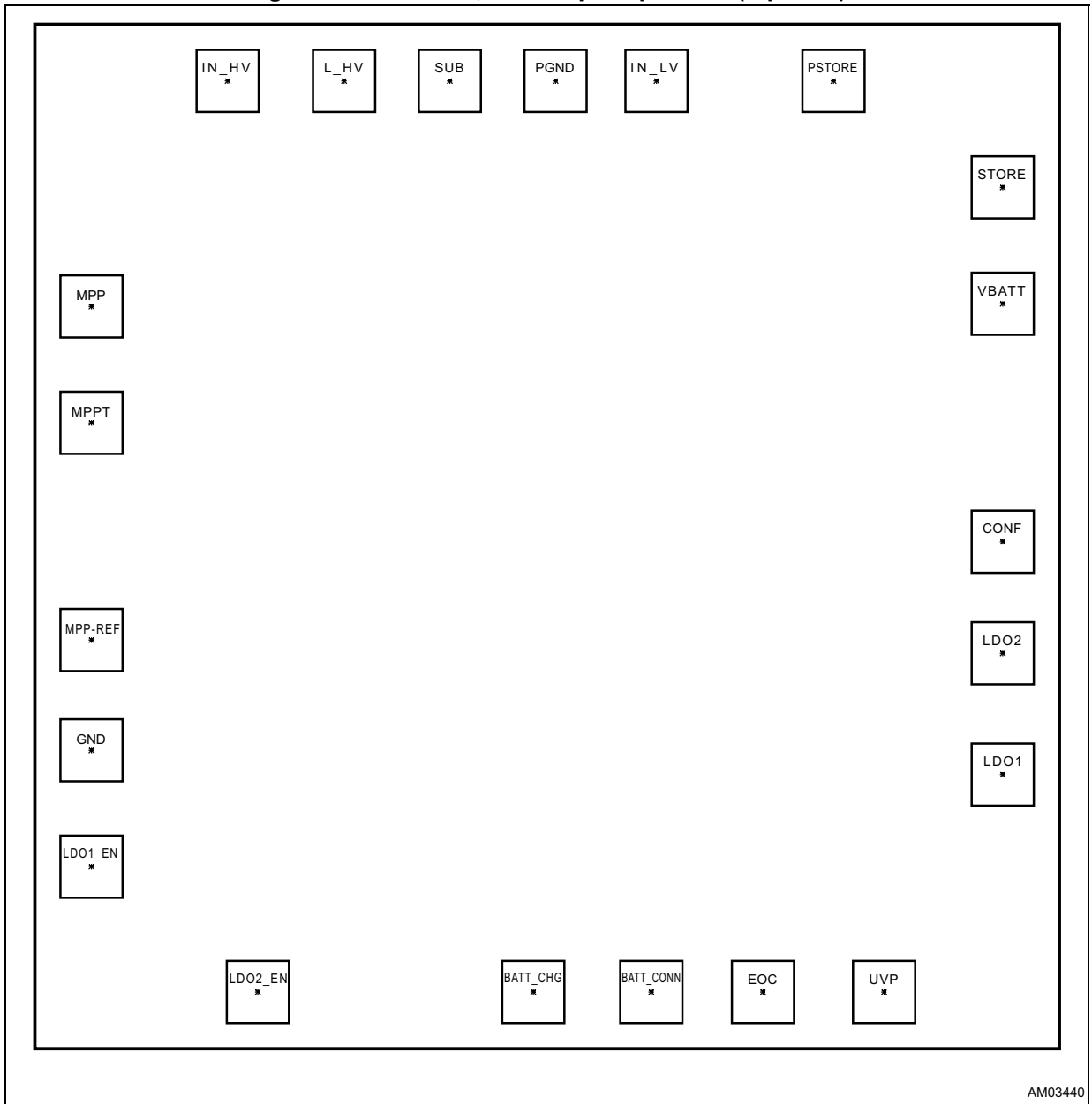


Table 6. WLCSP20, die pads coordinates and pads size

Pad name	X position [ $\mu\text{m}$ ]	Y position [ $\mu\text{m}$ ]	Pad dimension [ $\mu\text{m}$ ]
IN_HV	-416.55	594.09	81.05 x 81.05
L_HV	-264.75	594.09	
SUB	-126.87	594.09	
PGND	10.99	594.09	
IN_LV	142.65	594.09	
PSTORE	373.43	594.09	
STORE	594.09	455.22	
BATT	594.09	303.42	
CONF	594.09	-6.9	
LDO2	594.09	-152.33	
LDO1	594.09	-310.59	
UVP	439.39	-594.09	
EOC	281.45	-594.09	
BATT_OK	135.88	-594.09	
BATT_CHG	-18.03	-594.09	
LDO2_EN	-377.15	-594.09	
LDO1_EN	-594.09	-430.77	
GND	-594.09	-278.97	
MPP_REF	-594.09	-135.06	
MPP_SET	-594.09	148.12	
MPP	-594.09	299.92	

## 8 Ordering information

**Table 7. Device summary**

Order code	Op. temp. range (°C)	Package	Packing
SPV1050T	-40 to 85	VFQFPN 3 x 3 x 1 mm 20L	Tube
SPV1050TTR	-40 to 85	VFQFPN 3 x 3 x 1 20L	Tape and reel
SPV1050-WST	-40 to 85	WLCSP20	Tested waffle pack or sticky foil

## 9 Revision history

**Table 8. Document revision history**

Date	Revision	Changes
25-Nov-2013	1	Initial release.
28-Aug-2014	2	Document status promoted from preliminary data to production data, with comprehensive update of electrical characteristics and graphic content throughout the document.
18-Dec-2014	3	Document status corrected to reflect current phase of product development.

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