UT54ACS162245SLV

Schmitt CMOS 16-bit Bidirectional MultiPurpose Low Voltage Transceiver
Datasheet

September, 2014

AEROFLEX
A passion for performance.

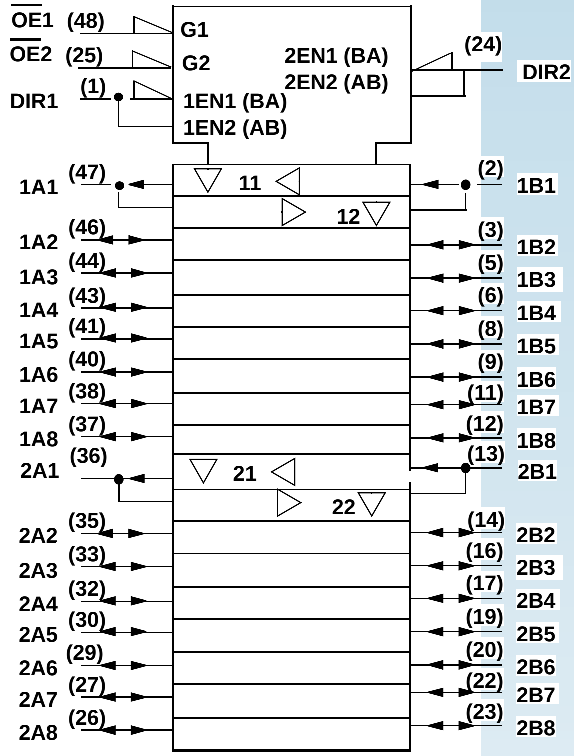
FEATURES

- Voltage translation
  - 3.3V bus to 2.5V bus
  - 2.5V bus to 3.3V bus
- Cold sparing all pins
- 0.25μ CMOS
- Operational environment
  - Total dose: 300Krad(Si) and 1Mrad(Si)
  - Single Event Latchup immune
- High speed, low power consumption
- Schmitt trigger inputs to filter noisy signals
- Cold and Warm Spare - all outputs
- Available QML Q or V processes
- Standard Microcircuit Drawing 5962-02543
- Package:
  - 48-lead flatpack, 25 mil pitch (.390 x .640), wgt 1.4 Grams

DESCRIPTION

The 16-bit wide UT54ACS162245SLV MultiPurpose low voltage transceiver is built using Aeroflex's epitaxial CMOS technology and is ideal for space applications. This high speed, low power UT54ACS162245SLV low voltage transceiver is designed to perform multiple functions including: asynchronous two-way communication, Schmitt input buffering, voltage translation, warm and cold sparing. With V_{DD} equal to zero volts, the UT54ACS162245SLV outputs and inputs present a minimum impedance of 1MΩ making it ideal for "cold spare" applications. Balanced outputs and low "on" output impedance make the UT54ACS162245SLV well suited for driving high capacitance loads and low impedance backplanes. The UT54ACS162245SLV enables system designers to interface 2.5 volt CMOS compatible components with 3.3 volt CMOS components. For voltage translation, the A port interfaces with the 2.5 volt bus; the B port interfaces with the 3.3 volt bus. The direction control (DIRx) controls the direction of data flow. The output enable ($\overline{OE}$x) overrides the direction control and disables both ports. These signals can be driven from either port A or B. The direction and output enable controls operate these devices as either two independent 8-bit transceivers or one 16-bit transceiver.

LOGIC SYMBOL

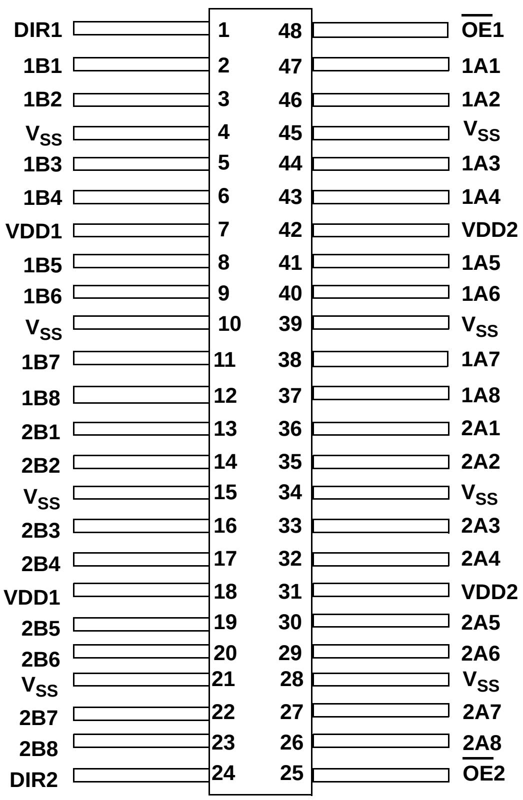


PIN DESCRIPTION

Pin Names	Description
$\overline{OE}$x	Output Enable Input (Active Low)
DIRx	Direction Control Inputs
xAx	Side A Inputs or 3-State Outputs (2.5V Port)
xBx	Side B Inputs or 3-State Outputs (3.3V Port)

PINOUTS

48-Lead Flatpack
Top View



POWER TABLE

Port B	Port A	OPERATION
3.3 Volts	2.5 Volts	Voltage Translator
3.3 Volts	3.3 Volts	Non Translating
2.5 Volts	2.5 Volts	Non Translating

FUNCTION TABLE

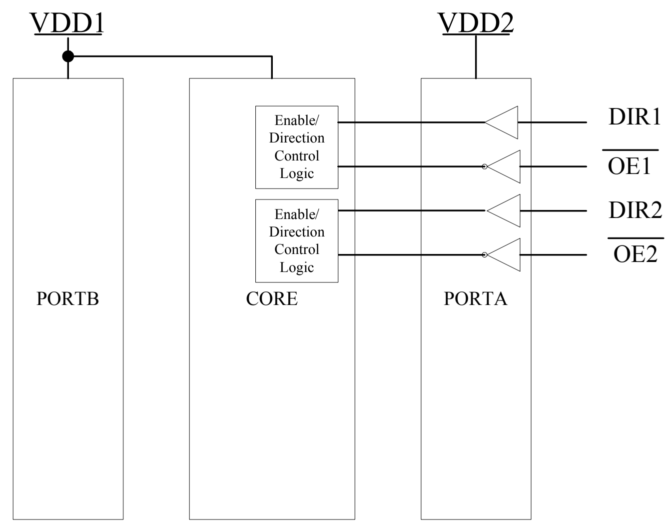
ENABLE $\overline{OEx}$	DIRECTION DIRx	OPERATION
L	L	B Data To A Bus
L	H	A Data To B Bus
H	X	Isolation

Power Application Guidelines

For proper operation, connect power to all V_{DD} pins and ground all V_{SS} pins (i.e., no floating V_{DD} or V_{SS} supply pins). If V_{DD1} and V_{DD2} are not powered up together, then V_{DD2} should be powered up first to ensure proper control of output enable (/OEx) and direction control (DIRx). Control of the outputs /OEx and DIRx pins is not guaranteed until V_{DD2} reaches 1.5 +/-5%. During normal operation of the device, after power up, insure $V_{DD1} \geq V_{DD2}$.

Power Up Sequence

Users should power up V_{DD2} before V_{DD1} because the DIRx and /OEx pins on the UT54ACS162245SLV are powered by V_{DD2}. If V_{DD1} is powered on first, V_{DD2} must be powered on within 1 second of V_{DD1} reaching 1.5V +/-5%. An elevated V_{DD1} supply current up to 150mA may occur when V_{DD1} > 1.5V+/5% and V_{DD2} < 1.5V +/-5%.



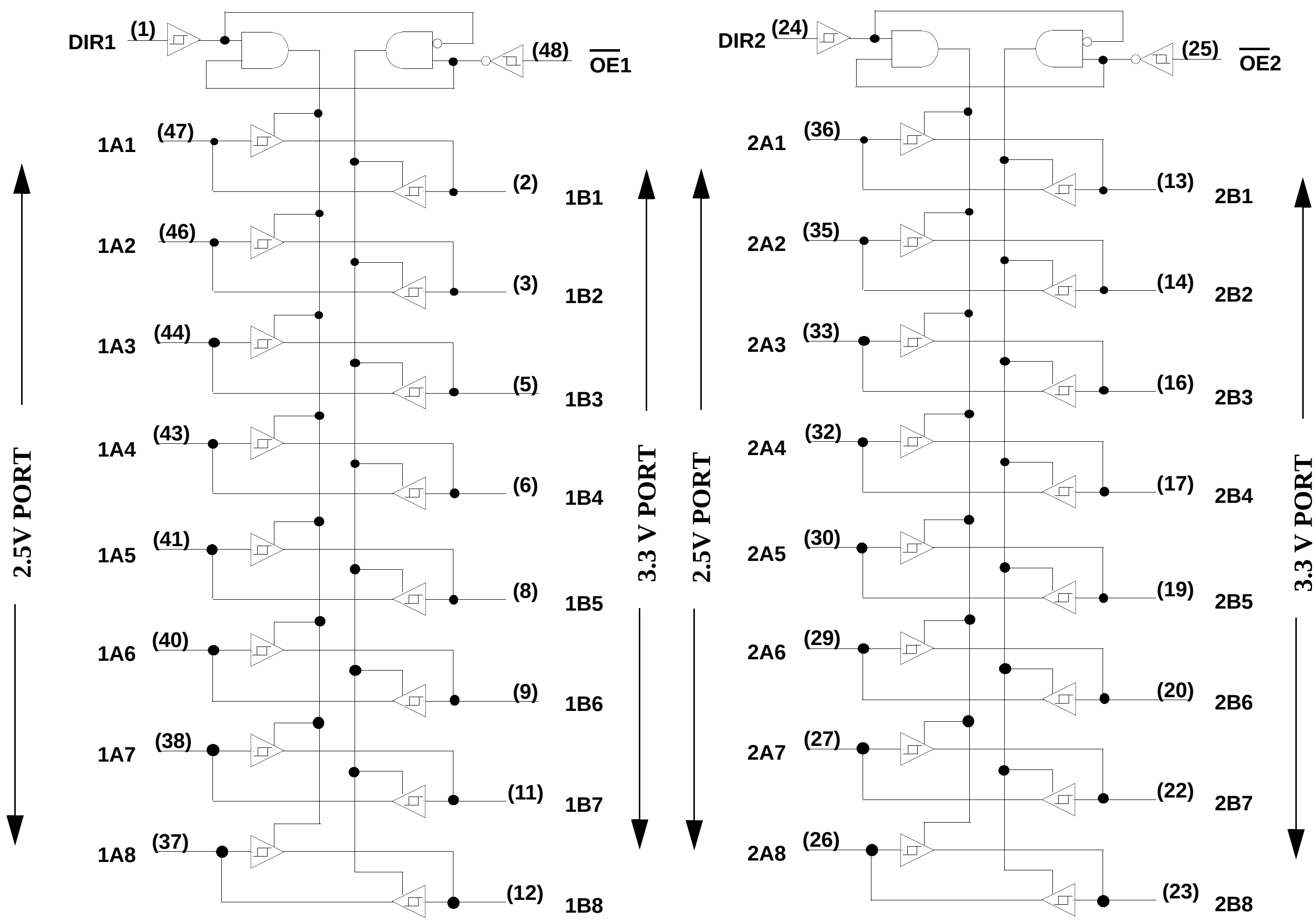
Warm Spare

Once the UT54ACS162245SLV is powered up with $V_{DD1} \geq V_{DD2}$, the application may place the device into "Warm Spare" mode by driving EITHER supply to V_{SS} +/- 0.25V with a maximum 1kΩ impedance between V_{DDx} and V_{SS}. While in Warm Spare, the device places all outputs into a high impedeance state (see DC electrical parameters, Iws).

Cold Spare

The UT54ACS162245SLV places the device into "Cold Spare" mode when BOTH supplies are set to V_{SS} +/- 0.25V with a maximum 1KΩ impedance between V_{DDx} and V_{SS}. While in Cold Spare, the device places all outputs into a high impedeance state (see DC electrical parameters, Ics).

LOGIC DIAGRAM



OPERATIONAL ENVIRONMENT [1]

PARAMETER	LIMIT	UNITS
Total Dose	1.0E5	rad(Si)
SEL Latchup	>113	MeV-cm^2/mg
Neutron Fluence (Note 2)	1.0E14	n/cm^2

Notes:
1. Logic will not latchup during radiation exposure within the limits defined in the table.
2. Not tested, inherent to CMOS technology.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	LIMIT (Mil only)	UNITS
$V_{I/O}$ (Note 2)	Voltage any pin	-.3 to V_{DD1} +.3	V
V_{DD1}	Supply voltage	-0.3 to 4.0	V
V_{DD2}	Supply voltage	-0.3 to 4.0	V
T_{STG}	Storage Temperature range	-65 to +150	°C
T_J (Note 3)	Maximum junction temperature	+150	°C
Θ_{JC}	Thermal resistance junction to case	20	°C/W
I_I	DC input current	±10	mA
P_D	Maximum power dissipation	1	W

Note:
1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, functional operation of the device at these or any other conditions beyond limits indicated in the operational sections is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and performance.
2. For Cold Spare mode (V_{DD1}=VSS, V_{DD2}=VSS), $V_{I/O}$ may be -0.3V to the maximum recommended operating level of V_{DD1} +0.3V.
3. Maximum junction temperature may be increased to +175°C during burn-in and life test.

DUAL SUPPLY OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMIT	UNITS
V_{DD1}	Supply voltage	2.3 to 3.6	V
V_{DD2}	Supply voltage	2.3 to 3.6	V
V_{IN}	Input voltage any pin	0 to V_{DD1}	V
T_C	Temperature range	-55 to + 125	°C

DC ELECTRICAL CHARACTERISTICS [1]
($-55°C < T_C < +125°C$)

SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNIT
V_T+	Schmitt Trigger, positive going threshold[2]	V_{DD} from 2.3 to 3.6		$.7V_{DD}$	V
V_T-	Schmitt Trigger, negative going threshold[2]	V_{DD} from 2.3 to 3.6	$.3V_{DD}$		V
V_{H1}	Schmitt Trigger range of hysteresis[9]	V_{DD} from 3.0 to 3.6	0.5		V
V_{H2}	Schmitt Trigger range of hysteresis[9]	V_{DD} from 2.3 to 2.7	0.4		V
I_{IN}	Input leakage current[9]	V_{DD} from 2.7 to 3.6 $V_{IN} = V_{DD}$ or V_{SS}	-1	3	µA
I_{OZ}	Three-state output leakage current[9]	V_{DD} from 2.7 to 3.6 $V_{IN} = V_{DD}$ or V_{SS}	-1	3	µA
I_{CS}	Cold sparing input leakage current[3,11]	$V_{IN} = 3.6$ $V_{DD} = V_{SS}$	-5	5	µA
I_{WS}	Warm sparing input leakage current[3,11]	$V_{IN} = V_{SS}$ or V_{DD}, $V_{DD1} = 0$, $V_{DD2} = V_{DD}$ or $V_{DD1} = V_{DD}$, $V_{DD2} = 0$	-5	5	µA
I_{OS1}	Short-circuit output current [5, 10]	$V_O = V_{DD}$ or V_{SS} V_{DD} from 3.0 to 3.6	-200	200	mA
I_{OS2}	Short-circuit output current [5, 10]	$V_O = V_{DD}$ or V_{SS} V_{DD} from 2.3 to 2.7	-100	100	mA
V_{OL1}	Low-level output voltage[9]	I_{OL}= 8mA I_{OL}= 100µA $V_{DD} = 3.0$		0.4 0.2	V
V_{OL2}	Low-level output voltage[9]	I_{OL}= 8mA I_{OL}= 100µA $V_{DD} = 2.3$		0.4 0.2	V
V_{OH1}	High-level output voltage[9]	I_{OH}= -8mA I_{OH}= -100µA $V_{DD} = 3.0$	V_{DD} - 0.7 V_{DD} - 0.2		V
V_{OH2}	High-level output voltage[9]	I_{OH}= -8mA I_{OH}= -100µA $V_{DD} = 2.3$	V_{DD} - 0.7 V_{DD} - 0.2		V

DC ELECTRICAL CHARACTERISTICS [1]

(-55°C < T_C < +125°C)

SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNIT
P_{total1}	Power dissipation[4,6,7]	C_L = 40pF V_{DD} from 3.0V to 3.6V		6.2	mW/ MHz
P_{total2}	Power dissipation[4,6,7]	C_L = 40pF V_{DD} from 2.3V to 2.7V		3	MHz
I_{DD}	Standby Supply Current V_{DD1} or V_{DD2}	$V_{IN} = V_{DD}$ or V_{SS} V_{DD} = 3.6V			
	Pre-Rad 25°C	$\overline{OE} = V_{DD}$		10	µA
	Pre-Rad -55°C to +125°C	$\overline{OE} = V_{DD}$		475	µA
	Post-Rad 25°C	$\overline{OE} = V_{DD}$		15	mA
C_{IN}	Input Capacitance[8]	*f* = 1MHz @ 0V V_{DD} from 2.3V to 3.6V		15	pF
C_{out}	Output Capacitance[8]	*f* = 1MHz @ 0V V_{DD} from 2.3V to 3.6V		15	pF
POR	V_{DD1} & V_{DD2} Power-On[4,13]	V_{DD1} or V_{DD2} Zero Volt Offset		250	mV
		V_{DD1} and V_{DD2} Rise-Time[12]		500	mS

Notes:

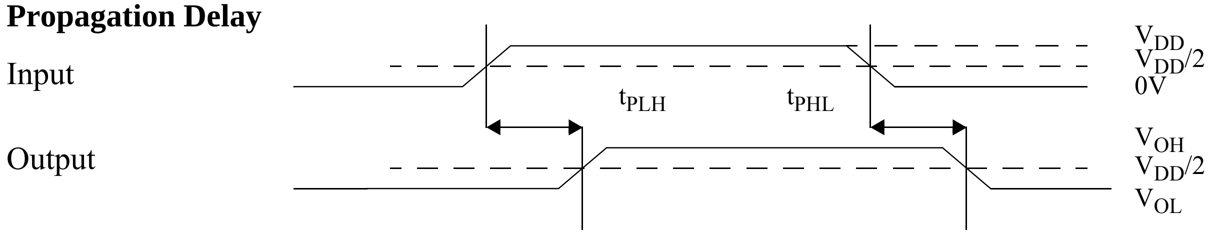
1. All specifications valid for radiation dose ≤ 1E5 rad(Si) per MIL-STD-883, Method 1019.
2. Functional tests are conducted in accordance with MIL-STD-883 with the following input test conditions: $V_{IH} = V_{IH}$(min) + 20%, - 0%; $V_{IL} = V_{IL}$(max) + 0%, -50%, as specified herein, for TTL, CMOS, or Schmitt compatible inputs. Devices may be tested using any input voltage within the above specified range, but are guaranteed to V_{IH}(min) and V_{IL}(max).
3. All combinations of $\overline{OE}$x and DIRx
4. Guaranteed by characterization.
5. Not more than one output may be shorted at a time for maximum duration of one second.
6. Power does not include power contribution of any CMOS output sink current.
7. Power dissipation specified per switching output.
8. Capacitance measured for initial qualification and when design changes may affect the value. Capacitance is measured between the designated terminal and V_{SS} at frequency of 1MHz and a signal amplitude of 50mV rms maximum.
9. Guaranteed; tested on a sample of pins per device.
10. Supplied as a design limit, but not guaranteed or tested.
11. Zero Volts is defined as 0.0 Volts +/- 0.25Volts.
12. V_{DD1} and V_{DD2} Voltage rise is monotonic.
13. Rise time measured from V_{DD} @ Zero Volts to V_{DD} @ greater than 2.3 V.

AC ELECTRICAL CHARACTERISTICS[1] (Port B = 3.3 Volt, Port A = 2.5 Volt)
(V_{DD1} = 3.0V to 3.6V; V_{DD2} = 2.3V to 2.7V, -55°C < T_C < +125°C)

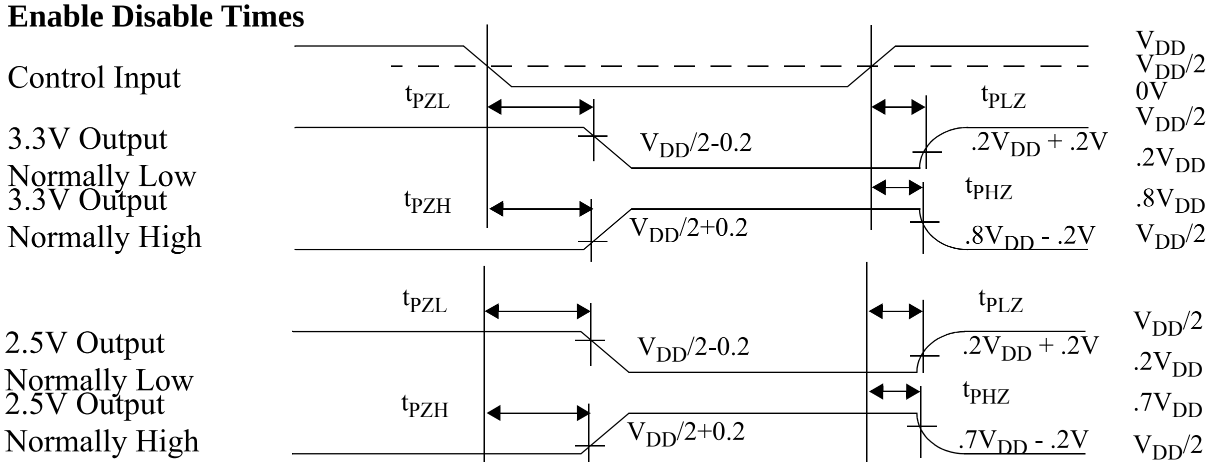
SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNIT
t_{PLH}	Propagation delay Data to Bus	2	10	ns
t_{PHL}	Propagation delay Data to Bus	2	10	ns
t_{PZL}	Output enable time $\overline{OE}$x to Bus	2	12	ns
t_{PZH}	Output enable time $\overline{OE}$x to Bus	2	12	ns
t_{PLZ}	Output disable time $\overline{OE}$x to Bus high impedance	2	15	ns
t_{PHZ}	Output disable time $\overline{OE}$x to Bus high impedance	2	15	ns
t_{PZL}[2]	Output enable time DIRx to Bus	2	12	ns
t_{PZH}[2]	Output enable time DIRx to Bus	2	12	ns
t_{PLZ}[2]	Output disable time DIRx to Bus high impedance	2	15	ns
t_{PHZ}[2]	Output disable time DIRx to Bus high impedance	2	15	ns
t_{SLH}[3]	Skew between outputs (40pF +/- 10 pF on each output)	0	900	ps
t_{SHL}[3]	Skew between outputs (40pF +/- 10 pF on each output)	0	900	ps

Notes:
1. All specifications valid for radiation dose ≤ 1E5 rad(Si) per MIL-STD-883, Method 1019.
2. DIRx to bus times are guaranteed by design, but not tested. $\overline{OE}$x to bus times are tested
3. Output skew is defined as a comparison of any two output transitions high-to-low vs. high-to-low and low-to-high vs. low-to-high

Propagation Delay



Enable Disable Times



AC ELECTRICAL CHARACTERISTICS[1] (Port A = Port B, 3.3 Volt Operation)
(V_{DD1} = 3.0 to 3.6V; V_{DD2} = 3.0V to 3.6V, -55°C < T_C < +125°C)

SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNIT
t_{PLH}	Propagation delay Data to Bus	2	7.5	ns
t_{PHL}	Propagation delay Data to Bus	2	7.5	ns
t_{PZL}	Output enable time $\overline{OE}$x to Bus	2	10	ns
t_{PZH}	Output enable time $\overline{OE}$x to Bus	2	10	ns
t_{PLZ}	Output disable time $\overline{OE}$x to Bus high impedance	2	12	ns
t_{PHZ}	Output disable time $\overline{OE}$x to Bus high impedance	2	12	ns
t_{PZL}[2]	Output enable time DIRx to Bus	2	10	ns
t_{PZH}[2]	Output enable time DIRx to Bus	2	10	ns
t_{PLZ}[2]	Output disable time DIRx to Bus high impedance	2	12	ns
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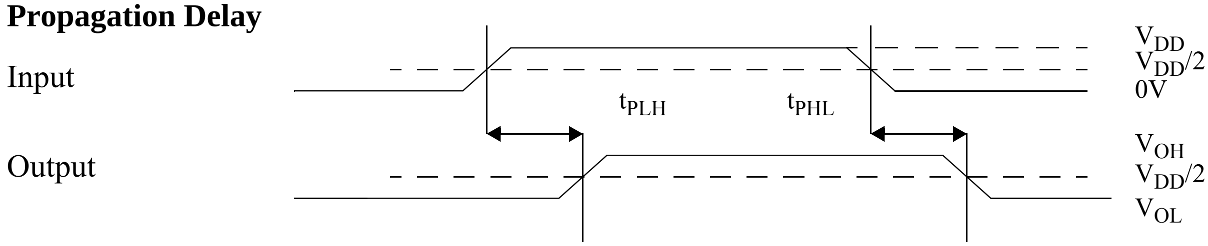
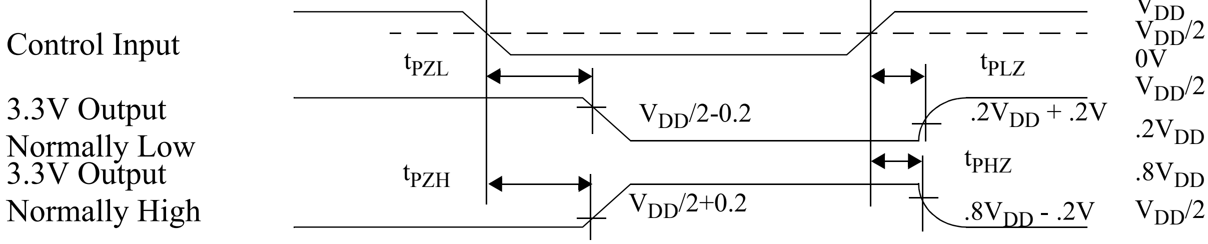
Notes:
1. All specifications valid for radiation dose ≤ 1E5 rad(Si) per MIL-STD-883, Method 1019.
2. DIRx to bus times are guaranteed by design, but not tested. $\overline{OE}$x to bus times are tested
3. Output skew is defined as a comparison of any two output transitions high-to-low vs. high-to-low and low-to-high vs. low-to-high

Propagation Delay



Enable Disable Times



AC ELECTRICAL CHARACTERISTICS[1] (Port A = Port B, 2.5 Volt Operation)
(V_{DD1} = 2.3V TO 2.7V; V_{DD2} = 2.3V to 2.7V, -55°C < T_C < +125°C)

SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNIT
t_{PLH}	Propagation delay Data to Bus	2	10	ns
t_{PHL}	Propagation delay Data to Bus	2	10	ns
t_{PZL}	Output enable time $\overline{OE}$x to Bus	2	12	ns
t_{PZH}	Output enable time $\overline{OE}$x to Bus	2	12	ns
t_{PLZ}	Output disable time $\overline{OE}$x to Bus high impedance	2	15	ns
t_{PHZ}	Output disable time $\overline{OE}$x to Bus high impedance	2	15	ns
t_{PZL}[2]	Output enable time DIRx to Bus	2	12	ns
t_{PZH}[2]	Output enable time DIRx to Bus	2	12	ns
t_{PLZ}[2]	Output disable time DIRx to Bus high impedance	2	15	ns
t_{PHZ}[2]	Output disable time DIRx to Bus high impedance	2	15	ns
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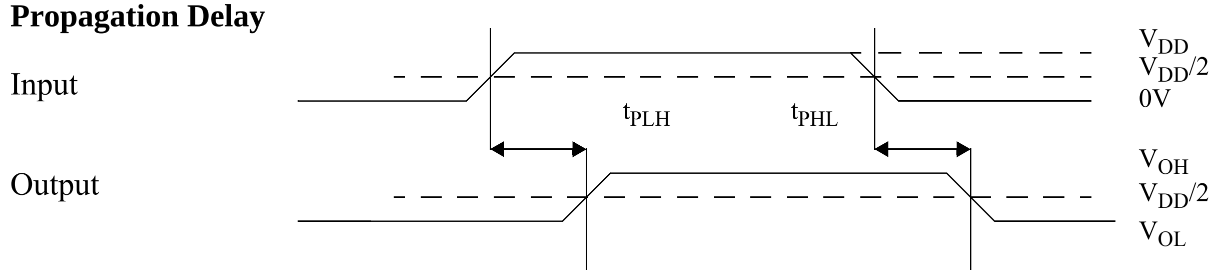
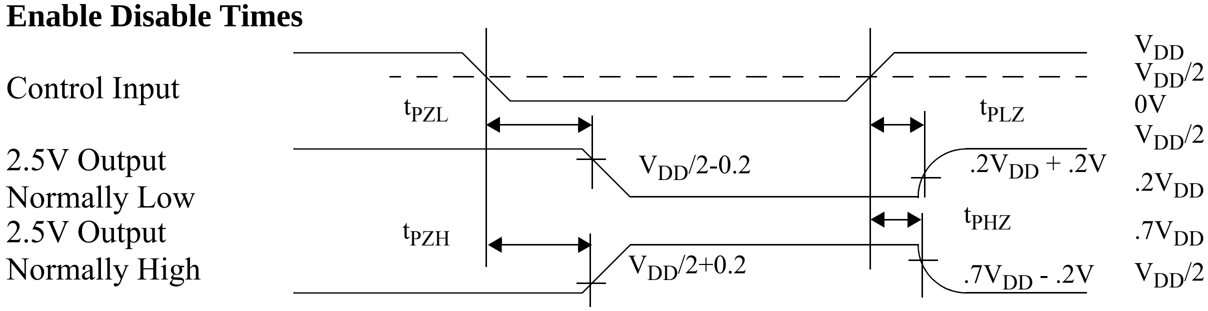
t_{SHL}[3]	Skew between outputs (40pF +/- 10 pF on each output)	0	900	ps

Notes:
1. All specifications valid for radiation dose ≤ 1E5 rad(Si) per MIL-STD-883, Method 1019.
2. DIRx to bus times are guaranteed by design, but not tested. $\overline{OE}$x to bus times are tested
3. Output skew is defined as a comparison of any two output transitions high-to-low vs. high-to-low and low-to-high vs. low-to-high

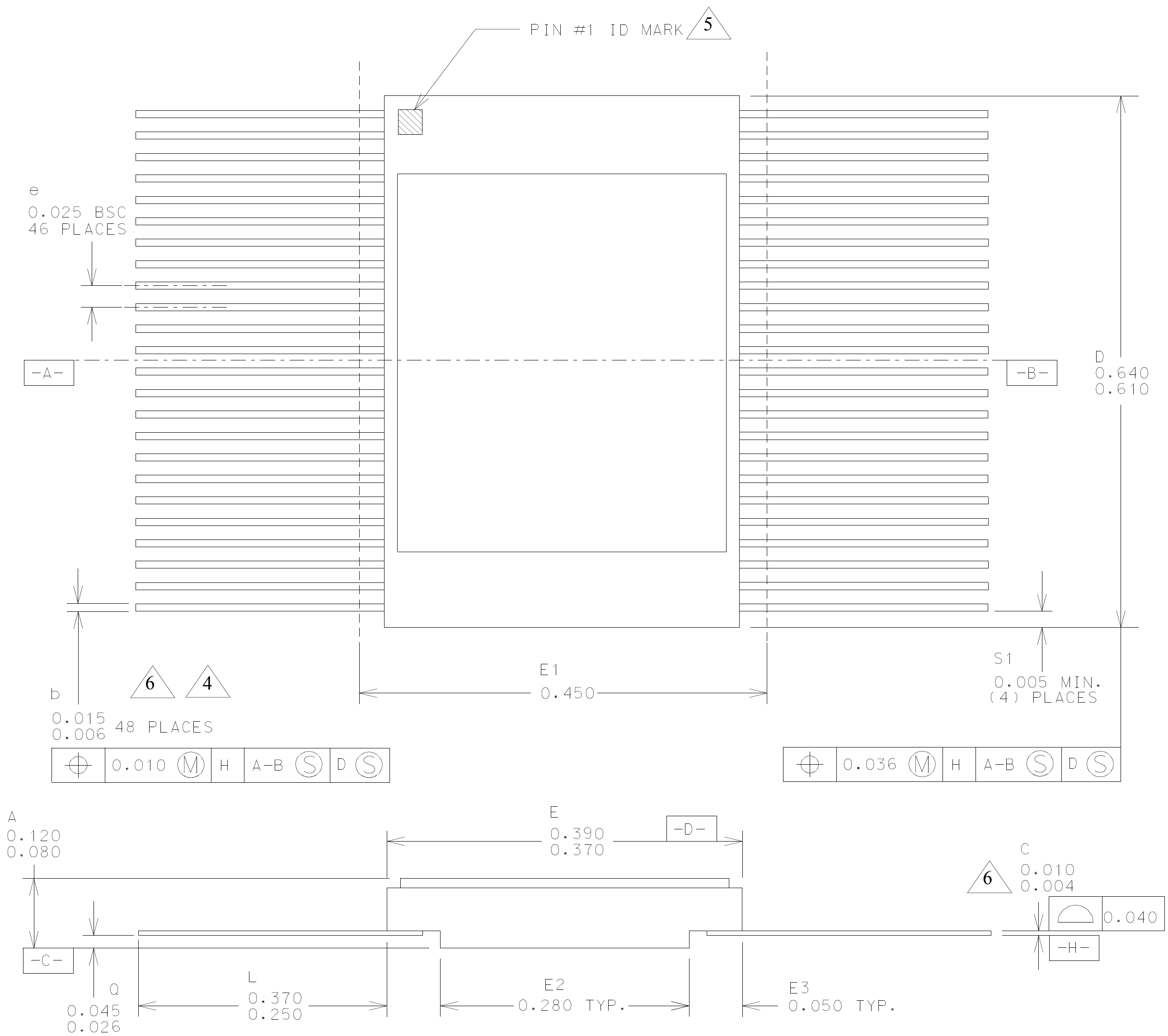
Propagation Delay



Enable Disable Times



PACKAGE



1. All exposed metalized areas are gold plated over electroplated nickel per MIL-PRF-38535.
2. The lid is electrically connected to VSS.
3. Lead finishes are in accordance with MIL-PRF-38535.
4. Lead position and colanarity are not measured.
5. ID mark symbol is vendor option.
6. With solder, increase maximum by 0.003.

Figure 1. 48-Lead Flatpack

ORDERING INFORMATION

UT54ACS162245SLV: SMD

5962 R 02543 01 * * *

Lead Finish:
(C) = Gold
(A) = Solder

Case Outline:
(X) = 48 lead FP

Class Designator:
(Q) = Class Q
(V) = Class V

Device Type
(01) = 16-bit MultiPurpose Low Voltage Transceiver

Drawing Number: 02543

Total Dose:
(R) = 1E5 rad(Si)
(F) = 3E5 rad(Si)
(G) = 5E5 rad(Si)
(H) = 1E6 rad(Si)

Federal Stock Class Designator

Notes:
1. Total dose radiation must be specified when ordering. QML Q and QML V not available without radiation hardening.

UT54ACS162245SLV

UT54 *** ****** * * *

Lead Finish:
(C) = Gold
(A) = Solder

Screening:
(C) = HiRel Temp
(P) = Prototype

Package Type:
(U) = 48-lead FP

Part Number:
(162245SLV) = 16-bit MultiPurpose Low Voltage Transceiver

I/O Type:
(ACS)= CMOS compatible I/O Level

Aeroflex Core Part Number

Notes:
1. HiRel Temperature Range flow per Aeroflex Colorado Springs Manufacturing Flows Document. Devices are tested -55C, room temp, and 125C. Radiation neither tested nor guaranteed.
2. Prototype flow per Aeroflex Colorado Springs Manufacturing Flows Document Tested at 25C only. Lead finish is gold only. Radiation neither tested nor guaranteed.

Aeroflex Colorado Springs - Datasheet Definition

Advanced Datasheet - Product In Development

Preliminary Datasheet - Shipping Prototype

Datasheet - Shipping QML & Reduced Hi-Rel

This product is controlled for export under the Export Administration Regulations (EAR). A license from the U.S. Government is required prior to the export of this product from the United States.

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A passion for performance.

Our passion for performance is defined by three attributes represented by these three icons: solution-minded, performance-driven and customer-focused