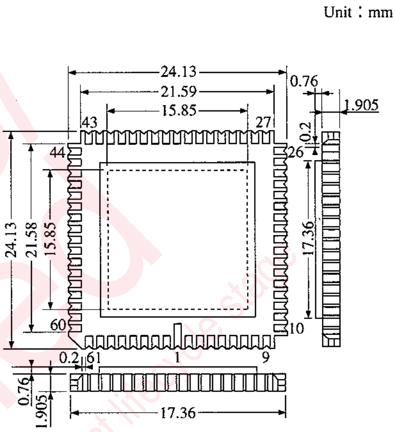
AN8101

Super High speed Low Power Consumption 8-Bit A/D Converter

■ Overview

The AN8101 is a 8-bit A/D converter for measurement which uses the high frequency bipolar process to suppress the power consumption.

It can operate with single power supply of –5.2V and maximum conversion rate of 500 MSPS, realizing the low error rate.



68-pin LCC Package (QFN068-C-S950)

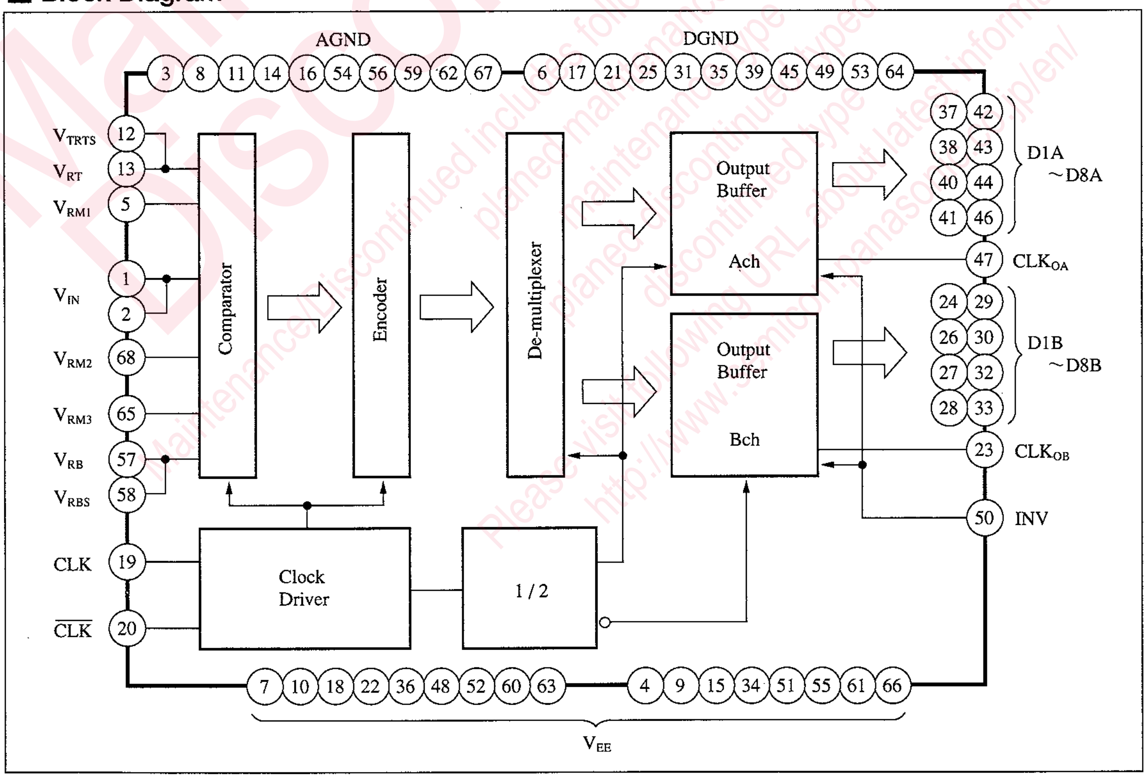
■ Features

- 8-bit resolution
- Super high speed : maximum conversion rate of 500 MSPS (min.)
- Low error rate : 10^{-12} tps or lower
- Low input capacitance : 17pF
- Input/Output form : ECL level

■ Application Field

- Measuring equipment such as digital oscilloscope
- Radar

■ Block Diagram



■ Absolute Maximum Rating (Ta=25℃)

Parameter	Symbol	Rating	Unit
Supply voltage	V_{EE}	−6.0 to +0.5	V
Analogue input voltage	V_{IN}	V_{EE} to +0.5	V
Digital input voltage	$V_{CLK}/\overline{V_{CLK}}$	V_{EE} to +0.5	V
Digital output current	$I_{CLKOA}/I_{CLKOB}/I_{D1A}$ to I_{D8B}	−20	mA
Reference resistive current	I_{RT}/I_{RB}	−20/+20	mA
Reference input voltage	V_{RB}/V_{RT}	V_{EE} to +0.5	V
Power dissipation	P_D	1582*	mW
Operating ambient temperature	T_{opr}	0 to 75	℃
Storage temperature	T_{stg}	−55 to +150	℃

* Ta=25℃

■ Recommended Operating Conditions (Ta=25℃)

Parameter	Symbol	min	typ	max	Unit
Negative supply voltage	V_{EE}	−5.4	−5.2	−5.0	V
Reference voltage	V_{RT}	—	0	—	V
	V_{RB}	—	−2.0	—	V
Analogue input voltage	V_{IN}	V_{RB}	—	V_{RT}	V
Digital input voltage	V_{IH}	—	−0.9	—	V
	V_{IL}	—	−1.7	—	V
Clock input pulse width *	t_H	—	1	—	ns

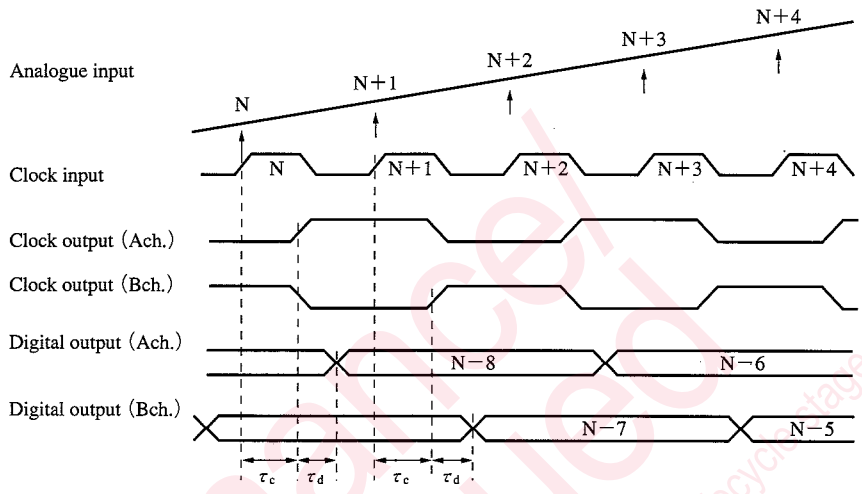
* f_{CLK}=500MHz

■ Electrical Characteristics (V_{EE}=−5.2V, Ta=25℃)

Parameter	Symbol	Condition	min	typ	max	Unit
Supply current	I_{EE}		−900	790	—	mA
Reference current	I_{RT}	V_{RT}=0V	—	6	12	mA
	I_{RB}	V_{RB}=−2.0V	−12	−6	—	mA
Input bias current	I_{IN}	V_{IN}=−1.0V	—	400	1000	μA
Clock input current	I_{IH}	V_{CLK}=−1.105V	—	—	20	μA
Digital output voltage	V_{OH}	R_L=100Ω TO V_T=−2.0V	−1.0	—	—	V
	V_{OL}		—	—	−1.6	V
Linearity error	E_L	$V_{IN}=2V_{p-p}$	—	—	±1.0	LSB
Differential linearity error	E_D	$V_{IN}=2V_{p-p}$	—	—	±0.5	LSB
Maximum conversion rate	F_{CMAX}		500	—	—	MHz
Input dynamic range			—	2	—	V_{p-p}
Equivalent input impedance *1	R_{IN}	V_{IN}=−1V	—	60	—	kΩ
Input capacitance *1	C_{IN}	V_{IN}=−1V	—	17	—	pF
Error rate *1		f_{CLK}=500MHz, f_{IN}=62.5MHz 8LSB or higher	—	—	10^{-12}	tps
Quantization noise *2	SINAD	f_{CLK}=500MHz, f_{IN}=50MHz	—	42	—	dB
		f_{CLK}=500MHz, f_{IN}=100MHz	—	35	—	dB
Input band *1	BW_F	−3dB	250	—	—	MHz
Clock duty *1		f_{CLK}=500MHz	40	50	60	%
Clock output delay *1	τ_c		(1.0)	1.2	(1.4)	ns
Digital output delay *1	τ_d		(0.4)	0.6	(0.8)	ns

*1 Design reference value but not guaranteed one
*2 Total harmonics distortion included

■ Timing Chart



■ Output Code

Step	Input signal	Digital output	
		INV=L	INV=H
	2.000VFS 7.8125mV STEP	M L 87654321	M L 87654321
000	−2.0000000	00000000	11111111
001	−1.9921875	00000001	11111110
.	.	.	.
.	.	.	.
127	−1.0078125	01111111	10000000
128	−1.0000000	10000000	01111111
.	.	.	.
.	.	.	.
254	−0.0078125	11111110	00000001
255	−0.0000000	11111111	00000000

Pin Descriptions

Pin No.	Symbol	Pin name	Standard waveform	Voltage level	Description
1 2	V_{IN}	Analogue input		0 to −2V	It is an input pin of analogue signal for A/D conversion circuit.
3, 8 11, 14 16, 54 56, 59 62, 67	AGND	Analogue ground		0V	Connect AGND and DGND with the possible lowest impedance at one point as near as possible to the chip.
4, 7 9, 10 15, 18 22, 34 36, 48 51, 52 55, 60 61, 63 66	V_{EE}	Negative power supply pin		−5.2V	Connect tantalum capacitor of several μF and ceramic capacitor of 0.1 μF as near as possible to this pin between this pin and AGND or DGND.
5 12 13 57 58 65 68	V_{RM1} V_{TRTS} V_{RT} V_{RB} V_{RBS} V_{RM3} V_{RM2}	Reference voltage middle point level Sense pin Reference voltage high level Reference voltage low level Sense pin, Reference voltage middle point level Reference voltage middle point level		−0.5V 0V 0V −2.0V −2.0V −1.0V −1.5V	It is used to set the reference voltage for comparator. Normally, V_{RT} is given 0V and V_{RB} is given −2V. Connect tantalum capacitor of several μF and ceramic capacitor of 0.1 μF in parallel between each pin and analogue ground. V_{RM} is provided for linearity compensation which gives middle point potential between V_{RT} and V_{RB}. However, it is normally opened.
6, 17 21, 25 31, 35 39, 45 49, 53 64	DGND	Digital ground		0V	Connect AGND and DGND with the possible lowest impedance at one point as near as possible to the chip.
19 20	CLK $\overline{CLK}$	Clock input	Refer to the timing chart	ECL	It is a clock for sampling. For their timing, refer to the timing chart.
23 47	CLK_{OB} CLK_{OA}	Clock output		ECL	It is a clock output pin of ECL level. With this signal, the digital output of A or B ch. can be latched.
24 26 27 28 29 30 32 33	D1B D2B D3B D4B D5B D6B D7B D8B	Bch. digital output (LSB) Bch. digital output Bch. digital output Bch. digital output Bch. digital output Bch. digital output Bch. digital output Bch. digital output (MSB)	Refer to the timing chart	ECL	It is an output pin of ECL Level.
37 38 40 41 42 43 44 46	D1A D2A D3A D4A D5A D6A D7A D8A	Ach. digital output (LSB) Ach. digital output Ach. digital output Ach. digital output Ach. digital output Ach. digital output Ach. digital output Ach. digital output (MSB)	Refer to the timing chart	ECL	It is an output pin of ECL level.
50	INV	Digital output reverse pin		ECL	Setting the INV pin to "H" level reverses all the data outputs (DIA~D8A, DIB~D8B). It operates synchronously with clock.

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