MN8357

Half Tone Processor(HTP)

■ Outline

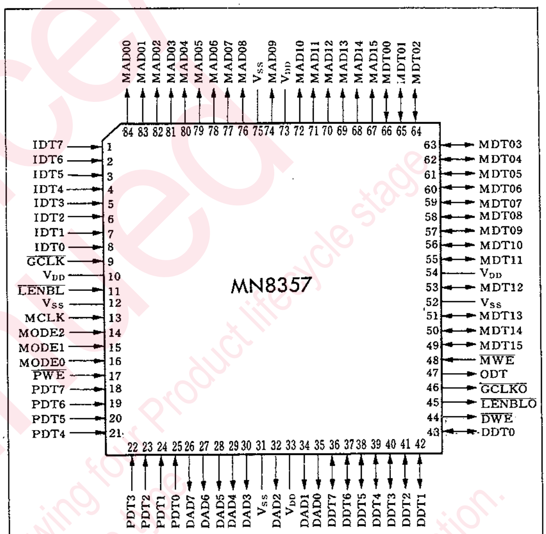
The half tone processor(HTP) MN8357 is an LSI which has a high-quality pseudo intermedicate toning (binary conversion)function, which output raster scan type multivalued image signals of facsimile and television signals to a binary output device such as Laser beam printer or static printer, and a moire eliminating function at the time of reading an image such as reticular point picture with periodicity

By combining with a scanner, the MN8357 can configure an advanced image input device which can handle various images such as character, pattern, reticular point picture, shaded picture, etc. as binary images.

■ Features

- Various pseudo intermediate tone processing function
  CAPIX 1(Character, line drawing, picture)
  CAPIX 2(Moire elimination only .... reticular point picture of printed matter, etc.)
  Texture dither(Various patterns enabled by an external loading system)(For example, concentrated type, distributed type, reticular point, etc.)
  Simple binary conversion
- Input data width and processing speed
  Max. 8 bits/pixel, Max. 350 ns/pixel

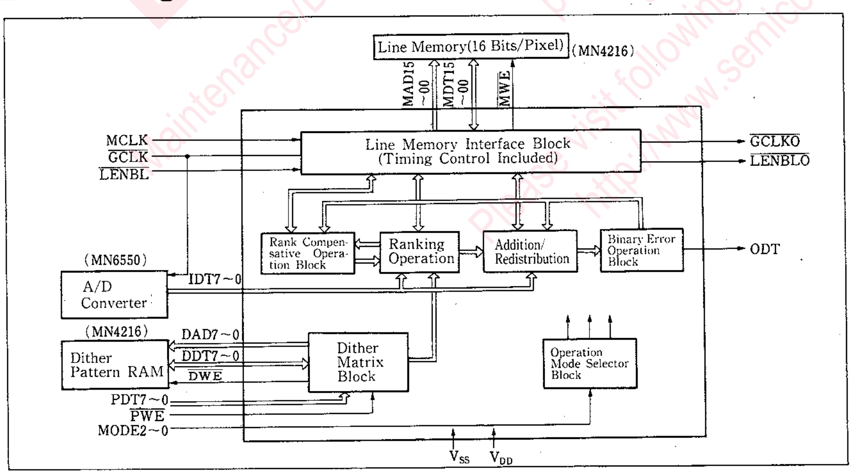
■ Pin Configuration


MN8357
IDT7 1
IDT6 2
IDT5 3
IDT4 4
IDT3 5
IDT2 6
IDT1 7
IDT0 8
GCLK 9
VDD 10
LENBL 11
VSS 12
MCLK 13
MODE2 14
MODE1 15
MODE0 16
PWE 17
PDT7 18
PDT6 19
PDT5 20
PDT4 21
PDT3 PDT2 PDT1 PDT0 DAD7 DAD6 DAD5 DAD4 DAD3 VSS DAD2 VDD DAD1 DAD0 DDT7 DDT6 DDT5 DDT4 DDT3 DDT2 DDT1
43 DDT0
44 DWE
45 LENBLO
46 GCLKO
47 ODT
48 MWE
49 MDT15
50 MDT14
51 MDT13
52 VSS
53 MDT12
54 VDD
55 MDT11
56 MDT10
57 MDT09
58 MDT08
59 MDT07
60 MDT06
61 MDT05
62 MDT04
63 MDT03
MAD00 MAD01 MAD02 MAD03 MAD04 MAD05 MAD06 MAD07 MAD08 VSS MAD09 VDD MAD10 MAD11 MAD12 MAD13 MAD14 MAD15 MDT00 MDT01 MDT02

(Top View)
⑰ 84-QFP

- Wide image processing space
  Horizontal scanning direction: Max. 65.536 pixels
  Vertical scanning direction: Limitless
- 84-pin flat package

■ Block Diagram


Line Memory(16 Bits/Pixel)
(MN4216)
MAD15~00
MDT15~00
MWE
MCLK
GCLK
LENBL
Line Memory Interface Block
(Timing Control Included)
GCLKO
LENBLO
Rank Compensative Operation Block
Ranking Operation
Addition/ Redistribution
Binary Error Operation Block
ODT
(MN6550)
A/D Converter
IDT7~0
(MN4216)
Dither Pattern RAM
DAD7~0
DDT7~0
DWE
Dither Matrix Block
Operation Mode Selector Block
PDT7~0
PWE
MODE2~0
VSS
VDD

■ Absolute Maximum Ratings(T=25°C, V_{SS}=0 V)

Item	Symbol	Rating	Unit
Supply voltage	V_{DD}	−0.3~+7.0	V
Input voltage	V_I	−0.3~V_{DD}+0.3	V
Output voltage	V_O	−0.3~V_{DD}+0.3	V
Output current	I_O	±20	mA
Power dissipation	P_D	500	mW
Operating ambient temperature	T_{opr}	0~+70	°C
Storage temperature	T_{stg}	−55~+150	°C

■ Operating Conditions(Ta=0~+70°C, V_{SS}=0V)

Item	Symbol	Condition	min.	typ.	max.	Unit
Operating supply voltage	V_{DD}		4.75	5.0	5.25	V

■ I/O Capacitance

Item	Symbol	Condition	min.	typ.	max.	Unit
Input pin	C_{IN}	V_{DD}=V_I=0V, f=1 MHz, Ta=25°C		10	20	pF
Output pin	C_{OUT}			10	20	pF
I/O pin	$C_{I/O}$			10	20	pF

■ Electrical Characteristics

● DC Characteristics(V_{DD}=4.75 ~ 5.25 V, V_{SS}=0 V, Ta=0 ~+70°C)

Item	Symbol	Condition	min.	typ.	max.	Unit
Static supply current	I_{DDS}	V_I=V_{DD} or V_{SS}, XI=V_{DD}			200	μA
Input voltage "H" level	I_{DDO}	V_I=V_{DD} or V_{SS}, V_{DD}=5 V, Output open f=20MHz		35	70	mA
Operating supply current	V_{IH}		V_{DD} ×0.7			V
Input voltage "L" level	V_{IL}				V_{DD} ×0.2	V
Input leakage current	I_{LI}	V_I=V_{DD} or V_{SS}	−10		−10	μA
Output voltage "H" level	V_{OH}	I_O=−4 mA, V_I=V_{DD} or V_{SS}	2.8			V
Output voltage "L" level	V_{OL}	I_O=−4 mA, V_I=V_{DD} or V_{SS}			0.5	V
Output leakage current	I_{LO}	V_O=HI-Z. V_O=V_{DD}orV_{SS} V_I=V_{DD} or V_{SS}	−10		−10	μA

● AC Characteristics

Item	Symbol	min.	typ.	max.	Unit
MCLK ↗ to $\overline{GCLK}$ setup time	t_0	25			ns
$\overline{GCLK}$ cycle time	t_1	t_{16*7}(350)			ns
$\overline{GCLK}$ "L" pulse width	t_2	t_{16}			ns
$\overline{GCLK}$ "H" pulse width	t_3	t_{16}			ns

● AC Characteristics (Continued)

Item	Symbol	min.	typ.	max.	Unit
$\overline{GCLK}$↘ to IDT steup time	t_4	0			ns
$\overline{GCLK}$↘ to IDT hold time	t_5	t_{16*2}			ns
$\overline{GCLK}$↘ to $\overline{GCLKO}$↘	t_6	0		50	ns
$\overline{GCLK}$↗ to $\overline{GCLKO}$↗	t_7	0		50	ns
$\overline{GCLKO}$↘ to ODT	t_8	0		50	ns
$\overline{LENBL}$ "H" pules width	t_9	t_{16*22}			ns
$\overline{LENBL}$↘ to $\overline{LENBLO}$↘	t_{10}	0		50	ns
$\overline{LENBL}$↗ to $\overline{LENBLO}$↗	t_{11}	0		50	ns
$\overline{GCLK}$↘ to $\overline{LENBL}$ setup time	t_{12}	50			ns
$\overline{GCLK}$↘ to $\overline{LENBL}$ hold time	t_{13}	t_{16*7}			ns
$\overline{LENBL}$↘ to $\overline{MODE}$ steup time	t_{14}	t_{16*22}			ns
$\overline{LENBL}$↗ to $\overline{MODE}$ hold time	t_{15}	t_{16*22}			ns
MCLK cycle time	t_{16}	50		2000	ns
MCLK "H" pulse width	t_{17}	20			ns
MCLK "L" pules width	t_{18}	20			ns
$\overline{PWE}$↘ to MODE stetup time	t_{19}	100			ns
$\overline{PWE}$↗ to MODE hold time	t_{20}	50			ns
$\overline{PWE}$ cycle time	t_{21}	400			ns
$\overline{PWE}$↘ to PDT setup time	t_{22}	0			ns
$\overline{PWE}$ palse width "L"	t_{23}	70			ns
$\overline{PWE}$↗ to PDT hold time	t_{24}	50			ns
$\overline{PWE}$↘ to $\overline{DWE}$↘	t_{25}			50	ns
$\overline{DWE}$ palse width "L"	t_{26}	t_{23_30}			ns
$\overline{PWE}$↗ to $\overline{DWE}$↗	t_{27}			50	ns
$\overline{DWE}$↘ to DDT VALID time	t_{28}	0			ns
$\overline{DWE}$↗ to DDT INVALID time	t_{29}			20	ns
$\overline{PWE}$↗ to DAD VALID time	t_{30}			200	ns
$\overline{DWE}$↗ to DAD INVALID time	t_{31}	0			ns
MCLK↗ to Read DAD VALID time	t_{32}			150	ns
DAD to Read DDT VALID time	t_{33}	$t_{16}X6-(t_{34}+t_{32})$			ns
MCLK↗ to Read DDT setup time	t_{34}	20			ns
MCLK↗ to Read DDT hold time	t_{35}	40			ns
MCLK↗ to Read MAD VALID time	t_{36}			60	ns

● AC Characteristics (Continued)

Item	Symbol	min.	typ.	max.	Unit
MAD to Read MDT VALID time	t_{37}	$t_{16}X3-(t_{38}+t_{36})$			ns
MCLK↗ to Read MDT setup time	t_{38}	20			ns
MCLK↗ to Write MAD VALID time	t_{39}			60	ns
MCLK↗ to $\overline{MWE}$↘	t_{40}			50	ns
$\overline{MWE}$↘ to MDT VALID time	t_{41}			20	ns
$\overline{MWE}$↗ to Write MDT setup time	t_{42}	40			ns
MCLK↗ to $\overline{MWE}$↗	t_{43}			50	ns
$\overline{MWE}$↗ to Write MDT INVALID time	t_{44}	0			ns
$\overline{MWE}$ pulse width "L"	t_{45}	60			ns

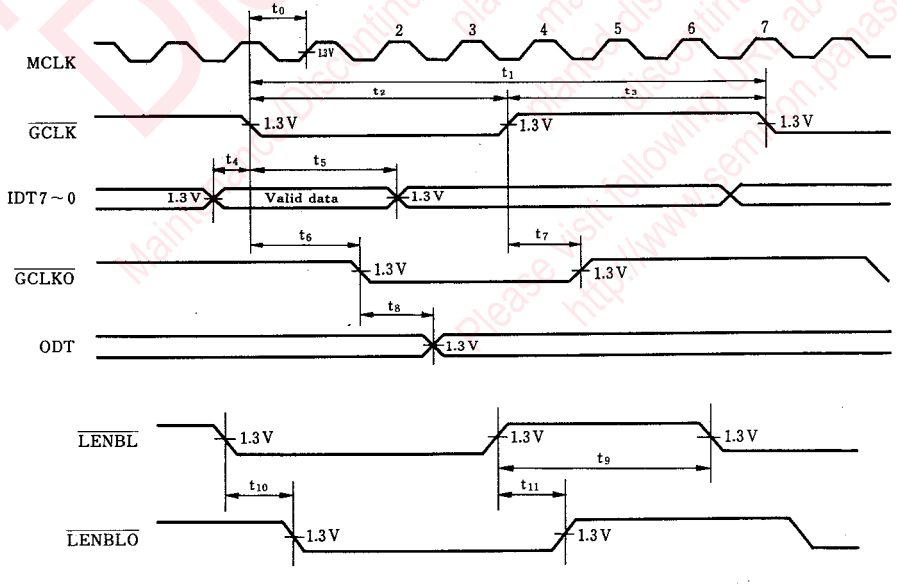
■ Pin Descriptions

Pin No.	Name	I/O	Description
1 ~ 8	IDT 7 ~ IDT 0	I	Pixel input data. Connects an 8-bit multivalued image input data line. Connects the MSB IDT7. Sets all the bits to the "H" level for the blackest image input data, and sets them to the "L" level for the whitest image input data.
9	$\overline{GCLK}$	I	Pixel clock. Supplies an "L" level signal when writing multivalued image data.
10, 54 33, 73	V_{DD}	—	+5 V power connection pin
11	$\overline{LENBL}$	I	Line enable. Supplies the "L" level signal when indicating that one line is enabled. The line starts when it is changed from the "H" to "L" level, and it ends when changed from the "L" to the "H" level.
12, 52 31, 75	V_{SS}	—	GND
13	MCLK	I	Master clock. Supplies a single-phase clock. A clock frequency is determined by the L-level pulse width and cycle of $\overline{GCLK}$.
14~16	MODE 2 ~ MODE 0	I	Operation mode. Supplies a 3-bit operation control signal. The HTP initialize/pattern load, CAPIX 1, CAPIX 2, dither 1 or dither 2 mode can be set by a combination.
17	$\overline{PWE}$	I	Pattern write enable. Supplies the "L" level signal when writing pattern cycle or pattern input data. Normally, pattern cycle and pattern input data are continuously written.
18~25	PDT 7 ~ PDT 0	I	Pattern cycle data. Connects an 8-bit pattern cycle/pattern input data signal line. PDT7 is the MSB.
26~30 32 34~35	DAD 7 ~ DAD 3 DAD 2 DAD 1 ~ DAD 0	O	Address output. Signal line for address output of the dither memory. DAD7 is the MSB.

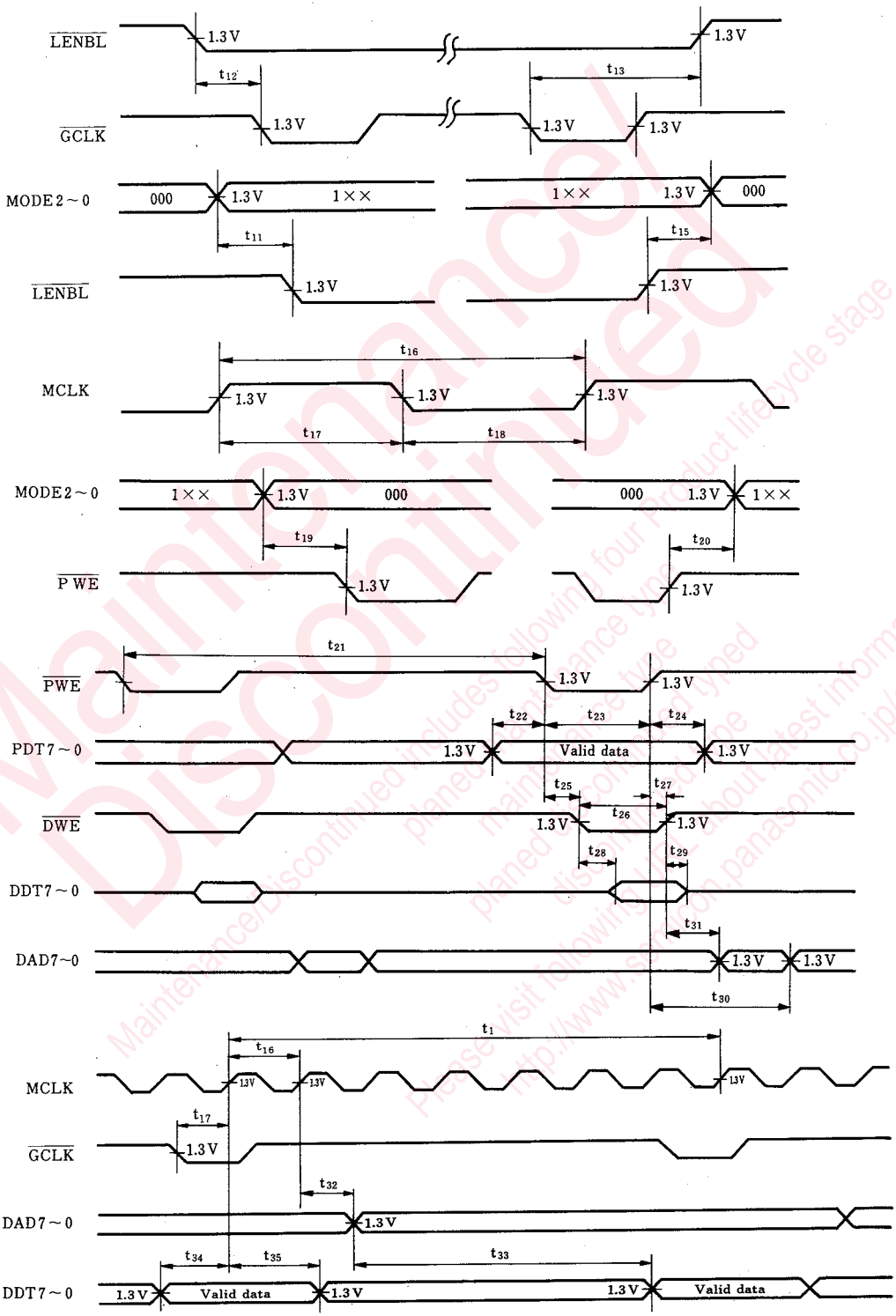
■ Pin Descriptions (Continued)

Pin No.	Name	I/O	Description
36~43	DDT7~DDT0	I/O	Data I/O. Bidirectional signal line for data I/O of the dither memory. DDT7 is the MSB. A data direction is an input when DWE is at the "H" level, and an output when at the "L" level.
44	$\overline{\text{DVE}}$	O	Write enable. Signal line to control data read/write of the dither memory. Data is read from the dither memory when it is at the "H" level, and it is written to the dither memory when at the "L" level.
45	$\overline{\text{LENBLO}}$	O	Write enable output. Output signal set to the "L" level when indicating that one line is enabled. Although synchronized with $\overline{\text{LENBL}}$, it is used when an accurate pixel position is required.
46	$\overline{\text{GCLKO}}$	O	Pixel clock output. Output signal set to the "L" level when indicating that a binary image output signal is enabled. Although synchronized with $\overline{\text{GCLK}}$, it is used when an accurate pixel position is required.
47	ODT	O	Pixel output data. Binary image output signal line with pseudo intermediate toning provided. "H" level for black pixel data, and "L" level for wnite pixel data
48	$\overline{\text{MWE}}$	I	Write enable. Signal line to control data read/write of the line memory. Data is read from the line memory when it is at the "H" level, and written to the line memory when at the "L" level.
49~51 53 55~66	MDT15~MDT13 MDT12 MDT11~MDT00	I/O	Data I/O. Bidirectional signal lines for data I/O of the line memory. MDT15 is the MSB. A data direction is an input when $\overline{\text{MWE}}$ is at the "H" level, and an output when at the "L" level.
67~72 74 76~84	MAD15~MAD10 MAD09 MAD08~MAD00	O	Address output. Signal line for address output of the line memory. MAD15 is the MSB.

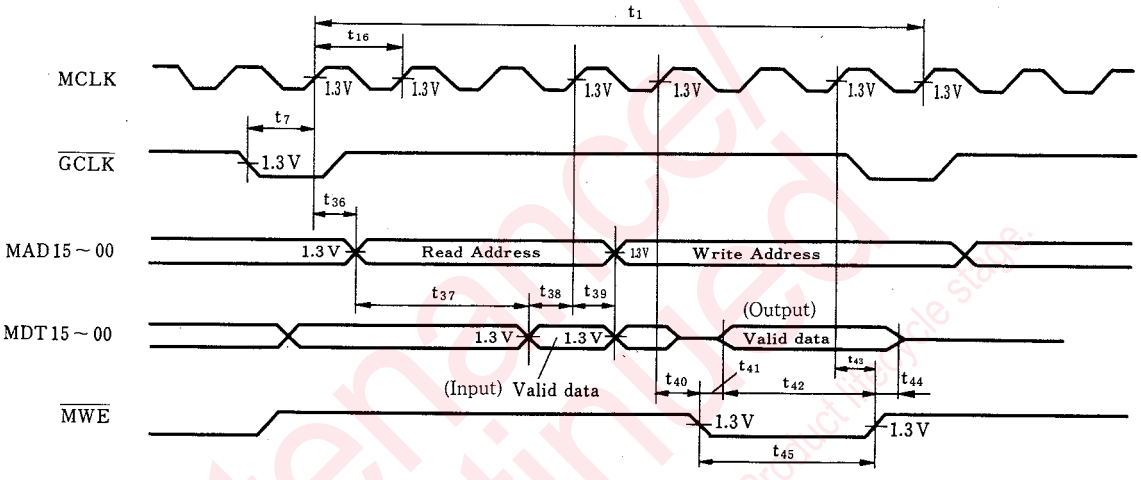
■ Timing Diagrams



■ Timing Diagrams (Countinued)



■ Timing Diagrams (Countinued)



■ Descriptions of Signal Processing

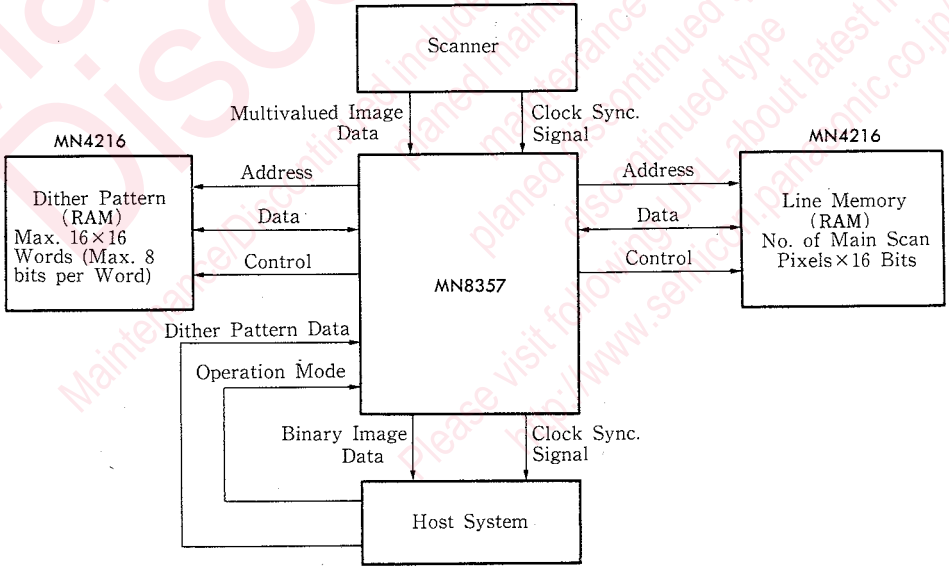
Item	Signal	Signal Direction/Q'ty		Description	Remarks
Image input	IDT 7～0	I	8	Image input data	IDT 7 : MSB, X'FF': Black
	$\overline{\text{GCLK}}$	I	1	Pixel clock	Cycle: 350 ns or more
	$\overline{\text{LENBL}}$	I	1	Write enable	
Image output	ODT	O	1	Pixel output data	"H": Black
	$\overline{\text{GCLKO}}$	O	1	Pixel clock output	
	$\overline{\text{LENBLO}}$	O	1	Write enable output	
Line memory	MAD15～00	O	16	Address output	MAD15 : MSB
	MDT15～00	I/O	16	Data output	MDD15 : MSB
	$\overline{\text{MWE}}$	O	1	Write enable	
Pattern input	PDT 7～0	I	8	Pattern cycle data	PDT 7 : MSB
	$\overline{\text{PWE}}$	I	1	Pattern write enable	
Dither memory	DAD 7～0	O	8	Address output	
	DDT 7～0	I/O	8	Data I/O	
	$\overline{\text{DWE}}$	O	1	Write enable	
Control signal	MCLK	I	1	Master clock	Max. 20 MHz
	MODE 2～0	I	3	Operation mode	000: HTP initialize/pattern load 100 : CAPIX 1 101 : CAPIX 2 110: Dither 1(max. 16×16) 111: Dither 2(max. 16×16)
Power supply line	V_{DD}	I	4	+5 V	
	V_{SS}	I	4	0 V	

■ Specifications

	Item	Description
LSI Factors	Process	CMOS 2.5μA1, 2 layers
	Package	84-pin flat package
	Clock	Max. 20 MHz
	Supply voltage	5V
	Power consumption	130mW/typ.
	Operating temperature range	0～70°C
Image Processing Functions	Processing speed	Max. 350 ns/pixel
	Input data width	Max. 8 bits/pixel
	Image space	Hor. scanning direction: Max. 65,536 pixels Vert. scanning direction: Limitless
	Operation mode	CAPIX 1(Character, line drawing, picture) CAPIX 2(Moire elimination only .... Reticular point picture of printed matter, etc.) Texture dither Dither matrix load system Optional cycle 1×1～16×16 Threshold value range 0～255

■ Applied Circuit

● When the MN8357 Is Applied as a Scanner Interface

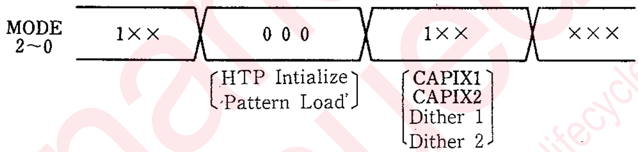


■ Description of Functions

HTP operations are controlled by a combination of control signals MODE 2-MODE 0 and classified into Pattern Load and 4 operation modes.

The following shows combinations of MODE 2-MODE 0 and their control sequences.

MODE 2	MODE 1	MODE 0	Operation Mode	MODE 2	MODE 1	MODE 0	Operation Mode
0	0	0	HTP Initialize/Pattern Load	1	0	0	CAPIX 1(Character, Line Drawing, Picture)
0	0	1	Combination Prohibited	1	0	1	CAPIX 2(Moire Elimination Only)
0	1	0	Combination Prohibited	1	1	0	Dither 1
0	1	1	Combination Prohibited	1	1	1	Dither 2



● HTP Initialize/Pattern Load

HTP Initialize/Pattern Load is initiated by changing the control signals MODE 2-MODE 0 from "1××" to "000" and terminated by changing them the other way.

(1) HTP Initialize

All the scan window register, processed data storage register, line memory address register, data register and pattern cycle control addresses are cleared while MODE 2-MODE 0 are "000".

(2) Pattern Load

While MODE 2-MODE 0 are "000", Pattern Load is executed by supplying pattern cycle and pattern data to PDT7-0, and L-level pulse signal to $\overline{PWE}$.

The following figure shows a signal supply timing and a pattern data supply sequence at Pattern Load time, and formats.

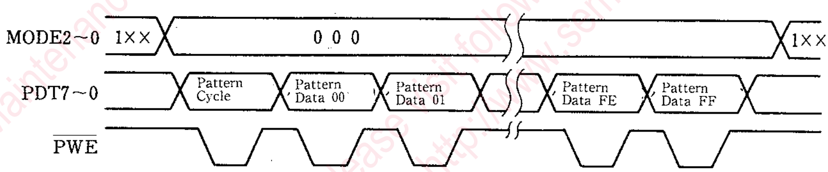
The pattern cycle and pattern data have a fixed supply sequence. If this sequence is a mistake, Pattern Load is not executed properly.

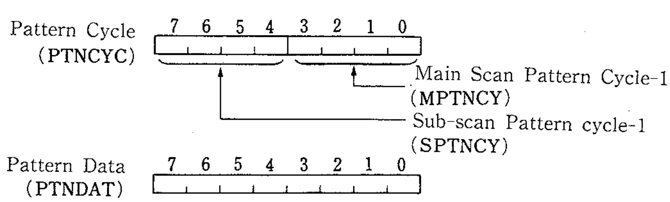
It is not necessary to always supply all the pattern data; you just supply from the pattern data. No.00 through pattern data which assumes the pattern cycle as its number. The number of pattern data supplied at that time is as follows.

No. of pattern data supplied = (SPTNCY − 1) × 16 + (MPTNCY)

Only the pattern cycle is required to be supplied when the ROM is used as dither memory.

● Pattern Load Timing





■ Description of Functions (Continued)

● Relations between Pattern Data Nos. and Positions

Main Scan Direction →

Sub-scan Direction ↓

00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
10	11	12	13												1F
															2F
															3F
															4F
															5F
															6F
															7F
															8F
															9F
															AF
															BF
															CF
															DF
															EF
												FD	FE	FF

● CAPIX I (Character, Line Drawing, Picture)

CAPIX 1 is initiated by changing the control signals MODE 2-MODE 0 from "000" to "100" and terminated by changing them the other way.

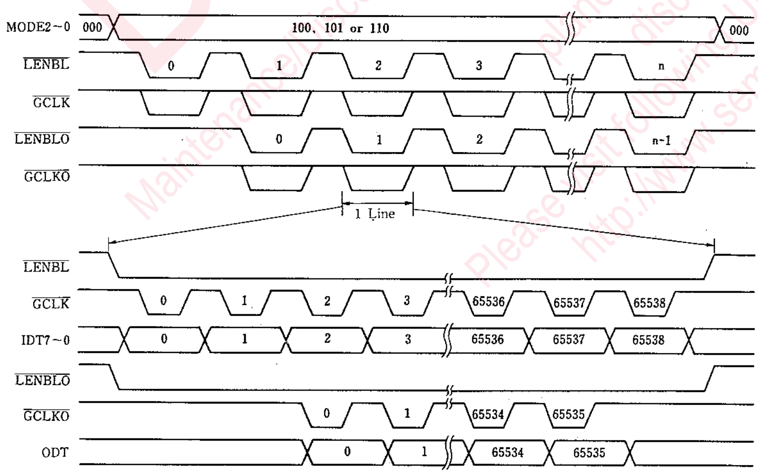
The following figure shows CAPIX 1 supply signal and output signal timings. Since the HTP performs processing by once reading into an internal scanning register, input pixel data and output DC data timings are shifted by 2 pixels in the main scan direction and by 1 pixel in the sub-scan direction, respectively.

Therefore, when an accurate positional relationship of processed pixel data is required, output pixel data are processed by using LENBLO and GCLKO.

The number of processed pixels in the main scan direction is up to 65,536. Even if GCLK is inputted, GCLKO is not outputted over 65,536 pulse. The number of processed pixels is also restricted by a line memory capacitance. When GCLK is inputted exceeding the capacitance, the contents of the line memory are destroyed and normal operation is not done, unless special protection is provided externally.

The table on the next page shows the patterns of Pattern Load which precedes CAPIX 1. The number of supplied patterns is 52.

● CAPIX I, CAPIX 2 and Dither I Timings



Note) Numbers indicate data numbers.

■ Description of Functions(Continued)

● CAPIX 1 Patterns

MODE: 100

Pattern Cycle: 33

Pattern Data

Upper \ Lower	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	84	84	7C	7C	×	×	×	×	×	×	×	×	×	×	×	×
1	84	84	7C	7C	×	×	×	×	×	×	×	×	×	×	×	×
2	7C	7C	84	84	×	×	×	×	×	×	×	×	×	×	×	×
3	7C	7C	84	84	×	×	×	×	×	×	×	×	×	×	×	×
4																
5																
6																
7																
8																
9																
A																
B																
C																
D																
E																
F																

Note 1) "Upper" and "Lower" indicate a pattern data sending sequence (00-FF) after sending the pattern cycles.

Note 2) × denotes indefiniet data, and blanks denote data which are required to be sent.

● CAPIX 2(Moire Elimination Only···Reticular Point Picture of Printed Matter, etc.)

CAPIX 2 is initiated by changing the control signals MODE 2-MODE 0 from "000" to "101" and terminated by changing them the other way.

CAPIX 2 supply signal and output signal timings are the same as those for CAPIX 1.

Pattern Load is not necessary for CAPIX 2.

● Dither 1

Dither is initiated by changing the control signals MODE 2-MODE 0 from "000" to "110" terminated by changing the other way.

Dither 1 supply signal and output signal timings are the same as those for CAPIX 1.

The following tables show the Pattern Load which procedes Dither 1. The number of pattern supplied depends on each pattern.

Relations between pattern data(PDT) and image input data(IDT), and image output data(ODT) are as follows:

When $IDT-PDT \geqq 0$, $ODT=1$

When $IDT-PDT<0$, $ODT=0$

$PDT=FF(Hex.)-$Dither pattern

● Distributed Dither Patterns

MODE: 11 n　　n=0: Dither 1

Pattern Cycle: 33　　n=1: Dither 2

Pattern Data

Upper \ Lower	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	F8	78	D8	58	×	×	×	×	×	×	×	×	×	×	×	×
1	38	B8	18	98	×	×	×	×	×	×	×	×	×	×	×	×
2	C8	48	E8	68	×	×	×	×	×	×	×	×	×	×	×	×
3	08	88	28	A8	×	×	×	×	×	×	×	×	×	×	×	×
4																
5																
6																
7																
8																
9																
A																
B																
C																
D																
E																
F																

● Reticular Point(45°) Patterns

MODE: 11 n　　n=0: Dither 1

Pattern Cycle: FF　　n=1: Dither 2

Pattern Data

Upper \ Lower	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	F8	E8	D4	A8	54	30	14	03	06	67	2A	56	AA	D6	EA	FC
1	E0	CC	BC	A0	5C	40	29	1D	1F	32	42	5E	A2	BE	CE	E2
2	C4	B4	98	90	6C	65	49	39	3B	4B	66	6E	92	9A	B6	C6
3	8C	88	84	7E	7D	79	75	71	73	77	7B	80	82	86	8A	8E
4	36	46	62	6B	97	9F	BB	CB	C9	B9	9D	95	98	60	44	34
5	1A	26	3F	5B	A7	C3	D3	E7	E5	D1	C1	A5	59	3C	2C	18
6	0A	13	2F	53	AF	DB	EF	F7	F5	ED	D9	AD	51	25	10	08
7	05	0F	23	4F	B3	DF	F3	FF	FB	F1	DD	B1	4D	21	0D	00
8	07	17	2B	57	AB	D7	EB	FD	F9	E9	D5	A9	55	31	15	02
9	1E	33	43	5F	A3	BF	CF	E3	E1	CD	BD	A1	5D	41	28	1C
A	3A	4A	67	6F	93	9B	B7	C7	C5	B5	99	91	6D	64	48	38
B	72	76	7A	81	83	87	8B	8F	8D	89	85	7F	7C	78	74	70
C	C8	B8	9C	94	69	61	45	35	37	47	63	6A	96	9E	BA	CA
D	E4	D0	C0	A4	58	3D	2D	19	1B	27	3E	5A	A6	C2	D2	E6
E	F4	EC	D8	AC	50	24	11	09	0B	12	2E	52	AE	DA	EE	F6
F	FA	F0	DC	B0	4C	20	0C	01	04	0E	22	4E	B2	DE	F2	FE

Note 1) "Upper" and "Lower" indicates a pattern data sending sequence(00-FF) after sending the pattern cycle.

Note 2) × denotes indefinite data. Blanks denote data which are not required to be sent.

● Simple Binary Conversion Patterns

MODE: 11 n　　n=0: Dither 1

Pattern Cycle: 00　　n=1: Dither 2

Pattern Data

Upper \ Lower	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	80															
1																
2																
3																
4																
5																
6																
7																
8																
9																
A																
B																
C																
D																
E																
F																

Note 1) "Upper" and "Lower" indicate a pattern data sending sequence(00-FF) after sending the pattern cycle.

Note 2) × denotes indifinite data, and blanks denote data which are not required to be sent.

■ Description of Function(Continued)

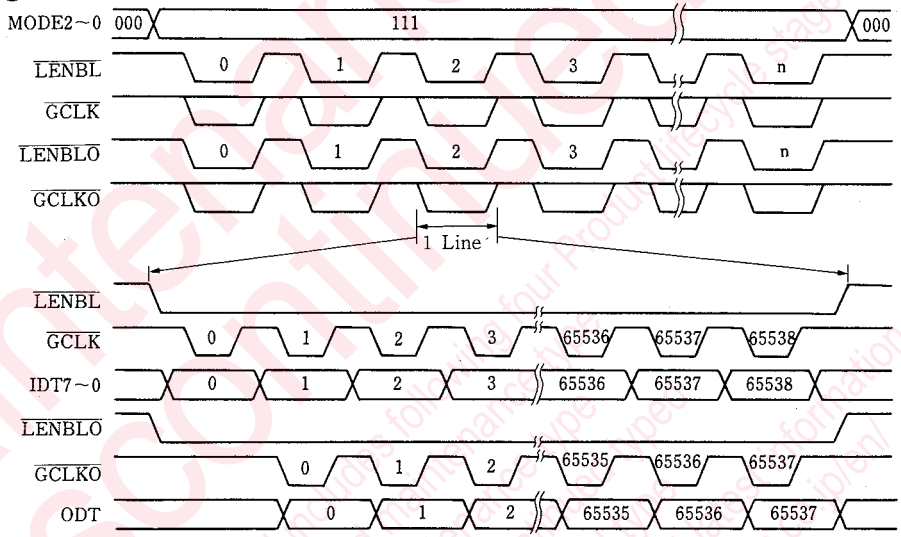
● Dither 2

Dither 2 is initiated by changing the control signals MODE 2-MODE 0 from "000" to "111" and terminated by changing the other way.

The following figure shows Dither 2 supply signal output signal timings. In order to adjust timings to CAPIX 1 or CAPIX 2, Dither 1 uses the line memory and performs processing by once reading data in the scanning register. Dither 2, however, performs processing without using the line memory and scanning register. Input pixel data and output pixel data timings are shifted by only 1 pixel in the main scan direction.

The number of processed pixels in the main scan direction is limitless. The patterns of Pattern Load, which precedes Dither 2, are the same as those for dither 1.

● Dither 2 Timing

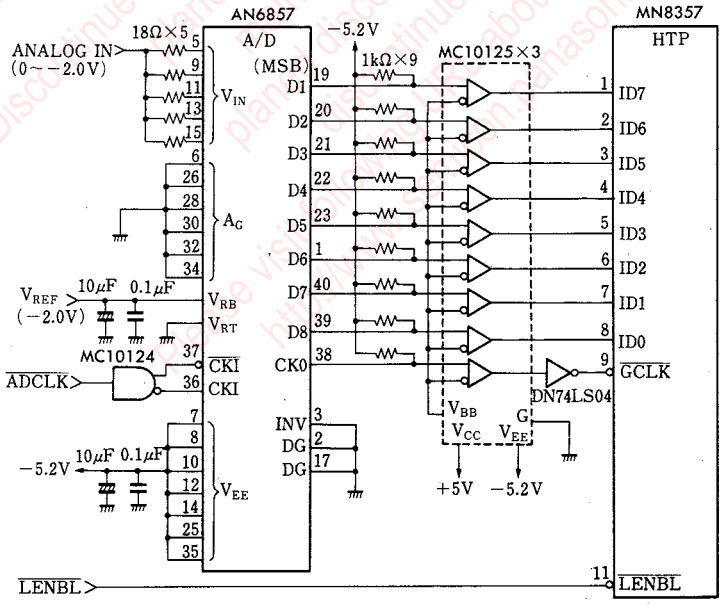


Note) Numbers indicate data numbers.

■ Application Examples

● Image Input Interface

The right figure shows an application example using an 8-bit A/D converter.



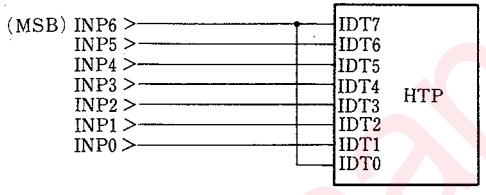
■ Application Examples (Continued)

Signal	Description	Remarks
ANALOG IN	Analog input signal	Write: −2 V, Black: 0 V
$\overline{\text{ADCLK}}$	Sampling clock	Enabled when changing from the "H" to "L" level.
$\overline{\text{LENBL}}$	Line enable signal	1-line data enable during the "L" level

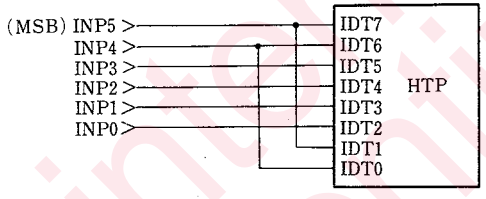
● Image Input Data Connections

(Connect as shown below when image input data is less than 8 bits)

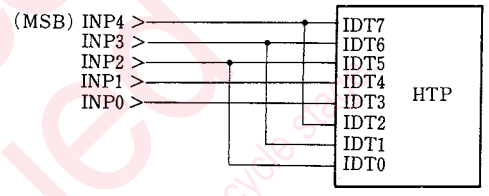
(a) For 7 bits



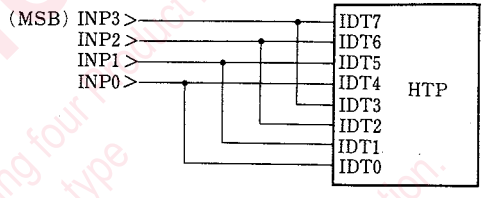
(b) For 6 bits



(c) For 5 bits

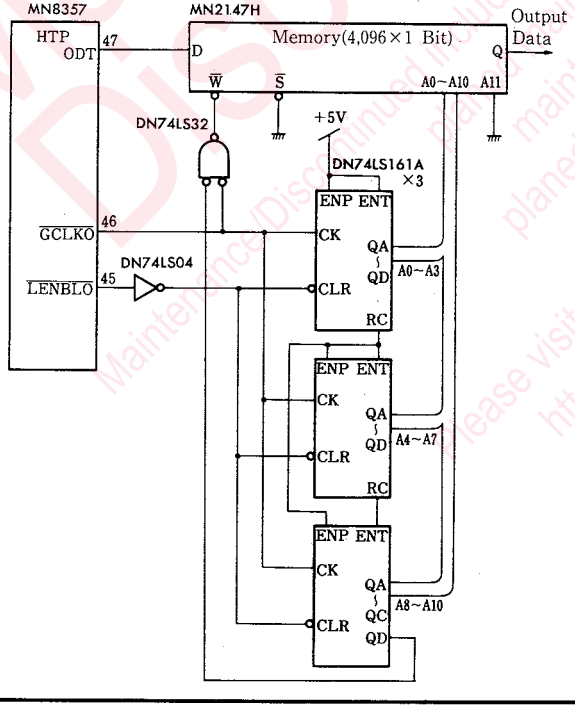


(d) For 4 bits



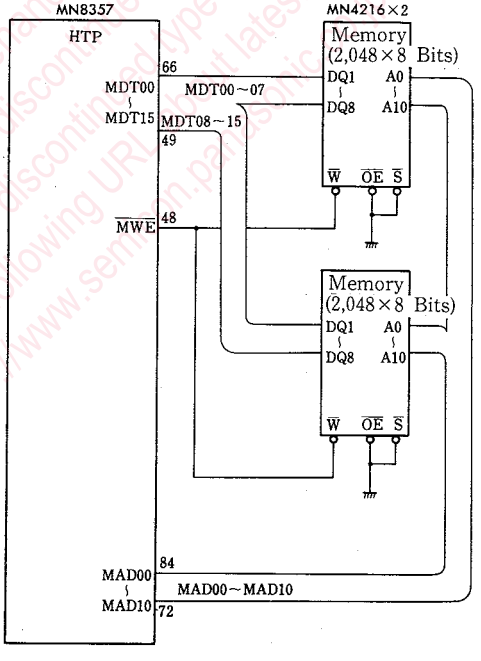
● Image Output Interface

The following figure shows an example of writing 2,048-pixel output data into the memory:



● Line Memory Interface

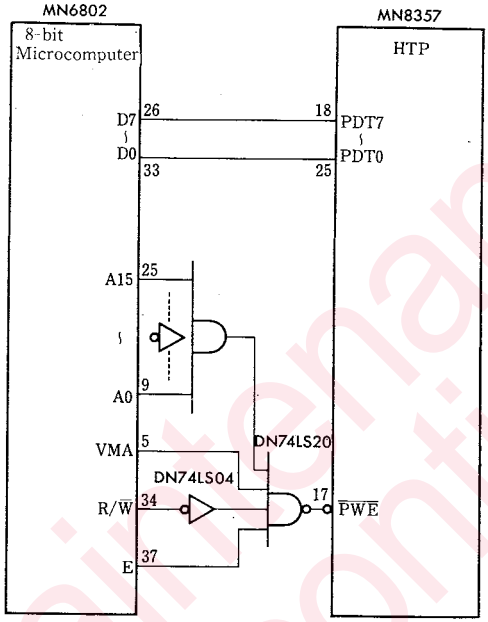
The following figure shows an example of processing 2,048 pixels:



■ Application Examples (Continued)

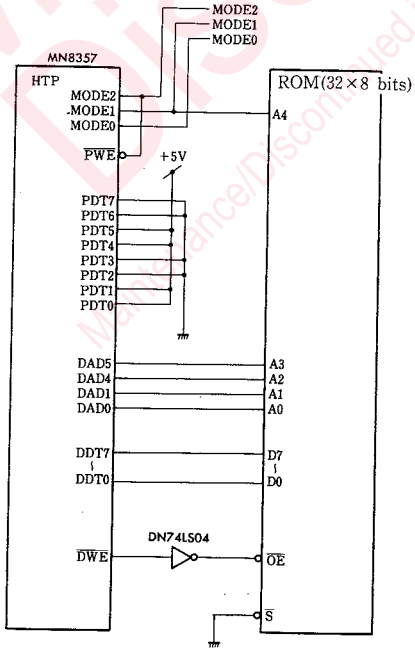
● Pattern Input Interface

The following figure shows an application example using an 8-bit microcomputer:



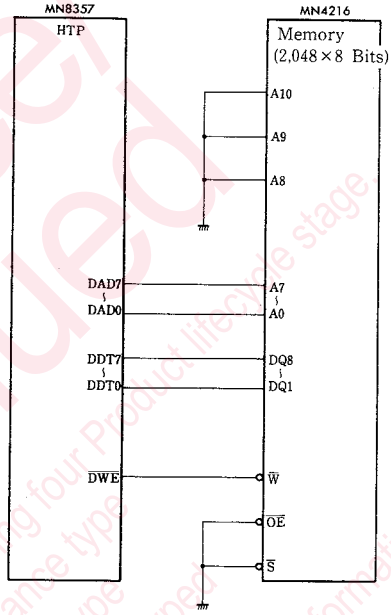
● Dither Memory Interface

(1) The following shows an example using the RAM:



● Dither Memory Interface

(2) The following figure shows an example using the ROM as the dither memory, and the following table shows ROM contents:



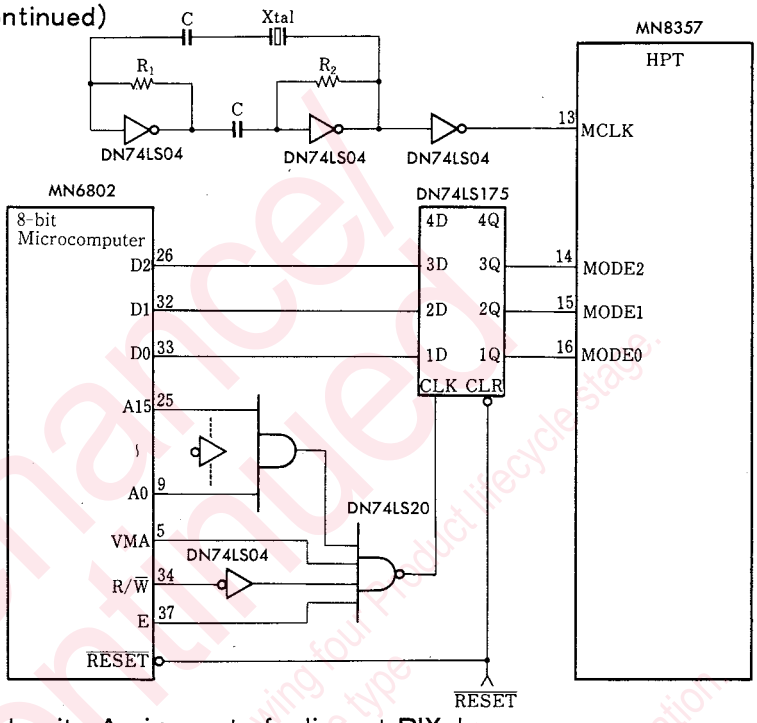
● ROM Contents

Corresponding OP. Mode	CAPIX	4×4 Distributed Dither
A 4 A 3~A 0	0	1
0000	84	F 8
0001	84	78
0010	7 C	D 8
0011	7 C	58
0100	84	38
0101	84	B 8
0110	7 C	18
0111	7 C	68
1000	7 C	C 8
1001	7 C	48
1010	84	E 8
1011	84	98
1100	7 C	08
1101	7 C	88
1110	84	28
1111	84	A 8

■ Application Examples(Continued)

● Control Signal Interface

The following figure shows an application example using a crystal osillation pin and an 8-bit microcomputer:



● CAPIX System-Correlative-density-Assignment of adjacent PIXels

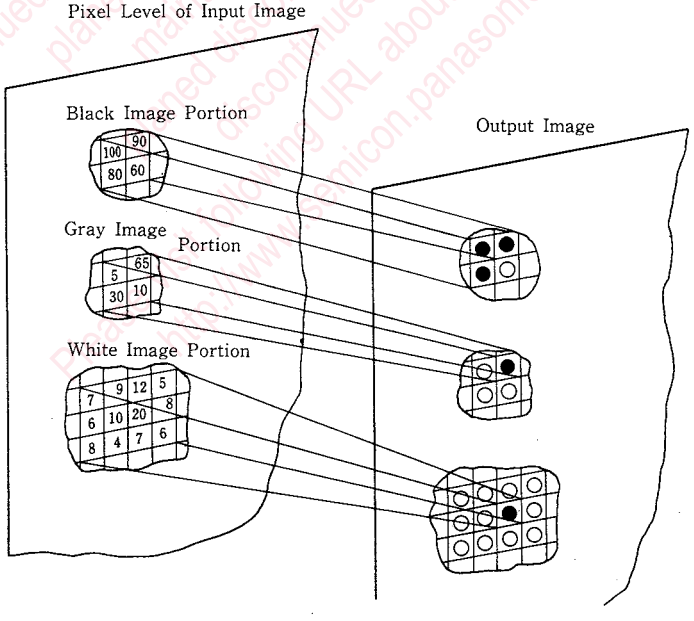
Sequentially adds the pixel level of an input image, and outputs one black when a sum reaches a level which generates one black. Therefore, the area to be added is not limited.

The right figure shows a concept of the CAPIX system when the pixel level of the input image comes to 100(black) from 0(white).

(1) Black image portion
A sum of 4 pixels comes to 330, and 3 blacks are outputted into 4 pixels in an descending order of the pixel level(one black is equivalent to 100).

(2) Gray image portion
A sum of 4 pixels comes to 110, and 1 black is outputted into 4 pixels.

(3) White image portion
A sum of 12 pixels comes to 102, and 1 black is outputted into 12 pixels.



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