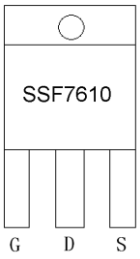
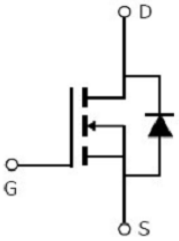
Main Product Characteristics

V_{DSS}	75V
R_{DS}(on)	6.5mΩ(typ.)
I_D	85A

TO-220



Marking and Pin Assignment



Schematic Diagram

Features and Benefits

- Advanced MOSFET process technology
- Special designed for PWM, load switching and general purpose applications
- Ultra low on-resistance with low gate charge
- Fast switching and reverse body recovery
- 175℃ operating temperature

Description

It utilizes the latest processing techniques to achieve the high cell density and reduces the on-resistance with high repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in power switching application and a wide variety of other applications.

Absolute Max Rating

Symbol	Parameter	Max.	Units
I_D @ TC = 25°C	Continuous Drain Current, V_{GS} @ 10V①	85	A
I_D @ TC = 100°C	Continuous Drain Current, V_{GS} @ 10V①	68	
I_{DM}	Pulsed Drain Current②	340	
P_D @TC = 25°C	Power Dissipation③	300	W
	Linear Derating Factor	2	W/°C
V_{DS}	Drain-Source Voltage	75	V
V_{GS}	Gate-to-Source Voltage	± 25	V
E_{AS}	Single Pulse Avalanche Energy @ L=0.3mH	453	mJ
I_{AS}	Avalanche Current @ L=0.3mH	55	A
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C

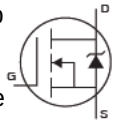
Thermal Resistance

Symbol	Characteristics	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-case③	—	0.5	°C /W
$R_{\theta JA}$	Junction-to-ambient (t ≤ 10s) ④	—	62	°C /W
	Junction-to-Ambient (PCB mounted, steady-state) ④	—	40	°C /W

Electrical Characteristics @T_A=25℃ unless otherwise specified

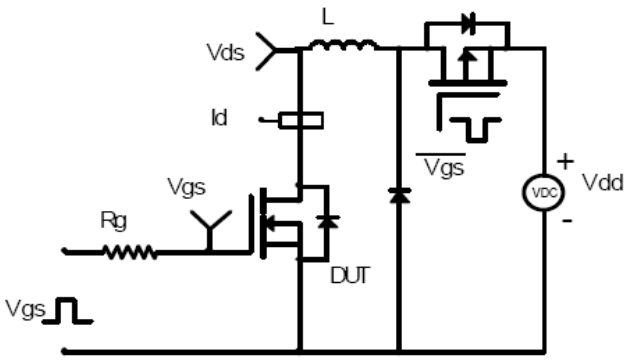
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source breakdown voltage	75	—	—	V	V_{GS} = 0V, ID = 250μA
$R_{DS(on)}$	Static Drain-to-Source on-resistance	—	6.5	10	mΩ	V_{GS}=10V,I_D = 40A
		—	11.1	—		T_J = 125°C
$V_{GS(th)}$	Gate threshold voltage	2	—	4	V	V_{DS} = V_{GS}, I_D = 250μA
		—	2.06	—		T_J = 125°C
I_{DSS}	Drain-to-Source leakage current	—	—	1	μA	V_{DS} = 75V,V_{GS} = 0V
		—	—	50		T_J = 125°C
I_{GSS}	Gate-to-Source forward leakage	—	—	100	nA	V_{GS} =25V
		—	—	-100		V_{GS} = -25V
Q_g	Total gate charge	—	80	—	nC	I_D = 80A,
Q_{gs}	Gate-to-Source charge	—	19	—		V_{DS}=64V,
Q_{gd}	Gate-to-Drain("Miller") charge	—	27	—		V_{GS} = 10V
$t_{d(on)}$	Turn-on delay time	—	25	—	ns	V_{GS}=10V, VDS=38V, R_{GEN}=6Ω,ID=42A
t_r	Rise time	—	20	—		
$t_{d(off)}$	Turn-Off delay time	—	71	—		
t_f	Fall time	—	47	—		
C_{iss}	Input capacitance	—	5961	—	pF	V_{GS} = 0V
C_{oss}	Output capacitance	—	452	—		V_{DS} = 30V
C_{rss}	Reverse transfer capacitance	—	169	—		ƒ = 1MHz

Source-Drain Ratings and Characteristics

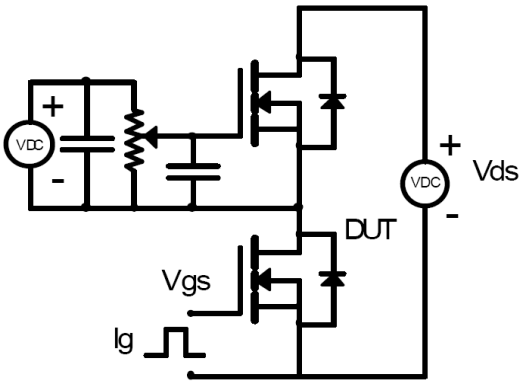
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	85	A	MOSFET symb showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode)	—	—	340	A	
V_{sd}	Diode Forward Voltage	—	0.8	1	V	I_S=20A, V_{GS}=0V
t_{rr}	Reverse Recovery Time	—	37	—	ns	T_J = 25°C, I_F =40A, di/dt = 100A/μs
Q_{rr}	Reverse Recovery Charge	—	50	—	nC	

Test circuits and Waveforms

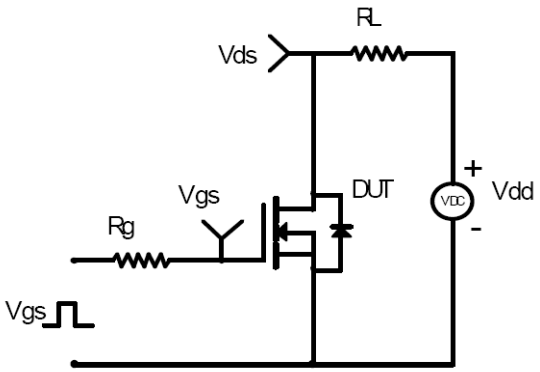
EAS Test Circuit



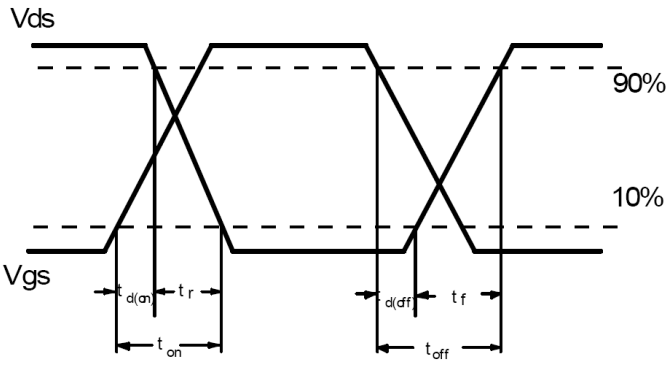
Gate charge test circuit



Switching Time Test Circuit



Switching Waveforms



Notes:

①Calculated continuous current based on maximum allowable junction temperature.

②Repetitive rating; pulse width limited by max. junction temperature.

③The power dissipation PD is based on max. junction temperature, using junction-to-case thermal resistance.

④The value of $R_{\theta JA}$ is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with TA =25°C

Typical electrical and thermal characteristics

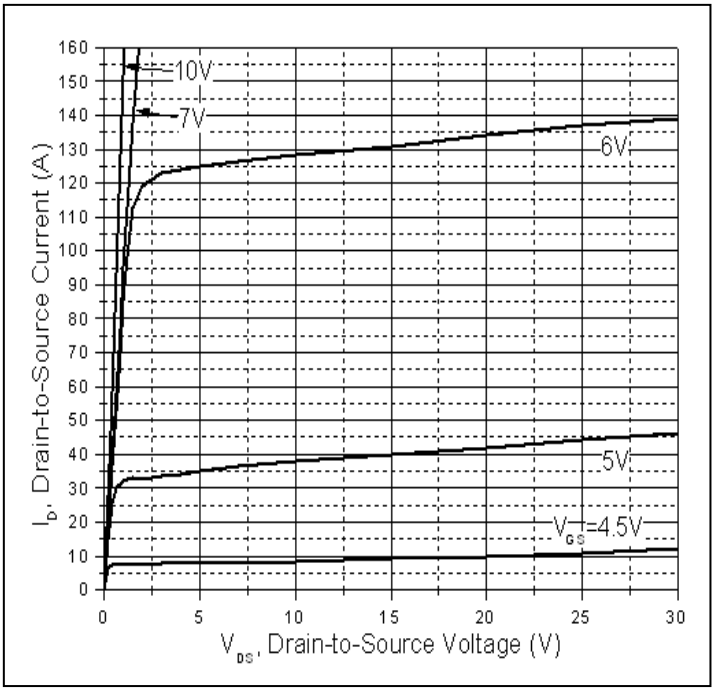


Figure 1: Typical Output Characteristics

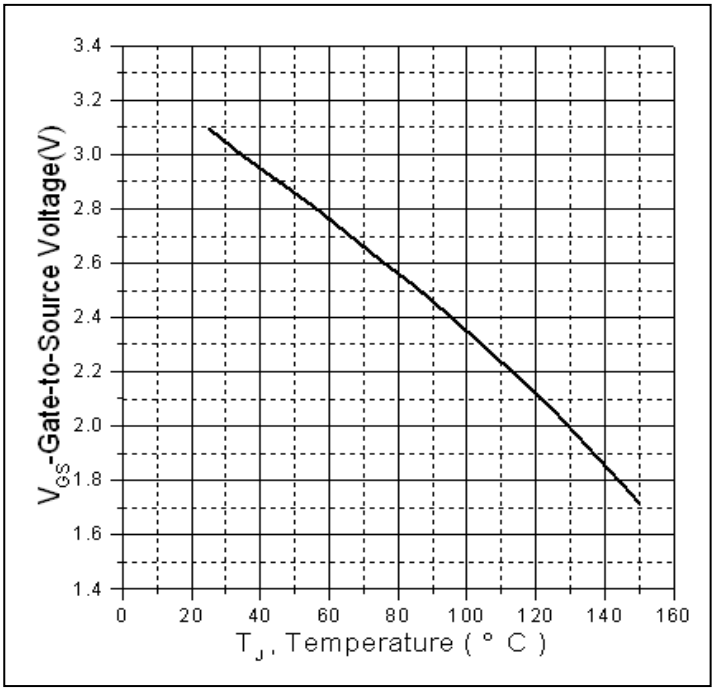


Figure 2. Gate to source cut-off voltage

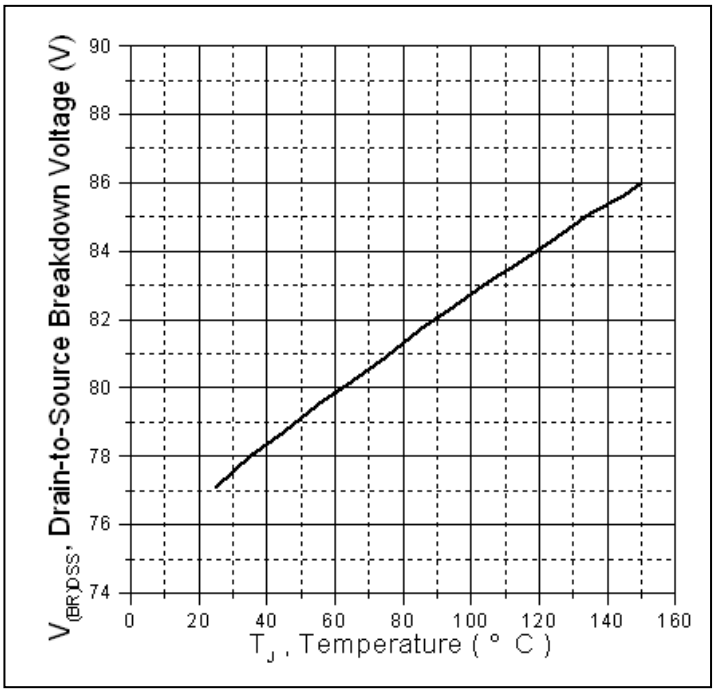


Figure 3. Drain-to-Source Breakdown Voltage Vs. Case Temperature

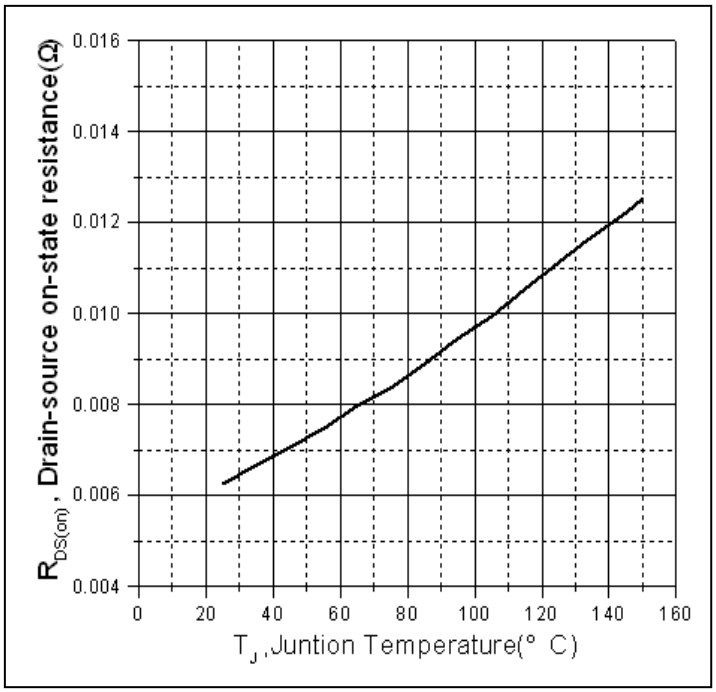


Figure 4: Normalized On-Resistance Vs. Case Temperature

Typical electrical and thermal characteristics

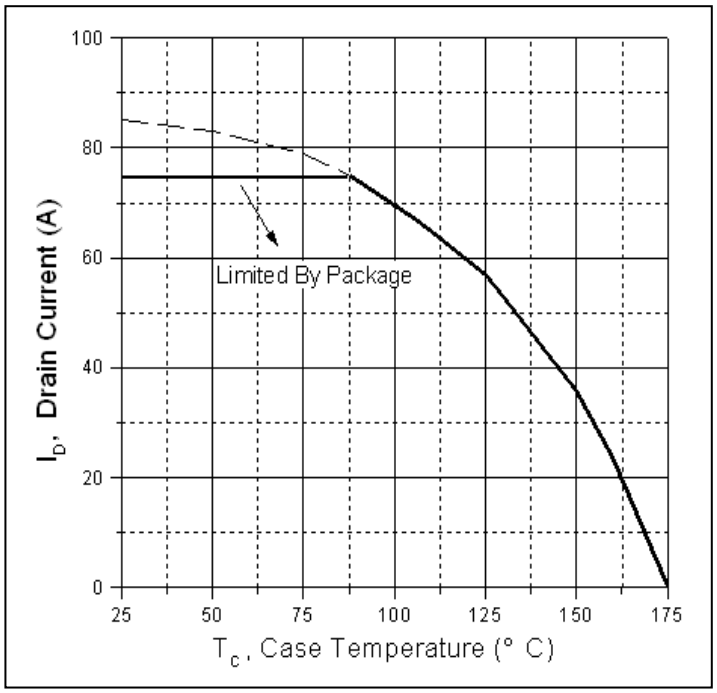


Figure 5. Maximum Drain Current Vs. Case Temperature

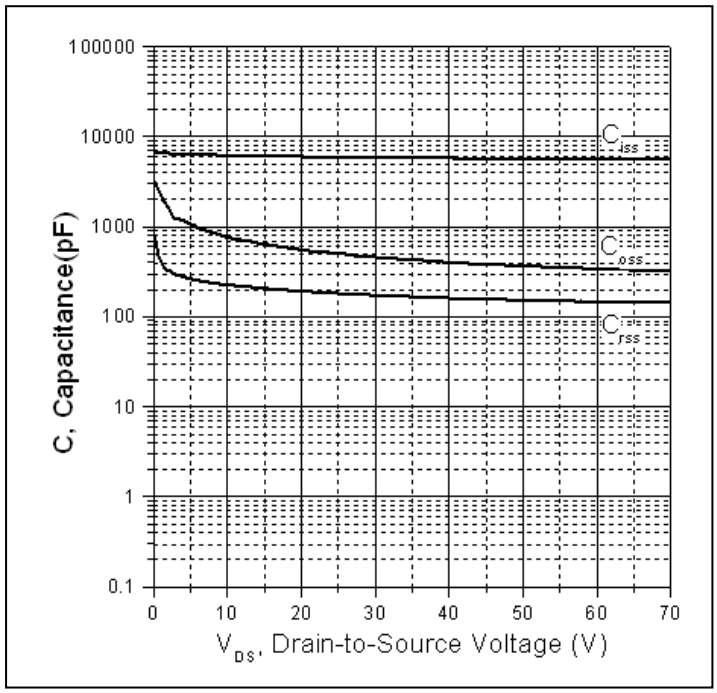


Figure 6.Typical Capacitance Vs. Drain-to-Source Voltage

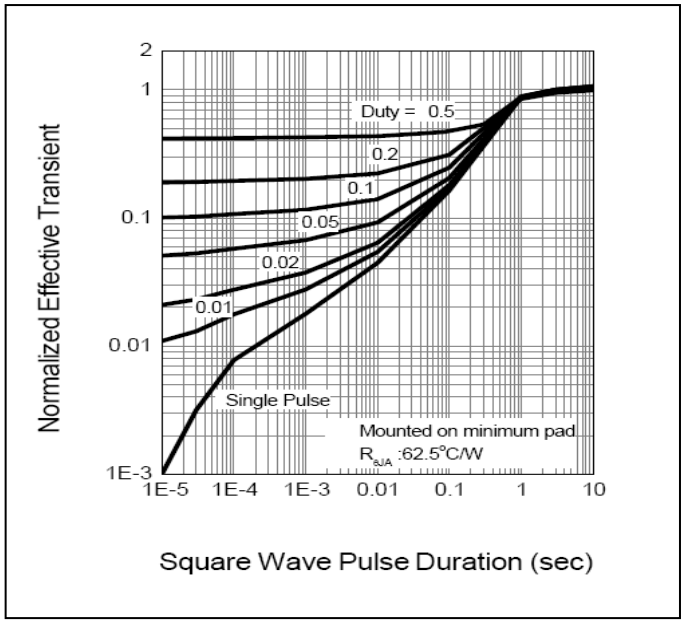
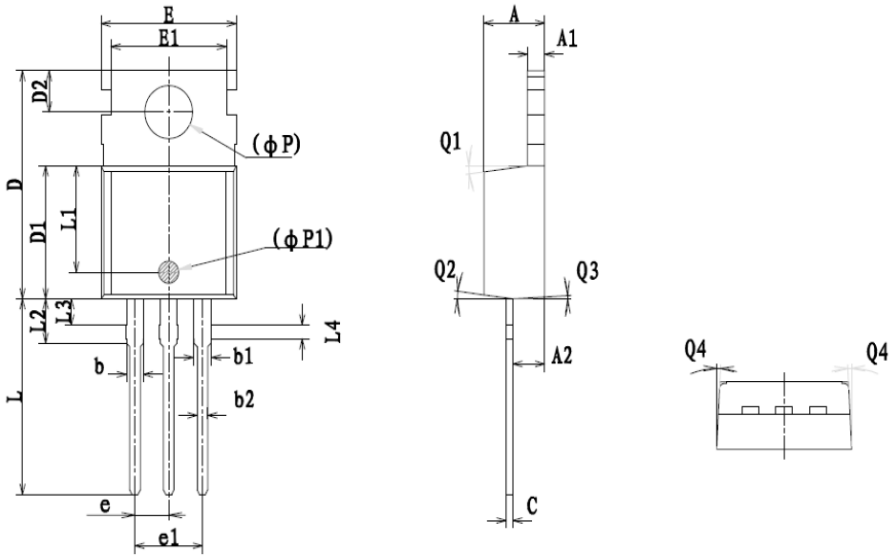


Figure7. Maximum Effective Transient Thermal Impedance, Junction-to-Case

Mechanical Data：

TO220 PACKAGE OUTLINE DIMENSION_GN



Symbol	Dimension In Millimeters			Dimension In Inches		
	Min	Nom	Max	Min	Nom	Max
A	4.400	4.550	4.700	0.173	0.179	0.185
A1	1.270	1.300	1.330	0.050	0.051	0.052
A2	2.240	2.340	2.440	0.088	0.092	0.096
b	–	1.270	–	-	0.050	-
b1	1.270	1.370	1.470	0.050	0.054	0.058
b2	0.750	0.800	0.850	0.030	0.031	0.033
C	0.480	0.500	0.520	0.019	0.020	0.021
D	15.100	15.400	15.700	0.594	0.606	0.618
D1	8.800	8.900	9.000	0.346	0.350	0.354
D2	2.730	2.800	2.870	0.107	0.110	0.113
E	9.900	10.000	10.100	0.390	0.394	0.398
E1	-	8.700	-	-	0.343	-
ΦP	3.570	3.600	3.630	0.141	0.142	0.143
ΦP1	1.400	1.500	1.600	0.055	0.059	0.063
e	2.54BSC			0.1BSC		
e1	5.08BSC			0.2BSC		
L	13.150	13.360	13.570	0.518	0.526	0.534
L1	7.35REF			0.29REF		
L2	2.900	3.000	3.100	0.114	0.118	0.122
L3	1.650	1.750	1.850	0.065	0.069	0.073
L4	0.900	1.000	1.100	0.035	0.039	0.043
Q1	5^0	7^0	9^0	5^0	7^0	9^0
Q2	5^0	7^0	9^0	5^0	7^0	9^0
Q3	5^0	7^0	9^0	5^0	7^0	9^0
Q4	1^0	3^0	5^0	1^0	3^0	5^0

Ordering and Marking Information

Device Marking: SSF7610

Package (Available)

TO-220

Operating Temperature Range

C : -55 to 150 ºC

Devices per Unit

Package Type	Units/ Tube	Tubes/Inner Box	Units/Inner Box	Inner Boxes/Carton Box	Units/Carton Box
TO-220	50	20	1000	6	6000

Reliability Test Program

Test Item	Conditions	Duration	Sample Size
High Temperature Reverse Bias(HTRB)	T_j=125℃ to 150℃ @ 80% of Max V_{DSS}/V_{CES}/VR	168 hours 500 hours 1000 hours	3 lots x 77 devices
High Temperature Gate Bias(HTGB)	T_j=150℃@ 100% of Max V_{GSS}	168 hours 500 hours 1000 hours	3 lots x 77 devices

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