Standard Products

UT54LVDS217 Serializer

Data Sheet

June, 2003

FEATURES

- 15 to 75 MHz shift clock support
- Low power consumption
- Power-down mode <216µW (max)
- Cold sparing all pins
- Narrow bus reduces cable size and cost
- Up to 1.575 Gbps throughput
- Up to 197 Megabytes/sec bandwidth
- 325 mV (typ) swing LVDS devices for low EMI
- PLL requires no external components
- Rising edge strobe
- Radiation-hardened design; total dose irradiation testing to MIL-STD-883 Method 1019
  - Total-dose: 300 krad(Si) and 1 Mrad(Si)
  - Latchup immune (LET > 100 MeV-cm^2/mg)
- Packaging options:
  - 48-lead flatpack
- Standard Microcircuit Drawing 5962-01534
  - QML Q and V compliant part
- Compatible with TIA/EIA-644 LVDS standard

INTRODUCTION

The UT54LVDS217 Serializer converts 21 bits of CMOS/TTL data into three LVDS (Low Voltage Differential Signaling) data streams. A phase-locked transmit clock is transmitted in parallel with the data streams over a fourth LVDS link. Every cycle of the transmit clock 21 bits of input data are sampled and transmitted.

At a transmit clock frequency of 75MHz, 21 bits of TTL data are transmitted at a rate of 525 Mbps per LVDS data channel. Using a 75MHz clock, the data throughput is 1.575 Gbit/s (197 Mbytes/sec).

The UT54LVDS217 Serializer allows the use of wide, high speed TTL interfaces while reducing overall EMI and cable size.

All pins have Cold Spare buffers. These buffers will be high impedance when V_{DD} is tied to V_{SS}.

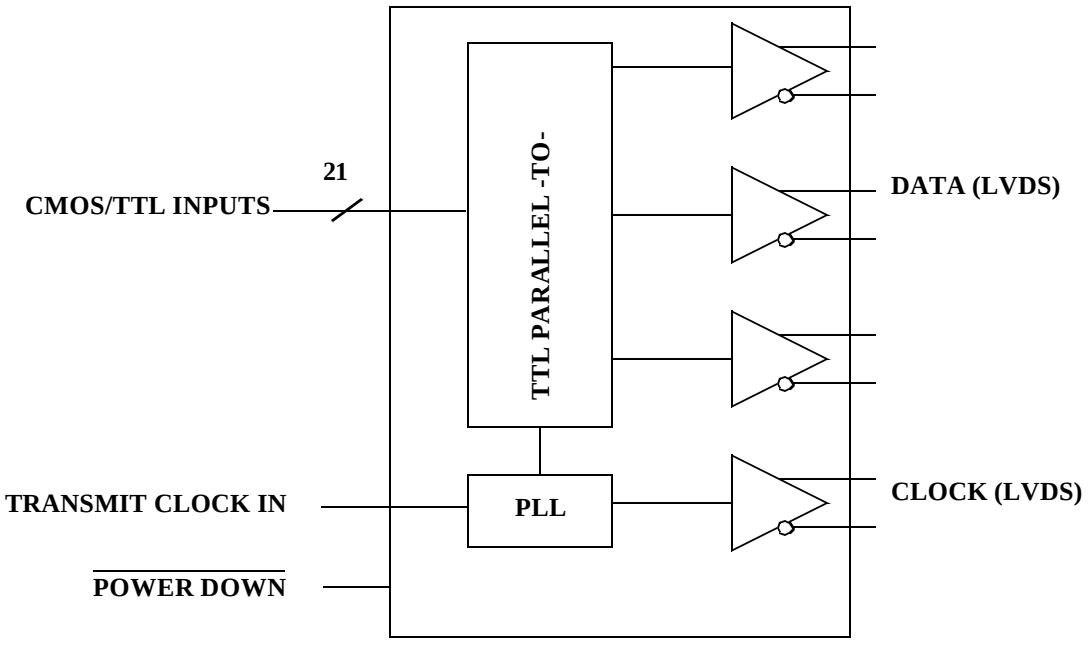


Figure 1. UT54LVDS217 Serializer Block Diagram

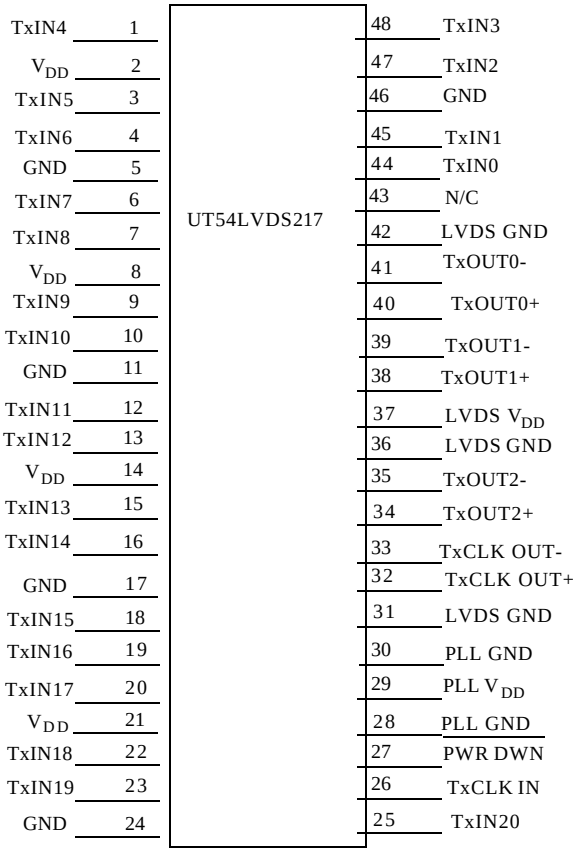


Figure 2. UT54LVDS217 Pinout

PIN DESCRIPTION

Pin Name	I/O	No.	Description
TxIN	**I**	**21**	TTL level input
TxOUT+	**O**	**3**	Positive LVDS differential data output
TxOUT-	**O**	**3**	Negative LVDS differential data output
TxCLK IN	**I**	**1**	TTL level clock input. The rising edge acts as data strobe. Pin name TxCLK IN
TxCLK OUT+	**O**	**1**	Positive LVDS differential clock output
TxCLK OUT-	**O**	**1**	Negative LVDS differential clock output
$\overline{\text{PWR DWN}}$	**I**	**1**	TTL level input. Assertion (low input) TRI-STATEs the clock and data outputs, ensuring low current at power down.
V_{DD}	**I**	**4**	Power supply pins for TTL inputs and logic
GND	**I**	**5**	Ground pins for TTL inputs and logic
PLL V_{DD}	**I**	**1**	Power supply pins for PLL
PLL GND	**I**	**2**	Ground pins for PPL
LVDS V_{DD}	**I**	**1**	Power supply pin for LVDS output
LVDS GND	**I**	**3**	Ground pins for LVDS outputs

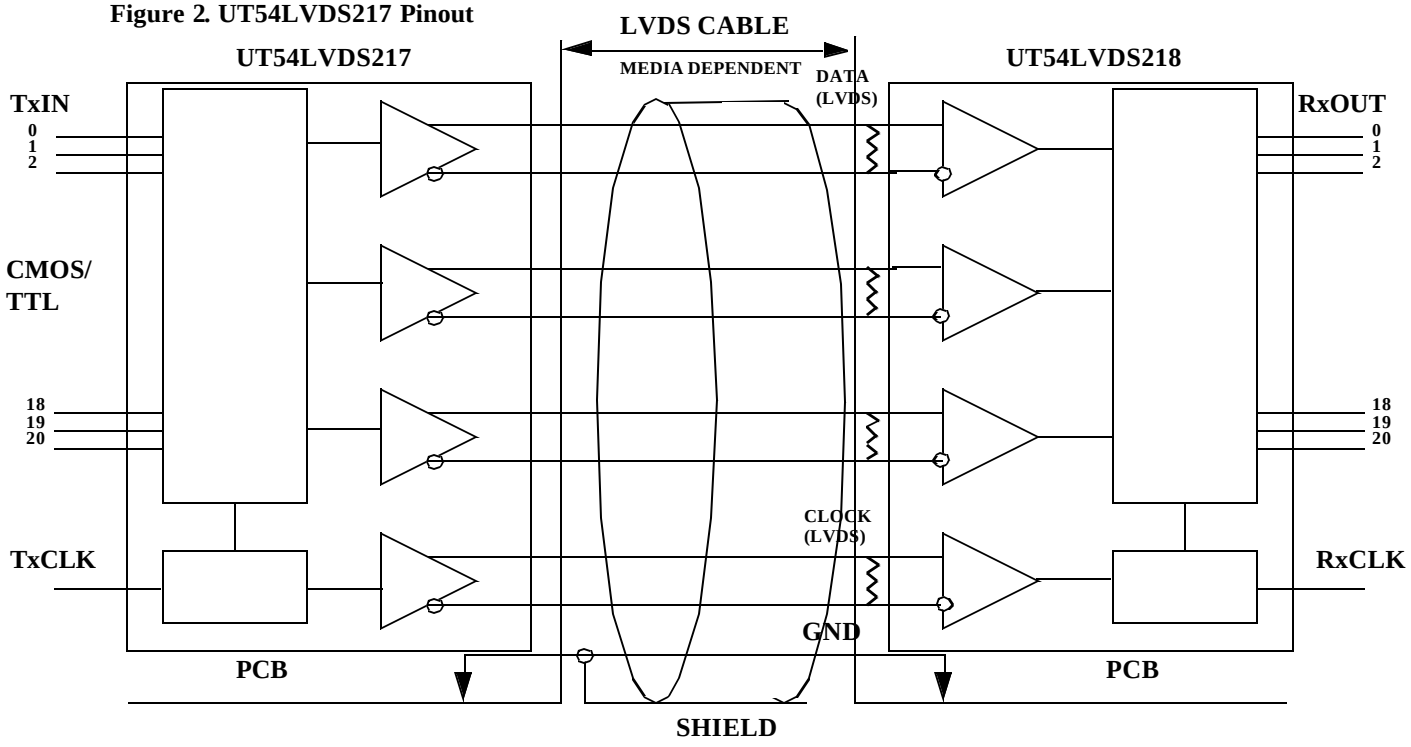


Figure 3. UT54LVDS217 Typical Application

ABSOLUTE MAXIMUM RATINGS[1]

(Referenced to V_{SS})

SYMBOL	PARAMETER	LIMITS
V_{DD}	DC supply voltage	-0.3 to 4.0V
$V_{I/O}$	Voltage on any pin[4]	-0.3 to (V_{DD} + 0.3V)
T_{STG}	Storage temperature	-65 to +150°C
P_D	Maximum power dissipation	2 W
T_J	Maximum junction temperature[2]	+150°C
Θ_{JC}	Thermal resistance, junction-to-case[3]	10°C/W
I_I	DC input current	±10mA

Notes:

1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and performance.
2. Maximum junction temperature may be increased to +175°C during burn-in and lifetest.
3. Test per MIL-STD-883, Method 1012.
4. For cold spare mode ($V_{DD} = V_{SS}$), $V_{I/O}$ may be 0.3V to the maximum recommended operating V_{DD} + 0.3V.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS
V_{DD}, $P_{LL}V_{DD}$, LVDS V_{DD}	Positive supply voltage	3.0 to 3.6V
T_C	Case temperature range	-55 to +125°C
V_{IN}	DC input voltage	0V to V_{DD}

DC ELECTRICAL CHARACTERISTICS[1]

(V_{DD} = 3.3V-0.3V; -55°C < T_C < +125°C)

SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNIT
CMOS/TTL DC SPECIFICATIONS					
V_{IH}	High-level input voltage		2.0	V_{DD}	V
V_{IL}	Low-level input voltage		GND	0.8	V
I_{IH}	High-level input current	V_{IN} = 3.6V; V_{DD} = 3.6V	-10	+10	µA
I_{IL}	Low-level input current	V_{IN} = 0V; V_{DD} = 3.6V	-10	+10	µA
V_{CL}	Input clamp voltage	I_{CL} = -18mA		-1.5	V
I_{CS}	Cold Spare Leakage current	V_{IN} = 3.6V; V_{DD} = V_{SS}	-20	+20	µA
LVDS OUTPUT DC SPECIFICATIONS (OUT+, OUT-)					
V_{OD}[5]	Differential Output Voltage	R_L = 100Ω (See Figure 14)	250	400	mV
ΔV_{OD}[5]	Change in V_{OD} between complimentary output states	R_L = 100Ω (See Figure 14)		35	mV
V_{OS}[5]	Offset Voltage	R_L = 100Ω, $\left(Vos = \frac{Voh + Vol}{2}\right)$	1.120	1.410	V
ΔV_{OS}[5]	Change in V_{OS} between complimentary output states	R_L = 100Ω		35	mV
I_{OZ}[4]	Output Three-State Current	PWR DWN = 0V V_{OUT} = 0V or V_{DD}	-10	+10	µA
I_{CSOUT}	Cold Spare Leakage Current	V_{IN}=3.6V, V_{DD} = V_{SS}	-20	+20	µA
I_{OS}[2,3]	Output Short Circuit Current	V_{OUT}+ or V_{OUT}- = 0V		5mA	mA
Supply Current					
I_{CCL}[4]	Transmitter supply current with loads	R_L = 100Ω all channels (figure 4) CL = 5pF, f = 50MHz		65.0	mA
I_{CCZ}[4,6]	Power down current	D_{IN} = V_{SS} $\overline{\text{PWR DWN}}$ = 0V, f = 0Hz		60.0	µA

Notes:

1. Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground.
2. Output short circuit current (I_{OS}) is specified as magnitude only, minus sign indicates direction only. Only one output should be shorted at a time, do not exceed maximum junction temperature specification.
3. Guaranteed by characterization.
4. Devices are tested @ 3.6V only.
5. Clock outputs guaranteed by design.
6. Post 100Krad and 300Krad, I_{CCZ} = 200µA.

AC SWITCHING CHARACTERISTICS[1]
(V_{DD} = 3.0V to 3.6V; TA = -55°C to +125°C)

SYMBOL	PARAMETER		MIN	MAX	UNIT
LLHT[2]	LVDS Low-to-High Transition Time (Figure 5)			1.5	ns
LHLT[2]	LVDS High-to-Low Transition Time (Figure 5)			1.5	ns
TPPos0[2]	Transmitter Output Pulse Position for Bit 0 (Figure 13)	f=75MHz	-0.18	0.270	ns
TPPos1[2]	Transmitter Output Pulse Position for Bit 1(Figure 13)	f=75MHz	1.72	2.17	ns
TPPos2[2]	Transmitter Output Pulse Position for Bit 2 (Figure 13)	f=75MHz	3.63	4.08	ns
TPPos3[2]	Transmitter Output Pulse Position for Bit 3 (Figure 13)	f=75MHz	5.53	5.98	ns
TPPos4[2]	Transmitter Output Pulse Position for Bit 4 (Figure 13)	f=75MHz	7.44	7.89	ns
TPPos5[2]	Transmitter Output Pulse Position for Bit 5 (Figure 13)	f=75MHz	9.34	9.79	ns
TPPos6[2]	Transmitter Output Pulse Position for Bit 6 (Figure 13)	f=75MHz	11.25	11.70	ns
TCCS[3]	Channel to Channel skew (Figure 7)			0.45	ns
TCIP	TxCLK IN Period (Figure 8)		13.3	66.7	ns
TCIH[4]	TxCLK IN High Time (Figure 8)		0.35Tcip	0.65Tcip	ns
TCIL[4]	TxCLK IN Low Time (Figure 8)		0.35Tcip	0.65Tcip	ns
TSTC[2]	TxIN Setup to TxCLK IN (Figure 8)	15MHz 75MHz	1.0 0.5		ns
THTC[2]	TxIN Hold to TxCLK IN (Figure 8)	15MHz 75MHz	0.7 0.5		ns
TCCD	TxCLK IN to TxCLK OUT Delay (Figure 9)		0.5	2.5	ns
TPLLS	Transmitter Phase Lock Loop Set (Figure 10)			10	ms
TPDD	Transmitter Powerdown Delay (Figure 12)			100	ns

Notes:
1. Recommend transistion time for TXCLK In is 1.0 to 6.0 ns (figure 6).
2. Guaranteed by characterization.
3. Channel to channel skew is defined as the difference between TPPOS max limit and TPPOS minimum limit.
4. Guaranteed by design.

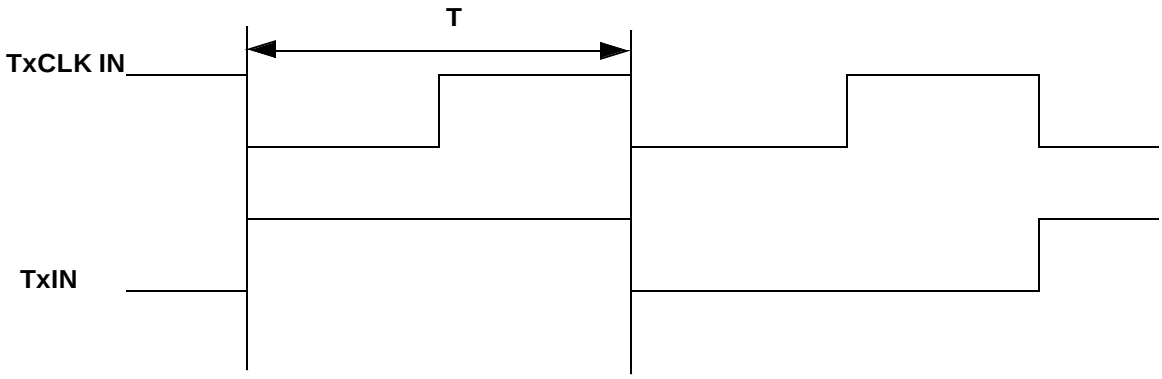


Figure 4. Test Pattern

AC TIMING DIAGRAMS

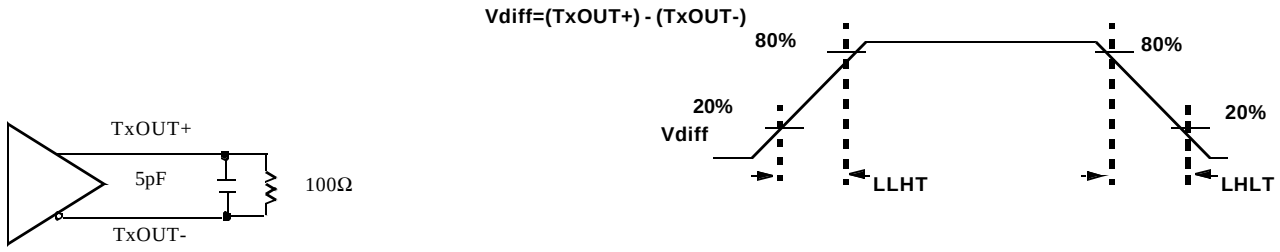


Figure 5. UT54LVDS217 Output Load and Transition Times

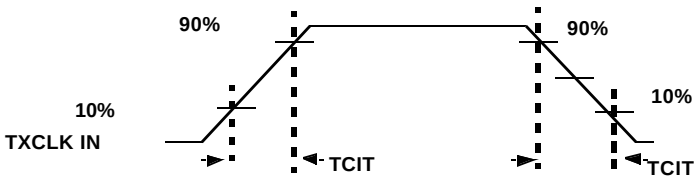
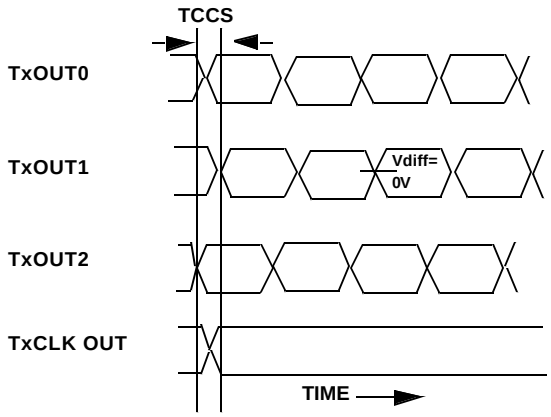


Figure 6. UT54LVDS217 Input Clock Transition Time



Notes:
1. Measurements at V_{DIFF} = 0V
2. TCCS measured between earliest and latest LVDS edges.
3. TxCLK Differential Low-High Edge.

Figure 7. UT54LVDS217 Channel-to-Channel Skew

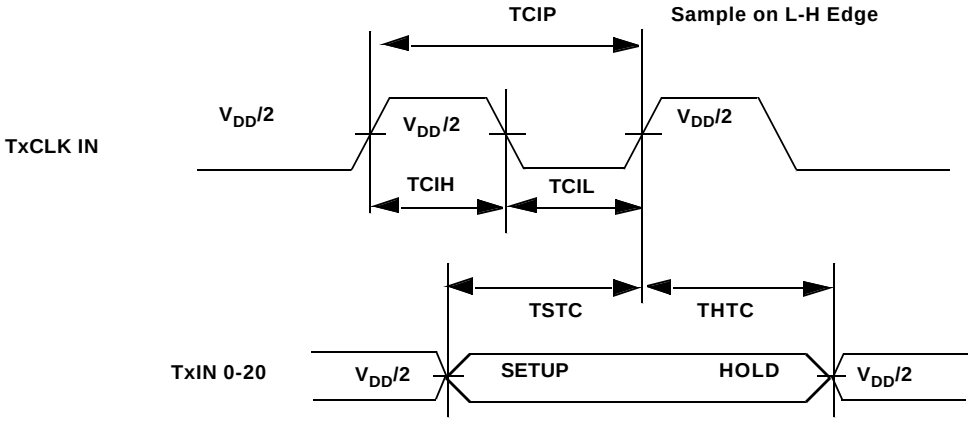


Figure 8. UT54LVDS217 Setup/Hold and High/Low Times

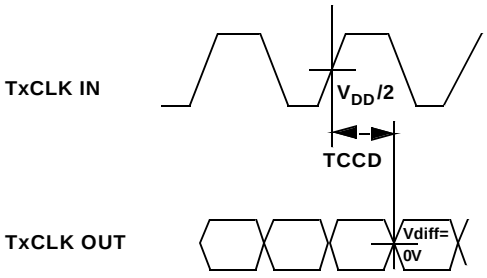


Figure 9. UT54LVDS217 Clock-to-Clock Out Delay

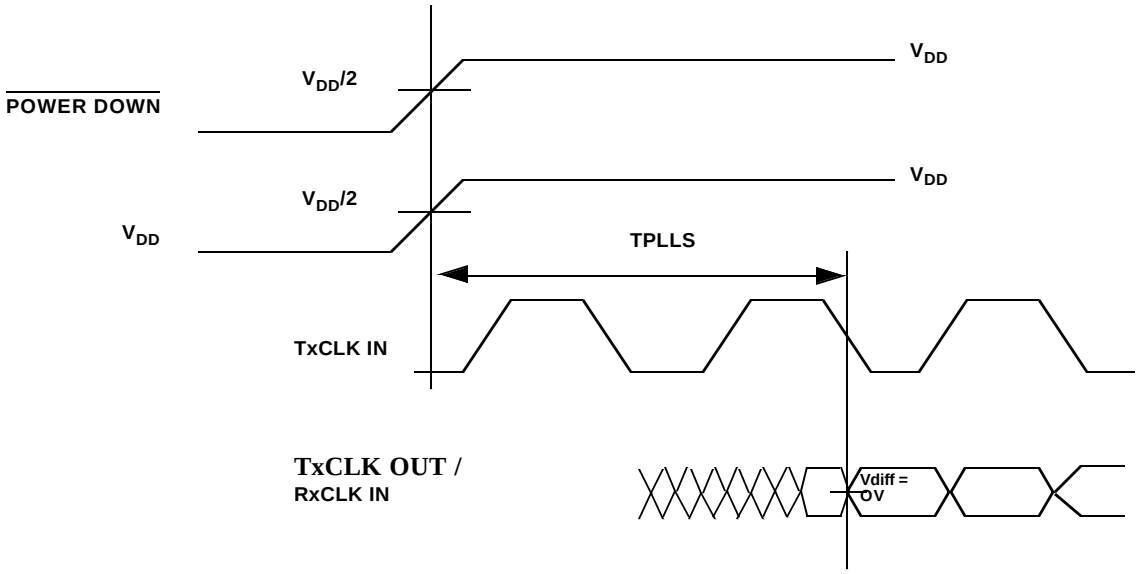


Figure 10. UT54LVDS217 Phase Lock Loop Set Time

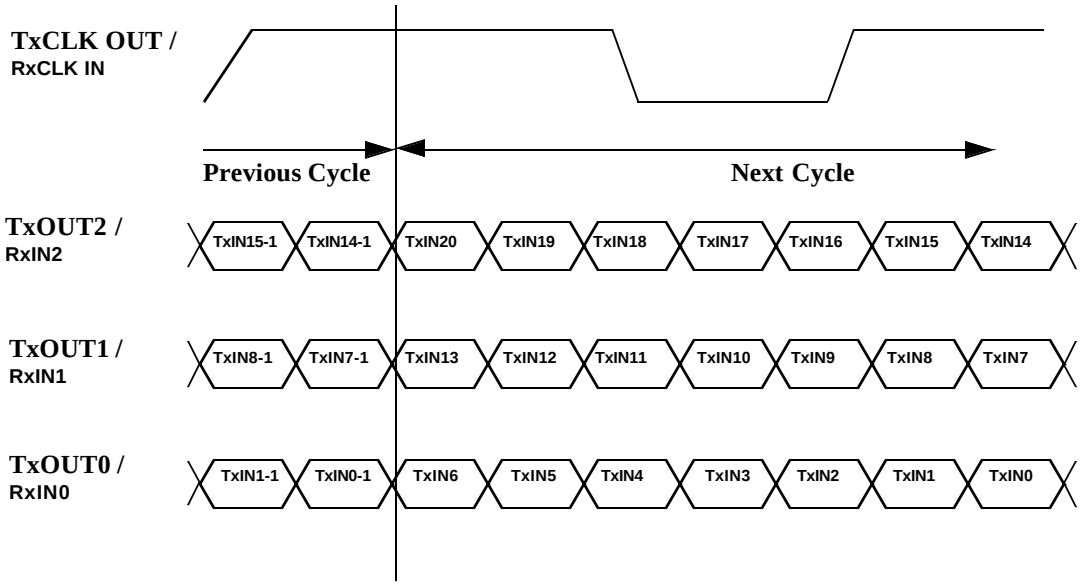


Figure 11. UT54LVDS217 Parallel TTL Data Inputs Mapped to LVDS Outputs

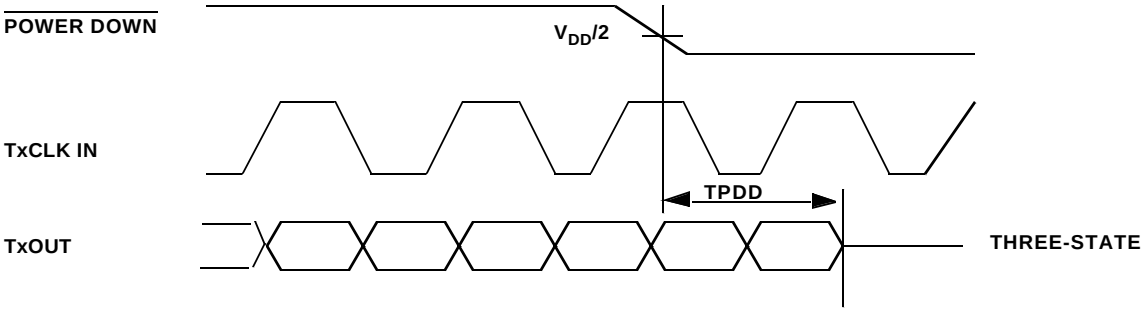


Figure 12. Transmitter Powerdown Delay

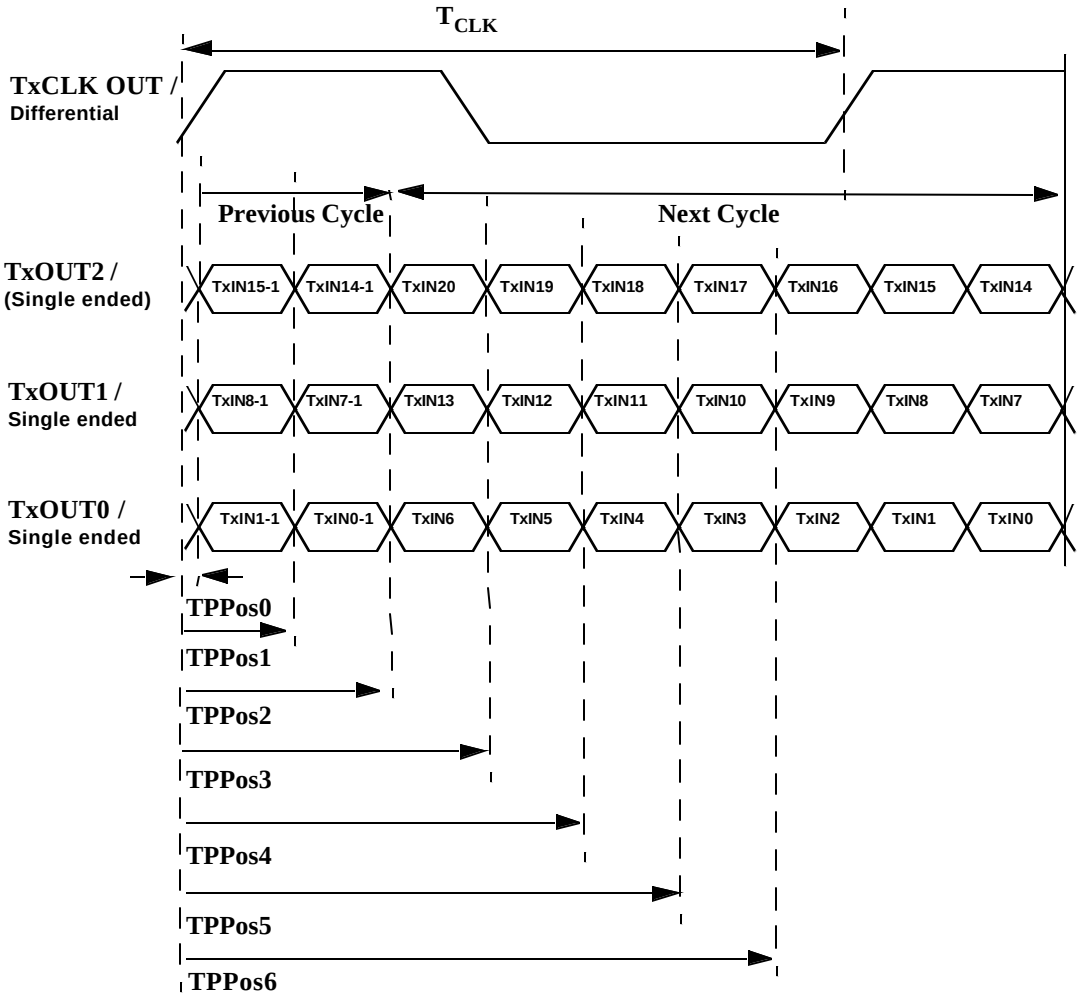


Figure 13. LVDS Output Pulse Position Measurement

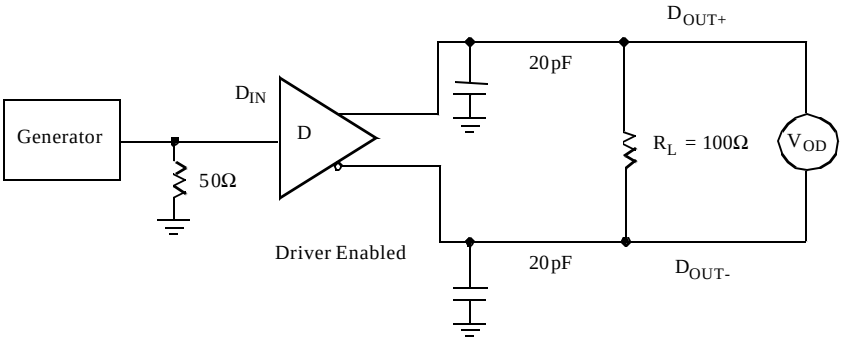
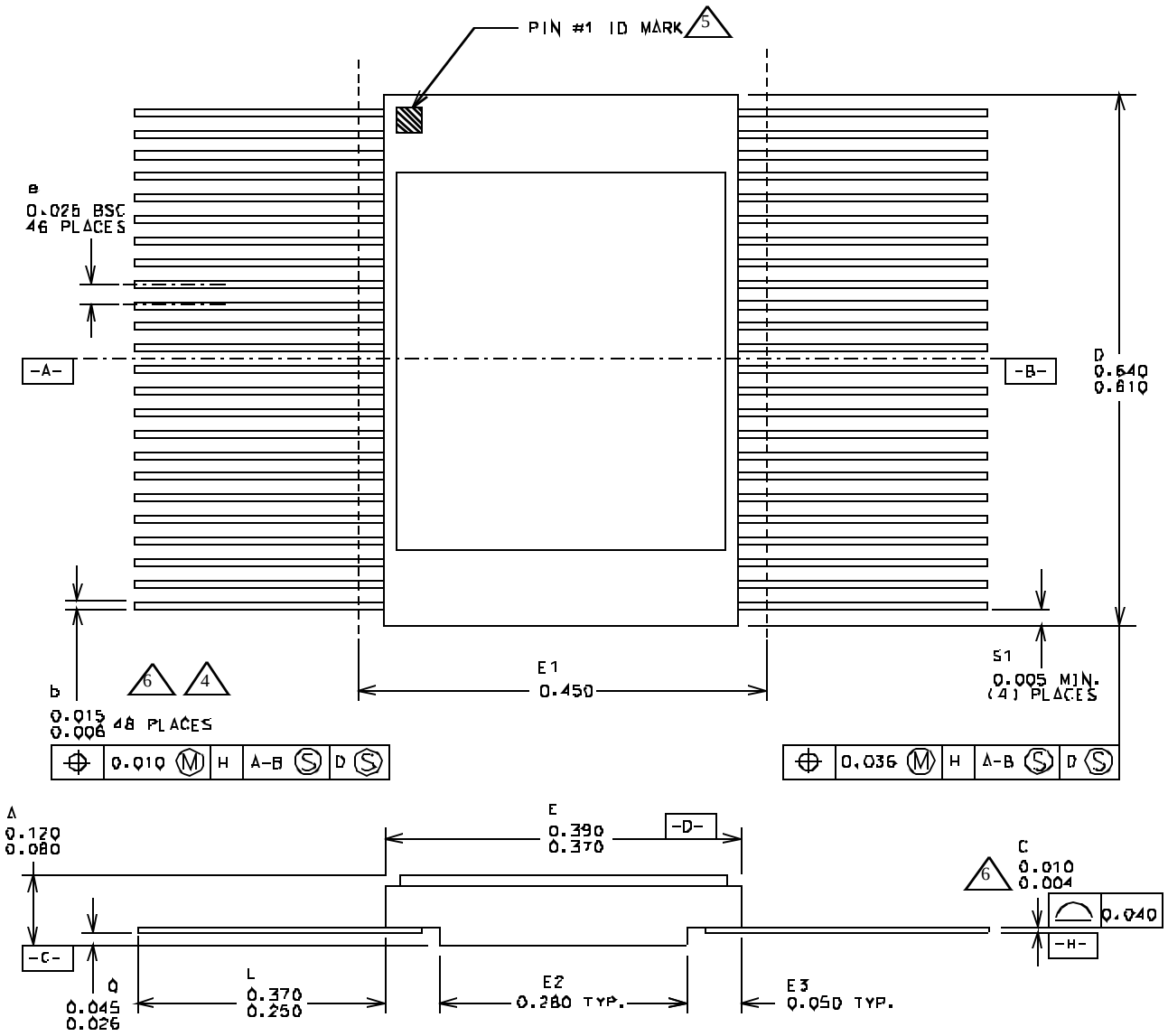


Figure 14. Driver V_{OD} and V_{OS} Test Circuit or Equivalent Circuit

PACKAGING

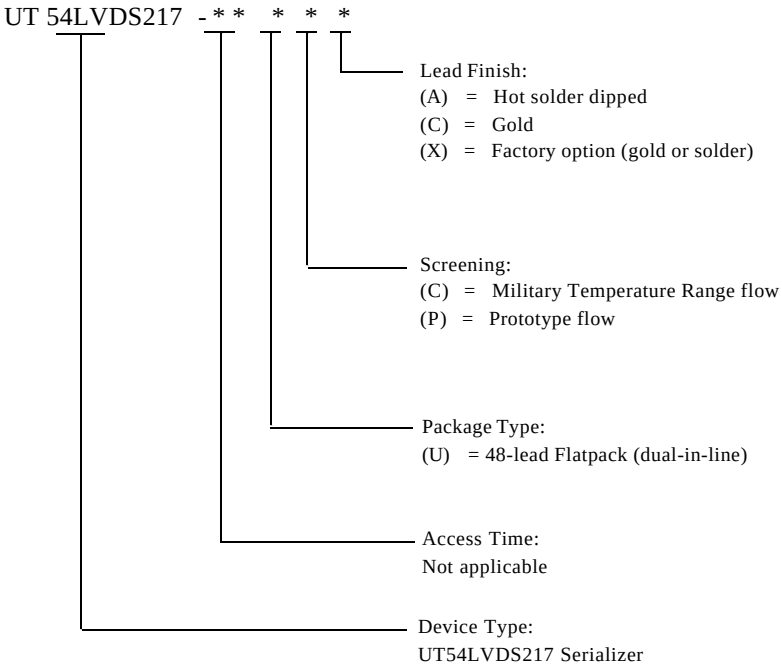


1. All exposed metalized areas are gold plated over electroplated nickel per MIL-PRF-38535.
2. The lid is electrically connected to VSS.
3. Lead finishes are in accordance with MIL-PRF-38535.
4. Lead position and colanarity are not measured.
5. ID mark symbol is vendor option.
6. With solder, increase maximum by 0.003.

Figure 15. 48-Lead Flatpack

ORDERING INFORMATION

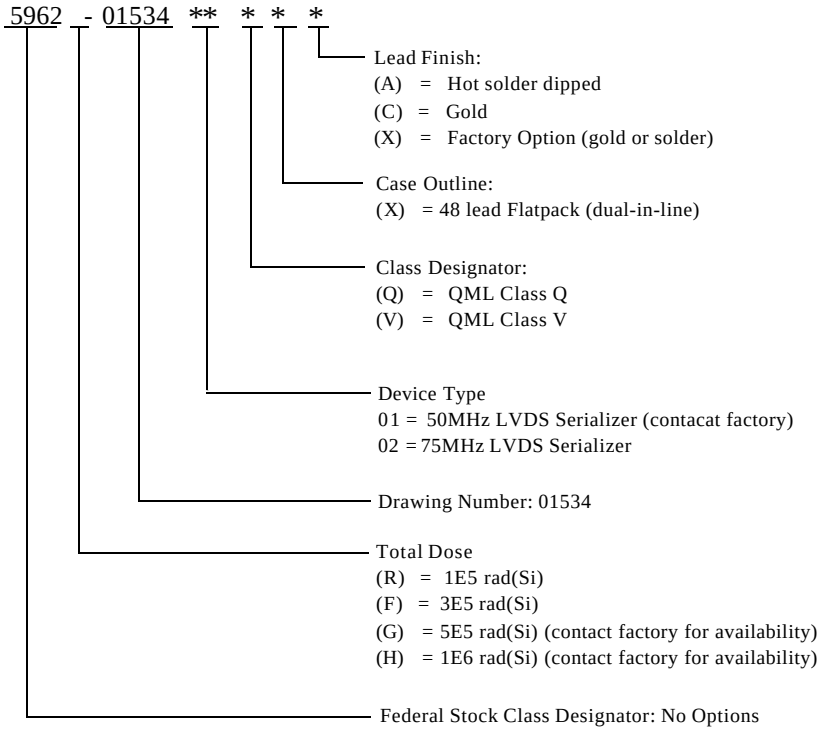
UT54LVDS217 Serializer:



Notes:

1. Lead finish (A,C, or X) must be specified.
2. If an "X" is specified when ordering, then the part marking will match the lead finish and will be either "A" (solder) or "C" (gold).
3. Prototype flow per UTMC Manufacturing Flows Document. Tested at 25°C only. Lead finish is GOLD ONLY. Radiation neither tested nor guaranteed.
4. Military Temperature Range flow per UTMC Manufacturing Flows Document. Devices are tested at -55°C, room temp, and 125 °C. Radiation neither tested nor guaranteed.

UT54LVDS217 Serializer: SMD



Notes:

1.Lead finish (A,C, or X) must be specified.

2.If an “X” is specified when ordering, part marking will match the lead finish and will be either “A” (solder) or “C” (gold).

3.Total dose radiation must be specified when ordering. QML Q and QML V not available without radiation hardening.