Marvell Avastar 88W8782 WLAN SoC

Supports SDIO for Connecting WLAN Activity to the Host

PRODUCT OVERVIEW

The Marvell® Avastar™ 88W8782 is a highly integrated wireless local area network (WLAN) system-on-chip (SoC), specifically designed to support high throughput data rates for next generation WLAN products and is part of the Marvell Avastar family of wireless devices. The Avastar family includes single-function and multi-function radios that establish new industry benchmarks for power consumption, wireless performance, solution footprint and advanced features.

The Marvell Avastar 88W8782 is designed to support IEEE 802.11a/g/b and 802.11n payload data rates. The device provides the combined functions of Direct Sequence Spread Spectrum (DSSS) and Orthogonal Frequency Division Multiplexing (OFDM) baseband modulation, Medium Access Controller (MAC), CPU, memory, host interfaces, and direct-conversion WLAN RF radio on a single integrated chip.

For security, the 88W8782 supports 802.11i security standards through implementation of the Advanced Encryption Standard (AES)/Counter Mode CBC-MAC Protocol (CCMP), Wired Equivalent Privacy (WEP) with Temporal Key Integrity Protocol (TKIP), Advanced Encryption Standard (AES)/Cipher-Based Message Authentication Code (CMAC), and WLAN Authentication and Privacy Infrastructure (WAPI) security mechanisms.

For video, voice, and multimedia applications, 802.11e Quality of Service (QoS) is supported. Also supported are 802.11h Dynamic Frequency Selection (DFS) for detecting radar pulses when operating in the 5 GHz range.

The device is also equipped with a coexistence interface for external, co-located 2.4 GHz radios.

The 88W8782 supports generic interfaces including SDIO and G-SPI for connecting WLAN activity to the host processor. Available packaging includes QFN and TFBGA options.

BLOCK DIAGRAM

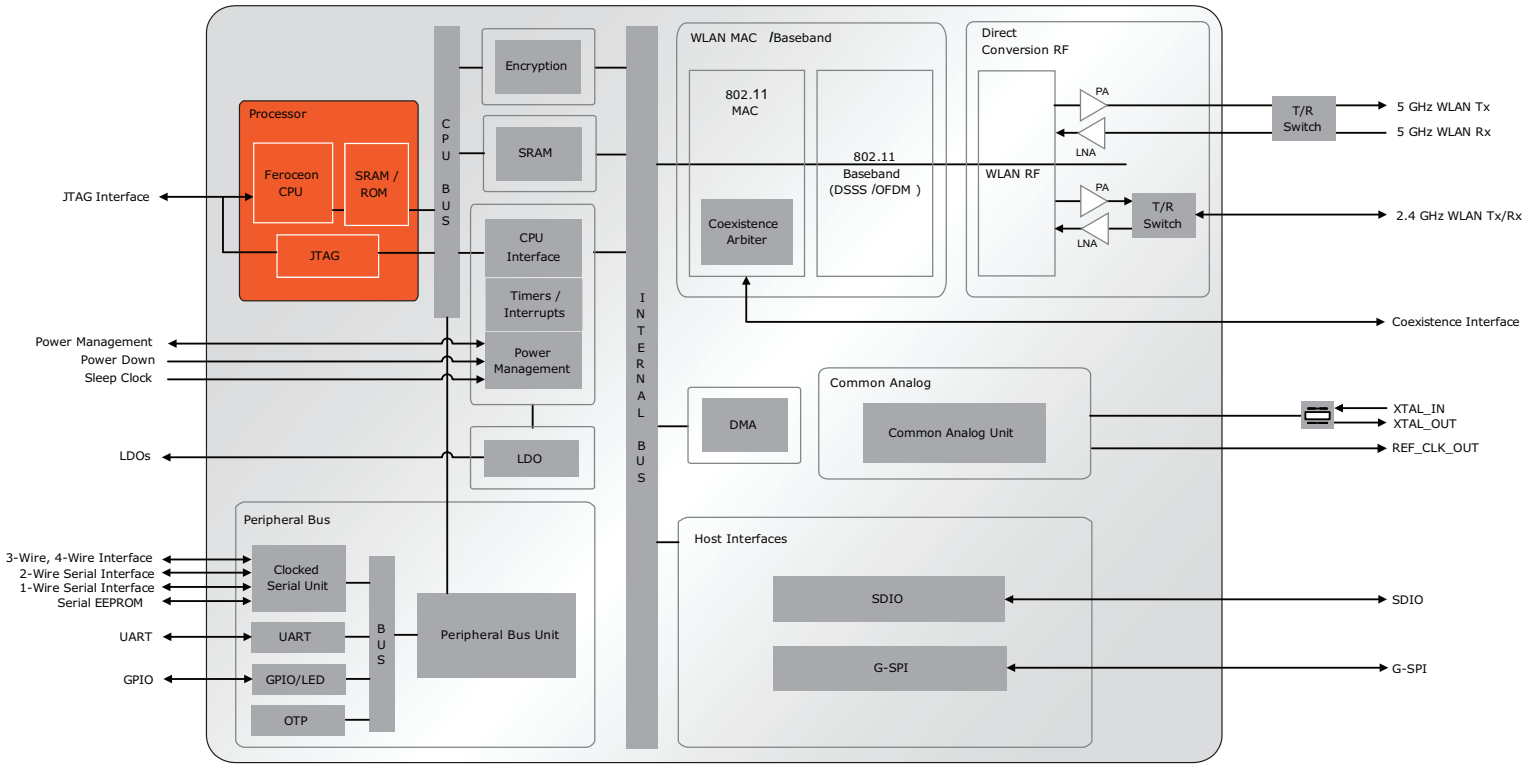

Fig 1. Avastar 88W8782 SoC Block Diagram

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SPECIFICATIONS

APPLICATIONS
- Imaging platforms (printers, digital still cameras (DSC), digital picture frames)
- Gaming platforms
- Consumer electronic devices (TV, DVD players, Blu-ray players, etc.)
- Cell phones and other mobile applications
- eBooks

GENERAL FEATURES
- Single-chip integration of 802.11 wireless radio, baseband, MAC, CPU, memory, host interface
- CMOS and low-swing sinewave input clock
- 12, 13, 19.2, 20, 24, 26, 38.4, 40, 44, and 52 MHz crystal clock support with auto-frequency detection if external sleep clock is available
- Low power operation supporting deep sleep and standby modes
- Power management with external sleep clock support for near zero deep sleep power
- Option to power directly from battery or to use 3.3V/1.8V/1.2V pre-regulated supplies
- One time programmable (OTP) memory to eliminate need for external EEPROM
- Fully compatible with Marvell Power Management device(s)

IEEE 802.11/STANDARDS
- 802.11 data rates of 1 and 2 Mbps
- 802.11b data rates of 5.5 and 11 Mbps
- 802.11a/g data rates 6, 9, 12, 18, 24, 36, 48, and 54 Mbps for multimedia content transmission
- 802.11g/b performance enhancements
- 802.11n compliant, with maximum data rates up to 72 Mbps (20 MHz channel) and 150 Mbps (40 MHz channel)
- 802.11d international roaming
- 802.11e QoS block acknowledgement (with support for 802.11n extension)
- 802.11h transmit power control
- 802.11h DFS radar pulse detection
- 802.11i enhanced security
- 802.11k radio resource measurement
- 802.11r fast hand-off for AP roaming
- 802.11w protected management frames
- Fully supports clients (stations) implementing IEEE Power Save mode
- Wi-Fi Direct connectivity

PACKAGING
- QFN
- TFBGA

PROCESSOR
- CPU
  - Integrated Marvell Feroceon® CPU (ARMv5TE-compliant)
  - 128 MHz maximum CPU clock speed
- DMA
  - Independent 2-Channel Direct Memory Access (DMA)

MEMORY
- Internal SRAM for Tx frame queues/Rx data buffers
- Boot ROM
- ROM patching capability

WLAN MAC
- Ad-Hoc and Infrastructure Modes
- RTS/CTS for operation under DCF
- Hardware filtering of 32 multicast addresses and duplicate frame detection for up to 32 unicast addresses
- On-chip Tx and Rx FIFO for maximum throughput
- Open System and Shared Key Authentication services
- A-MPDU Rx (de-aggregation) and Tx (aggregation)
- 20/40 MHz coexistence
- Reduced Inter-Frame Spacing (RIFS) bursting
- Management information base counters
- Radio resource measurement counters
- Block acknowledgement with 802.11n extension
- Dynamic frequency selection (DFS)
- Transmit beamformee support
- Transmit rate adaptation
- Transmit power control
- Long and short preamble generation on a frame-by-frame basis for 802.11b frames
- Marvell Mobile Hotspot

WLAN BASEBAND
- 802.11n 1x1 SISO (on-chip Marvell SISO RF radio)
- Backward compatibility with legacy 802.11a/g/b technology
- PHY data rates up to 150 Mbps
- 20 MHz bandwidth/channel, 40 MHz bandwidth/channel, upper/lower 20 MHz bandwidth in 40 MHz channel, and 20 MHz duplicate legacy bandwidth in 40 MHz channel mode operation
- Modulation and Coding Scheme (MCS)—0~7 and 32 (duplicate 6 Mbps)
- Enhanced radar detection for long and short pulse radar
- Enhanced AGC scheme for DFS channel
- Japan DFS requirements for W53 and W56
- Radio resource measurement
- Optional 802.11n SISO features:
  - 20/40 MHz coexistence
  - 1-stream STBC reception
  - Short guard interval
  - RIFS on receive path
  - Beamformee function and hardware acceleration
  - Greenfield Tx/Rx
- Power save features

WLAN RADIO
- Integrated direct-conversion radio
- 20 and 40 MHz channel bandwidths
- Integrated T/R switch, PA, and LNA for 2.4 GHz path
- Integrated PA and LNA for 5 GHz path

- WLAN Rx Path
  - Direct conversion architecture eliminates need for external SAW filter
  - On-chip gain selectable LNAs with optimized noise figure and power consumption
  - High dynamic range AGC function in receive mode

- WLAN Tx Path
  - Integrated power amplifiers with power control
  - Closed/open loop power control (0.5 dB increments)
  - Optimized Tx gain distribution for linearity and noise performance

- WLAN Local Oscillator
  - Fractional-N for multiple reference clock support
  - Fine channel step, AFC (adaptive frequency control)

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SPECIFICATIONS

WLAN ENCRYPTION

- WEP 64- and 128-bit encryption with hardware TKIP processing (WPA)
- AES-CCMP hardware implementation as part of 802.11i security standard (WPA2)
- Enhanced AES engine performance
- AES-Cipher-Based Message Authentication Code (CMAC) as part of the 802.11w security standard
- WLAN Authentication and Privacy Infrastructure (WAPI)

COEXISTENCE

- Coexistence interface for external, co-located 2.4 GHz radio
  - Marvell 3/4-wire interface
  - WL_ACTIVE 3/4-wire interface
  - WL_ACTIVE 2-wire interface

HOST INTERFACES

- SDIO device interface (SPI, 1-bit SDIO, 4-bit SDIO transfer modes at full clock range up to 75 MHz)
- G-SPI device interface
- USB 2.0 interface

PERIPHERAL BUS INTERFACES

- Clocked Serial Unit (CSU)
  - 3-Wire, 4-Wire Serial Interface
  - 2-Wire Serial Interface
  - 1-Wire Serial Interface
  - SPI EEPROM Interface
- 16550 UART
- General Purpose Input Output (GPIO)
- OTP memory to eliminate need for external EEPROM

TEST

- On-chip diagnostic information

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