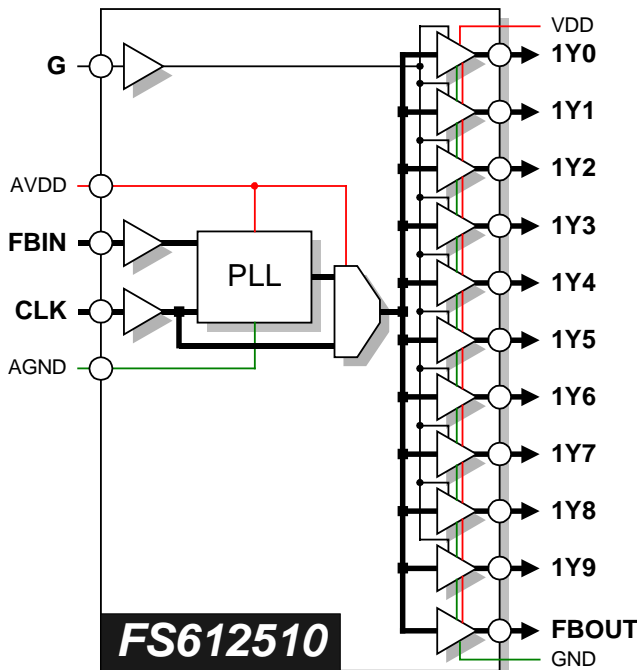


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### 1.0 Features

- Generates one bank of ten clock outputs (1Y0 to 1Y9) from one reference clock input (CLK)
- Designed to meet the PLL Component Specifications as noted in the PC133 SDRAM Registered DIMM Design Specification
- External feedback input (FBIN) to synchronize all clock outputs to the reference input
- Operating frequency 25MHz to 140MHz
- Tight tracking skew (spread-spectrum tolerant)
- On-chip 25Ω series damping resistors for driving point-to-point loads
- Output enable (G) enables or disables low all clock outputs
- Available with an auto power-down option that turns off the PLL and forces all outputs low when the reference clock stops (FS612510-02)
- Packaged in a 24-pin TSSOP

Figure 1: Block Diagram



### 2.0 Description

The FS612510 is a low skew, low jitter CMOS zero-delay phase-locked loop (PLL) clock buffer IC designed for high-speed motherboard applications, such as those using 133MHz SDRAM.

Ten buffered clock outputs are derived from an onboard open-loop PLL. The PLL aligns the frequency and phase of all output clocks to the reference input clock CLK, including an FBOUT clock that feeds back to FBIN to close the loop. Multiple power and ground supplies help reduce the effects of noise on device performance.

All ten outputs 1Y0 to 1Y9 are enabled and disabled low by the active-high G signal. The PLL can be bypassed for test purposes by pulling AVDD to ground.

Figure 2: Pin Configuration

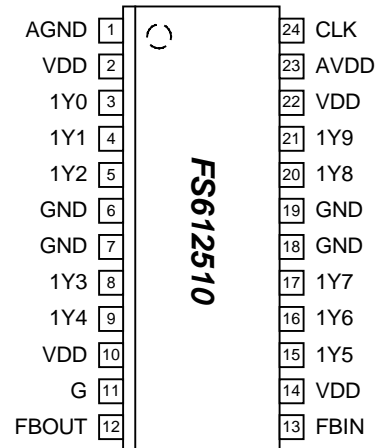


Table 1: Function Table

PLL	INPUT			OUTPUT	
	AVDD	G	CLK	1Y0-1Y9	FBOUT
Zero-Delay	H	L	L	L	L
	H	L	H	L	H
	H	H	L	L	L
	H	H	H	H	H
PLL Bypass	L	L	L	L	L
	L	L	H	L	H
	L	H	L	L	L
	L	H	H	H	H

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**Table 2: Pin Descriptions**

Key: AI = Analog Input; AO = Analog Output; DI = Digital Input; DI<sup>U</sup> = Input with Internal Pull-Up; DI<sub>D</sub> = Input with Internal Pull-Down; DIO = Digital Input/Output; DI-3 = Three-Level Digital Input, DO = Digital Output; P = Power/Ground; # = Active Low pin

PIN	TYPE	NAME	DESCRIPTION
3	DO	1Y0	Clock output
4	DO	1Y1	Clock output
5	DO	1Y2	Clock output
8	DO	1Y3	Clock output
9	DO	1Y4	Clock output
15	DO	1Y5	Clock output
16	DO	1Y6	Clock output
17	DO	1Y7	Clock output
20	DO	1Y8	Clock output
21	DO	1Y9	Clock output
23	P	AVDD	Power Supply / Test mode enable. This pin provides the power supply to the internal PLL. When the pin is pulled low, the PLL is bypassed and the output clocks directly follow the input clock
1	P	AGND	PLL supply ground
24	DI	CLK	Reference clock input ( <i>Note: -02 version has a pull-down on this pin</i> )
13	DI	FBIN	Feedback clock input; must be connected to FBOUT to complete the loop
12	DO	FBOUT	Feedback output clock
11	DI	G	Output enable stops all clocks (1Y0 – 1Y9) in a low state when this pin is low
6, 7, 18, 19	P	GND	Ground for all clock outputs
2, 10, 14, 22	P	VDD	Power supply for all clock outputs

Enabled by G

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### 3.0 Device Operation

The FS612510 is a zero-delay buffer intended for use on buffered PC133 SDRAM DIMMs.

The FS612510 precisely aligns the frequency and phase of the output clocks to the input CLK by use of an on-chip phase-lock loop (PLL). The PLL generates up to 10 low-skew, low-jitter copies of the CLK, with the outputs adjusted for 50% duty cycle.

The FBOUT clock must be hardwired to the FBIN pin to complete the loop. The PLL actively adjusts the output clocks so that there is no phase error between the reference clock (CLK) and the feedback clock (FBIN).

Since the device uses a PLL to lock the output clocks to the input clock, there is a power-up stabilization time that is required for the PLL to achieve phase lock.

Note that all inputs and outputs use LVCMOS signal levels.

#### 3.1 PLL Bypass

When the AVDD pin is pulled low, the reference clock signal bypasses the PLL and is muxed directly through to the outputs. The PLL is powered down, and device acts a fanout buffer.

Note that if AVDD is re-established, the PLL requires a power-up and stabilization time to lock to the input clock.

#### 3.2 Output Enable/Disable

All ten outputs are enabled or disabled as a group by the G enable signal.

A logic-high on G input enables all the clock outputs to swing in phase with the reference clock. A logic-low on G forces all of the clock outputs to a logic-low state.

The function table Table 1 shows the effect of the G enable signal on the clock outputs.

#### 3.3 Power-Down

The FS612510-02 version provides an auto power-down feature that shuts off the PLL, drives all outputs low, and places the device into a low current state if the reference clock stops. The power-down circuit is level sensitive, and detects either a DC high or low on the CLK input.

#### 4.0 Tracking Skew

PLL-based buffer ICs may be required to follow a spread-spectrum modulated reference clock for frequencies greater than 66MHz. Spread spectrum modulation limits peak EMI emissions by intentionally introducing jitter onto a clock signal, effectively spreading the peak energy over a range of frequencies.

A downstream PLL, contained in a clock buffer IC such as this one, must carefully track the modulated input reference clock. A measure of how closely the downstream PLL follows the modulated clock is called the tracking skew. To ensure a tight tracking skew, the loop bandwidth of a downstream PLL is increased and the loop phase angle is reduced over that of typical PLL-based clock generators.

The type of modulation profile used impacts tracking skew. The maximum frequency change occurs at the profile limits where the modulation changes the slew rate polarity. To track the sudden reversal in clock frequency, the downstream PLL must have a large loop bandwidth. The ability of the downstream PLL to catch up to the modulating clock is determined by the loop transfer function phase angle.

The spread-spectrum reference clock should be either a triangle-wave or a non-linear (Lexmark) modulation profile, with a modulation frequency of 50kHz or less.

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### 5.0 Electrical Specifications

**Table 3: Absolute Maximum Ratings**

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These conditions represent a stress rating only, and functional operation of the device at these or any other conditions above the operational limits noted in this specification is not implied. Exposure to maximum rating conditions for extended conditions may affect device performance, functionality, and reliability.

PARAMETER	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage, dc, Clock Buffers ( $V_{SS} = \text{ground}$ )	$AV_{DD}$	$V_{SS} - 0.5$	7	V
Supply Voltage, dc, Core	$V_{DD}$	$V_{SS} - 0.5$	7	V
Input Voltage, dc	$V_I$	$V_{SS} - 0.5$	$V_{DD}+0.5$	V
Output Voltage, dc	$V_O$	$V_{SS} - 0.5$	$V_{DD}+0.5$	V
Input Clamp Current, dc ( $V_I < 0$ or $V_I > V_{DD}$ )	$I_{IK}$	-50	50	mA
Output Clamp Current, dc ( $V_I < 0$ or $V_I > V_{DD}$ )	$I_{OK}$	-50	50	mA
Storage Temperature Range (non-condensing)	$T_S$	-65	150	°C
Ambient Temperature Range, Under Bias	$T_A$	-55	125	°C
Junction Temperature	$T_J$		125	°C
Lead Temperature (soldering, 10s)			260	°C
Static Discharge Voltage Protection (MIL-STD 883E, Method 3015.7)			2	kV



**CAUTION: ELECTROSTATIC SENSITIVE DEVICE**

Permanent damage resulting in a loss of functionality or performance may occur if this device is subjected to a high-energy electrostatic discharge.

**Table 4: Operating Conditions**

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	MIN.	TYP.	MAX.	UNITS
Supply Voltage, Core and Outputs	$V_{DD}$	$3.3V \pm 10\%$	3.0	3.3	3.6	V
Ambient Operating Temperature Range	$T_A$		0		70	°C
Output Load Capacitance	$C_L$				15	pF
Input Frequency	$f_{CLK}$	CLK	50		140	MHz
Input Duty Cycle		CLK	40		60	%
Input Rise/Fall Time		CLK			3	ns

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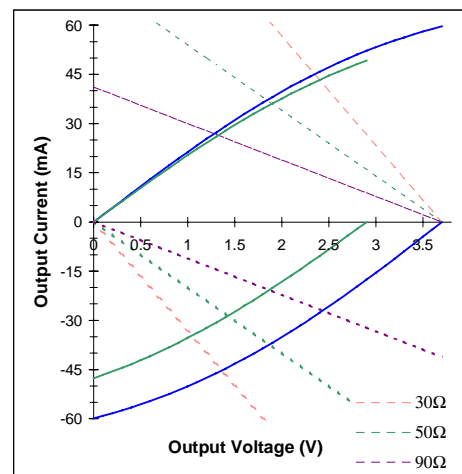
**Table 5: DC Electrical Specifications**

Unless otherwise stated, all power supplies = 3.3V%, no load on any output, and ambient temperature range  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ . Parameters denoted with an asterisk ( \* ) represent nominal characterization data and are not currently production tested to any specific limits. MIN and MAX characterization data are  $\pm 3\sigma$  from typical. Negative currents indicate current flows out of the device.

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	MIN.	TYP.	MAX.	UNITS
<b>Overall</b>						
Supply Current, Dynamic		$f_{\text{CLK}} = 133.33\text{MHz}$ ; $V_{\text{DD}} = 3.3\text{V}$		135		mA
Supply Current, Static	$I_{\text{DDL}}$	Outputs low; $V_{\text{DD}} = 3.3\text{V}$		3		mA
<b>Output Enable Input (G)</b>						
High-Level Input Voltage	$V_{\text{IH}}$		2.0		$V_{\text{DD}}+0.3$	V
Low-Level Input Voltage	$V_{\text{IL}}$		$V_{\text{SS}}-0.3$		0.8	V
Input Leakage Current	$I_{\text{I}}$		-5		5	$\mu\text{A}$
<b>Clock Inputs (CLK, FBIN)</b>						
High-Level Input Voltage	$V_{\text{IH}}$		2.0		$V_{\text{DD}}+0.3$	V
Low-Level Input Voltage	$V_{\text{IL}}$		$V_{\text{SS}}-0.3$		0.8	V
Input Leakage Current	$I_{\text{I}}$	-01 version -02 version has a pull-down on CLK	-5	28	5	$\mu\text{A}$
Input Loading Capacitance *	$C_{\text{L(in)}}$	As seen by an external clock driver		4		pF
<b>Clock Outputs (1Y0:9, FBOUT)</b>						
High-Level Output Source Current	$I_{\text{OH}}$	$V_{\text{DD}} = 2.9\text{V}$ , $V_{\text{O}} = 2.0\text{V}$ $V_{\text{DD}} = 3.7\text{V}$ , $V_{\text{O}} = 2.0\text{V}$		-18 -35	-12 -12	mA
Low-Level Output Sink Current	$I_{\text{OL}}$	$V_{\text{DD}} = 2.9\text{V}$ , $V_{\text{O}} = 0.8\text{V}$ $V_{\text{DD}} = 3.7\text{V}$ , $V_{\text{O}} = 0.8\text{V}$	12 12	16 17		mA
Output Impedance	$Z_{\text{O}}$			33		$\Omega$
Tristate Output Current	$I_{\text{OZ}}$		-10		10	$\mu\text{A}$
Short Circuit Source Current *	$I_{\text{OSH}}$	$V_{\text{O}} = 0\text{V}$ ; shorted for 30s, max.		-60		mA
Short Circuit Sink Current *	$I_{\text{OSL}}$	$V_{\text{O}} = 3.3\text{V}$ ; shorted for 30s, max.		90		mA

**Table 6: Clock Output Drive (1Y0:4, 2Y0:3, FBOUT)**

Voltage	Low Drive Current (mA)		High Drive Current (mA)	
	MIN	MAX	MIN	MAX
0.1 V	-47	-59	2	2
0.2 V	-45	-58	4	4
0.4 V	-43	-56	8	9
0.6 V	-40	-55	12	13
0.8 V	-38	-52	16	17
1.0 V	-35	-50	20	21
1.2 V	-32	-47	24	25
1.4 V	-29	-45	27	29
1.6 V	-26	-41	31	33
1.8 V	-22	-38	34	36
2.0 V	-18	-35	38	40
2.2 V	-15	-31	41	43
2.4 V	-10	-28	43	46
2.6 V	-6	-24	45	49
2.8 V	-2	-20	48	51
3.0 V	0	-15	49	53
3.3 V		-9		56
3.6 V		-2		59



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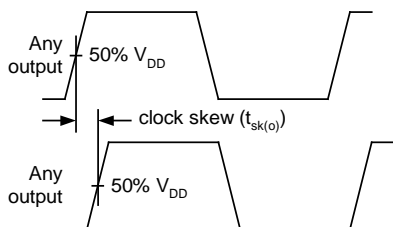
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**Table 7: AC Timing Specifications**

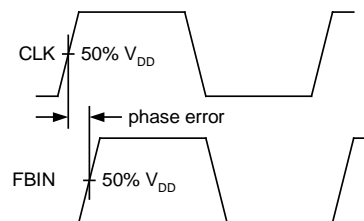
Unless otherwise stated, all power supplies = 3.3V, no load on any output, and ambient temperature  $T_A = 25^\circ\text{C}$ . Parameters denoted with an asterisk ( \* ) represent nominal characterization data and are not currently production tested to any specific limits. MIN and MAX characterization data are  $\pm 3\sigma$  from typical.

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	MIN.	TYP.	MAX.	UNITS
<b>Overall</b>						
Skew, Output to Output *	$t_{sk(o)}$	Measured on the rising edge at 1.65V; $C_L = 15\text{pF}$			150	ps
Skew, Tracking *		Measured using a $-0.5\%$ 31.5kHz spread spectrum reference clock at 133.33MHz			150	ps
Static Phase Error *		From rising edge on CLK to rising edge on FBIN		-120		ps
Clock Stabilization Time *		Time required for the PLL to achieve phase lock			3	ms
Loop Bandwidth *		For calculation of Tracking Skew			1.2	MHz
Phase Angle *		For calculation of Tracking Skew			-0.031	$^\circ$
<b>Clock Outputs (1Y0:9, FBOU7)</b>						
Duty Cycle *	$d_t$	Ratio of high pulse width to one clock period, measured at 1.65V	45		55	%
Jitter, Cycle-Cycle *	$t_{j(cc)}$	Adjacent cycles at 1.65V	-75		+75	ps
Jitter, Period (peak-peak) *	$t_{j(\Delta P)}$	From rising edge to next rising edge at 1.65V				
Rise Time *	$t_r$	$V_O = 0.4\text{V}$ to $2.0\text{V}$ ; $C_L = 15\text{pF}$		1.2		ns
Fall Time *	$t_f$	$V_O = 2.0\text{V}$ to $0.4\text{V}$ ; $C_L = 15\text{pF}$		1.4		ns
Enable Delay *	$t_{DLH}$	via G	1		10	ns
Disable Delay *	$t_{DHL}$	via G	1		10	ns

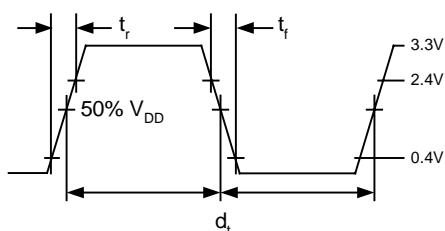
**Figure 3: Clock Skew Measurement**



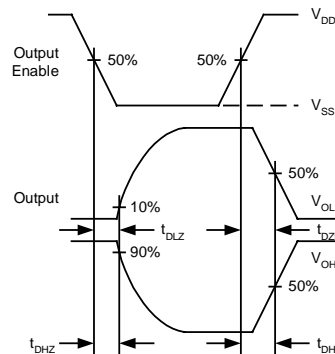
**Figure 4: Phase Error Measurement**



**Figure 5: Timing Measurement Points**



**Figure 6: Output Enable Measurement**

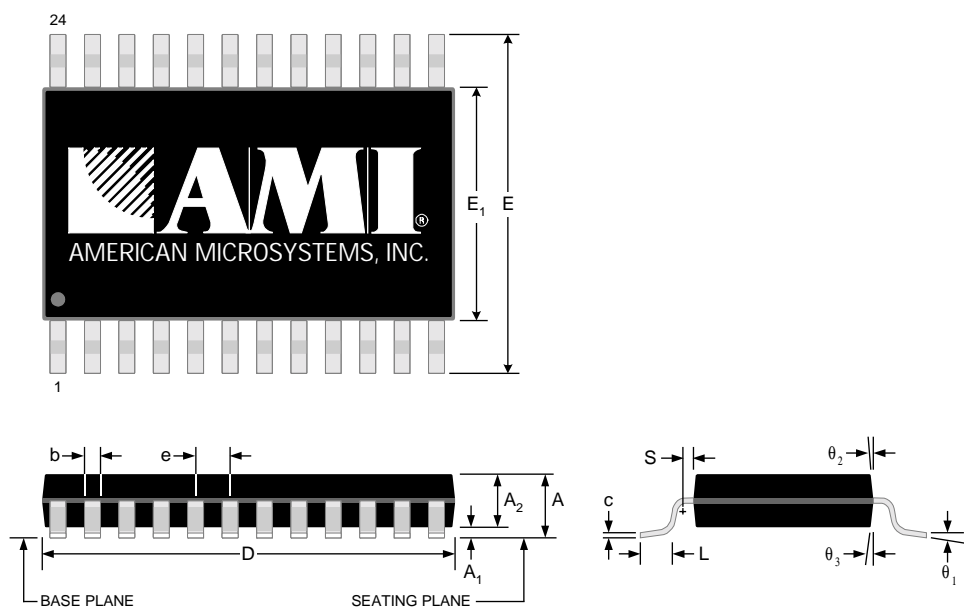


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### 6.0 Package Information

**Table 8: 24-pin TSSOP Package Dimensions**

	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	-	0.047	-	1.20
A <sub>1</sub>	0.002	0.006	0.05	0.15
A <sub>2</sub>	0.0315	0.0413	0.80	1.05
b	0.0075	0.0118	0.19	0.30
C	0.0035	0.0079	0.09	0.20
D	0.303	0.311	7.70	7.90
E <sub>1</sub>	0.169	0.177	4.30	4.50
E	0.252		6.40 BSC	
e	0.0256		0.65 BSC	
L	0.0177	0.0295	0.45	0.75
S	0.0079	-	0.20	-
θ <sub>1</sub>	0°	8°	0°	8°
θ <sub>2</sub>	12 REF		12 REF	
θ <sub>3</sub>	12 REF		12 REF	



**Table 9: 24-pin TSSOP Package Characteristics**

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	TYP.	UNITS
Thermal Impedance, Junction to Free-Air	θ <sub>JA</sub>	Air flow = 0 m/s	84	°C/W
Lead Inductance, Self	L <sub>11</sub>	Longest lead	1.7	nH
Lead Inductance, Mutual	L <sub>12</sub>	Longest lead to any 1 <sup>st</sup> adjacent lead	0.6	nH
	L <sub>13</sub>	Longest lead to any 2 <sup>nd</sup> adjacent lead	0.24	
Lead Capacitance, Bulk	C <sub>11</sub>	Longest lead to V <sub>SS</sub>	0.3	pF
Lead Capacitance, Mutual	C <sub>12</sub>	Longest lead to any 1 <sup>st</sup> adjacent lead	0.1	pF
	C <sub>13</sub>	Longest lead to any 2 <sup>nd</sup> adjacent lead	0.007	

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### 7.0 Ordering Information

**Table 10: Device Ordering Codes**

DEVICE NUMBER	ORDERING CODE	PACKAGE TYPE	OPERATING TEMPERATURE RANGE	SHIPPING CONFIGURATION
FS612510-01	<b>12055-102</b>	24-pin TSSOP (Thin Shrink Small Outline Package)	0°C to 70°C (Commercial)	Tape and Reel
FS612510-02	<b>12055-103</b>	24-pin TSSOP (Thin Shrink Small Outline Package)	0°C to 70°C (Commercial)	Tape and Reel

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