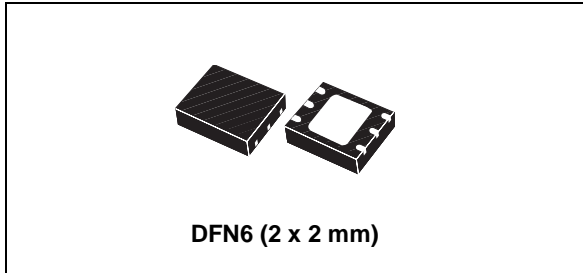


150 mA - ultra low noise - high PSRR linear voltage regulator IC

Datasheet - production data



- Internal current and thermal limit
- Package DFN6 (2 x 2 mm)
- Temperature range: - 40 °C to 125 °C

Description

The LDLN015 is an ultra low noise linear regulator which provides 150 mA maximum current from an input voltage ranging from 2.1 V to 5.5 V with a typical dropout voltage of 86 mV. With its 6.3 μV_{RMS} noise value in a band from 10 Hz to 100 kHz, the LDLN015 provides a very clean output suitable for ultra sensitive loads. It is stable with ceramic capacitors. High PSRR, low quiescent current and very low noise features make it suitable for low power battery powered applications. Power supply rejection is higher than 90 dB at low frequencies and starts to roll off at 10 kHz. The enable logic control function puts the LDLN015 into shutdown mode allowing a total current consumption lower than 1 μA . The device also includes a short-circuit constant current limiting and thermal protection. Typical applications are noise sensitive loads like ADC, VCO in mobile phones, and personal digital assistants (PDAs).

Features

- Ultra low noise: 6.3 μV_{RMS} from 10 Hz to 100 kHz
- Input voltage from 2.1 to 5.5 V
- Very low quiescent current (17 μA typ. at no load, 54 μA typ. at 150 mA load; 2 μA max. in off mode)
- Output voltage tolerance: $\pm 1\%$ at 25 °C
- 150 mA guaranteed output current
- Wide range of output voltage from 0.8 V to 3.3 V with 100 mV step
- Logic-controlled electronic shutdown
- Compatible with ceramic capacitor ($C_{\text{OUT}} = 0.47 \mu\text{F}$)
- No bypass capacitor is required

Table 1. Device summary

Order codes	Output voltages
LDLN015PU10R	1.0 V
LDLN015PU12R	1.2 V
LDLN015PU15R	1.5 V
LDLN015PU18R	1.8 V
LDLN015PU25R	2.5 V
LDLN015PU28R	2.8 V
LDLN015PU30R	3.0 V
LDLN015PU33R	3.3 V

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1 Application diagram

Figure 1. Block diagram

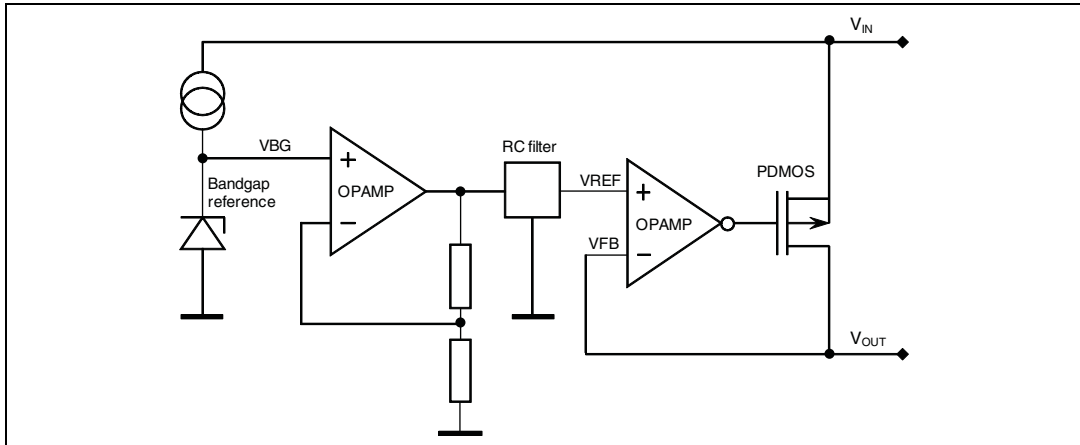
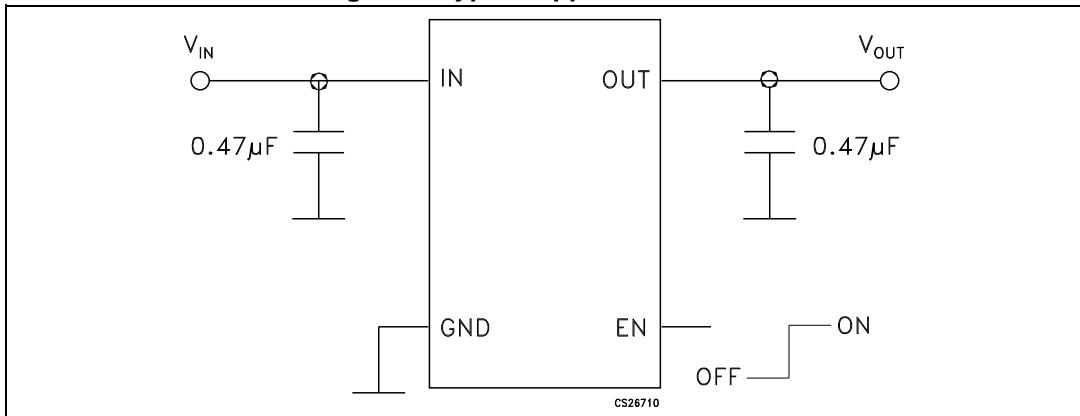


Figure 2. Typical application circuit



2 Pin configuration

Figure 3. Pin connections (top view)

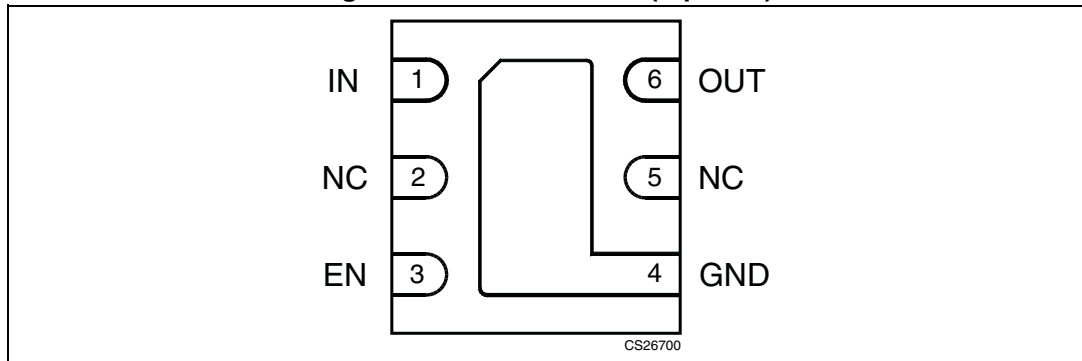


Table 2. Pin description

Pin n°	Symbol	Name and function
1	IN	Input voltage
2	NC	Not connected
3	EN	Enable input. Set $V_{EN} > 0.9$ to turn on the device Set $V_{EN} < 0.4$ to turn off the device
4	GND	Ground
5	NC	Not connected
6	OUT	Output voltage

Note: Exposed pad is electrically connected to GND.

3 Maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{IN}	DC input voltage	-0.3 to 7	V
V_{OUT}	DC output voltage	from -0.3 to 4.6	V
V_{EN}	Enable input voltage	from -0.3 to $V_{IN} + 0.3$	V
I_{OUT}	Output current	Internally limited	mA
P_D	Power dissipation	Internally limited	mW
T_{STG}	Storage temperature range	-65 to 150	°C
T_{OP}	Operating junction temperature range	-40 to 125	°C
ESD	Human body model	± 3	kV
	Machine model	± 300	V

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

Table 4. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction-ambient	105	°C/W
R_{thJC}	Thermal resistance junction-case	20	°C/W

4 Electrical characteristics

$T_J = 25\text{ }^\circ\text{C}$, $V_{IN} = V_{OUT(NOM)} + 1\text{ V}$, $C_{IN} = C_{OUT} = 0.47\text{ }\mu\text{F}$, $I_{OUT} = 1\text{ mA}$, $V_{EN} = V_{IN}$, unless otherwise specified.

Table 5. Electrical characteristics (1) (2)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IN}	Operating input voltage		2.1		5.5	V
V_{OUT}	V_{OUT} accuracy	$I_{OUT} = 1\text{ mA}$	-1		1	%
		$-40^\circ\text{C} < T_J < 125^\circ\text{C}$, $I_{OUT} = \text{from } 1\text{ mA to } 150\text{ mA}$, $V_{IN} = V_{OUT(NOM)} + 1\text{ V to } 5.5$	-2		2	
ΔV_{OUT}	Static line regulation	$V_{OUT} + 1\text{ V} \leq V_{IN} \leq 5.5\text{ V}$, $I_{OUT} = 1\text{ mA}$		0.005		%/V
ΔV_{OUT}	Static load regulation	$I_{OUT} = 1\text{ mA to } 150\text{ mA}$		0.001		%/mA
V_{DROP}	Dropout voltage (3)	$I_{OUT} = 150\text{ mA}$, $V_{OUT} > 1.9\text{ V}$ $-40^\circ\text{C} < T_J < 125^\circ\text{C}$		86	180	mV
e_N	Output noise voltage	10Hz to 100kHz, $I_{OUT} = 0\text{ mA}$, $V_{OUT} = 1.0\text{ V}$		6.3		μV_{RMS}
		10Hz to 100kHz, $I_{OUT} = 150\text{ mA}$, $V_{OUT} = 1.0\text{ V}$		9.9		
SVR	Supply voltage rejection $V_{OUT} = 1.0\text{ V}$	$V_{IN} = V_{OUT(NOM)} + 1\text{ V} \pm V_{RIPPLE}$ $V_{RIPPLE} = 0.5\text{ V Freq.} = 1\text{ kHz}$ $I_{OUT} = 10\text{ mA}$		92		dB
		$V_{IN} = V_{OUT(NOM)} + 1\text{ V} \pm V_{RIPPLE}$ $V_{RIPPLE} = 0.5\text{ V Freq.} = 10\text{ kHz}$ $I_{OUT} = 10\text{ mA}$		89		
		$V_{IN} = V_{OUT(NOM)} + 1\text{ V} \pm V_{RIPPLE}$ $V_{RIPPLE} = 0.5\text{ V Freq.} = 100\text{ kHz}$ $I_{OUT} = 1\text{ mA}$		50		
I_Q	Quiescent current	$I_{OUT} = 0\text{ mA}$ $I_{OUT} = 0\text{ mA}$, $-40^\circ\text{C} < T_J < 125^\circ\text{C}$		17	60	μA
		$I_{OUT} = 150\text{ mA}$ $I_{OUT} = 150\text{ mA}$, $-40^\circ\text{C} < T_J < 125^\circ\text{C}$		54	120	
		V_{IN} input current in OFF mode $V_{EN} = \text{GND}$		0.002	2	
I_{SC}	Short-circuit current	$R_L = 0$; $V_{IN} = 2.0\text{ V}$	300			mA
V_{EN}	Enable input logic low	$V_{IN} = 2.1\text{ V to } 5.5\text{ V}$, $-40^\circ\text{C} < T_J < 125^\circ\text{C}$			0.4	V
	Enable input logic high	$V_{IN} = 2.1\text{ V to } 5.5\text{ V}$, $-40^\circ\text{C} < T_J < 125^\circ\text{C}$	0.9			
I_{EN}	Enable pin input current	$V_{EN} = 5.5\text{ V}$		0.1	100	nA
T_{ON}	Turn-on time (4)			110		μs

Table 5. Electrical characteristics ⁽¹⁾ ⁽²⁾ (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
T _{SHDN}	Thermal shutdown			166		°C
	Hysteresis			10		
C _{OUT}	Output capacitor	Capacitance (see Figure 15)	0.33		4.7	μF

1. For $V_{OUT(NOM)} < 1.0\text{ V}$ $V_{IN} = 2\text{ V}$.
2. All transient values are guaranteed by design, not production tested.
3. Dropout voltage is the input-to-output voltage difference at which the output voltage is 100 mV below its nominal value. This specification does not apply for output voltages below 2 V.
4. Turn-on time is time measured between the enable input just exceeding V_{EN} high value and the output voltage just reaching 95% of its nominal value.

5 Typical performance characteristics

Figure 4. Output voltage vs. temperature

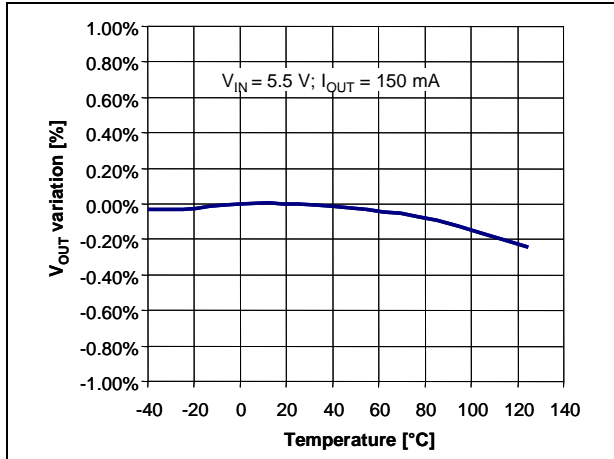


Figure 5. Output voltage vs. input voltage
 $V_{OUT} = 1 \text{ V}$

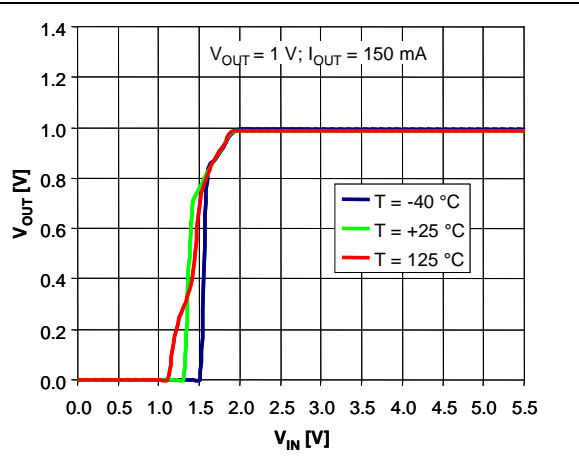


Figure 6. Output voltage vs. input voltage
 $V_{OUT} = 3.3 \text{ V}$

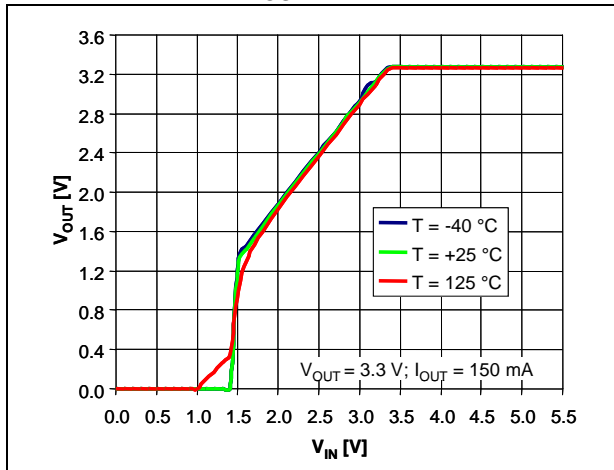


Figure 7. Dropout voltage vs. temperature

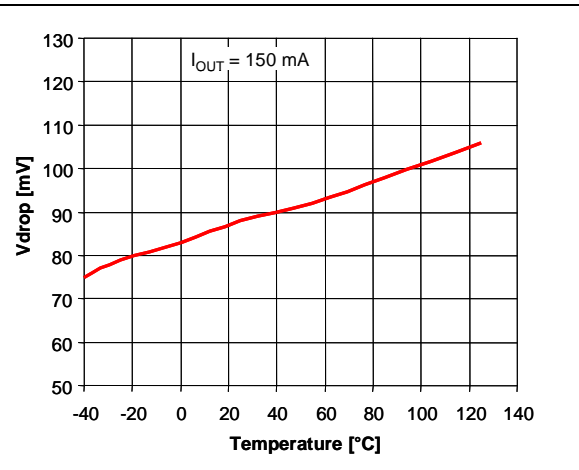


Figure 8. Dropout voltage vs. I_{OUT}

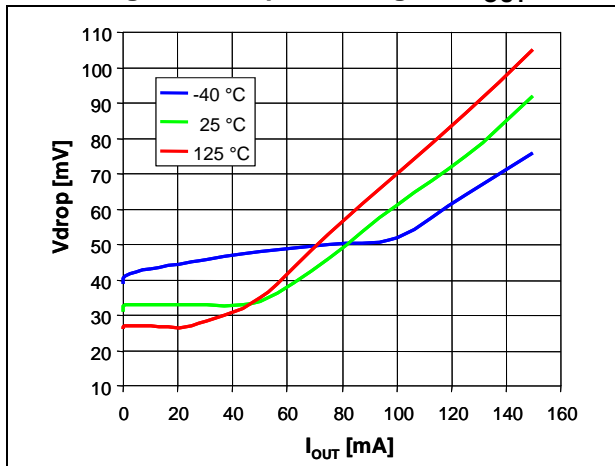


Figure 9. Quiescent current vs. temperature

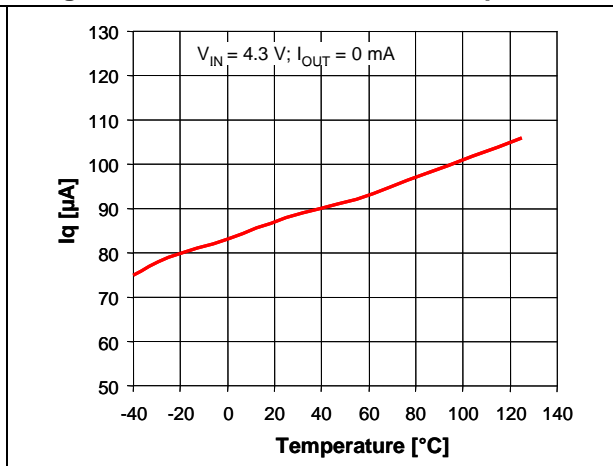


Figure 10. Quiescent current vs. I_{OUT}

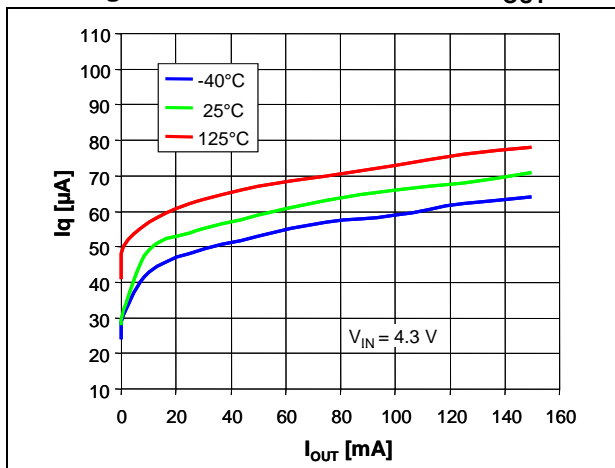


Figure 11. Quiescent current vs. V_{IN}

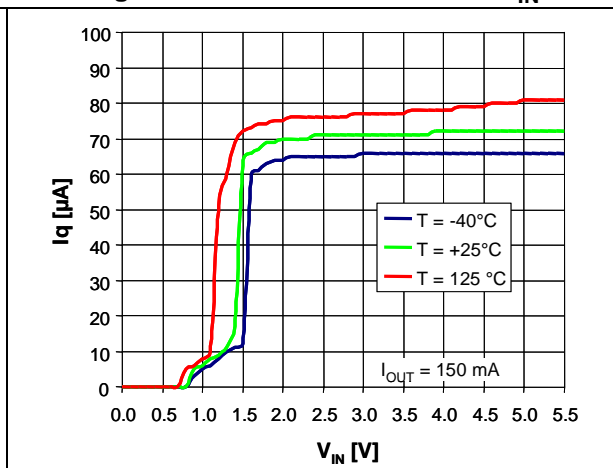


Figure 12. Supply voltage rejection vs. frequency

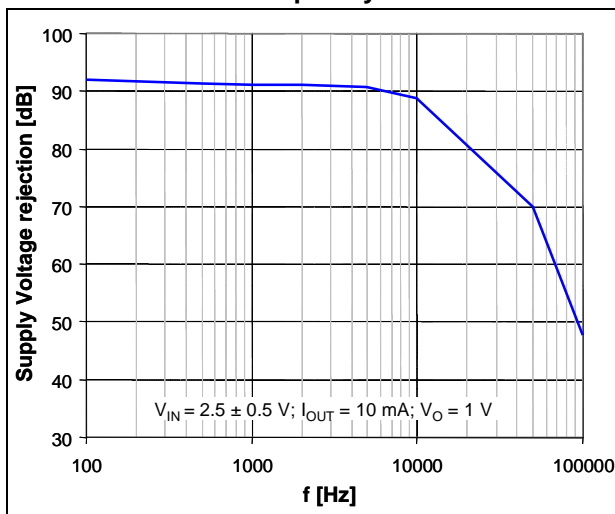


Figure 13. Supply voltage rejection vs. I_{OUT}

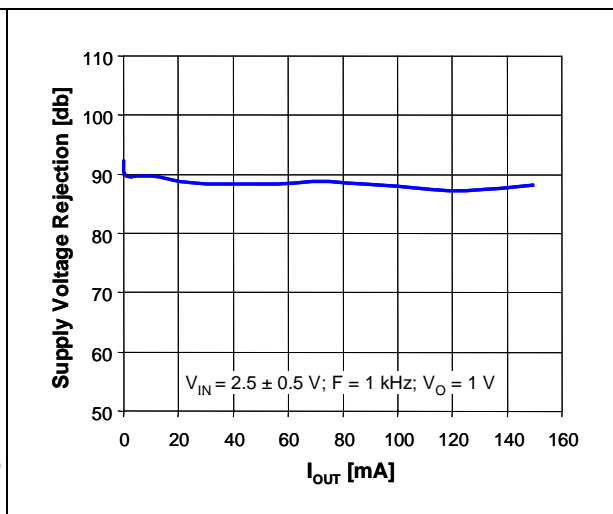


Figure 14. Noise spectral density

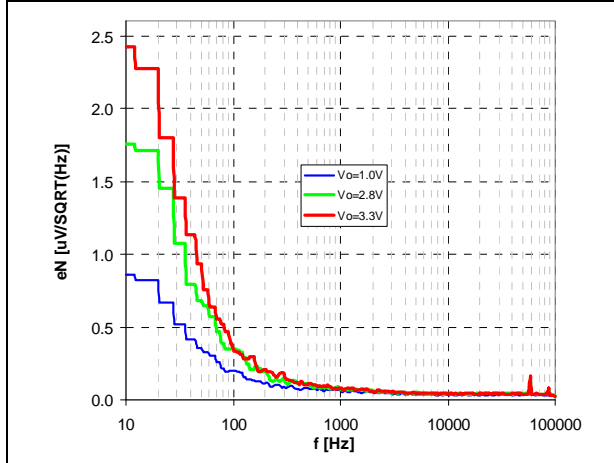


Figure 15. Stability area

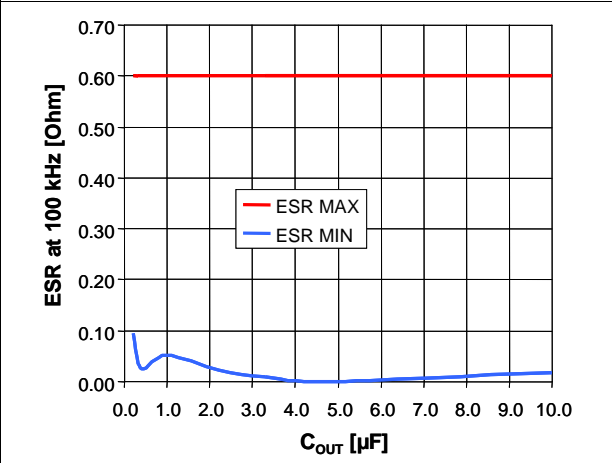


Figure 16. Load transient

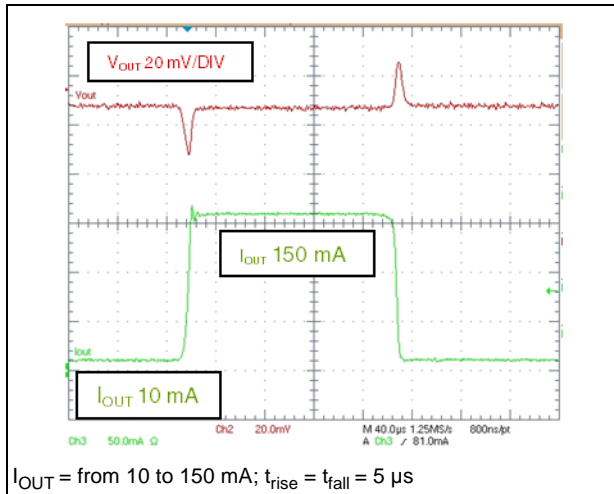


Figure 17. Line transient at $I_{OUT} = 1 \text{ mA}$

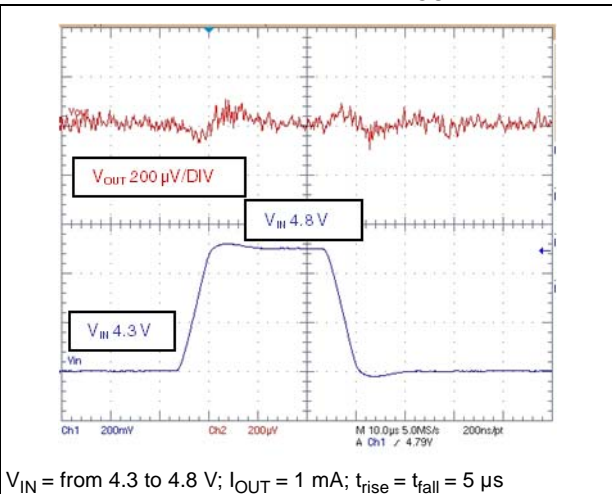


Figure 18. Line transient at $I_{OUT} = 150 \text{ mA}$

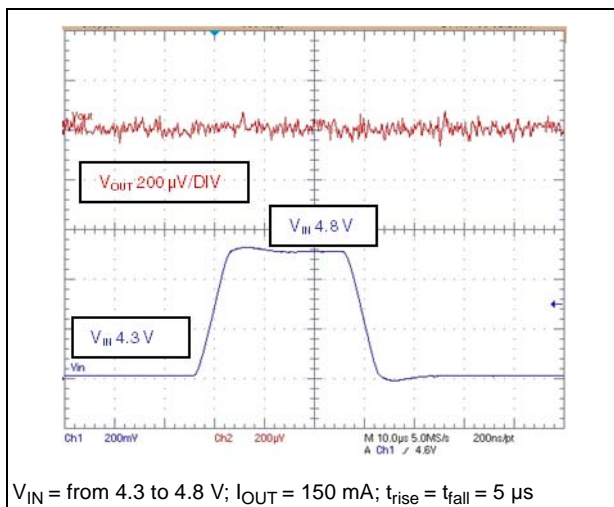


Figure 19. Turn-on time at $I_{OUT} = 1 \text{ mA}; V_{OUT} = 1 \text{ V}$

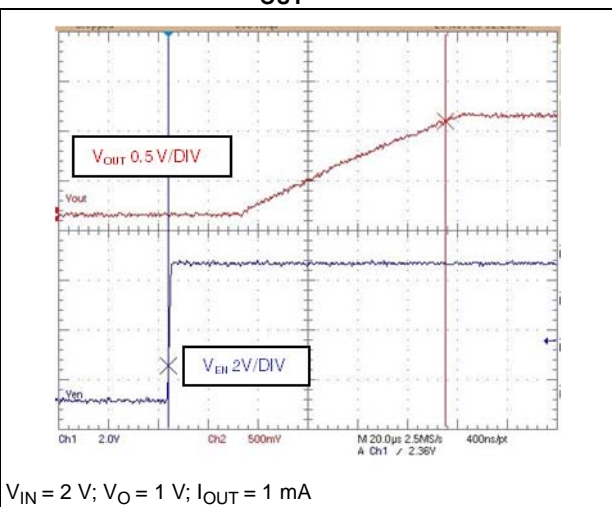


Figure 20. Turn-on time at $I_{OUT} = 150\text{ mA}$, $V_{OUT} = 1\text{ V}$

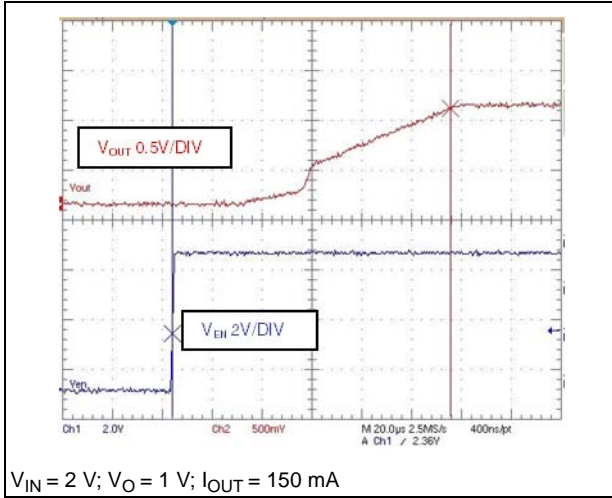


Figure 21. Turn-on time at $I_{OUT} = 1\text{ mA}$; $V_{OUT} = 3.3\text{ V}$

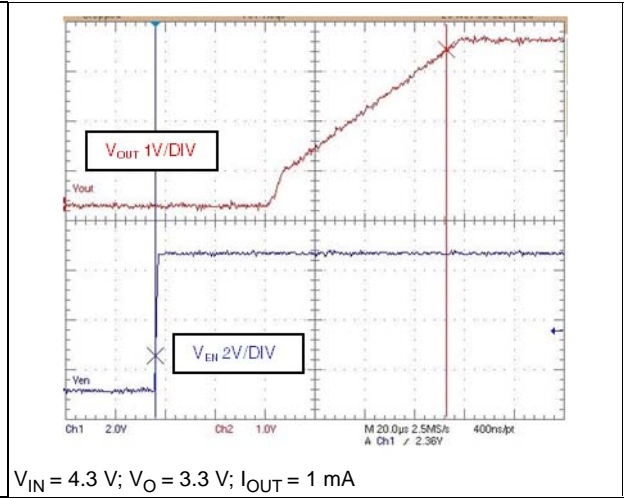


Figure 22. Turn-on time at $I_{OUT}=150\text{ mA}$, $V_{OUT} = 3.3\text{ V}$

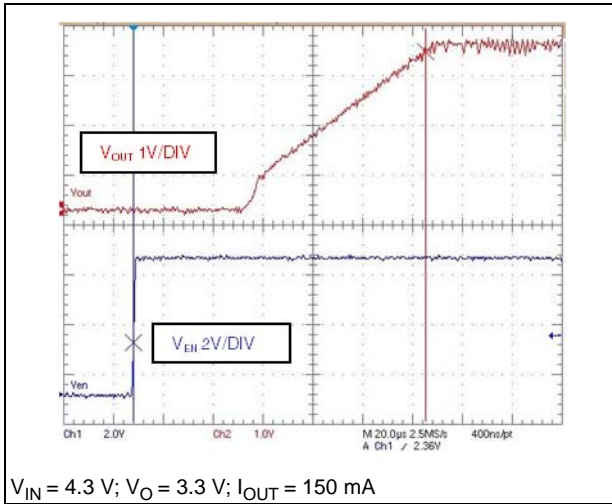
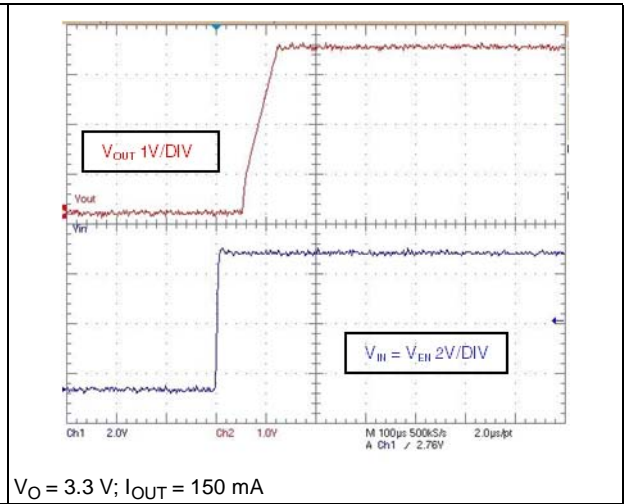


Figure 23. Startup transient



6 Package mechanical data

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Figure 24. DFN6 (2 x 2 mm) drawing dimensions

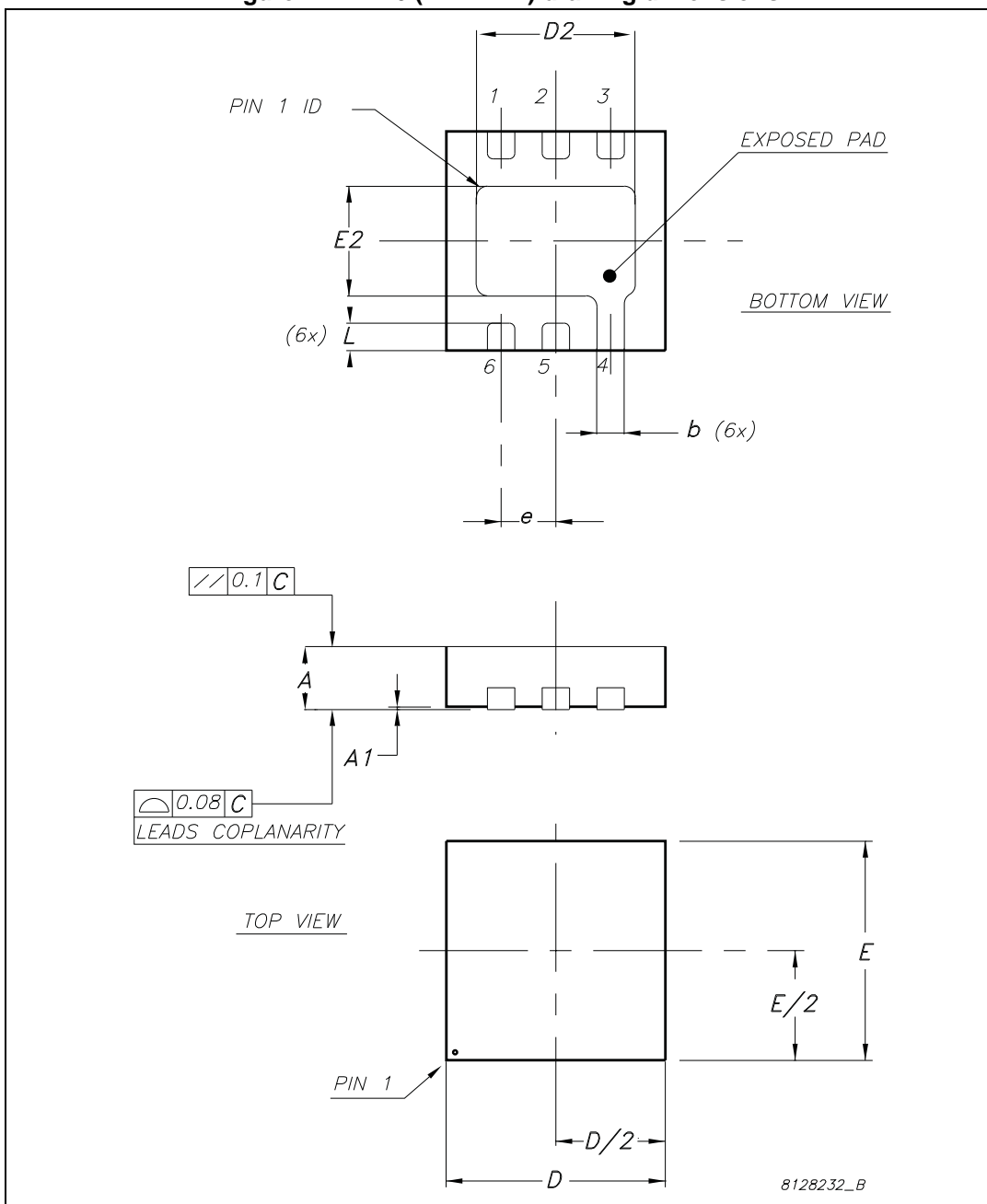
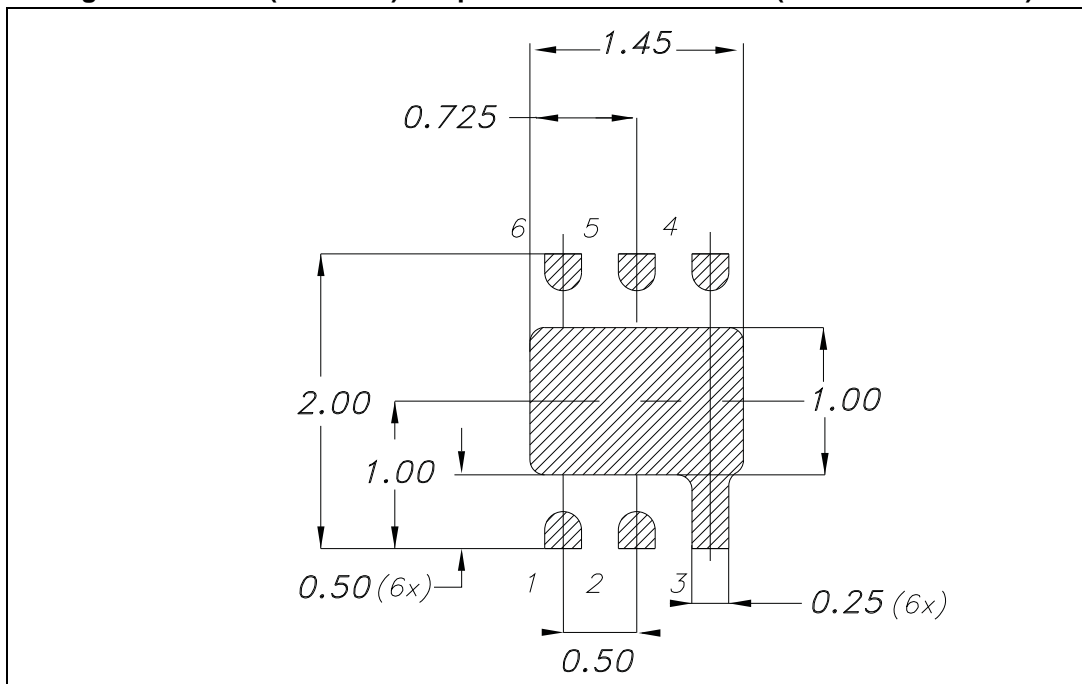


Table 6. DFN6 (2 x 2 mm) mechanical data

Dim.	mm.		
	Min.	Typ.	Max.
A	0.51	0.55	0.60
A1	0	0.02	0.05
b	0.18	0.25	0.30
D		2.00	
D2	1.30	1.45	1.55
E		2.00	
E2	0.85	1.00	1.10
e		0.50	
L	0.15	0.25	0.35

Figure 25. DFN6 (2 x 2 mm) footprint recommended data (dimensions in mm.)



7 Packaging mechanical data

Figure 26. DFN6 (2 x 2 mm) tape and reel dimensions

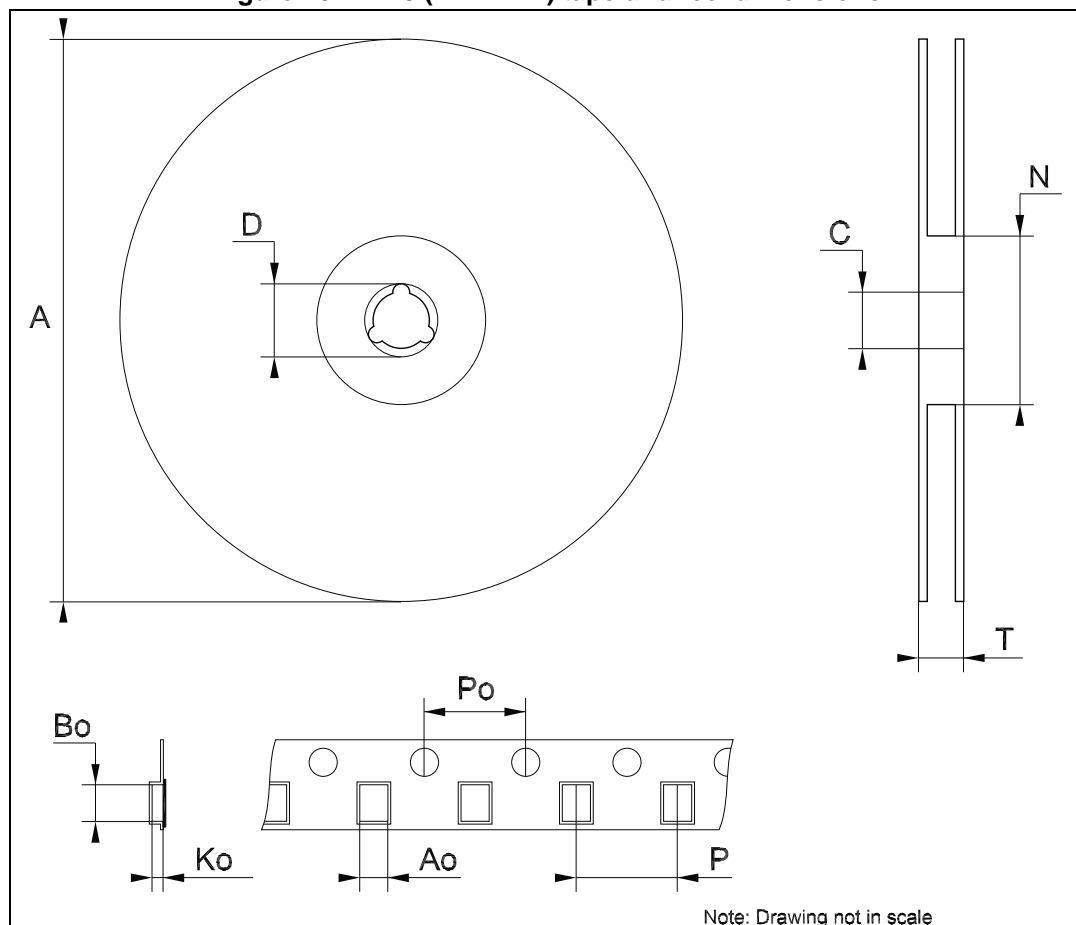


Table 7. DFN6 (2 x 2 mm) tape and reel mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			180
C	12.8		13.2
D	20.2		
N	60		
T			14.4
Ao		2.3	
Bo		2.3	
Ko		1.0	
Po		4	
P		8	

8 Revision history

Table 8. Document revision history

Date	Revision	Changes
31-Jan-2012	1	Initial release.
15-Jan-2014	2	Changed the LDLN015xx to LDLN015. Updated the Description in cover page. Updated Table 1: Device summary , Section 5: Typical performance characteristics and Section 6: Package mechanical data . Added Section 7: Packaging mechanical data . Minor text changes.

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