20 STERN AVE. SPRINGFIELD, NEW JERSEY 07081 U.S.A. **2N883**

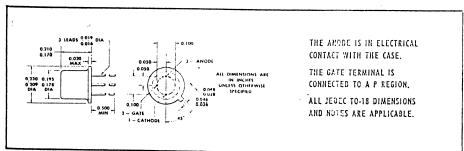
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P-N-P-N DIFFUSED SILICON REVERSE-BLOCKING TRIODE THYRISTOR

*mechanical data



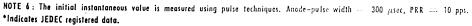
*absolute maximum ratings at (or below) 100°C case temperature (unless otherwise note

		UNIT
Continuous Forward Blocking Voltage, V _{FR} (See Note 1)	400	٧
Continuous Reverse Blocking Voltage, V _{RR} (See Note 2)	.400	٧
Continuous Anode Forward Current (See Note 3)	350	ma
Repetitive Peak Anode Forward Current (See Note 4)	20	а
Peak Anode Surge Current (See Note 5)	20	a
Peak Gate Reverse Voltage	5	Y
Peak Gate Forward Current (Pulse width \leq 8 msec)	250	ma
Operating Case Temperature Range	-65 to +150	°C
Storage Temperature Range	-65 to -i-150	°C
Lead Temperature \mathcal{X}_{6} Inch from Case for 10 Seconds	230	°C

- NOTES: 1. These values apply when the gate-cathode resistance $R_{\rm GK} \leq 1~{\rm k}\,\Omega.$
 - 2. These values apply when the gate-cathode resistance $R_{\text{GK}} \geq 1~k\,\Omega$.
 - 3. This value applies for continuous d-c operation with resistive load. Above 100°C derate according to Figure 1.
 - 4. This value applies for square-wave pulses, PRR \geq 60 pps, duty cycle \leq 0.1%, when the device is operating at (or below) rated values of peak reverse blocking voltage and anode forward current.
 - >. This value applies for one 200-usec square wave when the device is operating at (or below) rated values of peak reverse blocking voltage and anode forward current. Surge may be repeated after the device has returned to original thermal equilibrium.

*electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
I _{FR}	Static Anode Forward	$V_F = Rated V_{FR}$	$R_{GK} = 1 k \Omega$		10	μα
	Blocking Current	$V_F = Rated V_{FR}$	$R_{GK} = 1 k \Omega$, $T_{C} = 125$ °C		100	μα
I _{RR}	Static Anode Reverse	$V_R = Rated V_{RR}$	$R_{GK} = 1 k \Omega$		10	μα
	Blocking Current	$V_R = Rated V_{RR}$	$R_{GK} = 1 k \Omega$, $T_{C} = 125$ °C		100	μα
I_{GR}	Gate Reverse Current	$V_{GR} = 2 v$,	$I_A = 0$		10	μα
IGT	Gate Trigger Current	$V_{AA} = 5 v$	$R_L = 100 \Omega$, $PW_G \ge 10 \mu sec$		200	μa.
V _{GT}	Gate Trigger Voltage	$V_{AA} = 5 v$	$R_L = 100 \Omega$, $PW_G \ge 10 \mu sec$	0.4	0.8	γ
l _H	Holding Current	$V_{AA} = 5 v$	$I_G = -150 \mu a$		5	ma
٧ _۴	Forward Voltage	I _F = 0.2 a,	$R_{GK} \ge 1 \text{ k }\Omega$, See Note 6		1.5	Y





NJ Semi-Conductors reserves the right to change test conditions, parameter limits and package dimensions without notice Information furnished by NJ Semi-Conductors is believed to be both accurate and reliable at the time of going to press. However NJ Semi-Conductors assumes no responsibility for any errors or omissions discovered in its use. NJ Semi-Conductors encourages customers to verify that datasheets are current before placing orders.

^{*}Indicates JEDEC registered data.