DATASHEET

19MHz Radiation Hardened 40V Dual Rail-to-Rail Input-Output, Low-Power Operational Amplifier

ISL70244SEH

The ISL70244SEH features two low-power amplifiers optimized to provide maximum dynamic range. These op amps feature a unique combination of rail-to-rail operation on the input and output as well as a slew enhanced front end that provides ultra fast slew rates positively proportional to a given step size; thereby increasing accuracy under transient conditions, whether it's periodic or momentary. They also offer low power, low offset voltage, and low temperature drift, making it ideal for applications requiring both high DC accuracy and AC performance. With <5µs recovery for Single Event Transients (SET) (LET_{TH} = 86.4MeV•cm^2/mg), the number of filtering components needed is drastically reduced. The ISL70244SEH is also immune to Single Event Latch-up as it is fabricated in Intersil's Proprietary PR40 Silicon On Insulator (SOI) process.

They are designed to operate over a single supply range of 2.7V to 40V or a split supply voltage range of ±1.35V to ±20V. Applications for these amplifiers include precision instrumentation, data acquisition, precision power supply controls, and process controls.

The ISL70244SEH is available in a 10 Ld Hermetic Ceramic Flatpack that operates over the temperature range of -55°C to +125°C.

Related Literature

- ISL70244SEH Evaluation Board User's Guide AN1888
- ISL70244SEH Single Event Effects Report AN1961
- ISL70244SEH SMD 5962-13248
- ISL70244SEH Radiation Test Report

Features

- **Electrically screened to DLA SMD # 5962-13248**
  Acceptance tested to 50krad(Si) (LDR) wafer-by-wafer
- **<5µs recovery from SET (LET_{TH} = 86.4MeV•cm^2/mg)**
- **Unity gain stable**
- **Rail-to-rail input and output**
- **Wide gain-bandwidth product 19MHz**
- **Wide single and dual supply range. . . . . 2.7V to 40V Max**
- Low input offset voltage . . . . .400µV (+25°C, Max)
- Low current consumption (per amplifier) . . . . 1.2mA, Typ
- No phase reversal with input overdrive
- Slew rate
  - Large signal 60V/µs
- Operating temperature range. . . . . -55°C to +125°C
- Radiation tolerance
  - High dose rate (50-300rad(Si)/s). . . . . 300krad(Si)
  - Low dose rate (0.01rad(Si)/s) . . . . 100krad(Si)*
  - SEL/SEB LET_{TH} (V_S = ±19V) . . . . 86.4MeV•cm^2/mg

* Product capability established by initial characterization.

Applications

- Precision instruments
- Active filter blocks
- Data acquisition
- Power supply control
- Process control

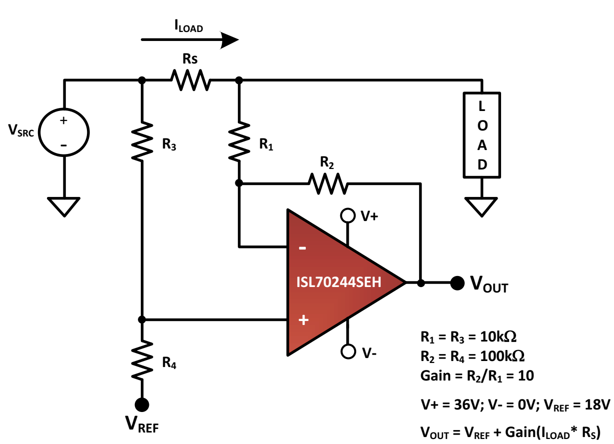


FIGURE 1. TYPICAL APPLICATION: SINGLE-SUPPLY, HIGH-SIDE CURRENT SENSE AMPLIFIER

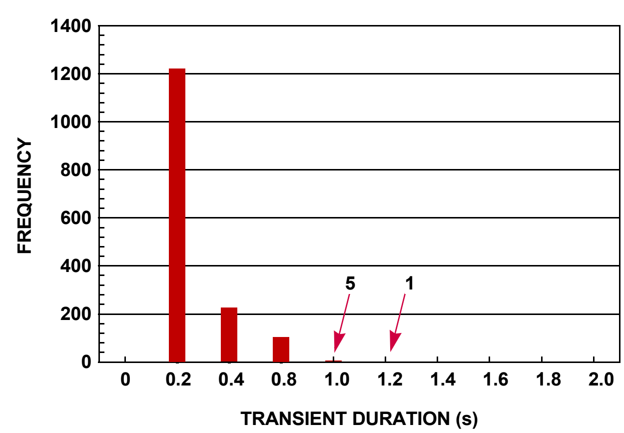
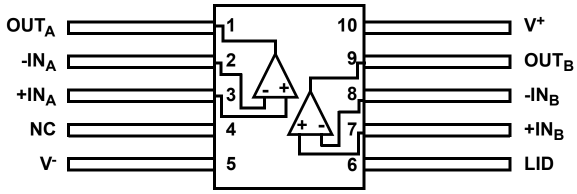


FIGURE 2. TYPICAL SINGLE EVENT TRANSIENT DURATION AT +25°C LET = 60 MeV•cm^2/ mg IN UNITY GAIN (V_S = ±18V)

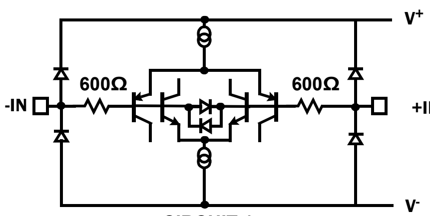
Pin Configuration

ISL70244SEH
(10 LD FLATPACK)
TOP VIEW

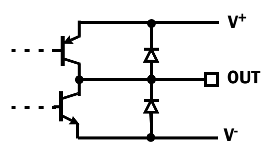


Pin Descriptions

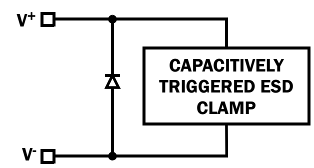
PIN NUMBER	PIN NAME	EQUIVALENT ESD CIRCUIT	DESCRIPTION
5	V^-	Circuit 3	Negative power supply
7	$+IN_B$	Circuit 1	Amplifier B noninverting input
8	$-IN_B$	Circuit 1	Amplifier B inverting input
9	OUT_B	Circuit 2	Amplifier B output
10	V^+	Circuit 3	Positive power supply
1	OUT_A	Circuit 2	Amplifier A output
2	$-IN_A$	Circuit 1	Amplifier A inverting input
4	NC	-	This pin is not electrically connected internally.
3	$+IN_A$	Circuit 1	Amplifier A noninverting input
6	LID	NA	Unbiased, tied to package lid



CIRCUIT 1



CIRCUIT 2



CIRCUIT 3

Ordering Information

ORDERING/SMD NUMBER (Note 2)	PART NUMBER (Note 1)	TEMP RANGE (°C)	PACKAGE (RoHS Compliant)	PKG. DWG. #
5962F1324801VXC	ISL70244SEHVF	-55 to +125	10 Ld Flatpack	K10.A
5962F1324801V9A	ISL70244SEHVX	-55 to +125	Die	
ISL70244SEHF/PROTO	ISL70244SEHF/PROTO	-55 to +125	10 Ld Flatpack	K10.A
ISL70244SEHF/SAMPLE	ISL70244SEHVX/SAMPLE	-55 to +125	Die	
ISL70244SEHEV1Z	ISL70244SEHEV1Z	Evaluation Board		

NOTES:

1. These Intersil Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
2. Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed in the "Ordering Information" table must be used when ordering.

Absolute Maximum Ratings

Maximum Supply Voltage Differential (V^+ to V^-) 42V
Maximum Supply Voltage Differential (V^+ to V^-) (Note 5) 38V
Maximum Differential Input Current 20mA
Maximum Differential Input Voltage . . . . 42V or V^- - 0.5V to V^+ + 0.5V
Min/Max Input Voltage . . . . 42V or V^- - 0.5V to V^+ + 0.5V
Max/Min Input Current for Input Voltage >V^+ or <V^-. . . . . ±20mA
ESD Tolerance
Human Body Model (Tested per MIL-PRF-883 3015.7). 2kV
Machine Model (Tested per JESD22-A115-A) 200V
Charged Device Model (Tested per CDM-22CI0ID). 750V

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
10 Ld Flatpack Package (Notes 3, 4).	44	10

Storage Temperature Range. . . . . -65°C to +150°C

Recommended Operating Conditions

Ambient Operating Temperature Range . . . . -55°C to +125°C
Maximum Operating Junction Temperature . . . . +150°C
Single Supply Voltage. . . . . 2.7V to 39.6V
Split Rail Supply Voltage . . . . ±1.35V to ±19.8V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

3. Theta-ja is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379 for details.
4. For θ_{JC}, the “case temp” location is the center of the package underside.
5. Tested in a heavy ion environment at LET = 86.4MeV • cm^2/mg at +125°C (T_C) for SEB. Refer to Single Event Effects Test Report for more information.

Electrical Specifications

V_S = ±19.8V, V_{CM} = V_O = 0V, R_L = Open, T_A= +25°C, unless otherwise noted. **Boldface limits apply across the operating temperature range, -55°C to +125°C; over a total ionizing dose of 300krad(Si) with exposure of a high dose rate of 50 to 300rad(Si)/s or over a total ionizing dose of 50krad(Si) with exposure at a low dose rate of <10mrad(Si)/s**

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
V_{OS}	Offset Voltage	V_{CM} = 0V	-400	25	400	µV
		V_{CM} = V^+ to V^-	**-500**	110	**500**	µV
TCV_{OS}	Offset Voltage Temperature Coefficient	V_{CM} = V^+ - 2V to V^- + 2V	-	0.5	-	µV/°C
ΔV_{OS}	Input Offset Channel-to-Channel Match	V_{CM} = V^+	-	135	**800**	µV
		V_{CM} = V^-	-	128	**800**	µV
I_B	Input Bias Current	V_{CM} = 0V	**-500**	210	**500**	nA
		V_{CM} = V^+	**-500**	200	**500**	nA
		V_{CM} = V^-	**-650**	290	**650**	nA
		V_{CM} = V^+ - 0.5V	**-500**	200	**500**	nA
		V_{CM} = V^- + 0.5V	**-650**	257	**650**	nA
I_{OS}	Input Offset Current	V_{CM} = V^+ to V^-	-30	0	30	nA
			-50	0	**50**	nA
V_{CMIR}	Common Mode Input Voltage Range		**V^-**	-	**V^+**	V
CMRR	Common-Mode Rejection Ratio	V_{CM} = V^- to V^+	-	112	-	dB
		V_{CM} = V^- to V^+	**70**	-	-	dB
		V_{CM} = V^+ - 0.5V to V^- + 0.5V	-	111	-	dB
		V_{CM} = V^+ - 0.5V to V^- + 0.5V	**80**	-	-	dB
PSRR	Power Supply Rejection Ratio	V^- = -18V; V^+ = 0.5V to 18V; V^+ = 18V; V^- = -0.5V to -18V	-	128	-	dB
			83	-	-	dB
A_{VOL}	Open-Loop Gain	R_L = 10kΩ to ground	-	125	-	dB
			90	-	-	dB
V_{OH}	Output Voltage High (V_{OUT} to V^+)	R_L = No Load	-	26	**160**	mV
		R_L = 10kΩ	-	78	**175**	mV

Electrical Specifications V_S = ±19.8V, V_{CM} = V_O = 0V, R_L = Open, T_A= +25°C, unless otherwise noted. **Boldface limits apply across the operating temperature range, -55°C to +125°C; over a total ionizing dose of 300krad(Si) with exposure of a high dose rate of 50 to 300rad(Si)/s or over a total ionizing dose of 50krad(Si) with exposure at a low dose rate of <10mrad(Si)/s** (Continued)

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
V_{OL}	Output Voltage Low (V_{OUT} to V^-)	R_L = No Load	-	21	**160**	mV
		R_L = 10kΩ	-	64	**175**	mV
I_{SRC}	Output Short Circuit Current	Sourcing; V_{IN} = 0V, V_{OUT} = -18V	**10**	-	-	mA
I_{SNK}	Output Short Circuit Current	Sinking; V_{IN} = 0V, V_{OUT} = +18V	**10**	-	-	mA
I_S	Supply Current/Amplifier	Unity gain	-	1.6	2.2	mA
		T_A = +25°C post HDR/LDR Rad	-	-	2.2	mA
		T_A = -55°C to +125°C	-	**2.2**	**2.8**	mA
AC SPECIFICATIONS						
GBWP	Gain Bandwidth Product	A_V = 1, R_L = 10k	**17**	19	-	MHz
e_n	Voltage Noise Density	f = 10kHz	-	11.3	-	nV/√Hz
i_n	Current Noise Density	f = 10kHz	-	0.312	-	pA/√Hz
SR	Large Signal Slew Rate	A_V = 1, R_L = 10kΩ, V_O = $10V_{P-P}$	**60**	-	-	V/µs

Electrical Specifications V_S = ±2.5V, V_{CM} = V_O = 0V, R_L = Open, T_A= +25°C, unless otherwise noted. **Boldface limits apply across the operating temperature range, -55°C to +125°C; over a total ionizing dose of 300krad(Si) with exposure of a high dose rate of 50 to 300rad(Si)/s or over a total ionizing dose of 50krad(Si) with exposure at a low dose rate of <10mrad(Si)/s.**

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
V_{OS}	Offset Voltage	V_{CM} = 0V	-400	20	400	µV
		V_{CM} = V^+ to V^-	-500	80	**500**	µV
TCV_{OS}	Offset Voltage Temperature Coefficient	V_{CM} = V^+ - 2V to V^- + 2V	-	0.5	-	µV/°C
ΔV_{OS}	Input Offset Channel-to-Channel Match	V_{CM} = V^+	-	132	**800**	µV
		V_{CM} = V^-	-	127	**800**	µV
I_B	Input Bias Current	V_{CM} = 0V	**-400**	226	**400**	nA
		V_{CM} = V^+	**-400**	182	**400**	nA
		V_{CM} = V^-	**-580**	260	**580**	nA
		V_{CM} = V^+ - 0.5V	**-400**	181	**400**	nA
		V_{CM} = V^- + 0.5V	**-580**	224	**580**	nA
I_{OS}	Input Offset Current	V_{CM} = V^+ to V^-	-30	0	30	nA
			-50	0	**50**	nA
V_{CMIR}	Common Mode Input Voltage Range		**V^-**	-	**V^+**	V
CMRR	Common-Mode Rejection Ratio	V_{CM} = V^- to V^+	-	92	-	dB
		V_{CM} = V^- to V^+	**70**	-	-	dB
		V_{CM} = V^+ - 0.5V to V^- + 0.5V	-	91	-	dB
		V_{CM} = V^+ - 0.5V to V^- + 0.5V	**74**	-	-	dB

Electrical Specifications V_S = ±2.5V, V_{CM} = V_O = 0V, R_L = Open, T_A= +25°C, unless otherwise noted. **Boldface limits apply across the operating temperature range, -55°C to +125°C; over a total ionizing dose of 300krad(Si) with exposure of a high dose rate of 50 to 300rad(Si)/s or over a total ionizing dose of 50krad(Si) with exposure at a low dose rate of <10mrad(Si)/s.** (Continued)

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
PSRR	Power Supply Rejection Ratio	V^- = -2.5V; V^+ = 4.5V to 2.5V; V^+ = 2.5V; V^- = -4.5V to -2.5V	-	123	-	dB
		V^- = -2.5V; V^+ = 4.5V to 2.5V; V^+ = 2.5V; V^- = -4.5V to -2.5V T_A = +125°C, T_A = +25°C OR T_A = +25°C with HDR/LDR Rad.	**80**	-	-	dB
		V^- = -2.5V; V^+ = 4.5V to 2.5V; V^+ = 2.5V; V^- = -4.5V to -2.5V T_A = -55°C	**70**	-	-	dB
A_{VOL}	Open-Loop Gain	R_L = 10kΩ to ground	-	118	-	dB
		R_L = 10kΩ to ground T_A = +125°C, T_A = +25°C OR T_A = +25°C with HDR/LDR Rad.	**90**	-	-	dB
		R_L = 10kΩ to ground T_A = -55°C	**80**	-	-	dB
V_{OH}	Output Voltage High (V_{OUT} to V^+)	R_L = No Load	-	15	**85**	mV
		R_L = 10kΩ	-	23	**105**	mV
		R_L = 600Ω	-	-	**400**	mV
V_{OL}	Output Voltage Low (V_{OUT} to V^-)	R_L = No Load	-	11	**85**	mV
		R_L = 10kΩ	-	18	**105**	mV
		R_L = 600Ω	-	-	**400**	mV
I_S	Supply Current/Amplifier	Unity gain	-	1.2	1.5	mA
		T_A = +25°C post HDR/LDR Rad	-	-	1.5	mA
		T_A = -55°C to +125°C	-	**1.7**	**2.0**	mA
AC SPECIFICATIONS						
GBWP	Gain Bandwidth Product	A_V = 1, R_L = 10k	**15**	17	-	MHz
e_n	Voltage Noise Density	f = 10kHz	-	12.3	-	nV/√Hz
i_n	Current Noise Density	f = 10kHz	-	0.313	-	pA/√Hz
SR	Large Signal Slew Rate	A_V = 1, R_L = 10kΩ, V_O = $3V_{P-P}$	-	35	-	V/µs

Electrical Specifications V_S = ±1.35V, V_{CM} = V_O = 0V, R_L = Open, T_A= +25°C, unless otherwise noted. **Boldface limits apply over the operating temperature range, -55°C to +125°C; over a total ionizing dose of 300krad(Si) with exposure of a high dose rate of 50 to 300rad(Si)/s or over a total ionizing dose of 50krad(Si) with exposure at a low dose rate of <10mrad(Si)/s.**

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
V_{OS}	Offset Voltage	V_{CM} = 0V	-400	51	400	µV
		V_{CM} = V_+ to V^-	-500	80	**500**	µV
ΔV_{OS}	Input Offset Channel-to-Channel Match	V_{CM} = V^+	-	79	**800**	µV
		V_{CM} = V^-		119	**800**	µV
I_B	Input Bias Current	V_{CM} = 0V	**-375**	110	**375**	nA
		V_{CM} = V^+	**-375**	180	**375**	nA
		V_{CM} = V^-	**-565**	225	**565**	nA
		V_{CM} = V^+ - 0.5V	**-375**	180	**375**	nA
		V_{CM} = V^- + 0.5V	**-565**	223	**565**	nA

Electrical Specifications V_S = ±1.35V, V_{CM} = V_O = 0V, R_L = Open, T_A= +25°C, unless otherwise noted. **Boldface limits apply over the operating temperature range, -55°C to +125°C; over a total ionizing dose of 300krad(Si) with exposure of a high dose rate of 50 to 300rad(Si)/s or over a total ionizing dose of 50krad(Si) with exposure at a low dose rate of <10mrad(Si)/s.** (Continued)

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
I_{OS}	Input Offset Current	V_{CM} = V^+ to V^-	-30	0	30	nA
			-50	0	**50**	nA
V_{CMIR}	Common Mode Input Voltage Range		**V^-**	-	**V^+**	V
V_{OH}	Output Voltage High (V_{OUT} to V^+)	R_L = No Load	-	14	**50**	mV
		R_L = 10kΩ	-	19	**70**	mV
V_{OL}	Output Voltage Low (V_{OUT} to V^-)	R_L = No Load	-	10	**50**	mV
		R_L = 10kΩ	-	14	**70**	mV
I_S	Supply Current/Amplifier	Unity Gain	-	1.1	1.5	mA
		T_A = +25°C post HDR/LDR Rad	-	-	1.5	mA
		T_A = -55°C to +125°C	-	**1.6**	**2.0**	mA
AC SPECIFICATIONS						
GBWP	Gain Bandwidth Product	A_V = 1, R_L = 10k	**10**	15	-	MHz
e_n	Voltage Noise Density	f = 10kHz	-	12	-	nV/√Hz
i_n	Current Noise Density	f = 10kHz	-	0.312	-	pA/√Hz

NOTE:

6. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

Typical Performance Curves

Unless otherwise specified, V_S ± 18V, V_{CM} = 0, V_O = 0V, T_A = +25°C.

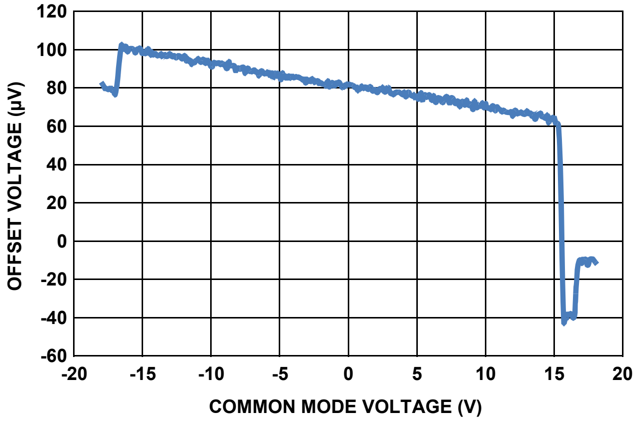


FIGURE 3. OFFSET VOLTAGE vs COMMON MODE VOLTAGE

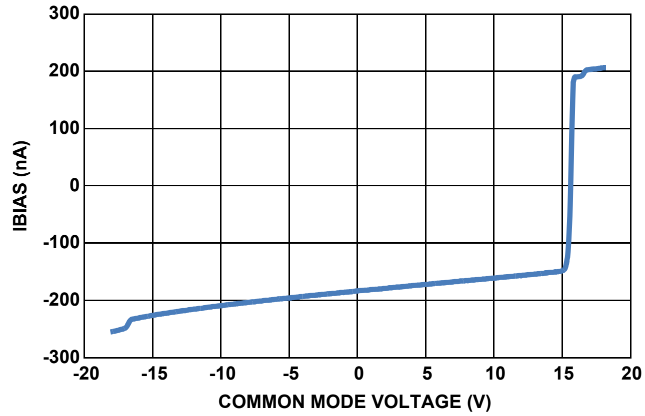


FIGURE 4. IBIAS vs COMMON MODE VOLTAGE

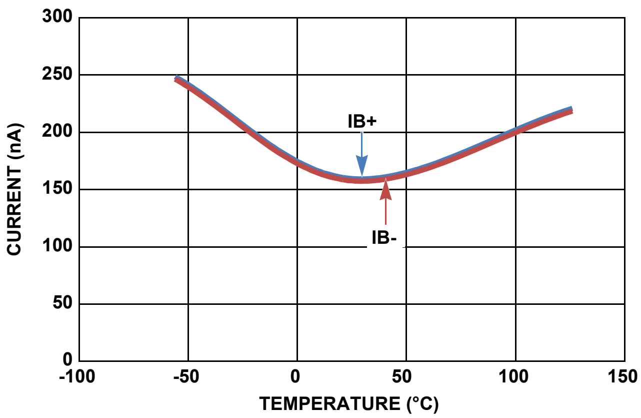


FIGURE 5. IBIAS vs TEMPERATURE (V_S = ±18V)

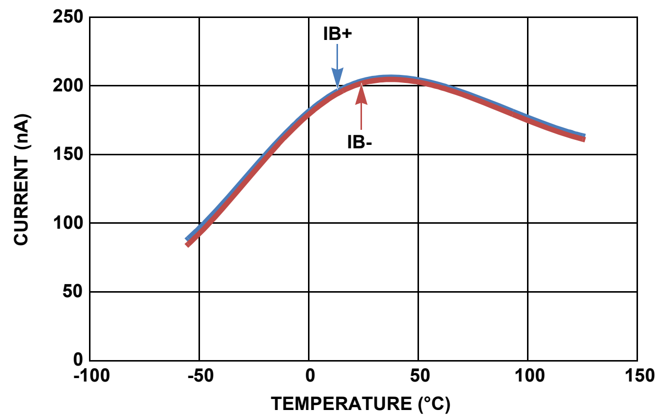


FIGURE 6. IBIAS vs TEMPERATURE (V_S = ±2.5V)

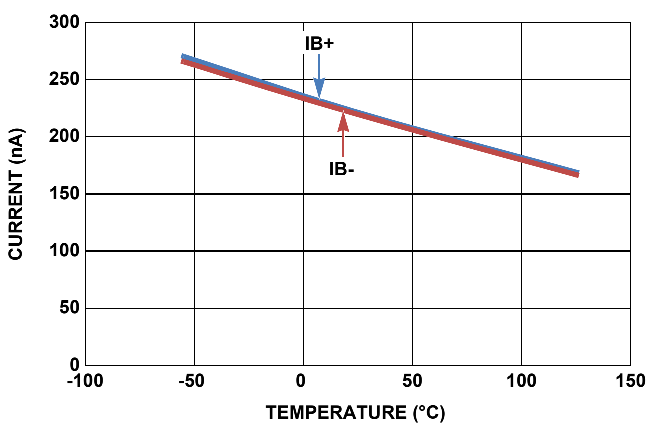


FIGURE 7. IBIAS vs TEMPERATURE, (V_S = ±1.5V)

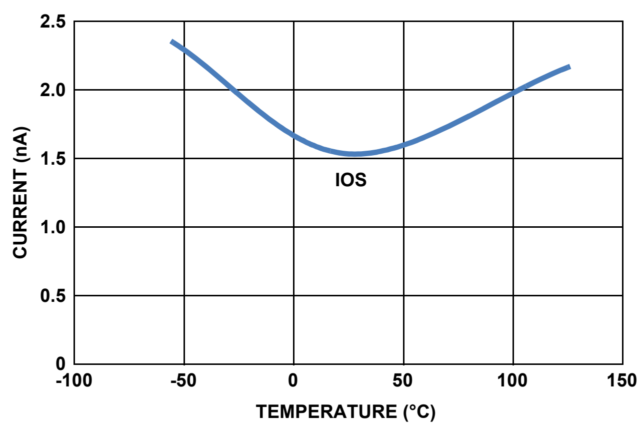


FIGURE 8. IOS vs TEMPERATURE (V_S = ±18V)

Typical Performance Curves
Unless otherwise specified, $V_S \pm 18V$, $V_{CM} = 0$, $V_O = 0V$, $T_A = +25°C$. **(Continued)**

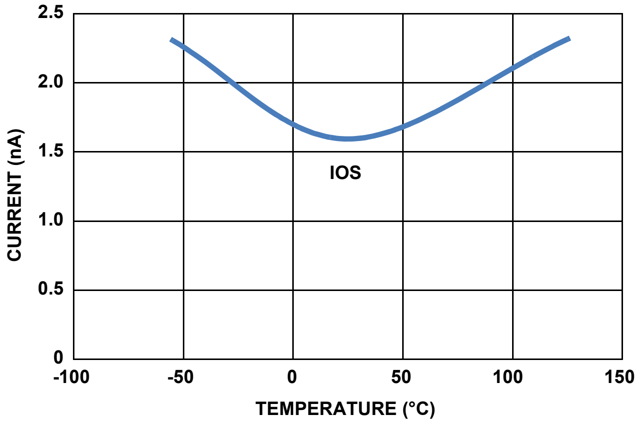


FIGURE 9. IOS vs TEMPERATURE ($V_S = \pm2.5V$)

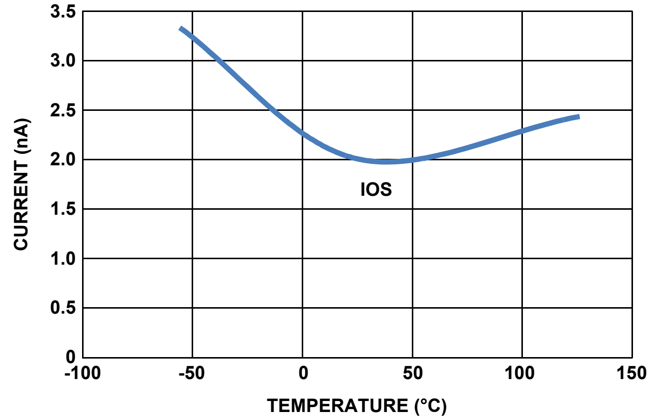


FIGURE 10. IOS vs TEMPERATURE ($V_S = \pm1.5V$)

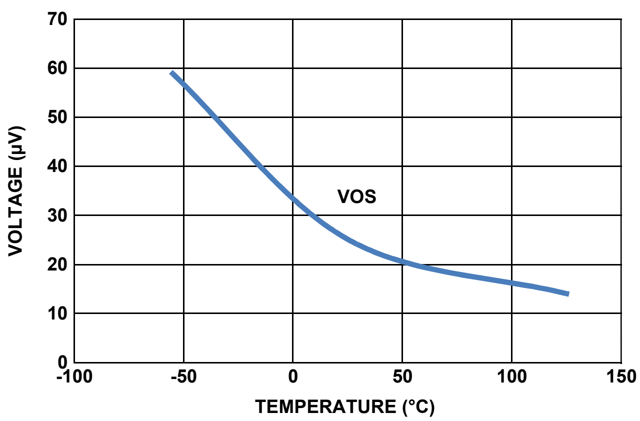


FIGURE 11. VOS vs TEMPERATURE ($V_S = \pm18V$)

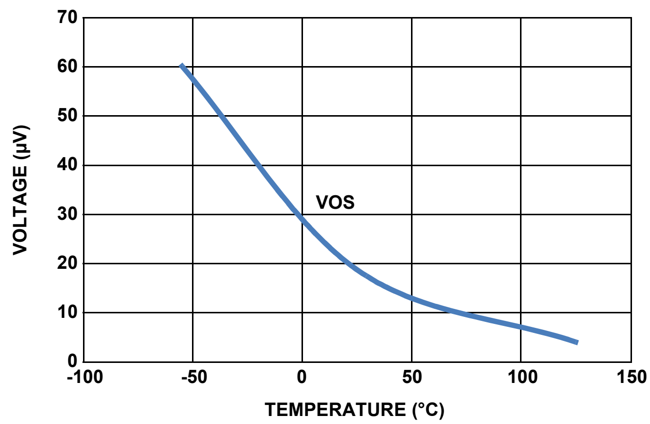


FIGURE 12. VOS vs TEMPERATURE ($V_S = \pm2.5V$)

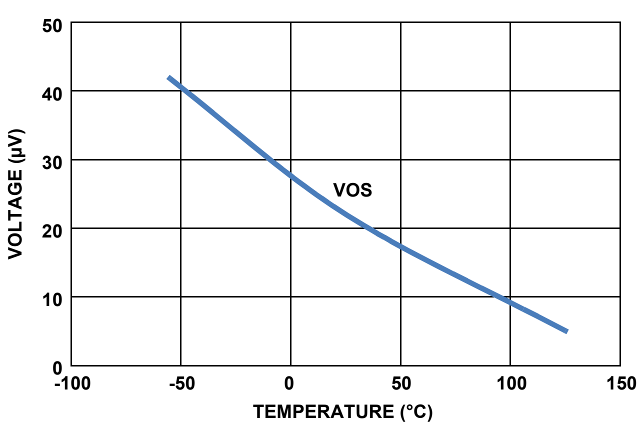


FIGURE 13. VOS vs TEMPERATURE ($V_S = \pm1.5V$)

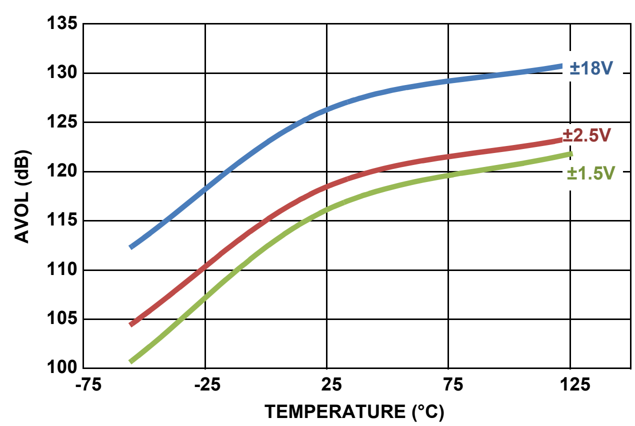


FIGURE 14. AVOL vs TEMPERATURE vs SUPPLY VOLTAGE

Typical Performance Curves
Unless otherwise specified, $V_S \pm 18V$, $V_{CM} = 0$, $V_O = 0V$, $T_A = +25°C$. **(Continued)**

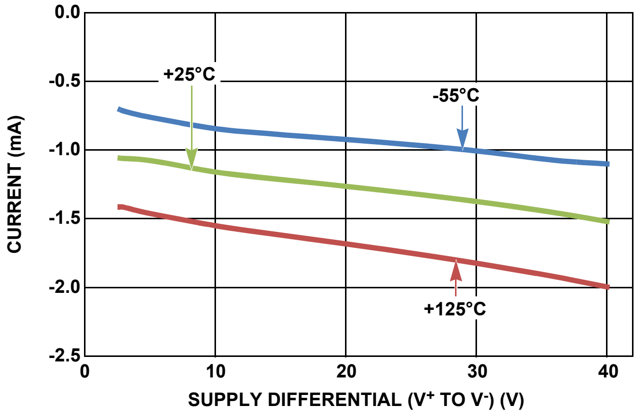


FIGURE 15. NEGATIVE SUPPLY CURRENT vs SUPPLY VOLTAGE

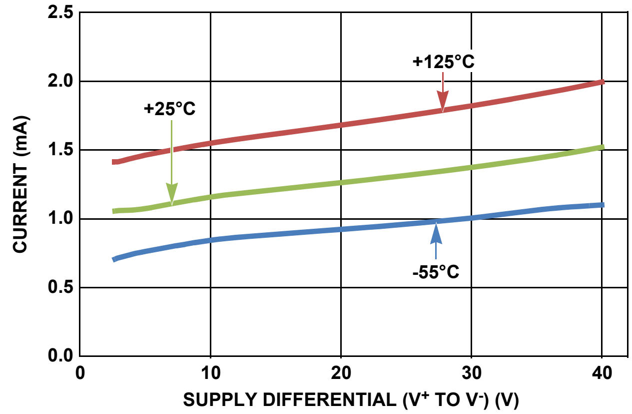


FIGURE 16. POSITIVE SUPPLY CURRENT vs SUPPLY VOLTAGE

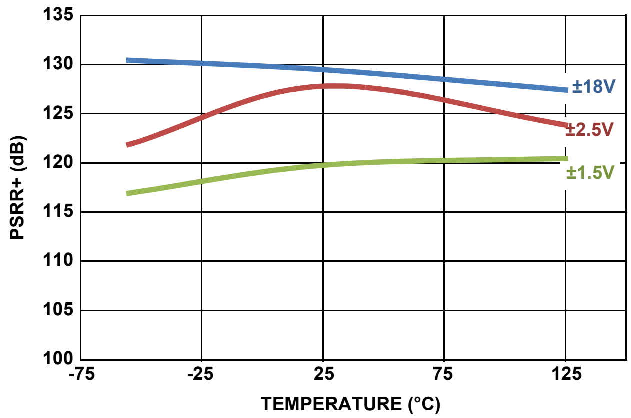


FIGURE 17. PSRR+ vs TEMPERATURE vs SUPPLY VOLTAGE

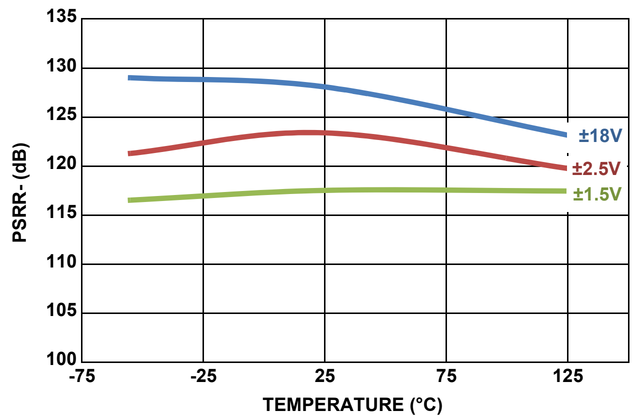


FIGURE 18. PSRR- vs TEMPERATURE vs SUPPLY VOLTAGE

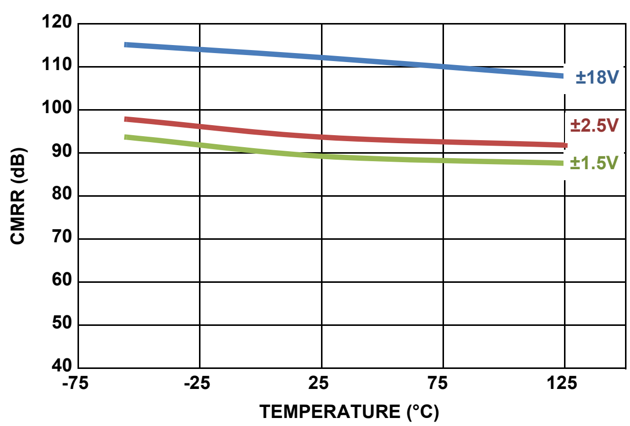


FIGURE 19. CMRR vs TEMPERATURE vs SUPPLY VOLTAGE

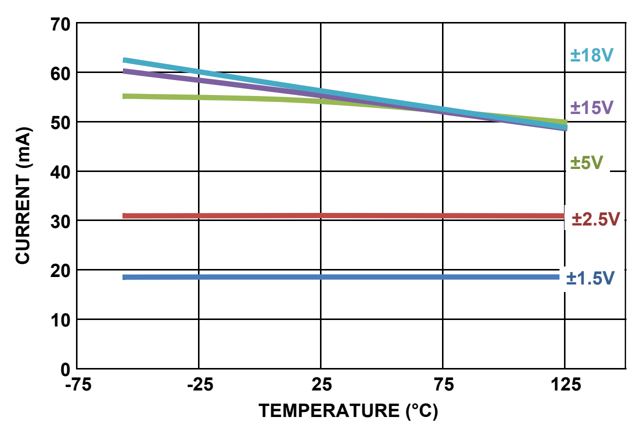


FIGURE 20. SHORT CIRCUIT CURRENT vs TEMPERATURE

Typical Performance Curves
Unless otherwise specified, $V_S \pm 18V$, $V_{CM} = 0$, $V_O = 0V$, $T_A = +25°C$. **(Continued)**

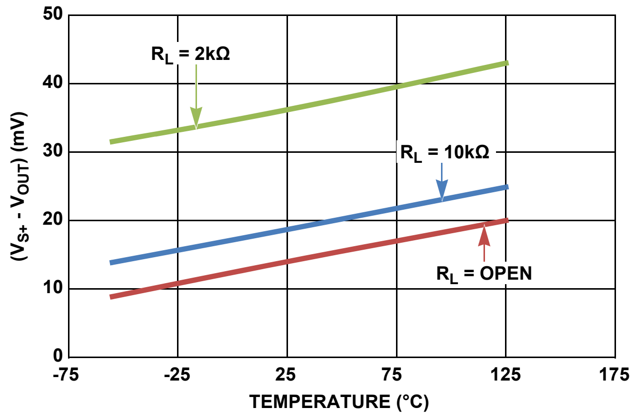


FIGURE 21. (V_S = ±1.5V) V_{OH} vs TEMPERATURE

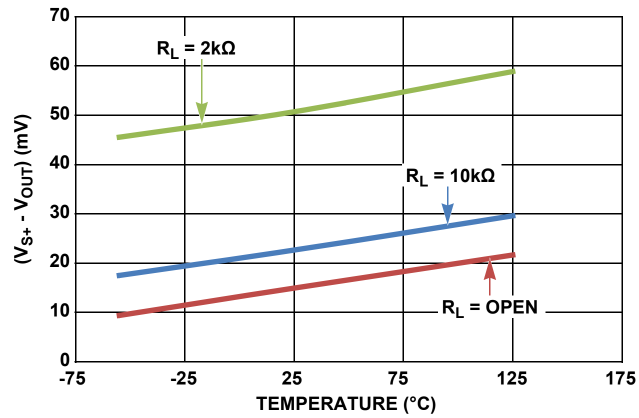


FIGURE 22. (V_S = ±2.5V) V_{OH} vs TEMPERATURE

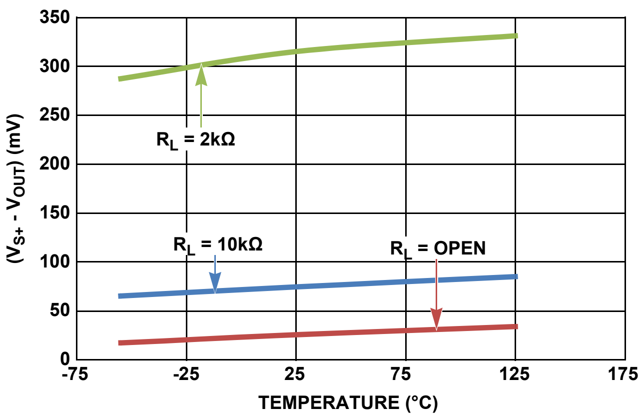


FIGURE 23. (V_S = ±18V) V_{OH} vs TEMPERATURE

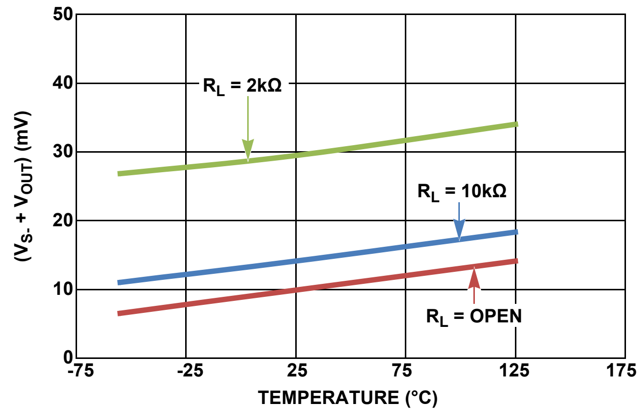


FIGURE 24. (V_S = ±1.5V) V_{OL} vs TEMPERATURE

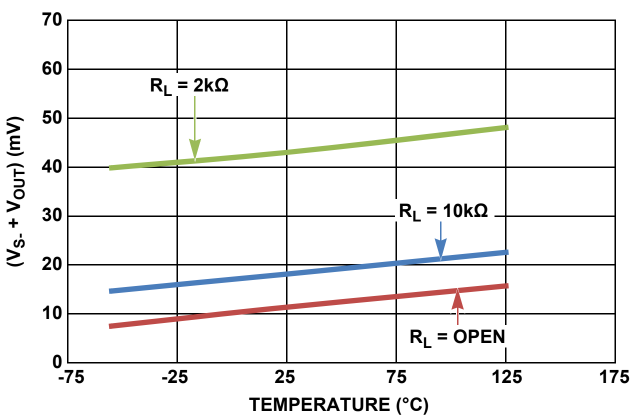


FIGURE 25. (V_S = ±2.5V) V_{OL} vs TEMPERATURE

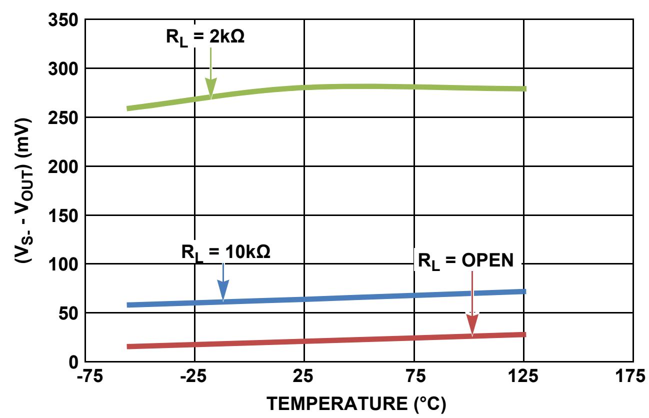


FIGURE 26. (V_S = ±18V) V_{OL} vs TEMPERATURE

Typical Performance Curves
Unless otherwise specified, V_S ± 18V, V_{CM} = 0, V_O = 0V, T_A = +25°C. **(Continued)**

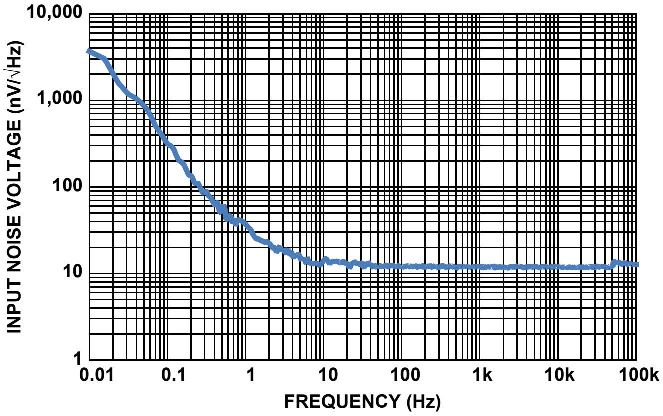


FIGURE 27. INPUT NOISE VOLTAGE SPECTRAL DENSITY (V_S = ±18V)

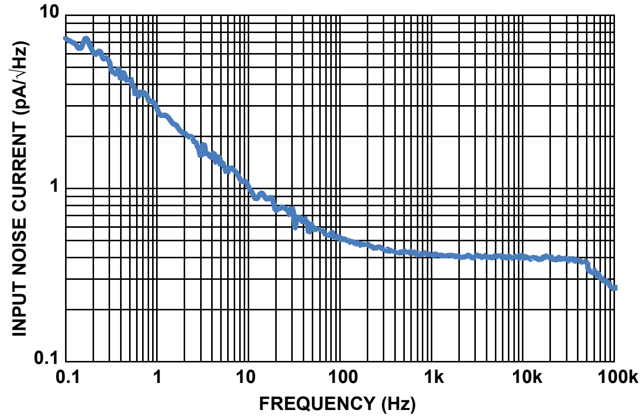


FIGURE 28. INPUT NOISE CURRENT SPECTRAL DENSITY (V_S = ±18V)

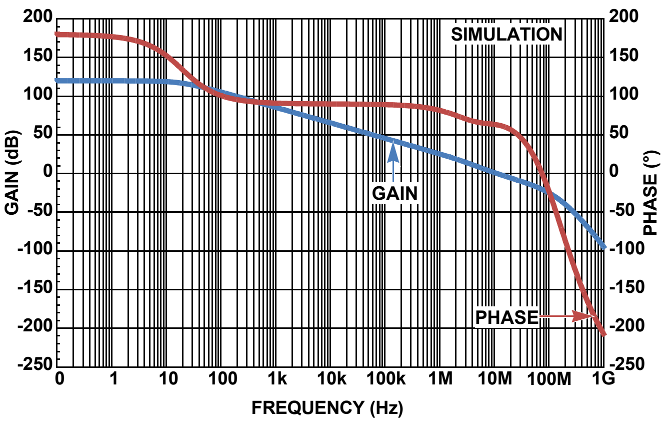


FIGURE 29. OPEN LOOP FREQUENCY RESPONSE (C_L = 0.01pF)

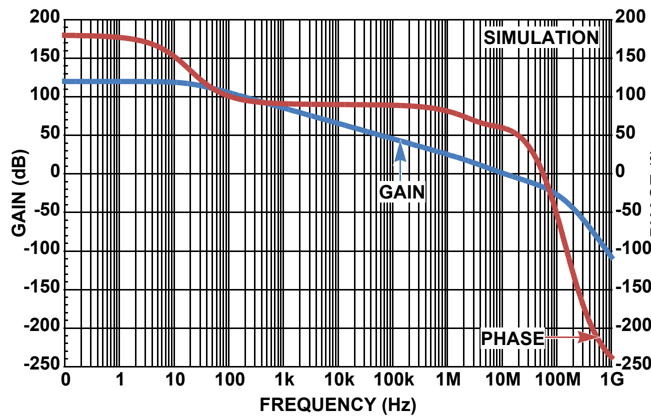


FIGURE 30. OPEN LOOP FREQUENCY RESPONSE (C_L = 10pF)

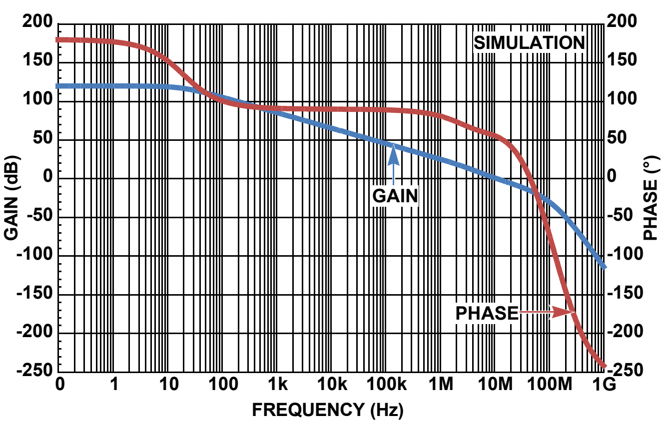


FIGURE 31. OPEN LOOP FREQUENCY RESPONSE (C_L = 22pF)

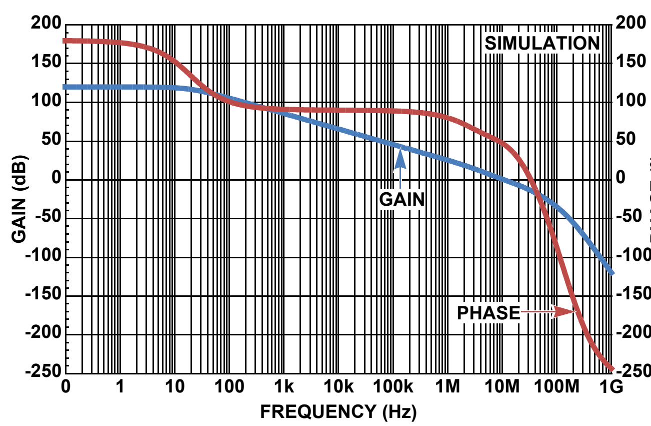


FIGURE 32. OPEN LOOP FREQUENCY RESPONSE (C_L = 47pF)

Typical Performance Curves

Unless otherwise specified, $V_S \pm 18V$, $V_{CM} = 0$, $V_O = 0V$, $T_A = +25°C$. **(Continued)**

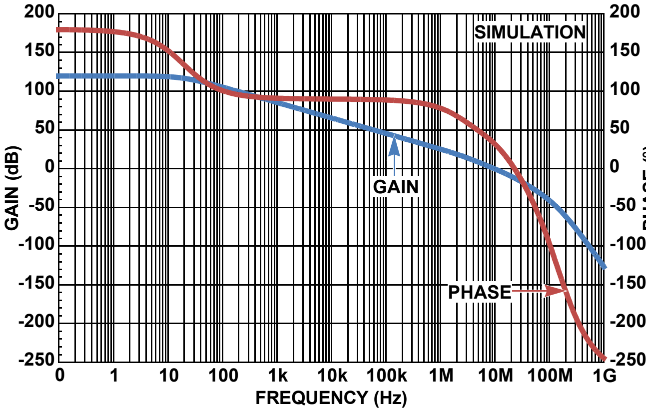


FIGURE 33. OPEN LOOP FREQUENCY RESPONSE (C_L = 100pF)

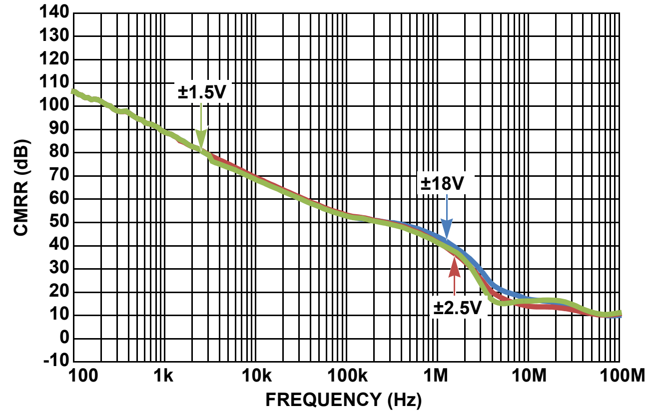


FIGURE 34. CMRR vs FREQUENCY

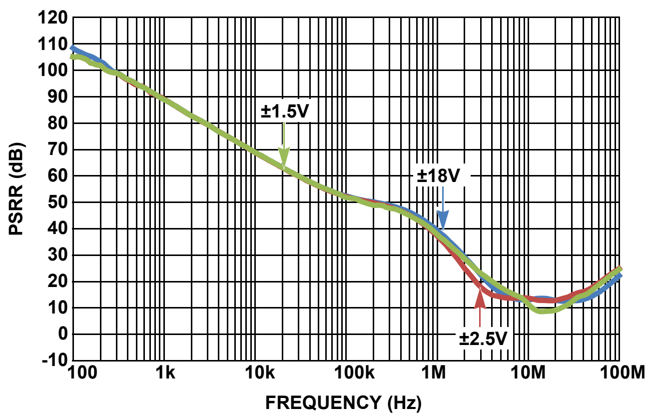


FIGURE 35. PSRR vs FREQUENCY

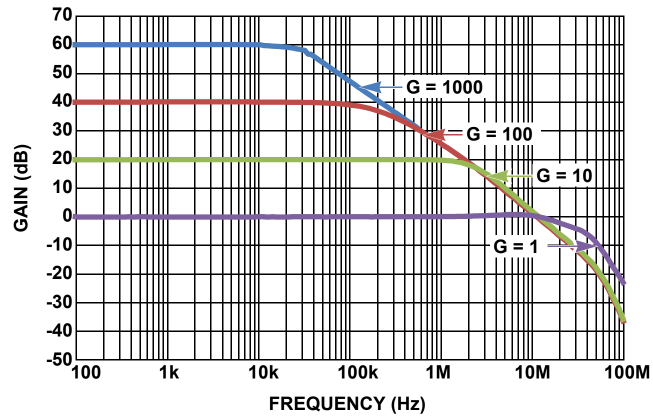


FIGURE 36. CLOSED LOOP GAIN vs FREQUENCY RESPONSE

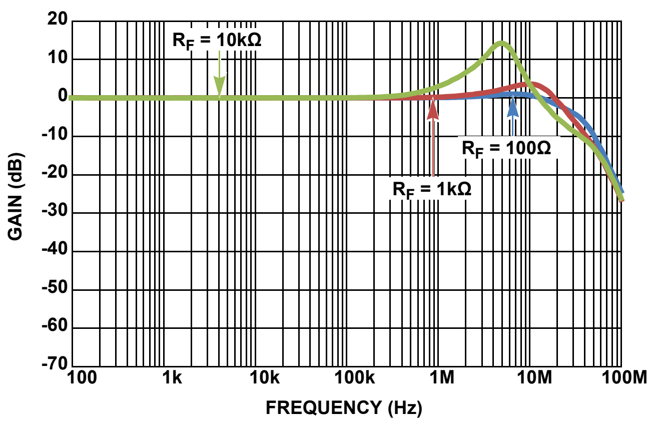


FIGURE 37. FEEDBACK RESISTANCE (R_F) vs FREQUENCY RESPONSE

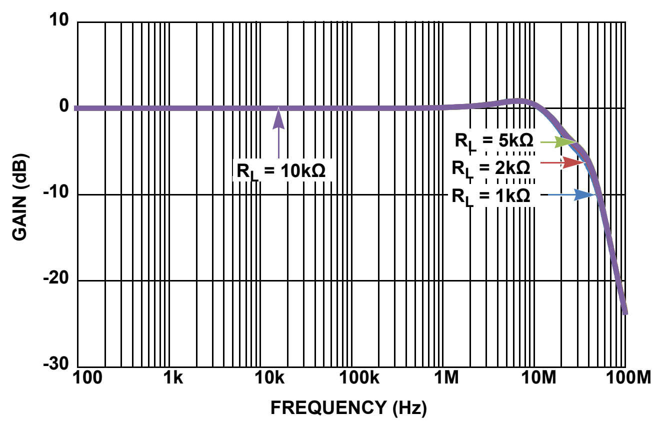


FIGURE 38. LOAD RESISTANCE vs FREQUENCY RESPONSE

Typical Performance Curves Unless otherwise specified, V_S ± 18V, V_{CM} = 0, V_O = 0V, T_A = +25°C. **(Continued)**

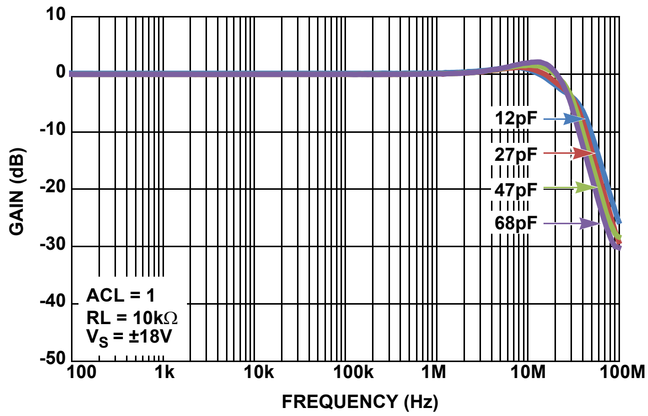


FIGURE 39. UNITY GAIN RESPONSE vs LOAD CAPACITANCE

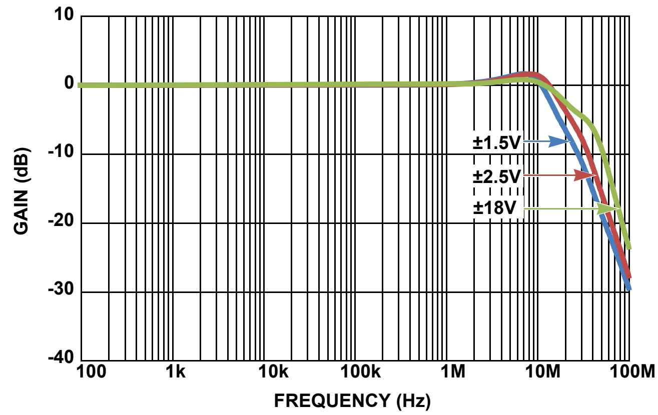


FIGURE 40. SUPPLY VOLTAGE vs FREQUENCY RESPONSE

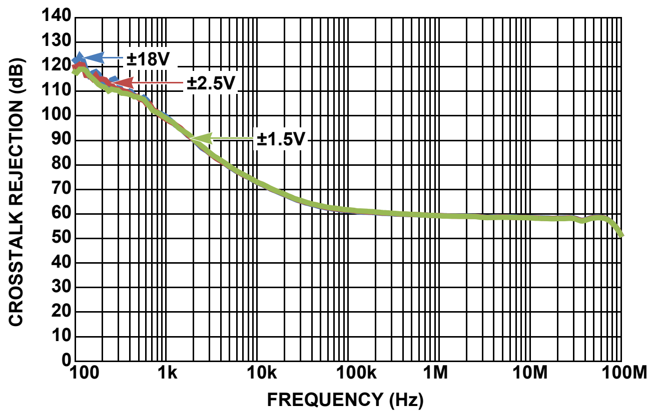


FIGURE 41. CROSSTALK REJECTION vs FREQUENCY

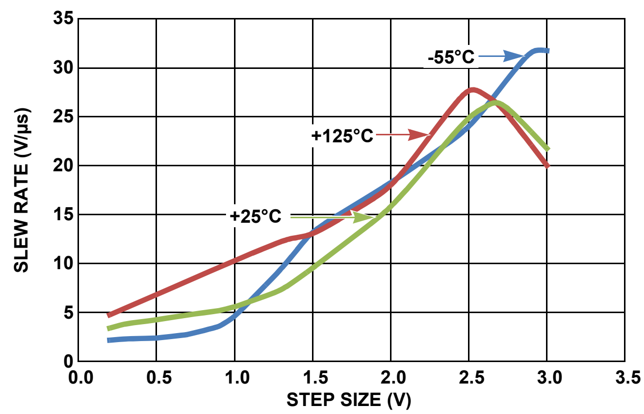


FIGURE 42. SLEW RATE vs STEP SIZE vs TEMPERATURE (V_S = ±1.5V)

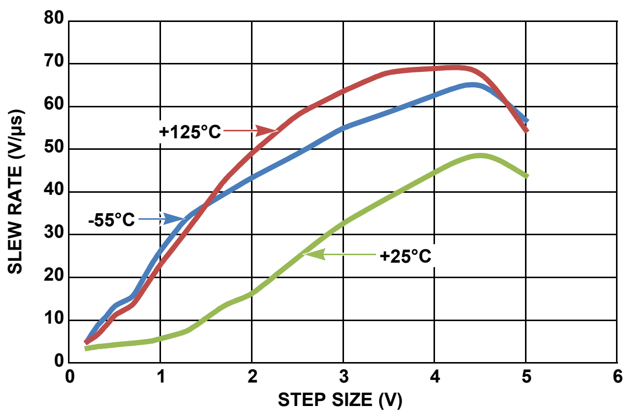


FIGURE 43. SLEW RATE vs STEP SIZE vs TEMPERATURE (V_S = ±2.5V)

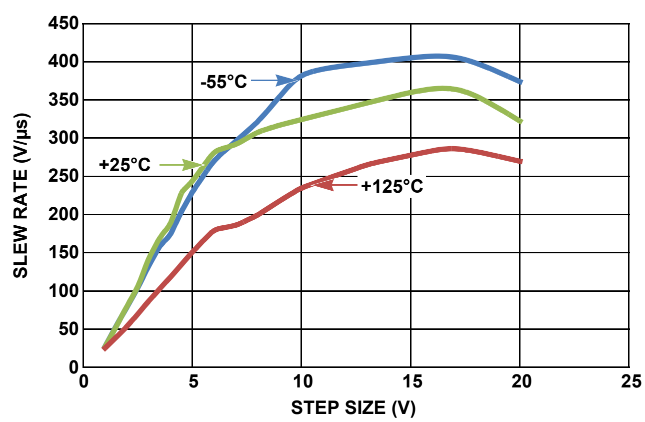


FIGURE 44. SLEW RATE vs STEP SIZE vs TEMPERATURE (V_S = ±18V)

Typical Performance Curves
Unless otherwise specified, V_S ± 18V, V_{CM} = 0, V_O = 0V, T_A = +25°C. **(Continued)**

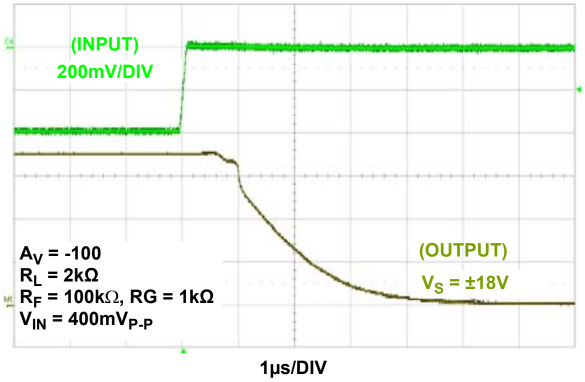


FIGURE 45. SATURATION RECOVERY (V_S = ±18V)

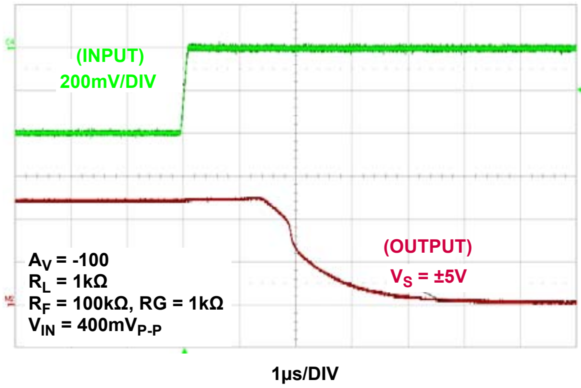


FIGURE 46. SATURATION RECOVERY (V_S = ±5V)

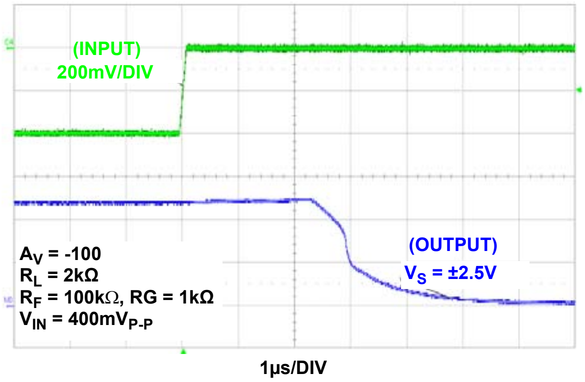


FIGURE 47. SATURATION RECOVERY (V_S = ±2.5V)

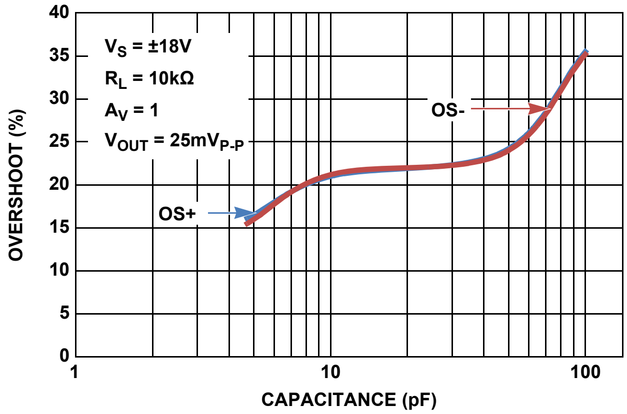


FIGURE 48. OVERSHOOT (%) vs LOAD CAPACITANCE

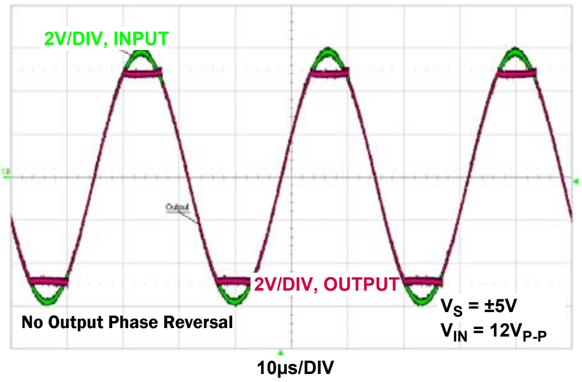


FIGURE 49. INPUT OVERDRIVE RESPONSE

Post High Dose Rate Radiation Characteristics

Unless otherwise specified, $V_S \pm 19.8V$, $V_{CM} = 0$, $V_O = 0V$, $T_A = +25°C$. This data is typical mean test data post radiation exposure at a high dose rate of 50 to 300rad(Si)/s. This data is intended to show typical parameter shifts due to high dose rate radiation. These are not limits nor are they guaranteed.

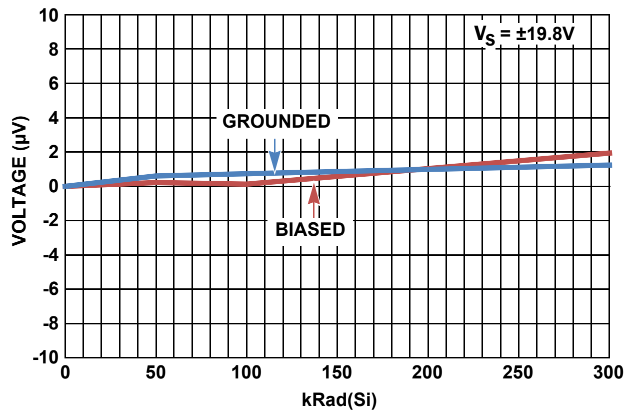


FIGURE 50. V_{OS} SHIFT vs HIGH DOSE RATE RADIATION

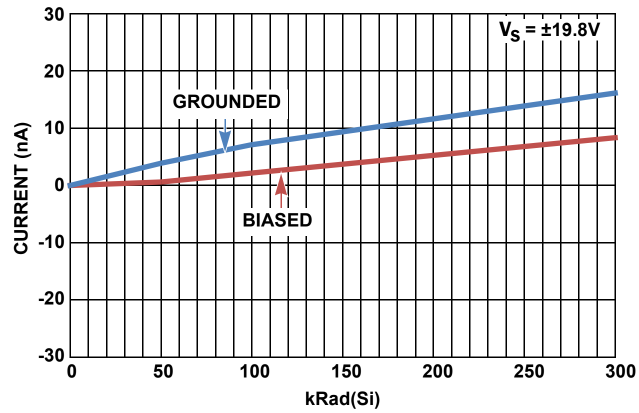


FIGURE 51. I_{BIAS+} SHIFT vs HIGH DOSE RATE RADIATION

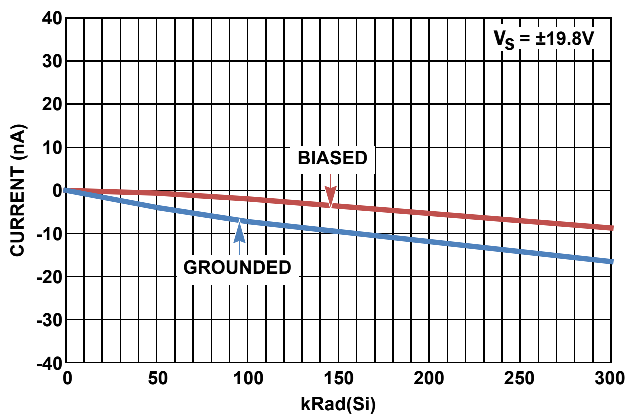


FIGURE 52. I_{BIAS}^- SHIFT vs HIGH DOSE RATE RADIATION

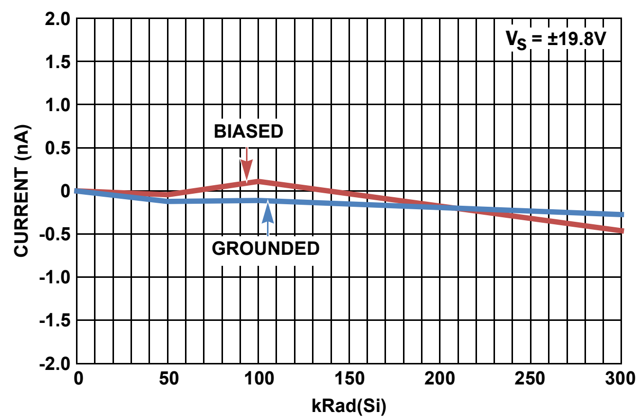


FIGURE 53. I_{OS} SHIFT vs HIGH DOSE RATE RADIATION

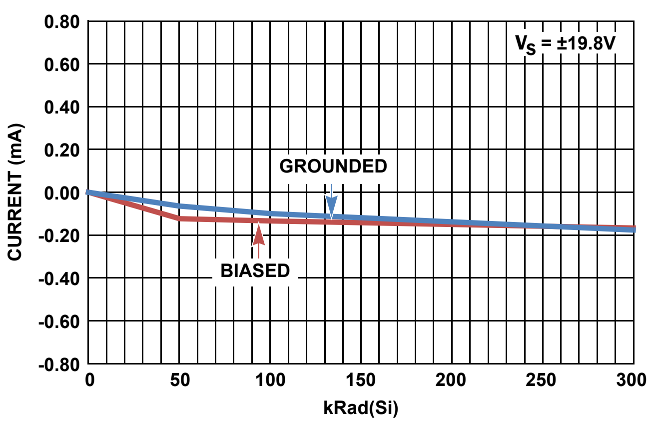


FIGURE 54. I+ vs HIGH DOSE RATE RADIATION

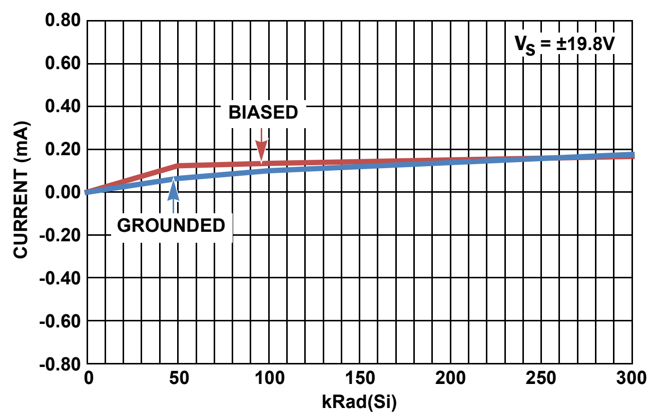


FIGURE 55. I- vs HIGH DOSE RATE RADIATION

Post Low Dose Rate Radiation Characteristics

Unless otherwise specified, $V_S \pm 19.8V$, $V_{CM} = 0$, $V_O = 0V$, $T_A = +25°C$. This data is typical mean test data post radiation exposure at a low dose rate of <10mrad(Si)/s. This data is intended to show typical parameter shifts due to high dose rate radiation. These are not limits nor are they guaranteed.

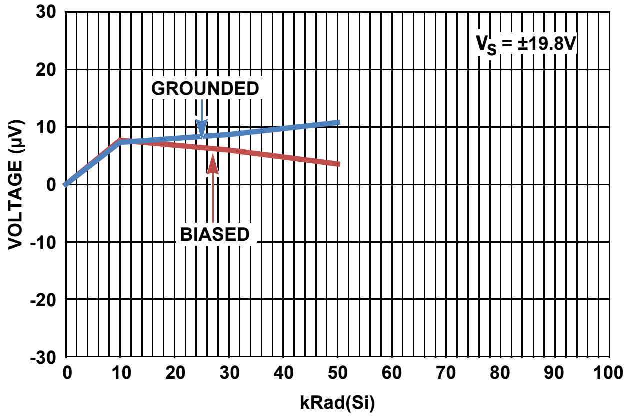


FIGURE 56. V_{OS} SHIFT vs LOW DOSE RATE RADIATION

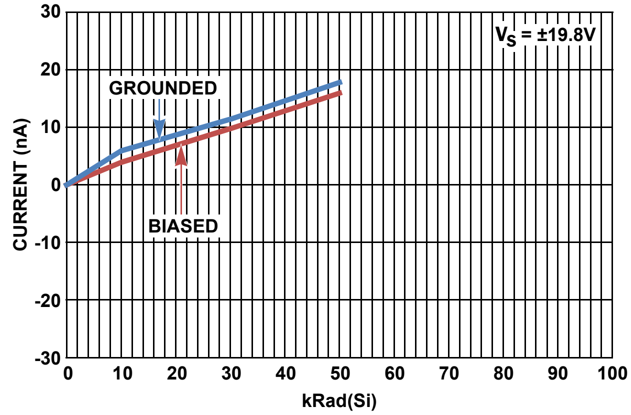


FIGURE 57. $I_{BIAS}+$ vs LOW DOSE RATE RADIATION

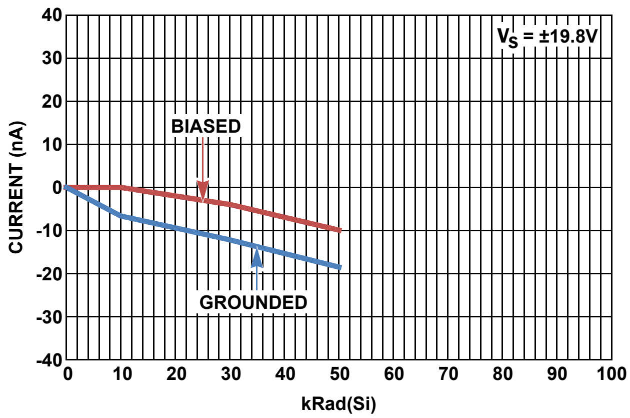


FIGURE 58. $I_{BIAS}-$ vs LOW DOSE RATE RADIATION

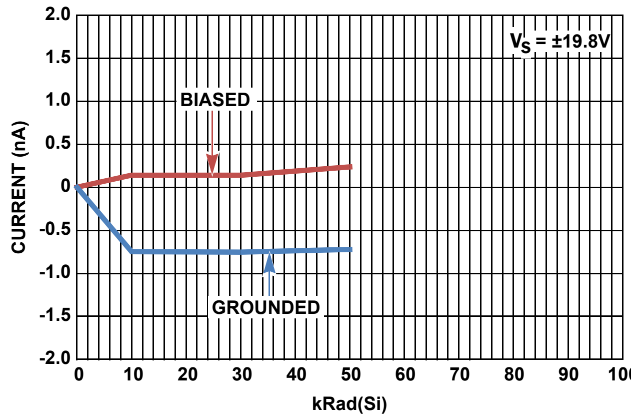


FIGURE 59. I_{OS} vs LOW DOSE RATE RADIATION

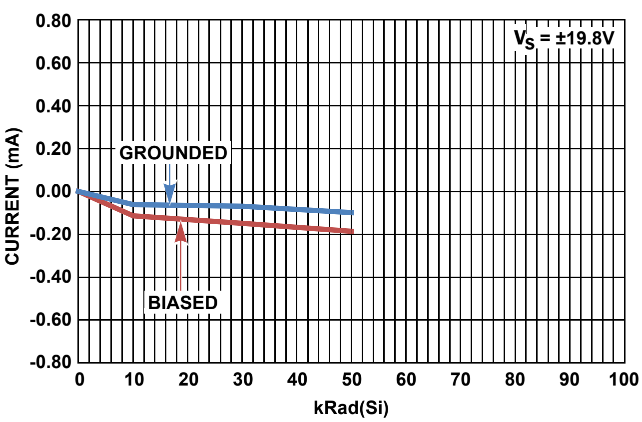


FIGURE 60. I^+ vs LOW DOSE RATE RADIATION

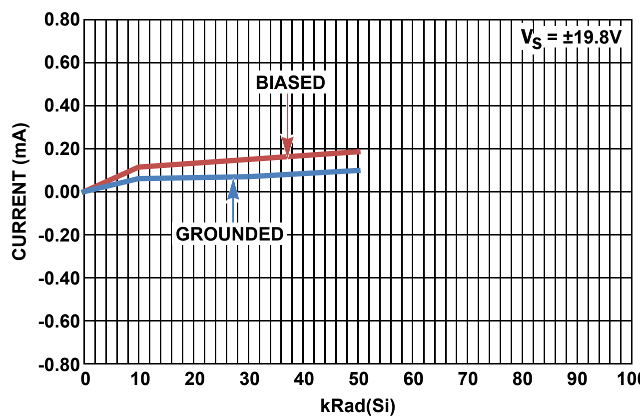


FIGURE 61. I^- vs LOW DOSE RATE RADIATION

Applications Information

Functional Description

The ISL70244SEH contains two high speed, low power op amps designed to take advantage of its full dynamic input and output voltage range with rail to rail operation. By offering low power, low offset voltage, and low temperature drift coupled with its high bandwidth and enhanced slew rates upwards of 50V/µs, these op amps are ideal for applications requiring both high DC accuracy and AC performance. The ISL70244SEH is manufactured in Intersil's PR40 silicon-on-insulator process, which makes this device immune to Single Event Latch-up and provides excellent radiation tolerance. This makes it the ideal choice for high reliability applications in harsh radiation-prone environments.

Operating Voltage Range

The devices are designed to operate with a split supply rail from ±1.35V to ±20V or a single supply rail from 2.7V to 40V. The ISL70244SEH is fully characterized in production for supply rails of 5V (±2.5V) and 36V (±18V). The Power Supply Rejection Ratio is typically 120dB with a nominal ±18V supply. The worst case common mode rejection ratio over temperature is within 1.5V to 2V of each rail. When V_{CM} is inside that range, the CMRR performance is typically >110dB with ±18V supplies. The minimum CMRR performance over the -55°C to +125°C temperature range and radiation is >70dB over the full common mode input range for power supply voltages from ±2.5V (5V) to ±18V (36V).

Input Performance

The slew enhanced front end is a block that is placed in parallel with the main input stage and functions based on the input differential voltage.

Input ESD Diode Protection

The input terminals (IN+ and IN-) have internal ESD protection diodes to the positive and negative supply rails, series connected 600Ω current limiting resistors and an anti-parallel diode pair across the inputs.

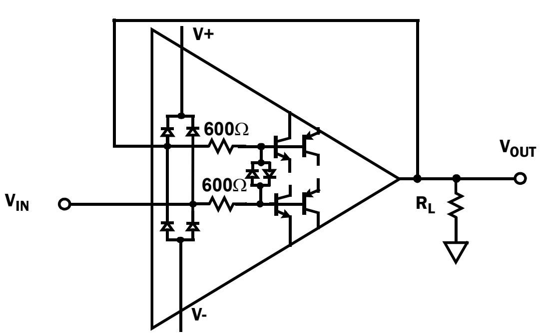


FIGURE 62. INPUT ESD DIODE CURRENT LIMITING, UNITY GAIN

Output Short Circuit Current Limiting

The output current limit has a worst case minimum limit of ±8mA but may reach as high as ±100mA. The op amp can withstand a short circuit to either rail for a short duration (<1 second) as long as the maximum operating junction temperature is not violated. This applies to only one amplifier at a given time. Continued use of the device in these conditions may degrade the long term reliability of the part and is not recommended. Figure 20 shows the typical short circuit currents that can be expected. The ISL70244SEH's current limiting circuitry will automatically lower the current limit of the device if short circuit conditions carry on for extended periods in time in an effort to protect itself from malfunction, however extended operation in this mode will degrade the output rail-to-rail performance by pulling V_{OH}/V_{OL} away from the rails.

Output Phase Reversal

Output phase reversal is a change of polarity in the amplifier transfer function when the input voltage exceeds the supply voltage. The ISL70244SEH is immune to output phase reversal, even when the input voltage is 1V beyond the supplies. This is illustrated in Figure 49.

Power Dissipation

It is possible to exceed the +150°C maximum junction temperatures under certain load and power supply conditions. It is therefore important to calculate the maximum junction temperature (T_{JMAX}) for all applications to determine if power supply voltages, load conditions, or package type need to be modified to remain in the safe operating area. These parameters are related using Equation 1:

$$T_{JMAX} = T_{MAX} + \theta_{JA} \times PD_{MAXTOTAL} \quad \text{(EQ. 1)}$$

where:

- $P_{DMAXTOTAL}$ is the sum of the maximum power dissipation of each amplifier in the package (PD_{MAX})
- PD_{MAX} for each amplifier can be calculated using Equation 2:

$$PD_{MAX} = V_S \times I_{qMAX} + (V_S - V_{OUTMAX}) \times \frac{V_{OUTMAX}}{R_L} \quad \text{(EQ. 2)}$$

where:

- T_{MAX} = Maximum ambient temperature
- θ_{JA} = Thermal resistance of the package
- PD_{MAX} = Maximum power dissipation of 1 amplifier
- V_S = Total supply voltage
- I_{qMAX} = Maximum quiescent supply current of 1 amplifier
- V_{OUTMAX} = Maximum output voltage swing of the application

Unused Channel Configuration

The ISL70244SEH is a dual op amp. If the application does not require the use of both op amps, the user must configure the unused channel to prevent it from oscillating. The unused channel will oscillate if the input and output pins are floating. This results in higher-than-expected supply currents and possible noise injection into the active channel. The proper way to prevent oscillation is to short the output to the inverting input, and ground the positive input (Figure 63).

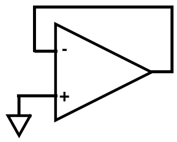


FIGURE 63. PREVENTING OSCILLATIONS IN UNUSED CHANNELS

Die Characteristics

Die Dimensions

2410µm x 1961µm (95mils x 77mils)
Thickness: 483µm ± 25µm (19mils ± 1 mil)

Interface Materials

GLASSIVATION

Type: Nitrox
Thickness: 15kÅ

TOP METALLIZATION

Type: AlCu (99.5%/0.5%)
Thickness: 30kÅ

BACKSIDE FINISH

Silicon

PROCESS

PR40

Assembly Related Information

SUBSTRATE POTENTIAL

Floating

ADDITIONAL INFORMATION

WORST CASE CURRENT DENSITY

$< 2 \times 10^5$ A/cm^2

TRANSISTOR COUNT

365

Weight of Packaged Device

0.3958 grams (Typical)

Lid Characteristics

Finish: Gold
Potential: Unbiased, tied to package pin 6
Case Isolation to Any Lead: 20×10^9 Ω (min)

Metallization Mask Layout

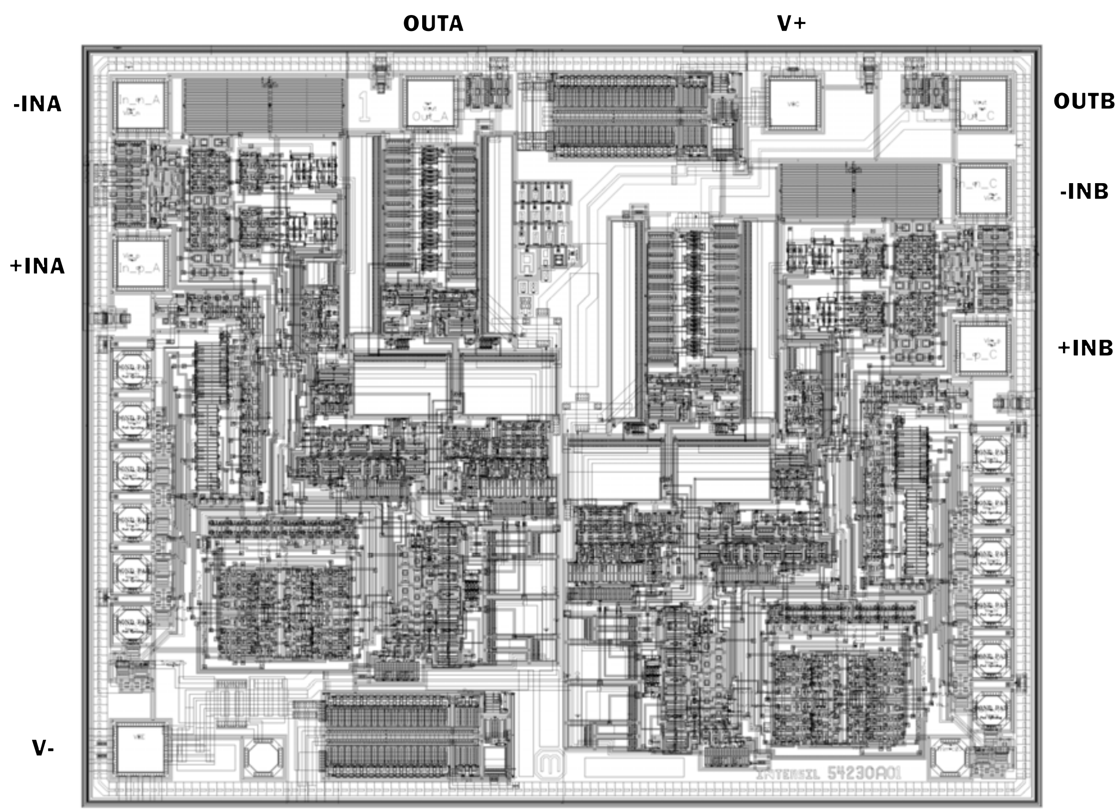


TABLE 1. DIE LAYOUT X-Y COORDINATES						
PAD NAME	PAD NUMBER	X (µm)	Y (µm)	dX (µm)	dY (µm)	BOND WIRES PER PAD
OUTB	1	1015.5	664.0	110	110	1
V+	2	557.0	664.0	110	110	1
OUTA	3	-317.0	664.0	110	110	1
-INA	4	-1015.5	658.0	110	110	1
+INA	5	-1015.5	270.5	110	110	1
V-	12	-1015.5	-918.0	110	110	1
+INB	21	1015.5	62.0	110	110	1
-INB	22	1015.5	449.5	110	110	1

NOTE:

7. Origin of coordinates is the centroid of the die.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
September 22, 2014	FN8592.0	Initial Release.

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

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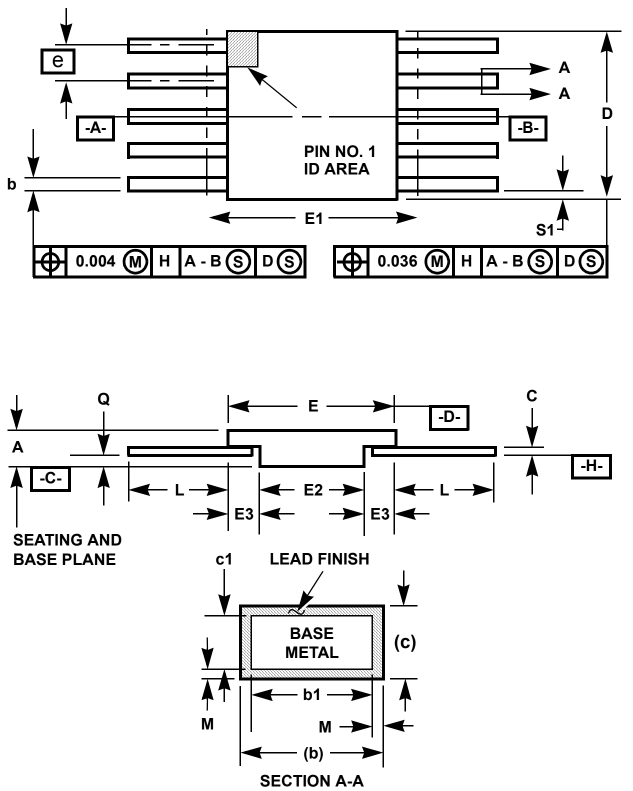
Ceramic Metal Seal Flatpack Packages (Flatpack)



K10.A MIL-STD-1835 CDFP3-F10 (F-4A, CONFIGURATION B)
10 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.045	0.115	1.14	2.92	-
b	0.015	0.022	0.38	0.56	-
b1	0.015	0.019	0.38	0.48	-
c	0.004	0.009	0.10	0.23	-
c1	0.004	0.006	0.10	0.15	-
D	-	0.290	-	7.37	3
E	0.240	0.260	6.10	6.60	-
E1	-	0.280	-	7.11	3
E2	0.125	-	3.18	-	-
E3	0.030	-	0.76	-	7
e	0.050 BSC		1.27 BSC		-
k	0.008	0.015	0.20	0.38	2
L	0.250	0.370	6.35	9.40	-
Q	0.026	0.045	0.66	1.14	8
S1	0.005	-	0.13	-	6
M	-	0.0015	-	0.04	-
N	10		10		-

Rev. 0 3/07

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab (dimension k) may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of dimension k do not apply.
3. This dimension allows for off-center lid, meniscus, and glass overrun.
4. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
5. N is the maximum number of terminal positions.
6. Measure dimension S1 at all four corners.
7. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
8. Dimension Q shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension Q minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.