BCM® in a VIA Package Bus Converter

BCM3814x60E10A5yzz

Isolated, Fixed-Ratio DC-DC Converter

Features & Benefits

- Up to 150A continuous low voltage side current
- Fixed transformation ratio(K) of 1/6
- Up to 769 W/in^3 power density
- 97.2% peak efficiency
- Integrated ceramic capacitance filtering
- Parallel operation for multi-kW arrays
- OV, OC, UV, short circuit and thermal protection
- 3814 package
- High MTBF
- Thermally enhanced VIA™ package
- PMBus™ management interface

Typical Applications

- DC Power Distribution
- Information and Communication Technology (ICT) Equipment
- High End Computing Systems
- Automated Test Equipment
- Industrial Systems
- High Density Energy Systems
- Transportation

Product Ratings	
V_{HI} = 54V (36 – 60V)	I_{LO} = up to 150A
V_{LO} = 9V (6 – 10V) (NO LOAD)	K = 1/6

Product Description

The BCM in a VIA package is a high efficiency Bus Converter, operating from a 36 to 60V_{DC} high voltage bus to deliver an isolated 6 to 10V_{DC} unregulated, low voltage.

This unique ultra-low profile module incorporates DC-DC conversion, integrated filtering and PMBus™ commands and controls in a chassis or PCB mount form factor.

The BCM offers low noise, fast transient response and industry leading efficiency and power density. A low voltage side referenced PMBus™ compatible telemetry and control interface provides access to the BCM's internal controller configuration, fault monitoring, and other telemetry functions.

Leveraging the thermal and density benefits of Vicor's VIA packaging technology, the BCM module offers flexible thermal management options with very low top and bottom side thermal impedances.

When combined with downstream Vicor DC-DC conversion components and regulators, the BCM allows the Power Design Engineer to employ a simple, low-profile design which will differentiate the end system without compromising on cost or performance metrics.

Size:
3.76 x 1.40 x 0.37 in
95.59 x 35.54 x 9.40 mm

Part Ordering Information

Product Function	Package Length	Package Width	Package Type	Max High Side Voltage	High Side Voltage Range Ratio	Max Low Side Voltage	Max Low Side Current	Product Grade (Case Temperature)	Option Field
BCM	38	14	x	60	E	10	A5	y	zz
BCM = Bus Converter Module	Length in Inches x 10	Width in Inches x 10	B = Board VIA V = Chassis VIA	Internal Reference				C = -20 to 100°C[1] T = -40 to 100°C[1]	02 = Chassis/PMBus 06 = Short Pin/PMBus 10 = Long Pin/PMBus

[1] High Temperature Current Derating may apply; See Figure 1, specified thermal operating area.

Electrical Specifications

Specifications apply over all line and load conditions, unless otherwise noted; **Boldface** specifications apply over the temperature range of -40°C ≤ T_{CASE} ≤100°C (T-Grade); All other specifications are at T_{CASE} = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
General Powertrain High Voltage Side to Low Voltage Side Specification (Forward Direction)						
High Side Input Voltage range, continuous	V_{HI_DC}		**36**		**60**	V
V_{HI} µController	$V_{\mu C\_ACTIVE}$	V_{HI_DC} voltage where µC is initialized, (powertrain inactive)			14	V
HI to LO Input Quiescent Current	I_{HI_Q}	Disabled, V_{HI_DC} = 54V		5		mA
		T_{CASE} ≤ 100°C			10	
HI to LO No Load Power Dissipation	P_{HI_NL}	V_{HI_DC} = 54V, T_{CASE} = 25°C		7.2	9	W
		V_{HI_DC} = 54V	**5**		**14**	
		V_{HI_DC} = 36V to 60V, T_{CASE} = 25 °C			12	
		V_{HI_DC} = 36V to 60V			**17**	
HI to LO Inrush Current Peak	$I_{HI\_INR\_PK}$	V_{HI_DC} = 60V, C_{LO_EXT} = 4000 µF, R_{LOAD_LO} = 20% of full load current		30		A
		T_{CASE} ≤ 100°C			35	
DC High Side Input Current	$I_{HI\_IN\_DC}$	At $I_{LO\_OUT\_DC}$ = 150A, T_{CASE} ≤ 85°C			25.5	A
Transformation Ratio	K	High voltage to low voltage, K = V_{LO_DC} / V_{HI_DC}, at no load		1/6		V/V
Low Side Output Current (continuous)	$I_{LO\_OUT\_DC}$	T_{CASE} ≤ 85°C			150	A
Low Side Output Current (pulsed)	$I_{LO\_OUT\_PULSE}$	10 ms pulse, 25% Duty cycle, $I_{LO\_OUT\_AVG}$ ≤ 50% rated $I_{LO\_OUT\_DC}$			180	A
HI to LO Efficiency (ambient)	η_{AMB}	V_{HI_DC} = 54V, $I_{LO\_OUT\_DC}$ = 150A	95.2	95.8		%
		V_{HI_DC} = 36V to 60V, $I_{LO\_OUT\_DC}$ = 150A	93.6			
		V_{HI_DC} = 54V, $I_{LO\_OUT\_DC}$ = 75A	96.7	97.2		
HI to LO Efficiency (hot)	η_{HOT}	V_{HI_DC} = 54V, $I_{LO\_OUT\_DC}$ = 150A, T_{CASE} = 85°C	95.4	95.6		%
HI to LO Efficiency (over load range)	$\eta_{20\%}$	30 A < $I_{LO\_OUT\_DC}$ < 150A	93			%
HI to LO Output Resistance	R_{LO_COLD}	V_{HI_DC} = 54V, $I_{LO\_OUT\_DC}$ = 150A, T_{CASE} = -40°C	0.9	1.7	2.1	mΩ
	R_{LO_AMB}	V_{HI_DC} = 54V, $I_{LO\_OUT\_DC}$ = 150A	2	2.1	2.4	
	R_{LO_HOT}	V_{HI_DC} = 54V, $I_{LO\_OUT\_DC}$ = 150A, T_{CASE} = 85°C	1.6	2.3	2.6	
Switching Frequency	F_{SW}	Frequency of the LO Side Voltage Ripple = 2x F_{SW}	**0.85**	0.90	**0.95**	MHz
Low Side Output Voltage Ripple	$V_{LO\_OUT\_PP}$	C_{LO_EXT} = 0µF, $I_{LO\_OUT\_DC}$ = 150A, V_{HI_DC} = 54V, 20 MHz BW		120		mV
		T_{CASE} ≤ 100°C			200	

Electrical Specifications (Cont.)

Specifications apply over all line and load conditions, unless otherwise noted; **Boldface** specifications apply over the temperature range of -40°C ≤ T_{CASE} ≤100°C (T-Grade); All other specifications are at T_{CASE} = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
General Powertrain High Voltage Side to Low Voltage Side Specification (Forward Direction) Cont.						
Effective HI Side Capacitance (Internal)	C_{HI_INT}	Effective Value at $54V_{HI\_DC}$		11.2		µF
Effective LO Side Capacitance (Internal)	C_{LO_INT}	Effective Value at $9V_{LO\_DC}$		202		µF
Effective LO Side Output Capacitance (External)	$C_{LO\_OUT\_EXT}$	Excessive capacitance may drive module into SC protection			**6000**	µF
Effective LO Side Output Capacitance (External)	$C_{LO\_OUT\_AEXT}$	$C_{LO\_OUT\_AEXT}$ Max = N * 0.5 * $C_{LO\_OUT\_EXT\ MAX}$, where N = the number of units in parallel				
Powertrain Protection High Voltage Side to Low Voltage Side (Forward Direction)						
Auto Restart Time	$t_{AUTO\_RESTART}$	Startup into a persistent fault condition. Non-Latching fault detection given $V_{HI\_DC} > V_{HI\_UVLO+}$	**490**		**560**	ms
HI Side Overvoltage Lockout Threshold	V_{HI_OVLO+}		**63**	67	**71**	V
HI Side Overvoltage Recovery Threshold	V_{HI_OVLO-}		**61**	65	**69**	V
HI Side Overvoltage Lockout Hysteresis	$V_{HI\_OVLO\_HYST}$			2		V
HI Side Overvoltage Lockout Response Time	t_{HI_OVLO}			100		µs
HI Side Soft-Start Time	$t_{HI\_SOFT-START}$	From powertrain active. Fast Current limit protection disabled during Soft-Start		1		ms
LO Side Output Overcurrent Trip Threshold	$I_{LO\_OUT\_OCP}$		**180**	204	**240**	A
LO Side Output Overcurrent Response Time Constant	$t_{LO\_OUT\_OCP}$	Effective internal RC filter		3		ms
LO Side Output Short Circuit Protection Trip Threshold	$I_{LO\_OUT\_SCP}$		**195**			A
LO Side Output Short Circuit Protection Response Time	$t_{LO\_OUT\_SCP}$			1		µs
Overtemperature Shutdown Threshold	t_{OTP+}	Temperature sensor located inside controller IC (Internal Temperature)	**125**			°C

Electrical Specifications (Cont.)

Specifications apply over all line and load conditions, unless otherwise noted; **Boldface** specifications apply over the temperature range of -40°C ≤ T_{CASE} ≤100°C (T-Grade); All other specifications are at T_{CASE} = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Powertrain Supervisory Limits HIGH VOLTAGE SIDE to LOW VOLTAGE SIDE (Forward Direction)						
HI Side Overvoltage Lockout Threshold	V_{HI_OVLO+}		**64**	66	**68**	V
HI Side Overvoltage Recovery Threshold	V_{HI_OVLO-}		**60**	64	**66**	V
HI Side Overvoltage Lockout Hysteresis	$V_{HI\_OVLO\_HYST}$			2		V
HI Side Overvoltage Lockout Response Time	t_{HI_OVLO}			100		µs
HI Side Undervoltage Lockout Threshold	V_{HI_UVLO-}		**26**	28	**30**	V
HI Side Undervoltage Recovery Threshold	V_{HI_UVLO+}		**28**	30	**32**	V
HI Side Undervoltage Lockout Hysteresis	$V_{HI\_UVLO\_HYST}$			2		V
HI Side Undervoltage Lockout Response Time	t_{HI_UVLO}			100		µs
HI Side Undervoltage Startup Delay	$t_{HI\_UVLO+\_DELAY}$	From V_{HI_DC} = V_{HI_UVLO+} to powertrain active, (i.e One time Startup delay form application of V_{HI_DC} to V_{LO_DC})		20		ms
LO Side Output Overcurrent Trip Threshold	$I_{LO\_OUT\_OCP}$		**193**	204	**215**	A
LO Side Output Overcurrent Response Time Constant	$t_{LO\_OUT\_OCP}$	Effective internal RC filter		3		ms
Overtemperature Shutdown Threshold	t_{OTP+}	Temperature sensor located inside controller IC (Internal Temperature)	**125**			°C
Overtemperature Recovery Threshold	t_{OTP-}	Temperature sensor located inside controller IC (Internal Temperature)	105	110	115	°C
Undertemperature Shutdown Threshold	t_{UTP}	Temperature sensor located inside controller IC; Protection not available for M-Grade units.			-45	°C
Undertemperature Restart Time	$t_{UTP\_RESTART}$	Startup into a persistent fault condition. Non-Latching fault detection given V_{HI_DC} > V_{HI_UVLO+}		3		s

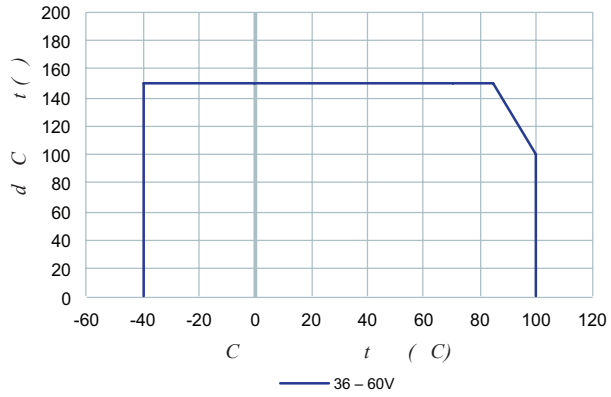
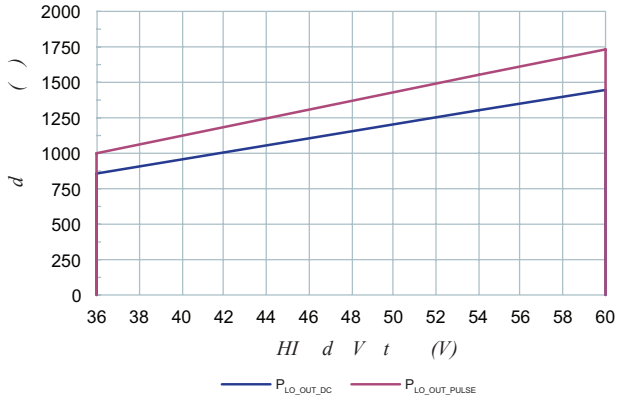


Figure 1 *— Specified thermal operating area*

1. The BCM in a VIA Package is cooled through bottom case (bottom housing).
2. The thermal rating of the BCM in a VIA Package is based on typical measured device efficiency.
3. The case temperature in the graph is the measured temperature of the bottom housing, such that operating internal junction temperature of the BCM in a VIA Package does not exceed 125°C.



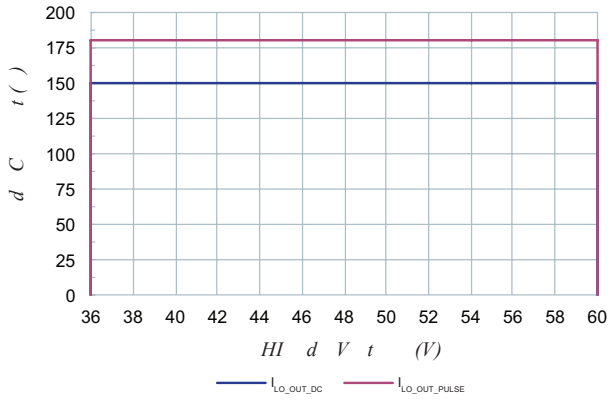


Figure 2 *— Specified electrical operating area using rated R_{LO_HOT}*

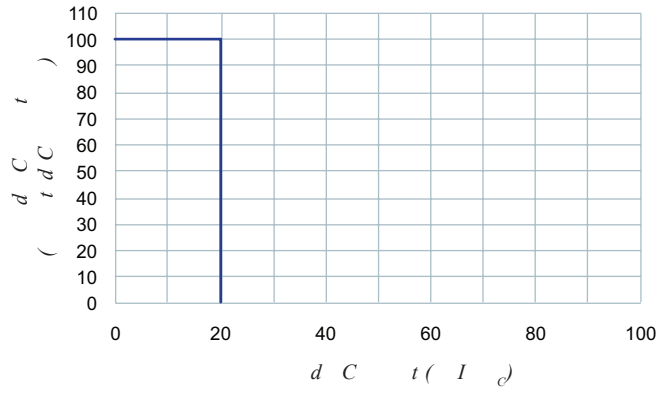


Figure 3 *— Specified HI side start-up into load current and external capacitance*

PMBus™ Reported Characteristics

Specifications apply over all line and load conditions, unless otherwise noted; **Boldface** specifications apply over the temperature range of -40°C ≤ T_{CASE} ≤100°C (T-Grade); All other specifications are at T_{CASE} = 25°C unless otherwise noted.

Monitored Telemetry					
• The BCM communication version is not intended to be used without a Digital Supervisor.					
ATTRIBUTE	**DIGITAL SUPERVISOR PMBus™ READ COMMAND**	**ACCURACY (RATED RANGE)**	**FUNCTIONAL REPORTING RANGE**	**UPDATE RATE**	**REPORTED UNITS**
HI Side Voltage	(88h) READ_VIN	± 5%(LL - HL)	28V to 66V	100µs	$V_{ACTUAL} = V_{REPORTED} \times 10^{-1}$
HI Side Current	(89h) READ_IIN	± 20%(10 - 20% of FL) ± 5%(20 - 133% of FL)	-1A to 34A	100µs	$I_{ACTUAL} = I_{REPORTED} \times 10^{-2}$
LO Side Voltage[1]	(8Bh) READ_VOUT	± 5%(LL - HL)	4.7V to 11V	100µs	$V_{ACTUAL} = V_{REPORTED} \times 10^{-1}$
LO Side Current	(8Ch) READ_IOUT	± 20%(10 - 20% of FL) ± 5%(20 - 133% of FL)	-6A to 204A	100µs	$I_{ACTUAL} = I_{REPORTED} \times 10^{-2}$
LO Side Resistance	(D4h) READ_ROUT	± 5%(50 - 100% of FL) at NL ± 10%(50 - 100% of FL)(LL - HL)	500u to 3000u	100ms	$R_{ACTUAL} = R_{REPORTED} \times 10^{-5}$
Temperature[2]	(8Dh) READ_TEMPERATURE_1	± 7°C(Full Range)	- 55°C to 130°C	100ms	$T_{ACTUAL} = T_{REPORTED}$

[1] Default READ LO Side Voltage returned when unit is disabled = -300V.
[2] Default READ Temperature returned when unit is disabled = -273°C.

Variable Parameter					
• Factory setting of all below Thresholds and Warning limits are 100% of listed protection values. • Variables can be written only when module is disabled either EN pulled low or $V_{HI} < V_{HI\_UVLO-}$. • Module must remain in a disabled mode for 3ms after any changes to the below variables allowing ample time to commit changes to EEPROM.					
ATTRIBUTE	**DIGITAL SUPERVISOR PMBus™ COMMAND [3]**	**CONDITIONS / NOTES**	**ACCURACY (RATED RANGE)**	**FUNCTIONAL REPORTING RANGE**	**DEFAULT VALUE**
HI Side Overvoltage Protection Limit	(55h) VIN_OV_FAULT_LIMIT	V_{HI_OVLO-} is automatically 3% lower than this set point	± 5%(LL - HL)	28V to 66V	100%
HI Side Overvoltage Warning Limit	(57h) VIN_OV_WARN_LIMIT		± 5%(LL - HL)	28V to 66V	100%
HI Side Undervoltage Protection Limit	(D7h) DISABLE_FAULTS	Can only be disabled to a preset default value	± 5%(LL - HL)	28V or 66V	100%
HI Side Overcurrent Protection Limit	(5Bh) IIN_OC_FAULT_LIMIT		± 20%(10 - 20% of FL) ± 5%(20 - 133% of FL)	0 to 34A	100%
HI Side Overcurrent Warning Limit	(5Dh) IIN_OC_WARN_LIMIT		± 20%(10 - 20% of FL) ± 5%(20 - 133% of FL)	0 to 34A	100%
Overtemperature Protection Limit	(4Fh) OT_FAULT_LIMIT	Internal Temperature	± 7°C(Full Range)	0 to 125°C	100%
Overtemperature Warning Limit	(51h) OT_WARN_LIMIT	Internal Temperature	± 7°C(Full Range)	0 to 125°C	100%
Turn on Delay	(60h) TON_DELAY	Additional time delay to the Undervoltage Startup Delay	± 50µs	0 to 100ms	0ms

[3] Refer to internal µc datasheet for complete list of supported commands.

Signal Characteristics

Specifications apply over all line and load conditions, unless otherwise noted; **Boldface** specifications apply over the temperature range of -40°C ≤ T_{CASE} ≤100°C (T-Grade); All other specifications are at T_{CASE} = 25°C unless otherwise noted. **Please note:** For chassis mount model, Vicor part number 42550 will be needed for applications requiring the use of the signal pins. Signal cable 42550 is rated up to five insertions and extractions. To avoid unnecessary stress on the connector, the cable should be tied to the chassis.

EXT. BIAS (VDDB) Pin

- 5V supply input, required to power the circuitry internal to the BCM in a VIA package for communication signals such as SCL, SDA, ADDR etc
- Voltage to EXT BIAS pin is needed for PMBus™ enable and disable control. It is not needed for PMBus monitoring voltage, current, power or temperature. Lower voltage is better. It will help to lower the power dissapation in the internal regulator that is generating 3.3V voltage for communication circuits.
- Apply voltage to this pin between 4.5V and 9V. The nominal voltage is 5V.

SIGNAL TYPE	STATE	ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	MIN	TYP	MAX	UNIT
INPUT	Regular Operation	VDDB Voltage	V_{VDDB}		4.5	5	9	V
		VDDB Current consumption	I_{VDDB}				50	mA
	Startup	Inrush Current Peak	I_{VDDB_INR}	V_{VDDB} Slew Rate = 1V/µs		3.5		A
		Turn on time	t_{VDDB_ON}	From V_{VDDB_MIN} to PMBus active		1.5		ms

SGND Pin

- This pin is supply return pin for Ext. Bias (VDDB) pin.
- All input and output signals (SCL, SDA, ADDR) are referenced to SGND pin.

Address (ADDR) Pin

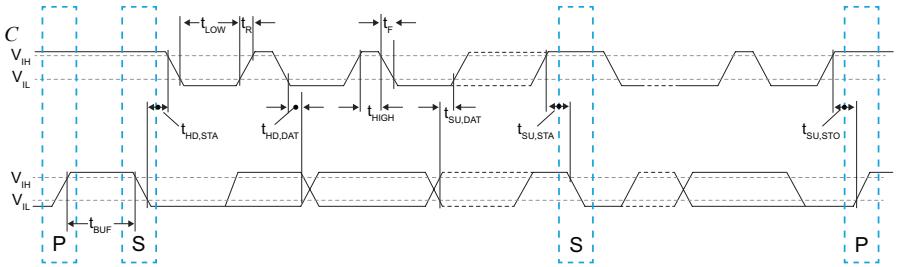
- This pin programs only a Fixed and Persistent slave address for BCM in a VIA package.
- This pin programs the address using a resistor between ADDR pin and signal ground.
- The address is sampled during startup and is used until power is reset.
- This pin has 10kΩ pullup resistor internally between ADDR pin and internal VDD.
- 16 addresses are available. Relative to nominal value of internal VDD (V_{VDD_NOM} = 3.3V), a 206.25mV range per address.

SIGNAL TYPE	STATE	ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	MIN	TYP	MAX	UNIT
MULTI-LEVEL INPUT	Regular Operation	ADDR Input Voltage	V_{SADDR}	See address section	0		3.3	V
		ADDR leakage current	I_{SADDR}	Leakage current			1	µA
	Startup	ADDR registration time	t_{SADDR}	From $V_{VDD\_IN\_MIN}$		1		ms

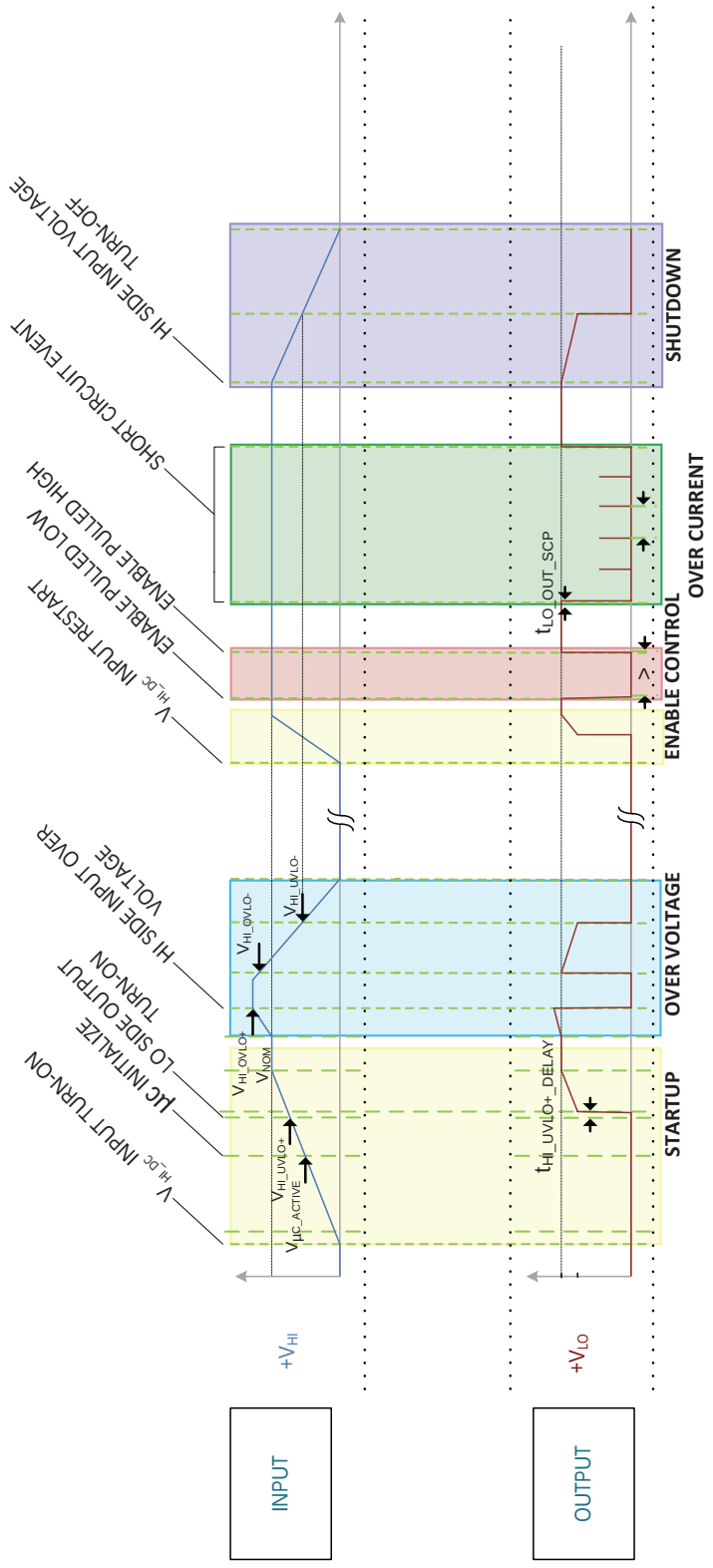
Serial Clock input (SCL) AND Serial Data (SDA) Pins

- High-power SMBus specification and SMBus physical layer compatible. Note that optional SMBALERT# is signal not supported.
- PMBus™ command compatible.
- The internal µC requires the use of a flip-flop to drive SSTOP. See system diagram section for more details.

SIGNAL TYPE	STATE	ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	MIN	TYP	MAX	UNIT
DIGITAL INPUT/OUTPUT	Regular Operation	**Electrical Parameters**						
		Input Voltage Threshold	V_{IH}	V_{VDD_IN} = 3.3V	2.1			V
			V_{IL}	V_{VDD_IN} = 3.3V			0.8	V
		Output Voltage Threshold	V_{OH}	V_{VDD_IN} = 3.3V	3			V
			V_{OL}	V_{VDD_IN} = 3.3V			0.4	V
		Leakage current	$I_{LEAK-PIN}$	Unpowered device			10	µA
		Signal Sink Current	I_{LOAD}	V_{OL} = 0.4V	4			mA
		Signal Capacitive Load	C_I	Total capacitive load of one device pin			10	pF
		Signal Noise Immunity	V_{NOISE_PP}	10MHz to 100MHz	300			mV
		Timing Parameters						
		Operating Frequency	F_{SMB}	Idle state = 0Hz	10		400	KHz
		Free time between Stop and Start Condition	t_{BUF}		1.3			µs
		Hold time after Start or Repeated Start condition	$t_{HD:STA}$	First clock is generated after this hold time	0.6			µs
		Repeat Start Condition Setup time	$t_{SU:STA}$		0.6			µs
		Stop Condition setup time	$t_{SU:STO}$		0.6			µs
		Data Hold time	$t_{HD:DAT}$		300			ns
		Data Setup time	$t_{SU:DAT}$		100			ns
		Clock low time out	$t_{TIMEOUT}$		25		35	ms
		Clock low period	t_{LOW}		1.3			µs
		Clock high period	t_{HIGH}		0.6		50	µs
		Cumulative clock low extend time	$t_{LOW:SEXT}$				25	ms
		Clock or Data Fall time	t_F	Measured from (V_{IL_MAX} −0.15) to (V_{IH_MIN} + 0.15)	20		300	ns
		Clock or Data Rise time	t_R	0.9 • $V_{VDD\_IN\_MAX}$ to (V_{IL_MAX} −0.15)	20		300	ns



Timing diagram (Foward Direction)



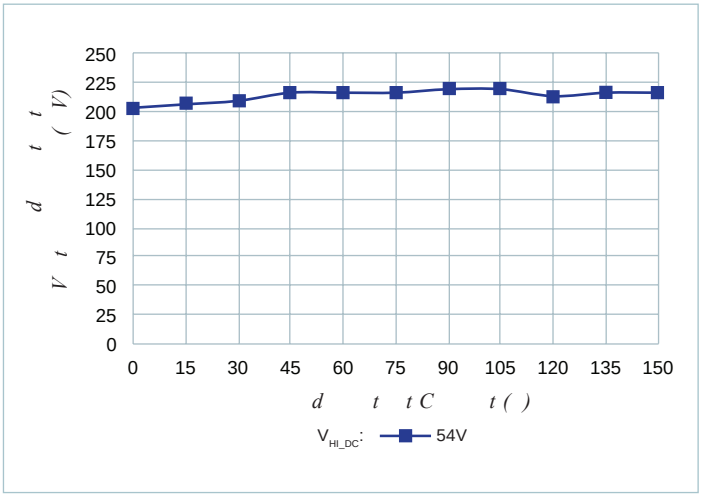


Figure 10 — *$V_{LO\_OUT\_PP}$ vs. I_{LO_DC} ; No external $C_{LO\_OUT\_EXT}$, Board mounted module, scope setting : 20MHz analog BW*

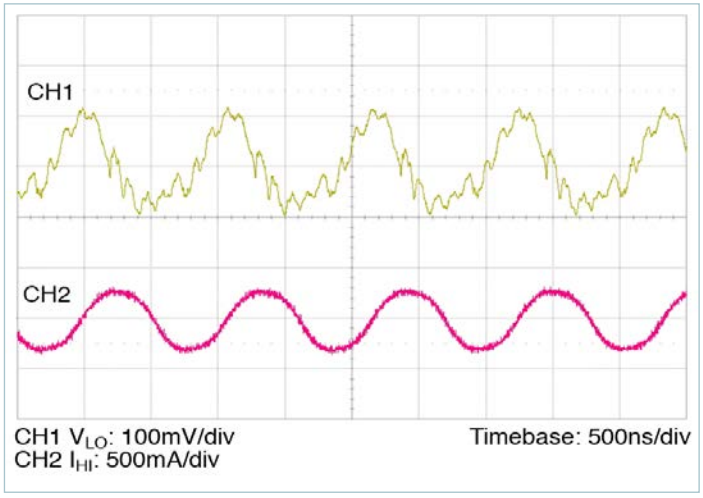


Figure 11 — *Full load ripple, 300µF $C_{HI\_IN\_EXT}$; No external $C_{LO\_OUT\_EXT}$, Board mounted module, scope setting : 20MHz analog BW*

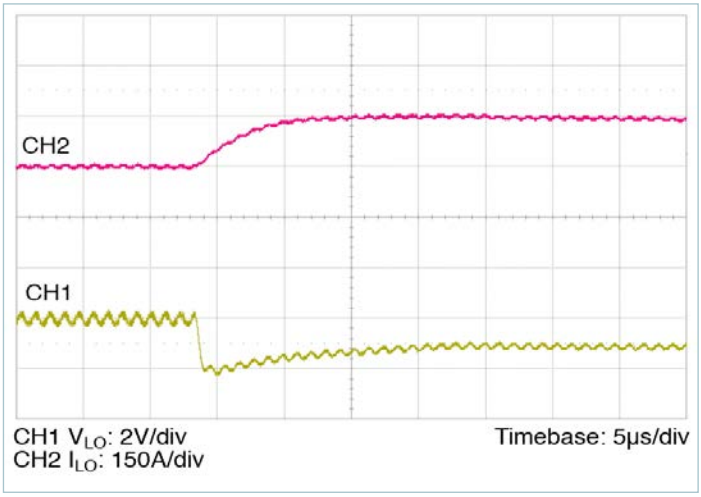


Figure 12 — *0 A– 150A transient response: $C_{HI\_IN\_EXT}$ = 300µF, no external $C_{LO\_OUT\_EXT}$*

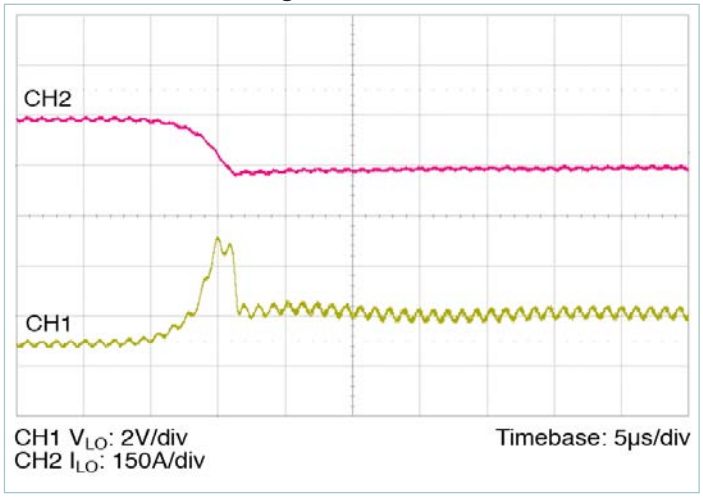


Figure 13 — *150A – 0A transient response: $C_{HI\_IN\_EXT}$ = 300µF, no external $C_{LO\_OUT\_EXT}$*

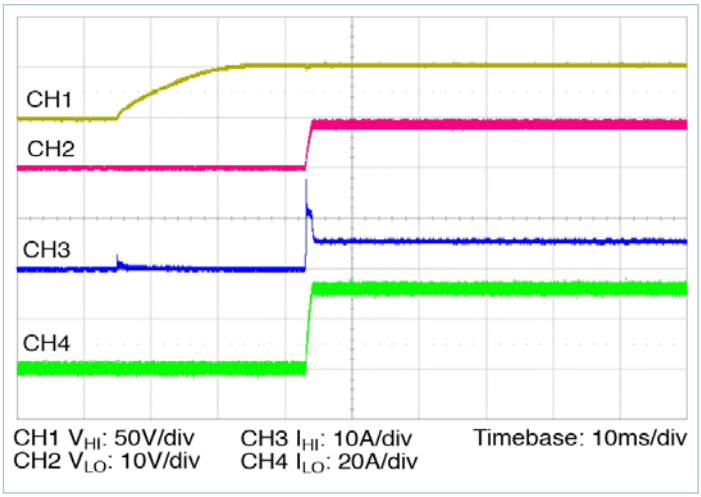


Figure 14 — *Start up from application of V_{HI_DC} = 54V, 20% I_{LO_DC}, 100% $C_{LO\_OUT\_EXT}$*

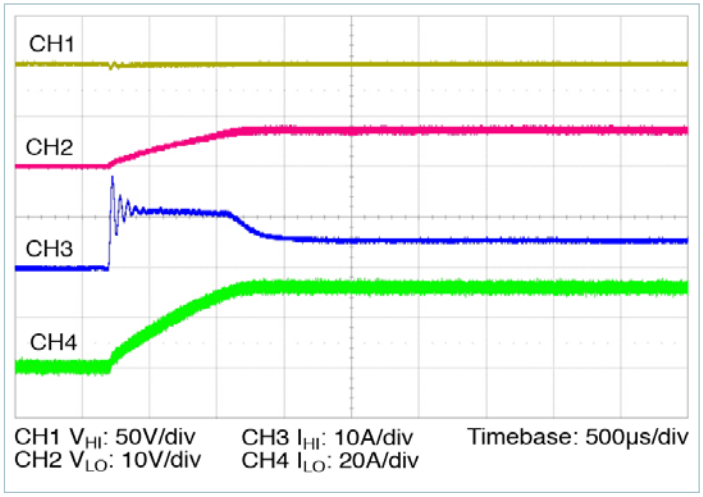


Figure 15 — *Start up from application of EN with pre-applied V_{HI_DC} = 54V, 20% I_{LO_DC}, 100% $C_{LO\_OUT\_EXT}$*

General Characteristics

Specifications apply over all line and load conditions, unless otherwise noted; **Boldface** specifications apply over the temperature range of -40°C ≤ T_{CASE} ≤100°C (T-Grade); All other specifications are at T_{CASE} = 25°C unless otherwise noted.

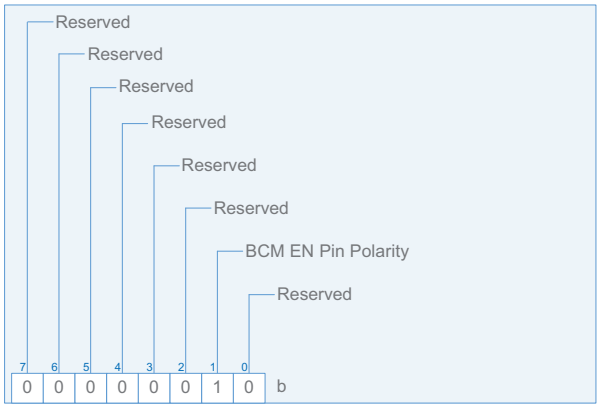
Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Mechanical						
Length	L	Lug (Chassis) Mount	95.34 / [3.75]	95.59 / [3.76]	95.84 / [3.77]	mm / [in]
Length	L	PCB (Board) Mount	97.55 / [3.84]	97.80 / [3.85]	98.05 / [3.86]	mm / [in]
Width	W		35.29 / [1.39]	35.54 / [1.40]	35.79 / [1.41]	mm / [in]
Height	H		9.019 / [0.355]	9.40 / [0.37]	9.781 / [0.385]	mm / [in]
Volume	Vol	Without heatsink		31.93 / [1.95]		cm^3/ [in^3]
Weight	W			130.4 / [4.6]		g / [oz]
Pin Material		C145 copper, 1/2 hard				
Underplate		Low stress ductile Nickel	50		100	µin
Pin Finish		Palladium	0.8		6	µin
		Soft Gold	0.12		2	
Thermal						
Operating junction temperature	$T_{INTERNAL}$	BCM3814x60E10A5yzz (T-Grade)	-40		125	°C
		BCM3814x60E10A5yzz (C-Grade)	-20		125	
Operating case temperature	T_{CASE}	BCM3814x60E10A5yzz (T-Grade), derating applied, see safe thermal operating area	-40		100	
		BCM3814x60E10A5yzz (C-Grade), derating applied, see safe thermal operating area	-20		100	
Thermal resistance top side	R_{JC_TOP}	Estimated thermal resistance to maximum temperature internal component from isothermal top		1.33		°C/W
Thermal Resistance Coupling between top case and bottom case	R_{HOU}	Estimated thermal resistance of thermal coupling between the top and bottom case surfaces		0.49		°C/W
Thermal resistance bottom side	R_{JC_BOT}	Estimated thermal resistance to maximum temperature internal component from isothermal bottom		0.71		°C/W
Thermal capacity				52		Ws/°C
Assembly						
Storage Temperature	T_{ST}	BCM3814x60E10A5yzz (T-Grade)	-40		125	°C
		BCM3814x60E10A5yzz (C-Grade)	-40		125	°C
ESD Withstand	ESD_{HBM}	Human Body Model, "ESDA / JEDEC JDS-001-2012" Class I-C (1kV to < 2 kV)	1000			
	ESD_{CDM}	Charge Device Model, "JESD 22-C101-E" Class II (200V to < 500V)	200			

General Characteristics (Cont.)

Specifications apply over all line, load conditions, unless otherwise noted; **Boldface** specifications apply over the temperature range of -40°C ≤ T^{CASE} ≤ 125°C (T-Grade); All other specifications are at T_{CASE} = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Safety						
Isolation capacitance	C_{HI_LO}	Unpowered unit	**620**	**780**	**940**	pF
Isolation resistance	R_{HI_LO}	At $500V_{DC}$	**10**			MΩ
MTBF		MIL-HDBK-217Plus Parts Count - 25°C Ground Benign, Stationary, Indoors / Computer		2.2		MHrs
		Telcordia Issue 2 - Method I Case III; 25°C Ground Benign, Controlled		3.6		MHrs
Agency approvals / standards						
		CE Marked for Low Voltage Directive and RoHS Recast Directive, as applicable				

BCM_EN_POLARITY Command (D0h)



The value of this register is set in nonvolatile memory and can only be written when the BCMs are disabled.

When PAGE COMMAND (00h) data byte is equal to (01h – 04h), this command defines the polarity of the EN pin. If BCM_EN_POLARITY is set, the BCM will startup once V_{HI} is greater than the under voltage threshold.

The BCM EN PIN is internally pulled-up to 3.3V. If the BCM_EN_POLARITY is cleared, an external pull-down is then required. Applying V_{HI} greater than the under voltage threshold will not suffice to start the BCM.

READ_K_FACTOR Command (D1h)

If PAGE data byte is equal to (01h - 04h) command will return a reported individual BCMs K factor in the following format:

$$K\_FACTOR_{ACTUAL} = K\_FACTOR_{REPORTED} \bullet 2^{-16} (V/V)$$

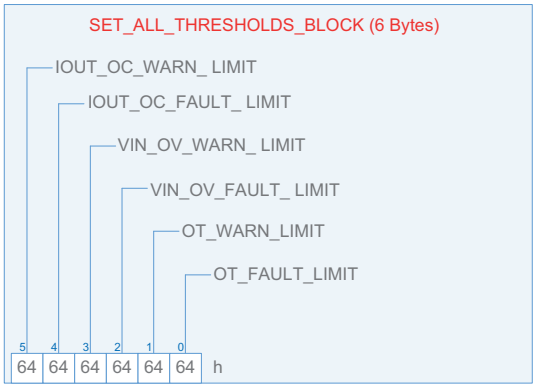
The K factor is defined in a BCM to represent the ratio of the transformer winding and hence is equal to V_{LO} / V_{HI}.

READ_BCM_ROUT Command (D4h)

If PAGE data byte is equal to (01h - 04h) command will return a reported individual BCM's LO side resistance in the following format:

$$BCM\_R_{LO\_ACTUAL} = BCM\_R_{LO\_REPORTED} \bullet 10^{-5} (\Omega)$$

SET_ALL_THRESHOLDS Command (D5h)



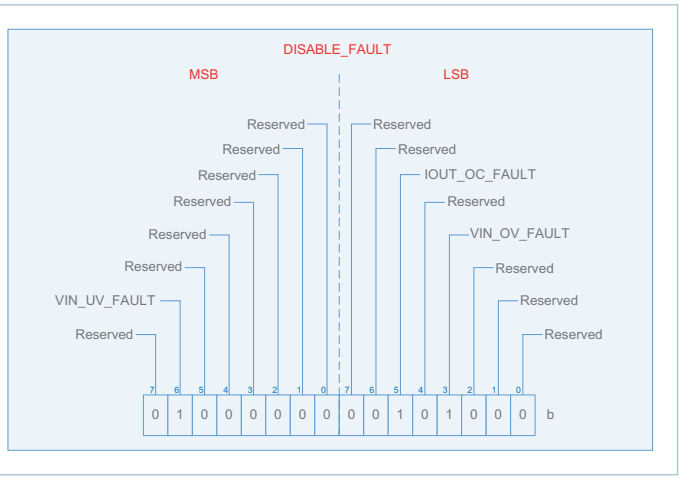
Values of this register block is set in nonvolatile memory and can only be written when the BCMs are disabled.

This command provides a convenient way to configure all the limits, or any combination of limits described previously using one command.

V_{HI} Overvoltage, Overcurrent and Overtemperature values are all set to 100% of the BCM datasheet supervisory limits by default and can only be set to a lower percentage.

To leave a particular threshold unchanged, set the corresponding threshold data byte to a value greater than (64h).

DISABLE_FAULT Command (D7h)



Unsupported bits are indicated above. A one indicates that the supervisory fault associated with the asserted bit is disabled.

The value of these registers is set in nonvolatile memory and can only be written when the BCMs are disabled.

This command allows the host to disable the supervisory faults and respective statuses. It does not disable the powertrain analog protections or warnings with respect to the set limits in the SET_ALL_THRESHOLDS Command.

The HI side undervoltage can only be disabled to a preset low limit as shown in the functional reporting range in the BCM data sheet.

The internal µC Implementation vs. PMBus™ Specification Rev 1.2

The internal µC is an I²C compliant, SMBus™ compatible device and PMBus command compliant device. This section denotes some deviation, perceived as differences from the PMBus Part I and Part II specification Rev 1.2.

1. The internal µC meets all Part I and II PMBus specification requirements with the following differences to the transport requirement.

Unmet DC parameter Implementation vs SMBus™ spec						
Symbol	Parameter	D44TL1A0		SMBus™ Rev 2.0		Units
		Min	Max	Min	Max	
V_{IL}[a]	Input Low Voltage	-	0.99	-	0.8	V
V_{IH}[a]	Input High Voltage	2.31	-	2.1	V_{VDD_IN}	V
I_{LEAK_PIN}[b]	Input Leakage per Pin	10	22	-	±5	µA

[a] V_{VDD_IN} = 3.3V
[b] V_{BUS} = 5V

2. The internal µC accepts 38 PMBus command codes. Implemented commands execute functions as described in the PMBus specification.

- Deviations from the PMBus specification:

  a. Section 15, fault related commands

  - The limits and Warnings unit implemented is percentage (%) a range from decimal (0-100) of the factory set limits.

3. The internal µC unsupported PMBus command code response as described in the Fault Management and Reporting:

- Deviations from the PMBus specification:

  a. PMBus section 10.2.5.3, exceptions

  - The busy bit of the STATUS_BYTE as implemented can be cleared (80h). In order to maintain compatibility with the specification (40h) can also be used.

- Manufacturer Implementation of the PMBus Spec

  a. PMBus section 10.5, setting the response to a detected fault condition

  - All powertrain responses are pre-set and cannot be changed. Refer to the BCM datasheet for details.

  b. PMBus section 10.6, reporting faults and warnings to the Host

  - SMBALERT# signal and Direct PMBus Device to Host Communication are not supported. However, the Digital Supervisor will set the corresponding fault status bits and will wait for the host to poll.

  c. PMBus section 10.7, clearing a shutdown due to a fault

  - There is no RESET pin or EN pin in the internal µC. Cycling power to the internal µC will not clear a BCM Shutdown. The BCM will clear itself once the fault condition is removed. Refer to the BCM datasheet for details.

  d. PMBus Section 10.8.1, corrupted data transmission faults:

  - Packet error checking is not supported.

Data Transmission Faults Implementation

This section describes data transmission faults as implemented in the internal µC.

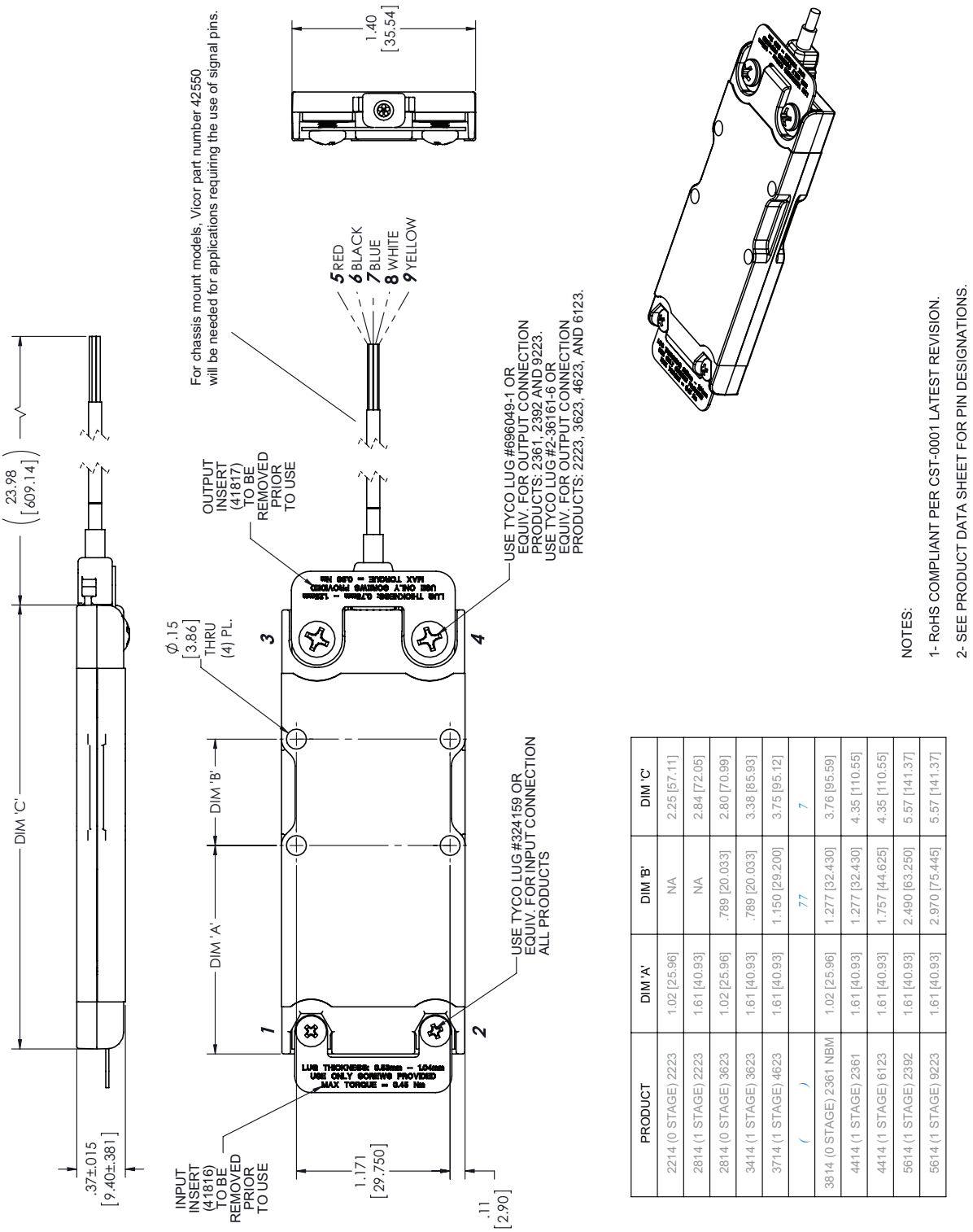
Section	Description	Response to Host		STATUS_BYTE	STATUS_CML		Notes
		NAK	FFh	CML	Other Fault	Unsupported Data	
10.8.1	Corrupted data						No response; PEC not supported
10.8.2	Sending too few bits			X	X		
10.8.3	Reading too few bits			X	X		
10.8.4	Host sends or reads too few bytes			X	X		
10.8.5	Host sends too many bytes	X		X		X	
10.8.6	Reading too many bytes		X	X	X		
10.8.7	Device busy	X	X				Device will ACK own address BUSY bit in STATUS_BYTE even if STATUS_WORD is set

Data Content Faults Implementation

This section describes data content fault as implemented in the internal µC.

Section	Description	Response to Host	STATUS_BYTE	STATUS_CML			Notes
		NAK	CML	Other Fault	Unsupported Command	Unsupported Data	
10.9.1	Improperly Set Read Bit In The Address Byte	X	X	X			
10.9.2	Unsupported Command Code	X	X		X		
10.9.3	Invalid or Unsupported Data		X			X	
10.9.4	Data Out of Range		X			X	
10.9.5	Reserved Bits						No response; not a fault

BCM in VIA Package Chassis (Lug) Mount Package Mechanical Drawing



PRODUCT	DIM 'A'	DIM 'B'	DIM 'C'
2214 (0 STAGE) 2223	1.02 [25.96]	NA	2.25 [57.11]
2814 (1 STAGE) 2223	1.61 [40.93]	NA	2.84 [72.05]
2814 (0 STAGE) 3623	1.02 [25.96]	.789 [20.033]	2.80 [70.99]
3414 (1 STAGE) 3623	1.61 [40.93]	.789 [20.033]	3.38 [85.93]
3714 (1 STAGE) 4623	1.61 [40.93]	1.150 [29.200]	3.75 [95.12]
( )	)	77	7
3814 (0 STAGE) 2361 NBM	1.02 [25.96]	1.277 [32.430]	3.76 [95.59]
4414 (1 STAGE) 2361	1.61 [40.93]	1.277 [32.430]	4.35 [110.55]
4414 (1 STAGE) 6123	1.61 [40.93]	1.757 [44.625]	4.35 [110.55]
5614 (1 STAGE) 2392	1.61 [40.93]	2.490 [63.250]	5.57 [141.37]
5614 (1 STAGE) 9223	1.61 [40.93]	2.970 [75.445]	5.57 [141.37]

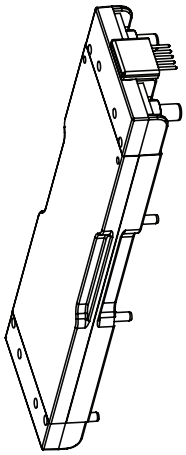
NOTES:

1- RoHS COMPLIANT PER CST-0001 LATEST REVISION.

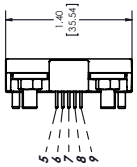
2- SEE PRODUCT DATA SHEET FOR PIN DESIGNATIONS.

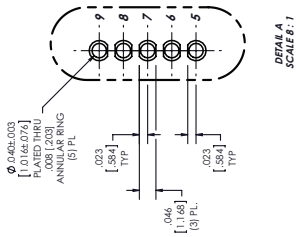
BCM in VIA Package PCB (Board) Mount Package Mechanical Drawing and Recommended Hole Pattern

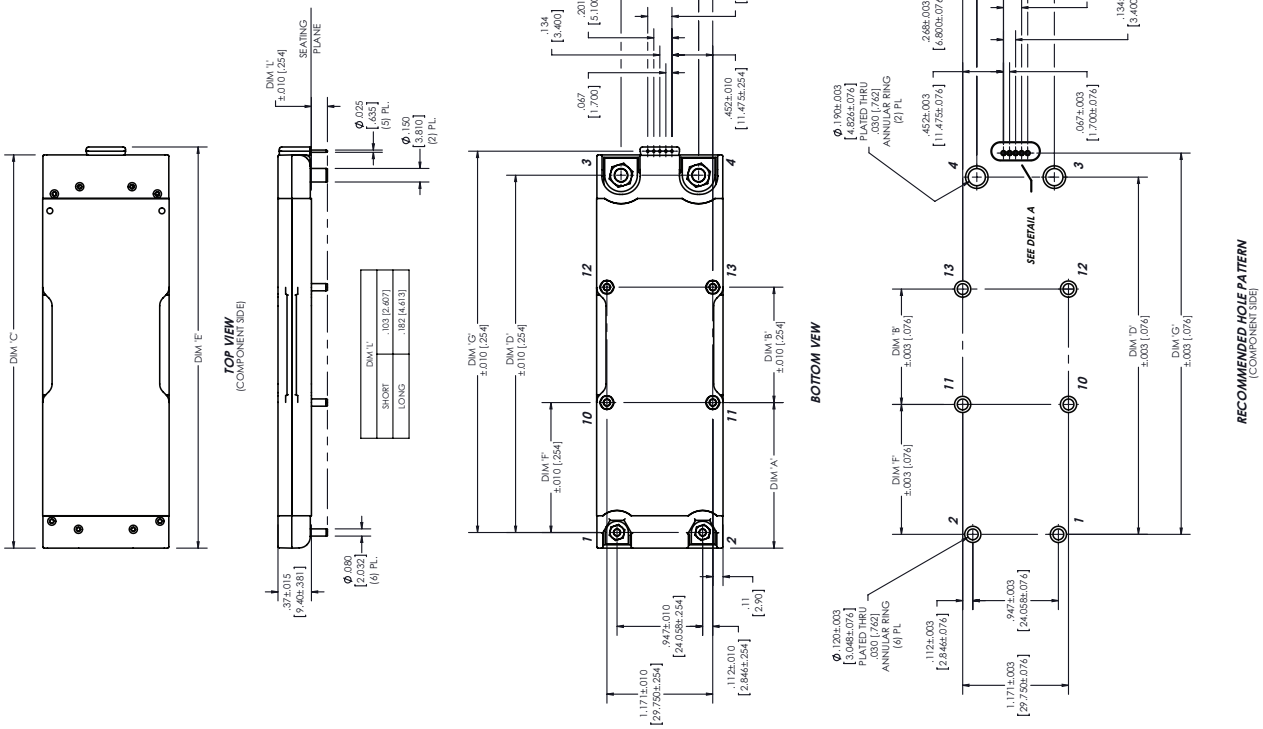
PRODUCT	DIM 'A'	DIM 'B'	DIM 'C'	DIM 'D'	DIM 'E'	DIM 'F'	DIM 'G'
( )		7,7	7		7		
3814 (0 STAGE) 2361 NBM	1.02 [25.96]	1.277 [32.430]	3.76 [95.59]	3.368 [85.554]	3.85 [97.780]	.850 [21.590]	3.632 [92.243]
4414 (1 STAGE) 2361	1.61 [40.93]	1.277 [32.430]	4.36 [110.55]	3.957 [100.517]	4.44 [112.76]	1.439 [36.553]	4.221 [107.206]
5614 (1 STAGE) 2392	1.61 [40.93]	2.490 [63.250]	5.57 [141.37]	5.171 [131.337]	5.65 [143.58]	1.439 [36.553]	5.434 [138.026]



NOTES:
1- RoHS COMPLIANT PER CST-0001 LATEST REVISION.
2- SEE PRODUCT DATA SHEET FOR PIN DESIGNATIONS.







Revision History

Revision	Date	Description	Page Number(s)
1.0	03/3/16	Initial release	n/a
1.1	05/2/16	New Power Pin Nomenclature	All

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