

Integrated Device Technology, Inc.

# HIGH-PERFORMANCE CMOS BUFFERS

**IDT54/74FCT827A**  
**IDT54/74FCT827B**  
**IDT54/74FCT827C**

## FEATURES:

- Faster than AMD's Am29827 series
- Equivalent to AMD's Am29827 bipolar buffers in pinout/function, speed and output drive over full temperature and voltage supply extremes
- IDT54/74FCT827A equivalent to FAST™
- **IDT54/74FCT827B 35% faster than FAST**
- **IDT54/74FCT827C 45% faster than FAST**
- IOL = 48mA (commercial), and 32mA (military)
- Clamp diodes on all inputs for ringing suppression
- CMOS power levels (1mW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Substantially lower input current levels than AMD's bipolar Am29800 series (5µA max.)
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

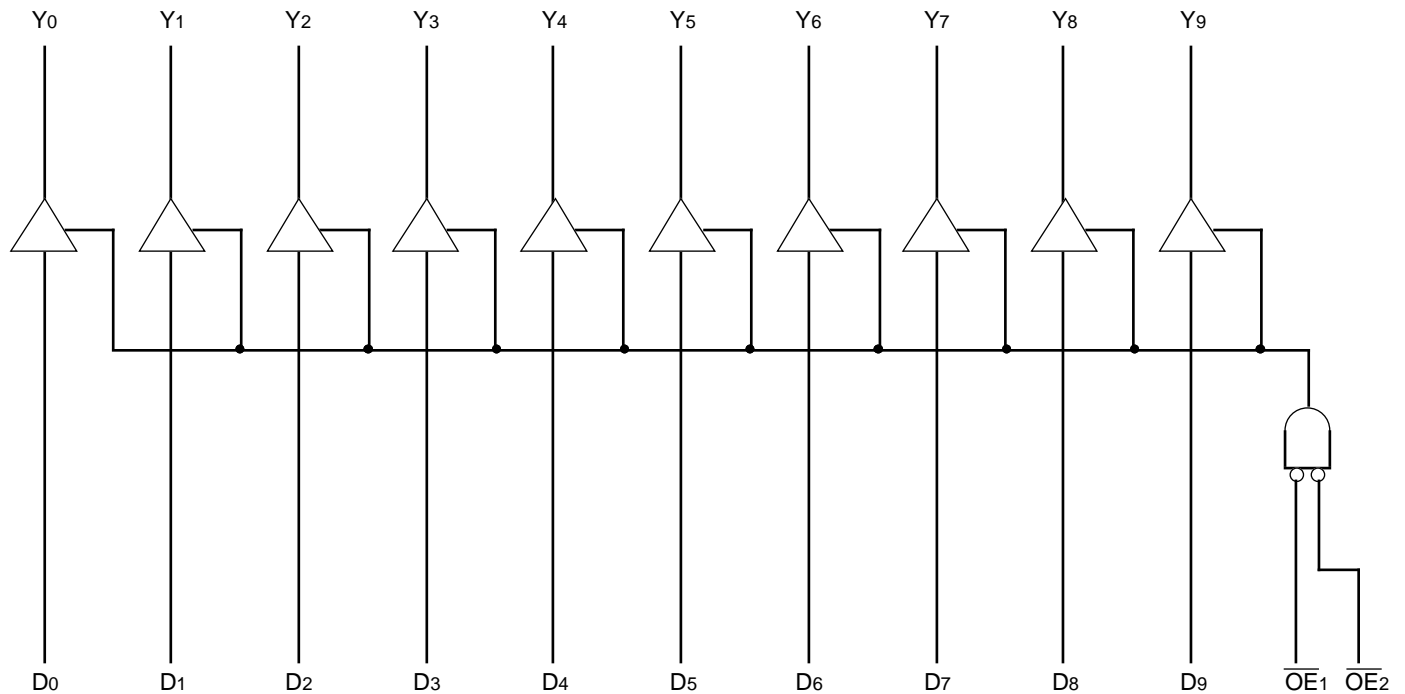
## DESCRIPTION:

The IDT54/74FCT800 series is built using an advanced dual metal CMOS technology.

The IDT54/74FCT827A/B/C 10-bit bus drivers provide high-performance bus interface buffering for wide data/address paths or buses carrying parity. The 10-bit buffers have NAND-ed output enables for maximum control flexibility.

All of the IDT54/74FCT800 high-performance interface family are designed for high-capacitance load drive capability, while providing low-capacitance bus loading at both inputs and outputs. All inputs have clamp diodes and all outputs are designed for low-capacitance bus loading in high-impedance state.

## FUNCTIONAL BLOCK DIAGRAM



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## PRODUCT SELECTOR GUIDE

	<b>10-Bit Buffer</b>
Non-inverting	IDT54/74FCT827A/B/C

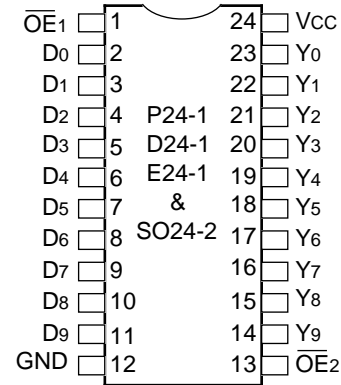
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FAST is a trademark of National Semiconductor Co.

## MILITARY AND COMMERCIAL TEMPERATURE RANGES

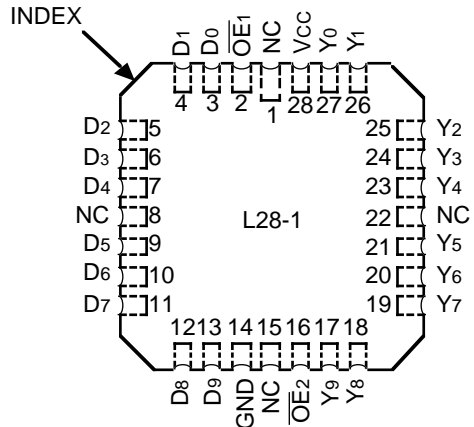
**MAY 1992**

**PIN CONFIGURATIONS**



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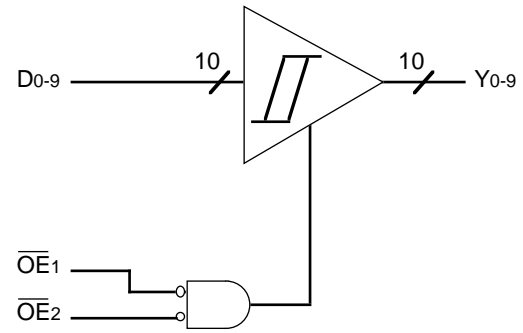
**DIP/CERPACK/SOIC  
TOP VIEW**



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**LCC  
TOP VIEW**

**LOGIC SYMBOL**



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**PIN DESCRIPTION**

Name	I/O	Description
$\overline{OE}_i$	I	When both are LOW, the outputs are enabled. When either one or both are HIGH, the outputs are High Z.
$D_i$	I	10-bit data input.
$Y_i$	O	10-bit data output.

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**FUNCTION TABLE<sup>(1)</sup>**

Inputs			Output	Function
$\overline{OE}_1$	$\overline{OE}_2$	$D_i$	$Y_i$	
L	L	L	L	Transparent
L	L	H	H	
H	X	X	Z	Three-State
X	H	X	Z	

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**NOTE:**  
1. H = HIGH, L = LOW, X = Don't Care, Z = High Impedance

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

Symbol	Rating	Commercial	Military	Unit
$V_{TERM}^{(2)}$	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
$V_{TERM}^{(3)}$	Terminal Voltage with Respect to GND	-0.5 to VCC	-0.5 to VCC	V
$T_A$	Operating Temperature	0 to +70	-55 to +125	°C
$T_{BIAS}$	Temperature Under Bias	-55 to +125	-65 to +135	°C
$T_{STG}$	Storage Temperature	-55 to +125	-65 to +150	°C
$P_T$	Power Dissipation	0.5	0.5	W
$I_{OUT}$	DC Output Current	120	120	mA

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- NOTES:**
- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
  - Input and VCC terminals only.
  - Outputs and I/O terminals only.

**CAPACITANCE** ( $T_A = +25^\circ\text{C}$ ,  $f = 1.0\text{MHz}$ )

Symbol	Parameter <sup>(1)</sup>	Conditions	Typ.	Max.	Unit
$C_{IN}$	Input Capacitance	$V_{IN} = 0V$	6	10	pF
$C_{OUT}$	Output Capacitance	$V_{OUT} = 0V$	8	12	pF

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**NOTE:**  
1. This parameter is measured at characterization but not tested.

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:  $V_{LC} = 0.2V$ ;  $V_{HC} = V_{CC} - 0.2V$

Commercial:  $T_A = 0^\circ C$  to  $+70^\circ C$ ,  $V_{CC} = 5.0V \pm 5\%$ ; Military:  $T_A = -55^\circ C$  to  $+125^\circ C$ ,  $V_{CC} = 5.0V \pm 10\%$

Symbol	Parameter	Test Conditions <sup>(1)</sup>	Min.	Typ. <sup>(2)</sup>	Max.	Unit	
$V_{IH}$	Input HIGH Level	Guaranteed Logic HIGH Level	2.0	—	—	V	
$V_{IL}$	Input LOW Level	Guaranteed Logic LOW Level	—	—	0.8	V	
$I_{IH}$	Input HIGH Current	$V_{CC} = \text{Max.}$	$V_I = V_{CC}$	—	—	5	$\mu A$
			$V_I = 2.7V$	—	—	5 <sup>(4)</sup>	
$I_{IL}$	Input LOW Current		$V_I = 0.5V$	—	—	-5 <sup>(4)</sup>	
		$V_I = GND$	—	—	-5		
$I_{OZH}$	Off State (High Impedance) Output Current	$V_{CC} = \text{Max.}$	$V_O = V_{CC}$	—	—	10	$\mu A$
			$V_O = 2.7V$	—	—	10 <sup>(4)</sup>	
$I_{OZL}$			$V_O = 0.5V$	—	—	-10 <sup>(4)</sup>	
			$V_O = GND$	—	—	-10	
$V_{IK}$	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_N = -18mA$	—	-0.7	-1.2	V	
$I_{OS}$	Short Circuit Current	$V_{CC} = \text{Max.}^{(3)}, V_O = GND$	-75	-120	—	mA	
$V_{OH}$	Output HIGH Voltage	$V_{CC} = 3V, V_{IN} = V_{LC} \text{ or } V_{HC}, I_{OH} = -32\mu A$	$V_{HC}$	$V_{CC}$	—	V	
		$V_{CC} = \text{Min.}$	$I_{OH} = -300\mu A$	$V_{HC}$	$V_{CC}$		—
		$V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -15mA \text{ MIL.}$	2.4	4.3		—
			$I_{OH} = -24mA \text{ COM'L.}$	2.4	4.3		—
$V_{OL}$	Output LOW Voltage	$V_{CC} = 3V, V_{IN} = V_{LC} \text{ or } V_{HC}, I_{OL} = 300\mu A$	—	GND	$V_{LC}$	V	
		$V_{CC} = \text{Min.}$	$I_{OL} = 300\mu A$	—	GND		$V_{LC}^{(4)}$
		$V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 32mA \text{ MIL.}$	—	0.3		0.5
			$I_{OL} = 48mA \text{ COM'L.}$	—	0.3		0.5

**NOTES:**

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1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at  $V_{CC} = 5.0V$ ,  $+25^\circ C$  ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

**POWER SUPPLY CHARACTERISTICS**  $V_{LC} = 0.2V$ ;  $V_{HC} = V_{CC} - 0.2V$

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Typ. <sup>(2)</sup>	Max.	Unit
I <sub>CC</sub>	Quiescent Power Supply Current	V <sub>CC</sub> = Max. V <sub>IN</sub> ≥ V <sub>HC</sub> ; V <sub>IN</sub> ≤ V <sub>LC</sub>		—	0.2	1.5	mA
ΔI <sub>CC</sub>	Quiescent Power Supply Current TTL Inputs HIGH	V <sub>CC</sub> = Max. V <sub>IN</sub> = 3.4V <sup>(3)</sup>		—	0.5	2.0	mA
I <sub>CCD</sub>	Dynamic Power Supply Current <sup>(4)</sup>	V <sub>CC</sub> = Max. Outputs Open $\overline{OE}_1 = \overline{OE}_2 = GND$ One Input Toggling 50% Duty Cycle	V <sub>IN</sub> ≥ V <sub>HC</sub> V <sub>IN</sub> ≤ V <sub>LC</sub>	—	0.15	0.25	mA/ MHz
I <sub>C</sub>	Total Power Supply Current <sup>(6)</sup>	V <sub>CC</sub> = Max. Outputs Open f <sub>i</sub> = 10MHz 50% Duty Cycle $\overline{OE}_1 = \overline{OE}_2 = GND$ One Bit Toggling	V <sub>IN</sub> ≥ V <sub>HC</sub> V <sub>IN</sub> ≤ V <sub>LC</sub> (FCT)	—	1.7	4.0	mA
			V <sub>IN</sub> = 3.4V V <sub>IN</sub> = GND	—	2.0	5.0	
		V <sub>CC</sub> = Max. Outputs Open f <sub>i</sub> = 2.5MHz 50% Duty Cycle $\overline{OE}_1 = \overline{OE}_2 = GND$ Eight Bits Toggling	V <sub>IN</sub> ≥ V <sub>HC</sub> V <sub>IN</sub> ≤ V <sub>LC</sub> (FCT)	—	3.2	6.5 <sup>(5)</sup>	
			V <sub>IN</sub> = 3.4V V <sub>IN</sub> = GND	—	5.2	14.5 <sup>(5)</sup>	

**NOTES:**

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- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V<sub>CC</sub> = 5.0V, +25°C ambient.
- Per TTL driven input (V<sub>IN</sub> = 3.4V); all other inputs at V<sub>CC</sub> or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
- Values for these conditions are examples of the I<sub>CC</sub> formula. These limits are guaranteed but not tested.
- I<sub>C</sub> = I<sub>QUIESCENT</sub> + I<sub>INPUTS</sub> + I<sub>DYNAMIC</sub>  
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$   
 I<sub>CC</sub> = Quiescent Current  
 ΔI<sub>CC</sub> = Power Supply Current for a TTL High Input (V<sub>IN</sub> = 3.4V)  
 D<sub>H</sub> = Duty Cycle for TTL Inputs High  
 N<sub>T</sub> = Number of TTL Inputs at D<sub>H</sub>  
 I<sub>CCD</sub> = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)  
 f<sub>CP</sub> = Clock Frequency for Register Devices (Zero for Non-Register Devices)  
 f<sub>i</sub> = Input Frequency  
 N<sub>i</sub> = Number of Inputs at f<sub>i</sub>  
 All currents are in milliamps and all frequencies are in megahertz.

**SWITCHING CHARACTERISTICS OVER OPERATING RANGE**

Parameter	Description	Conditions <sup>(1)</sup>	IDT54/74FCT827A				IDT54/74FCT827B				IDT54/74FCT827C				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay D <sub>I</sub> to Y <sub>I</sub>	CL = 50pF RL = 500Ω	1.5	8.0	1.5	9.0	1.5	5.0	1.5	6.5	1.5	4.4	1.5	5.0	ns
		CL = 300pF <sup>(3)</sup> RL = 500Ω	1.5	15.0	1.5	17.0	1.5	13.0	1.5	14.0	1.5	10.0	1.5	11.0	
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time O <sub>Ei</sub> to Y <sub>I</sub>	CL = 50pF RL = 500Ω	1.5	12.0	1.5	13.0	1.5	8.0	1.5	9.0	1.5	7.0	1.5	8.0	ns
		CL = 300pF <sup>(3)</sup> RL = 500Ω	1.5	23.0	1.5	25.0	1.5	15.0	1.5	16.0	1.5	14.0	1.5	15.0	
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time O <sub>Ei</sub> to Y <sub>I</sub>	CL = 5pF <sup>(3)</sup> RL = 500Ω	1.5	9.0	1.5	9.0	1.5	6.0	1.5	7.0	1.5	5.7	1.5	6.7	ns
		CL = 50pF RL = 500Ω	1.5	10.0	1.5	10.0	1.5	7.0	1.5	8.0	1.5	6.0	1.5	7.0	

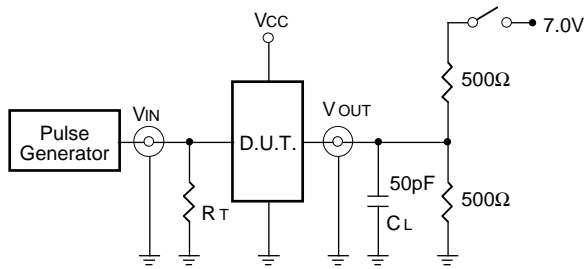
**NOTES:**

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. These parameters are guaranteed but not tested.

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## TEST CIRCUITS AND WAVEFORMS

### TEST CIRCUITS FOR ALL OUTPUTS



### SWITCH POSITION

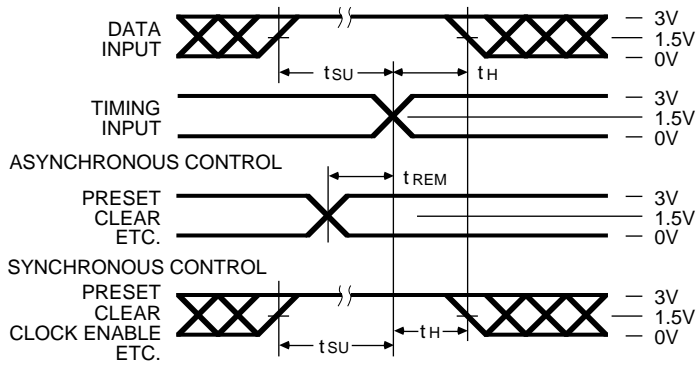
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

#### DEFINITIONS:

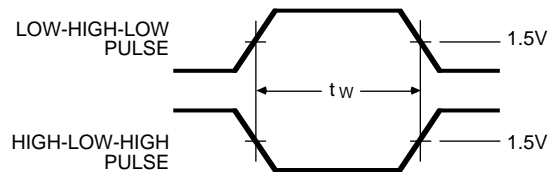
CL = Load capacitance: includes jig and probe capacitance.  
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

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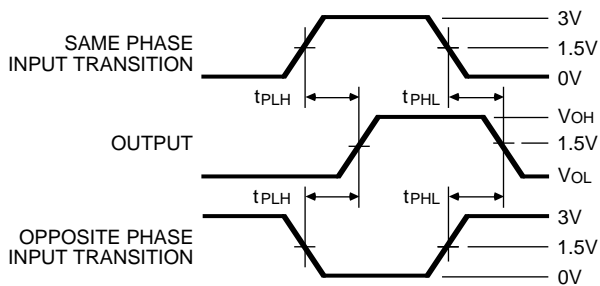
### SET-UP, HOLD AND RELEASE TIMES



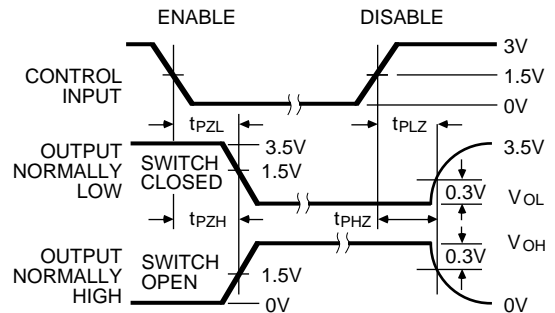
### PULSE WIDTH



### PROPAGATION DELAY



### ENABLE AND DISABLE TIMES

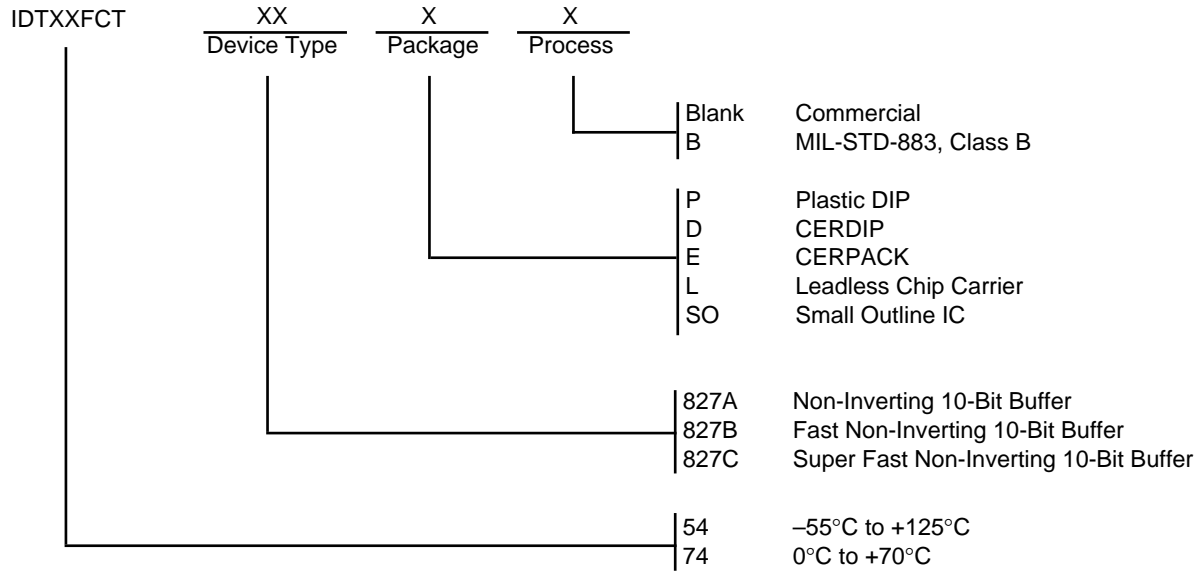


#### NOTES

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
- Pulse Generator for All Pulses: Rate  $\leq 1.0$  MHz;  $Z_o \leq 50\Omega$ ;  $t_f \leq 2.5$ ns;  $t_r \leq 2.5$ ns.

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## ORDERING INFORMATION



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