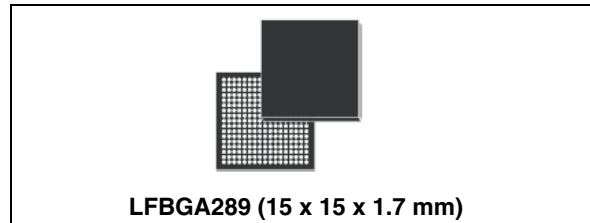


## Embedded MPU with ARM926 core for industrial and consumer applications

Datasheet – production data

### Features

- ARM926EJ-S CPU core, up to 333 MHz
- Multilayer bus matrix, up to 166 MHz
- Internal memories: 32 KB ROM, 8 KB SRAM
- Memory interfaces:
  - DDR controller (DDR2-666, LPDDR-333), 8-/16-bit
  - Serial NOR Flash controller
  - Parallel NAND Flash controller, 8-/16-bit data bus
  - Parallel NOR Flash/FPGA interface, 8-/16-bit data bus
- Connectivity:
  - 2 x USB 2.0 Host ports (integrated PHY)
  - 1 x USB 2.0 Device port (integrated PHY)
  - 2 x Fast Ethernet ports (external MII/RMII PHY)
  - 1 x MMC-SD card/SDIO controller
  - 2 x CAN 2.0 ports
  - 7 x UART ports
  - 3 x I2C ports: master/slave
  - 3 x synchronous serial ports, SPI/Microwire/TI protocols, master/slave
  - 1 x RS485 interface
  - 1 x fast IrDA interface
  - 1 x legacy parallel port (IEEE 1284), slave mode
  - 10-bit ADC, 8 channels, 1 Msps
  - Up to 102 GPIOs with interrupt capability
- HMI support:
  - LCD display controller, up to XGA (1024 x 768, 24 bpp)
  - Resistive touchscreen interface
  - JPEG codec accelerator
  - 1 x I2S digital audio port
- Security
  - Cryptographic co-processor



- Miscellaneous functions:
  - System controller, vectored interrupt controller, watchdog, real-time clock
  - Dynamic power-saving features
  - 8-channel DMA controller
  - 6 x 16-bit general purpose timers with prescaler and 4 capture inputs
  - 4 x PWM generators
  - Debug and trace interfaces: JTAG/ETM

### Applications

The SPEAr320S embedded MPU is configurable for a range of industrial and consumer applications such as:

- Human machine interface (HMI) terminals
- Factory automation / PLCs
- Medical equipment
- Smart energy meters and gateways
- VoIP phones
- Small printers

The device is hardware-compliant to the support of both real-time (RTOS) and high-level (HLOS) operating systems, such as Linux and Windows Embedded Compact 7.

**Table 1. Device summary**

| Order code  | Temp range, °C | Package                           | Packing |
|-------------|----------------|-----------------------------------|---------|
| SPEAr320S-2 | -40 to 85      | LFBGA289 (15x15 mm, pitch 0.8 mm) | Tray    |

# Contents

|          |   |           |
|----------|---|-----------|
| <b>1</b> | <b>Description</b> .....                        | <b>9</b>  |
| <b>2</b> | <b>Device functions</b> .....                   | <b>11</b> |
| 2.1      | CPU subsystem .....                             | 11        |
| 2.2      | Internal memories (BootROM/SRAM) .....          | 11        |
| 2.3      | Multiport DDR controller (MPMC) .....           | 12        |
| 2.4      | Serial NOR Flash controller (SMI) .....         | 12        |
| 2.5      | Parallel NAND Flash controller (FSMC) .....     | 14        |
| 2.6      | External memory interface (EMI) .....           | 15        |
| 2.7      | USB 2.0 Host ports (UHC) .....                  | 15        |
| 2.8      | USB 2.0 Device port (UDC) .....                 | 16        |
| 2.9      | Fast Ethernet ports (MII/RMII) .....            | 16        |
| 2.9.1    | MII0 Ethernet controller .....                  | 16        |
| 2.9.2    | RMII0 and MII1/RMII1 Ethernet controllers ..... | 17        |
| 2.10     | MMC-SD card/SDIO controller .....               | 17        |
| 2.11     | CAN 2.0 ports .....                             | 18        |
| 2.12     | Asynchronous serial ports (UART) .....          | 19        |
| 2.13     | I2C bus ports (I2C) .....                       | 20        |
| 2.14     | Synchronous serial ports (SSP) .....            | 20        |
| 2.15     | RS485 port (RS485) .....                        | 21        |
| 2.16     | Fast infrared port (IrDA) .....                 | 21        |
| 2.17     | Legacy IEEE 1284 parallel port (SPP) .....      | 21        |
| 2.18     | A/D converter (ADC) .....                       | 22        |
| 2.19     | General purpose I/Os (GPIO/XGPIO) .....         | 22        |
| 2.20     | LCD display controller (CLCD) .....             | 23        |
| 2.21     | Touchscreen interface (TOUCHSCREEN) .....       | 23        |
| 2.22     | JPEG codec accelerator (JPGC) .....             | 24        |
| 2.23     | Digital audio port (I2S) .....                  | 24        |
| 2.24     | Cryptographic co-processor (C3) .....           | 24        |
| 2.25     | System controller (SYSCTR) .....                | 25        |
| 2.25.1   | Reset and clock generator .....                 | 26        |

|          |   |           |
|----------|---|-----------|
| 2.26     | Vectored interrupt controller (VIC) .....                     | 26        |
| 2.27     | Watchdog timer (WDT) .....                                    | 27        |
| 2.28     | Real-time clock (RTC) .....                                   | 27        |
| 2.29     | DMA controller (DMAC) .....                                   | 27        |
| 2.30     | General purpose timers (GPT) .....                            | 28        |
| 2.31     | Pulse width modulators (PWM) .....                            | 28        |
| <b>3</b> | <b>Pin description .....</b>                                  | <b>29</b> |
| 3.1      | Pin/ball map .....  | 30        |
| 3.2      | Required external components .....                            | 31        |
| 3.3      | Dedicated pins description .....                              | 31        |
| 3.3.1    | Clock, reset and 3V3 comparator pins .....                    | 31        |
| 3.3.2    | Power supply pins .....                                       | 32        |
| 3.3.3    | Debug pins .....  | 33        |
| 3.3.4    | Non-multiplexed pins .....                                    | 33        |
| 3.4      | Shared IO pins (PL_GPIOs) .....                               | 37        |
| 3.4.1    | PL_GPIO / PL_CLK pins description .....                       | 37        |
| 3.4.2    | Extended mode: RMII automation networking mode .....          | 37        |
| 3.4.3    | Alternate functions .....                                     | 38        |
| 3.4.4    | Legacy configuration modes .....                              | 38        |
| 3.4.5    | Boot pins .....   | 41        |
| 3.4.6    | GPIOs .....   | 41        |
| 3.4.7    | Multiplexing scheme .....                                     | 42        |
| 3.4.8    | Multiplexed signals description .....                         | 49        |
| 3.5      | PL_GPIO and PL_CLK pin sharing for debug and test modes ..... | 66        |
| <b>4</b> | <b>Electrical characteristics .....</b>                       | <b>67</b> |
| 4.1      | Absolute maximum ratings .....                                | 67        |
| 4.2      | Maximum power consumption .....                               | 67        |
| 4.3      | Recommended operating conditions .....                        | 68        |
| 4.4      | Overshoot and undershoot .....                                | 68        |
| 4.5      | 3.3V I/O characteristics .....                                | 69        |
| 4.6      | Clocking parameters .....                                     | 70        |
| 4.6.1    | Master clock (MCLK) .....                                     | 70        |
| 4.6.2    | Real-time clock (RTC) .....                                   | 72        |

|          |   |           |
|----------|---|-----------|
| 4.7      | LPDDR and DDR2 pin characteristics            | 74        |
| 4.8      | ADC pin characteristics                       | 75        |
| 4.9      | Power-up sequence                             | 76        |
| 4.10     | Power-down sequence                           | 76        |
| 4.11     | Reset release                                 | 77        |
| <b>5</b> | <b>Timing requirements</b>                    | <b>78</b> |
| 5.1      | External interrupt timing characteristics     | 78        |
| 5.2      | Reset timing characteristics                  | 78        |
| 5.3      | CAN timing characteristics                    | 79        |
| 5.4      | CLCD timing characteristics                   | 80        |
| 5.5      | DDR2/LPDDR timing characteristics             | 81        |
| 5.5.1    | DDR2/LPDDR read cycle timing characteristics  | 81        |
| 5.5.2    | DDR2/LPDDR write cycle timing characteristics | 82        |
| 5.5.3    | DDR2/LPDDR command timing characteristics     | 82        |
| 5.6      | EMI timing characteristics                    | 83        |
| 5.7      | Ethernet MII timing characteristics           | 85        |
| 5.7.1    | MII transmit timing characteristics           | 85        |
| 5.7.2    | MII receive timing characteristics            | 86        |
| 5.7.3    | MDC/MDIO timing characteristics               | 86        |
| 5.8      | Ethernet RMII timing characteristics          | 87        |
| 5.8.1    | RMII transmit timing characteristics          | 87        |
| 5.8.2    | RMII receive timing characteristics           | 87        |
| 5.9      | FSMC timing characteristics                   | 89        |
| 5.10     | GPIO/XGPIO timing characteristics             | 91        |
| 5.11     | I <sup>2</sup> C timing characteristics       | 92        |
| 5.12     | I2S timing characteristics                    | 94        |
| 5.13     | PWM timing characteristics                    | 94        |
| 5.14     | SD timing characteristics                     | 96        |
| 5.15     | SMI timing characteristics                    | 97        |
| 5.16     | SSP timing characteristics                    | 98        |
| 5.16.1   | SPI master mode timings                       | 98        |
| 5.16.2   | SPI slave mode timings                        | 103       |
| 5.17     | SPP timing characteristics                    | 103       |

---

|                         |                                   |            |
|-------------------------|-----------------------------------|------------|
| 5.18                    | UART timing characteristics ..... | 103        |
| <b>6</b>                | <b>Package information .....</b>  | <b>106</b> |
| <b>Appendix A</b>       | <b>Acronyms .....</b>             | <b>108</b> |
| <b>Revision history</b> | <b>.....</b>                      | <b>111</b> |

## List of tables

|           |  |    |
|-----------|--|----|
| Table 1.  | Device summary . . . . .   | 1  |
| Table 2.  | NAND Flash devices supported by the BootROM firmware . . . . .                             | 14 |
| Table 3.  | SPEAr320S UART capabilities . . . . .  | 19 |
| Table 4.  | Pixel widths and formats available for different display types. . . . .                    | 23 |
| Table 5.  | Headers/abbreviations . . . . .  | 29 |
| Table 6.  | MCLK, RTC, Reset and 3.3 V comparator pins description . . . . .                           | 31 |
| Table 7.  | Power supply pins description . . . . .  | 32 |
| Table 8.  | Debug pins description . . . . .   | 33 |
| Table 9.  | SMI pins description . . . . .   | 33 |
| Table 10. | USB pins description . . . . .   | 34 |
| Table 11. | ADC pins description . . . . .   | 34 |
| Table 12. | DDR pins description . . . . .   | 35 |
| Table 13. | PL_GPIO / PL_CLK pins description . . . . .  | 37 |
| Table 14. | Boot pins description . . . . .  | 41 |
| Table 15. | PL_GPIO/PL_CLK multiplexing scheme and reset states . . . . .                              | 43 |
| Table 16. | Table shading reference for Table 15 multiplexing scheme . . . . .                         | 48 |
| Table 17. | FSMC signals description . . . . .   | 49 |
| Table 18. | EMI signals description . . . . .  | 50 |
| Table 19. | CLCD signals description . . . . .   | 52 |
| Table 20. | Touchscreen signal description . . . . .   | 53 |
| Table 21. | UART signals description . . . . .   | 53 |
| Table 22. | CAN signals description . . . . .  | 55 |
| Table 23. | MMC-SD/SDIO controller signals description . . . . .                                       | 56 |
| Table 24. | PWM signals description . . . . .  | 56 |
| Table 25. | GPT signals description . . . . .  | 57 |
| Table 26. | IrDA signals description . . . . .   | 57 |
| Table 27. | SSP signals description . . . . .  | 58 |
| Table 28. | I2C signals description . . . . .  | 60 |
| Table 29. | I2S signals description . . . . .  | 60 |
| Table 30. | SPP signals description . . . . .  | 61 |
| Table 31. | Ethernet signals description . . . . .   | 62 |
| Table 32. | Ball sharing during debug . . . . .  | 66 |
| Table 33. | Absolute maximum ratings . . . . .   | 67 |
| Table 34. | Maximum power consumption . . . . .  | 67 |
| Table 35. | Recommended operating conditions . . . . .   | 68 |
| Table 36. | Overshoot and undershoot specifications. . . . .   | 68 |
| Table 37. | Low voltage TTL DC input specification ( $3\text{ V} < V_{DD} < 3.6\text{ V}$ ) . . . . .  | 69 |
| Table 38. | Low voltage TTL DC output specification ( $3\text{ V} < V_{DD} < 3.6\text{ V}$ ) . . . . . | 69 |
| Table 39. | Pull-up and pull-down characteristics . . . . .  | 69 |
| Table 40. | MCLK oscillator characteristics. . . . .   | 70 |
| Table 41. | MCLK external user clock source characteristics . . . . .                                  | 71 |
| Table 42. | RTC oscillator characteristics . . . . .   | 72 |
| Table 43. | RTC external user clock source characteristics . . . . .                                   | 73 |
| Table 44. | DC characteristics . . . . .   | 74 |
| Table 45. | Driver characteristics . . . . .   | 74 |
| Table 46. | On-die termination . . . . .   | 74 |
| Table 47. | Reference voltage . . . . .  | 74 |
| Table 48. | ADC pin characteristics . . . . .  | 75 |

|           |  |     |
|-----------|--|-----|
| Table 49. | PL_GPIO external interrupt input timing . . . . .                              | 78  |
| Table 50. | Reset timing characteristics . . . . .   | 78  |
| Table 51. | CAN timing characteristics . . . . .   | 79  |
| Table 52. | CLCD timing requirements . . . . .   | 80  |
| Table 53. | DDR2/LPDDR read cycle timing requirements . . . . .                            | 81  |
| Table 54. | DDR2/LPDDR write cycle timing requirements . . . . .                           | 82  |
| Table 55. | DDR2/LPDDR command timing requirements . . . . .                               | 82  |
| Table 56. | EMI timing requirements for read cycle with acknowledgement on WAIT . . . . .  | 83  |
| Table 57. | EMI timing requirements for write cycle with acknowledgement on WAIT . . . . . | 84  |
| Table 58. | EMI signals timing requirements . . . . .                                      | 85  |
| Table 59. | MII TX timing requirements . . . . .   | 85  |
| Table 60. | MII RX timing requirements . . . . .   | 86  |
| Table 61. | MDC timing requirements . . . . .  | 86  |
| Table 62. | RMII TX timing requirements . . . . .  | 87  |
| Table 63. | RMII RX timing requirements . . . . .  | 88  |
| Table 64. | FSMC timing requirements . . . . .   | 90  |
| Table 65. | FSMC signals timing requirements . . . . .                                     | 90  |
| Table 66. | I <sup>2</sup> C timing requirements in high-speed mode . . . . .              | 93  |
| Table 67. | I <sup>2</sup> C timing requirements in fast-speed mode . . . . .              | 93  |
| Table 68. | I <sup>2</sup> C timing requirements in standard-speed mode . . . . .          | 93  |
| Table 69. | I2S timing requirements . . . . .  | 94  |
| Table 70. | PWM timing characteristics . . . . .   | 95  |
| Table 71. | SD timing requirements (high-speed mode, 48 MHz) . . . . .                     | 96  |
| Table 72. | SD timing requirements (full-speed mode, 24 MHz) . . . . .                     | 96  |
| Table 73. | SMI timing requirements . . . . .  | 97  |
| Table 74. | SPI master mode timing characteristics (SPH = 0, SPO=0) . . . . .              | 99  |
| Table 75. | SPI master mode timing characteristics (SPH = 0, SPO=1) . . . . .              | 100 |
| Table 76. | SPI master mode timing characteristics (SPH = 1, SPO=0) . . . . .              | 101 |
| Table 77. | SPI master mode timing characteristics (SPH = 1, SPO=1) . . . . .              | 102 |
| Table 78. | SSP timing characteristics (slave mode) . . . . .                              | 103 |
| Table 79. | UART transmit timing characteristics . . . . .                                 | 104 |
| Table 80. | UART receive timing characteristics . . . . .                                  | 104 |
| Table 81. | RS485_OE transmit and receive timing characteristics . . . . .                 | 105 |
| Table 82. | LFBGA289 (15 x 15 x 1.7 mm) mechanical data . . . . .                          | 106 |
| Table 83. | LFBGA289 package thermal characteristics . . . . .                             | 107 |
| Table 84. | List of acronyms . . . . .   | 108 |
| Table 85. | Document revision history . . . . .  | 111 |

## List of figures

|            |  |     |
|------------|--|-----|
| Figure 1.  | SPEAr320S architectural block diagram.....                         | 10  |
| Figure 2.  | SPEAr320S pin/ball map .....                                       | 30  |
| Figure 3.  | Hierarchical multiplexing scheme .....                             | 42  |
| Figure 4.  | MCLK crystal connection .....                                      | 70  |
| Figure 5.  | RTC crystal connection.....  | 72  |
| Figure 6.  | Power-up sequence .....  | 76  |
| Figure 7.  | Cold reset release .....   | 77  |
| Figure 8.  | Warm reset release .....   | 77  |
| Figure 9.  | CLCD waveform .....  | 80  |
| Figure 10. | DDR2/LPDDR read cycle waveform .....                               | 81  |
| Figure 11. | DDR2/LPDDR write cycle waveform.....                               | 82  |
| Figure 12. | DDR2/LPDDR command waveform .....                                  | 82  |
| Figure 13. | EMI read cycle waveform with acknowledgement on EMI_WAIT.....      | 83  |
| Figure 14. | EMI write cycle waveform with acknowledgement on EMI_WAIT .....    | 83  |
| Figure 15. | EMI read cycle waveform without acknowledgement on EMI_WAIT .....  | 84  |
| Figure 16. | EMI write cycle waveform without acknowledgement on EMI_WAIT ..... | 84  |
| Figure 17. | MII TX waveform.....   | 85  |
| Figure 18. | MII RX waveform .....  | 86  |
| Figure 19. | MDC waveform .....   | 86  |
| Figure 20. | RMII TX waveform .....   | 87  |
| Figure 21. | RMII RX waveform .....   | 87  |
| Figure 22. | Output command signal waveform .....                               | 89  |
| Figure 23. | Output address signal waveform .....                               | 89  |
| Figure 24. | In/out data address signal waveform .....                          | 89  |
| Figure 25. | Output signal waveform for I <sup>2</sup> C signals .....          | 92  |
| Figure 26. | RC delay circuit.....  | 93  |
| Figure 27. | I2S waveform .....   | 94  |
| Figure 28. | PWM timing waveforms .....   | 94  |
| Figure 29. | SD timing waveform .....   | 96  |
| Figure 30. | SMI input/output waveform.....                                     | 97  |
| Figure 31. | SSP_SCK waveform.....  | 98  |
| Figure 32. | SPI master mode external timing waveform (SPH= 0, SPO =0 ) .....   | 98  |
| Figure 33. | SPI master mode external timing waveform (SPH= 0, SPO =1 ) .....   | 100 |
| Figure 34. | SPI master mode external timing waveform (SPH = 1, SPO = 0).....   | 101 |
| Figure 35. | SPI master mode external timing waveform (SPH = 1, SPO = 1).....   | 102 |
| Figure 36. | SPP timing waveform .....  | 103 |
| Figure 37. | UART transmit and receive waveform .....                           | 103 |
| Figure 38. | RS485_OE transmit and receive waveform .....                       | 104 |
| Figure 39. | LFPGA289 package dimensions .....                                  | 107 |



# 1 Description

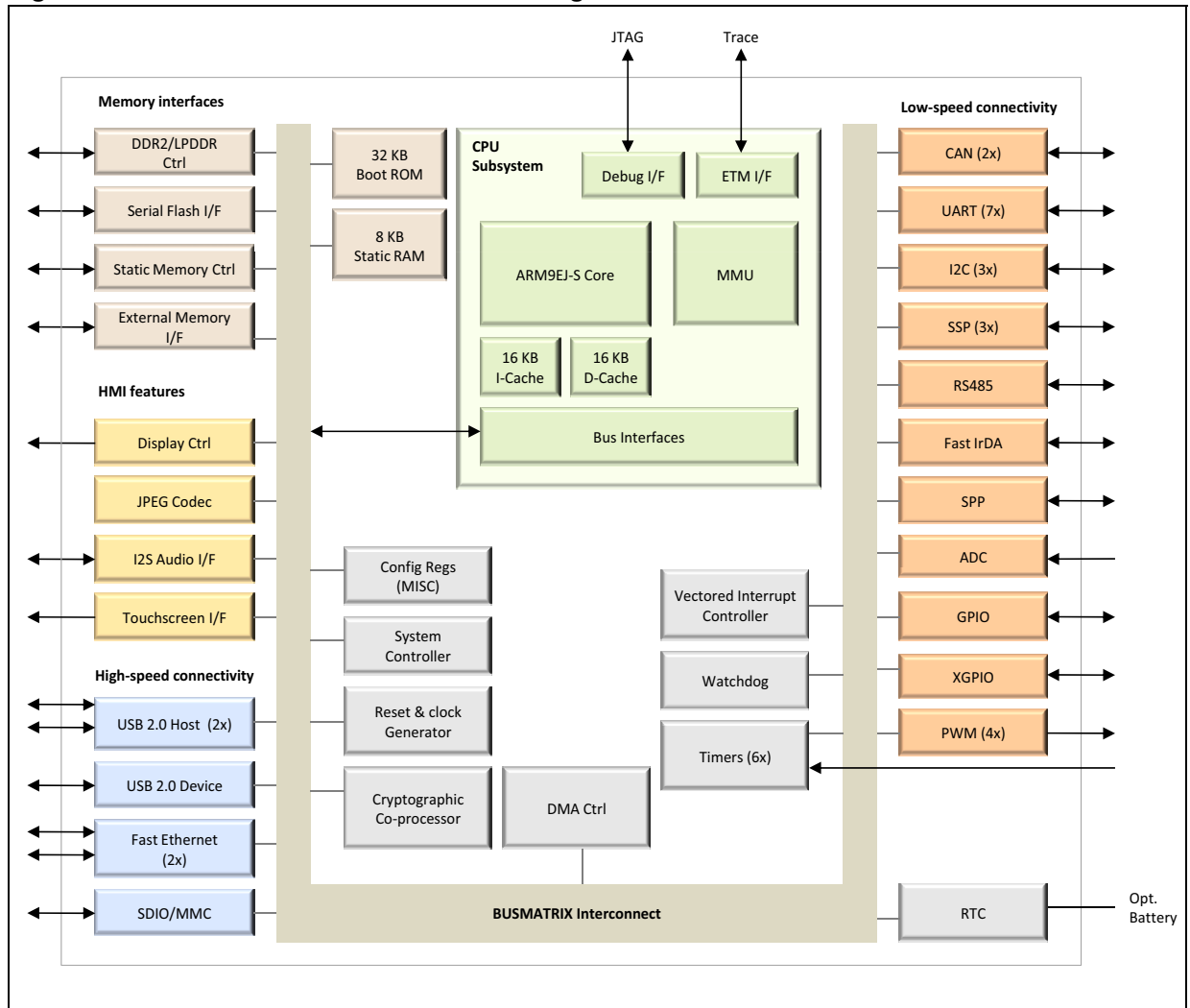
SPEAr320S is a member of the SPEAr family of embedded MPUs and is optimized for industrial automation and consumer markets. The device is based on the ARM926EJ-S processor (up to 333 MHz), widely used in applications where the processing performance is required to be higher than the one achievable with microcontrollers.

SPEAr320S provides an integrated MMU (memory management unit) which enables to support high-level operating systems (HLOS), such as Linux and Windows Embedded Compact 7. In addition, a rich set of integrated peripherals (memory interfaces, connectivity, HMI, cryptography) allows the device to be used in a wide range of embedded applications.

The SPEAr320S architecture is based on multiple functional blocks interacting through a multilayer interconnection bus matrix. The switch matrix structure allows different subsystem data flows to be executed in parallel improving the core platform efficiency. High performance master agents are directly interconnected with the memory controller reducing the memory access latency. The overall memory bandwidth assigned to each master port can be programmed and optimized through an internal efficient weighted round-robin arbitration mechanism.

The SPEAr320S device is fully backward-compatible with the previous SPEAr320 product at both hardware and software programming levels. The extended functionality is achieved by enhanced I/O multiplexing, preserving the same pinout and ball map, as well as by a new software-definable configuration mode.

Figure 1. SPEAr320S architectural block diagram



## 2 Device functions

### 2.1 CPU subsystem

The core of the SPEAr320S is an ARM926EJ-S reduced instruction set computer (RISC) processor.

**Main features:**

- Supports the 32-bit ARM and 16-bit Thumb instruction sets, enabling the user to trade off between high performance and high code density. It also includes features for efficient execution of Java byte codes.
- The ARM CPU can be clocked at a frequency up to 333 MHz and includes both an instruction (16 KB) and a data cache (16 KB). In addition to the capability of running any real-time operating system (RTOS) available for ARM9 processors, the ARM926EJ-S subsystem also provides a memory management unit (MMU) that enables to support high-level operating systems (HLOS) like Linux and Windows Embedded Compact 7.
- Includes an embedded trace module (ETM Medium+) for real-time CPU activity tracing and debugging. It supports 4-bit and 8-bit normal trace mode and 4-bit demultiplexed trace mode, with normal or half-rate clock.

For detailed information, please refer to the following public documents available from the ARM Ltd. website:

- *CPU Core:*  
ARM9EJ-S, Technical Reference Manual, Revision: r1p2  
<http://infocenter.arm.com/help/topic/com.arm.doc.ddi0222b/DDI0222.pdf>
- *CPU Subsystem:*  
ARM926EJ-S, Technical Reference Manual, Revision: r0p5  
[http://infocenter.arm.com/help/topic/com.arm.doc.ddi0198e/DDI0198E\\_arm926ejs\\_r0p5\\_tm.pdf](http://infocenter.arm.com/help/topic/com.arm.doc.ddi0198e/DDI0198E_arm926ejs_r0p5_tm.pdf)

### 2.2 Internal memories (BootROM/SRAM)

SPEAr320S integrates two embedded memories:

- 32 KB ROM (BootROM), storing a factory-defined device bootstrap firmware.
- 8 KB Static RAM (SRAM), partly used by bootstrap firmware, but also available as general-purpose memory after system startup.

The firmware in BootROM is automatically executed after SPEAr320S reset and supports the following bootstrap modes:

- Boot from serial NOR Flash
- Boot from parallel NAND Flash
- Boot from parallel NOR Flash
- Boot from USB Device port
- Boot from UART0
- Boot from Ethernet (MII0)

The BootROM firmware selects the boot mode from the boot pin settings (see [Section 3.4.5: Boot pins](#)). A setting is also available to allow the BootROM execution to be bypassed.

The first three modes support alternate ways of locating and starting the selected operating system or target custom software. Such modes require a second-level boot firmware to be stored in external Flash memory. A reference code for such boot loader (called “XLoader”) is provided by STMicroelectronics in source and binary formats for the SPEAr320S evaluation boards. Such code must be adapted according to the specific DDR memory components found on target customer systems.

The fourth mode can be used for installing and updating the software on external Flash memories through a PC-based software utility provided by STMicroelectronics exploiting a USB link between a PC and a target SPEAr320S board.

The sixth mode used the MII0 port and is based on two standard protocols: DHCP (to get an IP address over the network) and TFTP (for receiving xloader and u-boot binary images).

## 2.3 Multiport DDR controller (MPMC)

SPEAr320S integrates a high-performance controller able to manage DDR2 (double data rate) and LPDDR (low power DDR) external dynamic memory devices.

### Main features:

- Support for DDR2 up to 333 MHz (666 MT/sec)
- Support for LPDDR up to 166 MHz (333 MT/sec)
- Support for 8-/16-bit external data bus
- Support for up to 1 GByte DDR2/LPDDR memory address space
- Full initialization of memories on controller reset
- 6 independent internal ports: five of them are used to access the external memory while one is reserved for programming the controller configuration registers
- Programmable built-in port arbitration scheme to ensure high memory bandwidth utilization
- Fully pipelined read and write commands
- Self-refresh mode for power saving
- Integrated physical layer (PHY) and delay locked loops (DLLs) for fine tuning of the timing parameters, maximizing the data valid windows at different frequencies

## 2.4 Serial NOR Flash controller (SMI)

SPEAr320S integrates a Flash memory controller able to manage serial, SPI-compatible, NOR Flash and EEPROM external memory devices.

### Main features:

- Support for up to 32 MByte external serial memory storage capacity (2 x 16 MB addressable banks by independent chip select signals)
- SMI clock up to 50 MHz (fast read mode) or 20 MHz (normal mode), with software configurable 7-bit prescaler

The bootstrap requires that the external serial Flash is located at bank 0 (enabled after power-on reset). During the boot phase, a sequence of instructions is automatically sent to bank 0. Refer to the SPEAr320S reference manuals for more details.

The BootROM firmware has been tested with the following external serial memory components:

- Micron M25P and M45P families (SPI Flash)
- STMicroelectronics M95 family (SPI EEPROM), except for M95040, M95020 and M95010
- ATMEL AT25F family (SPI Flash)
- YMC Y25F family (SPI Flash)
- Microchip/SST SST25LF family (SPI Flash)

## 2.5 Parallel NAND Flash controller (FSMC)

SPEAr320S integrates a flexible static memory controller able to manage external parallel NAND Flash memories.

**Main features:**

- 8-/16-bit external data bus; 16-bit only supported when Mode 3 (expanded automation mode) chip configuration is selected by software.
- Support for up to 4 memory banks
- Independent timing configuration and chip select signal for each memory bank
- Fully programmable timings:
  - wait states (up to 31)
  - bus turnaround cycles (up to 15)
  - output enable and write enable delays (up to 15)
- External asynchronous wait control
- Internal AHB bus burst transfer support to reduce Flash memory access time

The BootROM firmware directly supports the external NAND Flash components shown in [Table 2](#).

**Table 2. NAND Flash devices supported by the BootROM firmware**

| Part number     | Vendor  | Density | Capacity | Bus width | Page size             |
|-----------------|---------|---------|----------|-----------|-----------------------|
| K9F1208V0A      | Samsung | 64 Mb   | 8 MB     | x8        | 512 + 16 bytes        |
| NAND128W3A28N6  | Micron  | 128 Mb  | 16 MB    | x8        | 512 + 16 bytes        |
| NAND256W3A2BN6  | Micron  | 256 Mb  | 32 MB    | x8        | 512 + 16 bytes        |
| KM29U256        | Samsung | 256 Mb  | 32 MB    | x8        | 512 + 16 bytes        |
| NAND512W3A2C2A6 | Micron  | 512 Mb  | 64 MB    | x8        | 512 + 16 bytes        |
| NAND01GW3B2BN6  | Micron  | 1 Gb    | 128 MB   | x8        | 2048 + 64 bytes       |
| NAND01GW4B2AN6  | Micron  | 1 Gb    | 128 MB   | x16       | 1024 words + 32 bytes |
| K9F1G16U0M      | Samsung | 1 Gb    | 128 MB   | x16       | 1024 words + 32 bytes |
| NAND01GR3B      | Micron  | 1 Gb    | 128 MB   | x8        | 2048 + 64 bytes       |
| NAND02GW3B2CN6  | Micron  | 2 Gb    | 256 MB   | x8        | 2048 + 64 bytes       |

**Table 2. NAND Flash devices supported by the BootROM firmware (continued)**

| Part number    | Vendor  | Density | Capacity | Bus width | Page size       |
|----------------|---------|---------|----------|-----------|-----------------|
| NAND02GW3A     | Micron  | 2 Gb    | 256 MB   | x8        | 2048 + 64 bytes |
| K9F2G08V0A     | Samsung | 2 Gb    | 256 MB   | x8        | 512 + 16 bytes  |
| NAND04GW3B2BN6 | Micron  | 4 Gb    | 512 MB   | x8        | 2048 + 64 bytes |
| K9F4G08V0A     | Samsung | 4 Gb    | 512 MB   | x8        | 512 + 16 bytes  |
| NAND08GW3B2CN6 | Micron  | 8 Gb    | 1 GB     | x8        | 2048 + 64 bytes |
| K9K8G08V0A     | Samsung | 8 Gb    | 1 GB     | x8        | 512 + 16 bytes  |
| K9F8G08V0M     | Samsung | 8 Gb    | 1 GB     | x8        | 512 + 16 bytes  |

## 2.6 External memory interface (EMI)

SPEAr320S integrates an additional external memory interface that can be used to manage external parallel NOR Flash memories as well as FPGA devices. This interface is available only when Mode 3 (expanded automation mode) chip configuration is selected by software.

### Main features:

- 24-bit address bus
- 16-bit data bus
- 4 chip select signals
- Support for single asynchronous transfers
- Support for peripherals using Byte Lane procedure

The external Flash component must be in read mode at reset. Usually, this is true for most parallel NOR devices.

## 2.7 USB 2.0 Host ports (UHC)

SPEAr320S provides two USB 2.0 Host ports with integrated PHYs.

### Main features:

- Each port can be independently configured for high-speed mode (USB 2.0, up to 480 Mbps); in this case, the corresponding controller is programmed according to standard EHCI specifications.
- Each port can be independently configured for full-speed mode (USB 1.1, up to 12 Mbps) or low-speed mode (USB 1.1, up to 1.5 Mbps); in this case, the corresponding controller is programmed according to standard OHCI specifications.
- Internal 2 KB FIFO queues
- Internal DMA support
- Dedicated output control signals to manage external power switches
- Dedicated input signals to sense any over-current condition detected by external power switches

## 2.8 USB 2.0 Device port (UDC)

SPEAr320S provides a USB 2.0 Device port with integrated PHY.

### Main features:

- Support for all standard modes:
  - high-speed mode (USB 2.0, up to 480 Mbps)
  - full-speed mode (USB 1.1, up to 12 Mbps)
  - low-speed mode (USB 1.1, up to 1.5 Mbps)
- Up to 16 physical endpoints, configurable as different logical endpoints
- Internal 4 KB FIFO queue (shared among all the endpoints)
- DMA mode, with descriptor-based structures in application memory
- Slave-only mode
- Support for 8-, 16- and 32-bit wide data transactions on the internal bus
- Support for USB plug detection (UPD)

## 2.9 Fast Ethernet ports (MII/RMII)

SPEAr320S features three multiplexed Ethernet MACs, supporting up to two ports concurrently.

The three controllers are named:

- MII0
- RMII0
- MII1/RMII1

### 2.9.1 MII0 Ethernet controller

#### Main features:

- Media independent interface (MII) to an external PHY as defined in the IEEE 802.3u specification
- Support for 10 and 100 Mbps data transfer rates
- Support for both full-duplex and half-duplex (CSMA/CD protocol) operating modes
- Integrated FIFO queues (4 KB RX, 2 KB TX)
- Native DMA with single-channel transmit and receive engines, providing 32-/64-/128-bit data transfers; DMA provides ring-buffer or linked-list descriptor options.
- Programmable Ethernet frame length to support both standard and jumbo frames (with size up to 16 KB)
- Flexible address filtering modes
- Statistics counter registers for RMON/MIB
- Support for 802.1Q VLAN tagging
- Wake-on-LAN support
- Automatic padding and CRC generation on transmitted frames



## 2.9.2 RMII0 and MII1/RMII1 Ethernet controllers

These functional blocks extend Ethernet capability by covering the Media independent interface (MII) and Reduced media independent interface (RMII) standards.

They can be used in two ways:

- as a single additional MAC controller with Media independent interface (MII1)
- as two MAC controllers with Reduced media independent interface (RMII0, RMII1)

In *RMII configuration*, each controller has an independent set of data and control lines. The reference clock (50 MHz) is shared by the controllers.

### Main features:

- Compatible with IEEE Standard 802.3
- UNH tested
- 10 and 100 Mbit/s operation
- Full and half duplex operation
- Statistics counter registers for RMON/MIB
- Automatic pad and CRC generation on transmitted frames
- Automatic discard of frames received with errors
- Address checking logic supports up to four specific 48-bit addresses
- Supports promiscuous mode where all valid received frames are copied to memory
- Hash matching of unicast and multicast destination addresses
- External address matching of received frames
- Supports serial network interface operation
- Half-duplex flow control by forcing collisions on incoming frames
- Full-duplex flow control with recognition of incoming pause frames and hardware generation of transmitted pause frames
- Support for 802.1Q VLAN tagging with recognition of incoming VLAN and priority tagged frames
- Multiple buffers per receive and transmit frame
- Jumbo frames of up to 10240 bytes supported

## 2.10 MMC-SD card/SDIO controller

The MMC-SD card /SDIO controller conforms to the SD Host Controller Standard Specification, version 2.0. It handles SD/SDIO protocol at transmission level by packing data, adding cyclic redundancy check (CRC) and start/end bit as well as checking for transaction format correctness.

The controller is designed to work with I/O cards, read-only cards and read/write cards, and can operate either in SD mode (1-bit, 4-bit, 8-bit) or in SPI mode.

The interface is compliant to the following standards:

- SD Host Controller Standard Specification, version 2.0
- SDIO Card Specification, version 2.0
- SD Memory Card Specification Draft, version 2.0
- SD Memory Card Security Specification, version 1.01
- MMC Specification, version 3.31 and 4.2

**Main features:**

- Up to 100 Mbps data rate using 4 parallel data lines (SD4 bit mode)
- Up to 416 Mbps data rate using 8-bit parallel data lines (SD8 bit mode)
- DMA-based and non-DMA modes of operation
- Support for MMC Plus and MMC Mobile
- Card detection (insertion / removal)
- Card password protection
- Host clock rate variable between 0 and 48 MHz
- Multimedia card interrupt mode
- Cyclic redundancy check: CRC7 (command) and CRC16 (data integrity)
- Error correction code (ECC) support for MMC4.2 cards
- Supports for Read Wait Control and Suspend/Resume
- FIFO overrun and under-run handling by stopping SD clock

## 2.11 CAN 2.0 ports

SPEAr320S provides two independent CAN (controller area network) bus ports, typically used in automotive, industrial and medical applications. For the connection to the physical layer, an additional transceiver per port is required.

For communication on a CAN network, the controller enables to configure individual message objects. The message objects and identifier masks for acceptance filtering of received messages are stored in an integrated message RAM. All functions concerning the handling of messages are implemented by a message handler. Those functions are the acceptance filtering, the transfer of messages between the CAN core and the message RAM, the handling of transmission requests as well as the generation of interrupts.

**Main features:**

- Support for CAN protocol, version 2.0 part A and B
- Transfer rate up to 1 Mbps
- Internal RAM storage for up to 16 message objects (16 x 136 bytes memory)
- Identifier mask per message object
- Maskable interrupts
- Programmable loop-back mode for self-test operation
- Disabled automatic retransmission mode for time triggered CAN applications

## 2.12 Asynchronous serial ports (UART)

The SPEAr320S has 7 UART ports. The actual number of concurrently exploitable ports depends on the selected chip operating mode. The different capabilities of each port are summarized in [Table 3](#) below.

**Table 3. SPEAr320S UART capabilities**

| Port      | Speed        | Hardware flow control         | Modem signals                 |
|-----------|--------------|-------------------------------|-------------------------------|
| UART0     | Up to 3 Mbps | Yes                           | Yes (as alternate function)   |
| UART1     | Up to 7 Mbps | Yes (except for Mode 1 and 2) | Yes (except for Mode 1 and 2) |
| UART2 - 6 | Up to 7 Mbps | No                            | No                            |

### Main features:

- Programmable baud rate generator
- Transmit FIFO queue (8-bit data, 16 entries) and receive FIFO queue (12-bit data/status, 16 entries) with disabling option (1-byte buffer depth)
- Supports for DMA operation
- Hardware flow control (RTS,CTS) for some ports and configurations
- Modem control signals (DCD, DSR, DTS, RI) for some ports and configurations
- Fully programmable serial interface with following parameters:
  - data bits: 5, 6, 7 or 8
  - parity: even, odd, stick or none (generation and detection)
  - stop bits: 1 or 2
  - line break handling (generation and detection)
- Flexible interrupt handing and masking

## 2.13 I2C bus ports (I2C)

The SPEAr320S provides three independent I2C bus ports. Each port can be configured as I2C bus master or slave.

### Main features:

- Compliant to the I2C bus specification (Philips)
- Support for the 3 standard speeds:
  - Standard (100 Kbps)
  - Fast (400 kbps)
  - High-speed
- Support for direct memory access (DMA)
- Clock synchronization
- Support for slave operation in multimaster environment
- 7-bit or 10-bit addressing
- 7-bit or 10-bit combined format transfers
- Slave bulk transfer mode
- Transmit and receive buffers
- Interrupt or polled-mode operation
- Handling of bit and byte waiting at all bus speeds
- Digital filter for the received SDA and SCL lines
- Filtering out of legacy CBUS addresses

## 2.14 Synchronous serial ports (SSP)

SPEAr320S provides three independent synchronous serial ports. Each port can be configured as master or slave.

### Main features:

- Support for the following protocols:
  - SPI (Motorola)
  - Microwire (National Semiconductor)
  - SSI (Texas Instruments)
- Programmable parameters:
  - Clock bit rate and prescale
  - Data frame size (from 4 to 16 bits)
- Separate transmit and receive FIFO queues (8 x 16-bit entries)
- Independent masking of transmit FIFO, receive FIFO, and receive overrun interrupts
- Internal loopback test mode available
- DMA interface

## 2.15 RS485 port (RS485)

SPEAr320S provides an additional UART port specialized for the RS485 standard.

### Main features:

- Transmit FIFO queue (8-bit data, 16 entries) and receive FIFO queue (12-bit data/status, 16 entries) with disabling option (1-byte buffer depth)
- Speed up to 7 Mbps

## 2.16 Fast infrared port (IrDA)

SPEAr320S provides an infrared interface compliant to the IrDA (Infrared Data Association) standard specification. An external infrared transceiver is assumed. The Fast IrDa controller performs the modulation and demodulation of the infrared signals as well as the wrapping of IrDA link access protocol (IrLAP) frames.

### Main features:

- Support for the following standards:
  - IrDA serial infrared physical layer specification (IrPHY), version 1.3
  - IrDA link access protocol (IrLAP), version 1.1
- Support for the following modes and baud rates:
  - Serial infrared (SIR): 9.6 Kbps, 19.2 Kbps, 38.4 Kbps, 57.6 Kbps, 115.2 Kbps
  - Medium infrared (MIR): 576 Kbps, 1152 Kbps
  - Fast infrared (FIR): 4 Mbps
- Support for half-duplex infrared frame transmission and reception
- Interface compliant to all IrDA transceivers with configurable polarity of TX and RX signals
- Integrated CRC algorithm: 16-bit (SIR, MIR), 32-bit (FIR)
- Automatic generation of preamble, start and stop flags
- RZI (return-to-zero inverted) modulation/demodulation scheme for SIR and MIR modes
- 4PPM (4-pulse position modulation) modulation/demodulation scheme for FIR mode
- Synchronization by DPLL in FIR mode
- Payload data transfer controllable by either CPU or DMA controller
- Two clock domains:
  - Dedicated clock (IRDA\_CLK signal) for accurate signal generation (48 MHz)
  - Independent and variable clock for the bus interface (13 MHz)

## 2.17 Legacy IEEE 1284 parallel port (SPP)

SPEAr320S provides a parallel port (slave mode only) compliant to the legacy IEEE 1284 standard.

### Main features:

- Unidirectional 8-bit data transfer from external host to SPEAr320S slave
- Additional 9th bit for parity/data/command
- Maskable interrupts for data, device reset, auto line feed

## 2.18 A/D converter (ADC)

SPEAr320S provides an integrated analog-to-digital converter.

### Main features:

- Successive approximation conversion method
- 8 x analog input channels, ranging from 0 to 2.5 V
- 10-bit resolution
- Sampling rate up to 1 Msamples/s
- Support for 13.5-bit resolution at 8 Ksamples/s by oversampling and accumulation
- $INL \pm 1$  LSB,  $DNL \pm 1$  LSB
- Programmable conversion speed (minimum conversion time is 1  $\mu$ s)
- Programmable averaging of multiple values from 1 (no averaging) up to 128
- Programmable auto scan for all the 8 channels

## 2.19 General purpose I/Os (GPIO/XGPIO)

Up to 102 GPIOs are available in SPEAr320S when some embedded IPs are not needed in the customer application (see [Section 3.4: Shared IO pins \(PL\\_GPIOs\)](#)).

SPEAr320S provides two mechanisms:

- a basic GPIO module (called “basGPIO”): this functional block provides 6 pins, each one programmable by software with the following features:
  - Programmable direction: input (default at reset) or output
  - Programmable edge-sensitive and level-sensitive interrupt triggering
- extended GPIOs (XGPIO): this capability allows any PL\_GPIO pin to be configured and used as an alternative to the corresponding predefined signal purpose. XGPIOs have a different register programming model from basic GPIOs with the following features:
  - Programmable direction: input or output
  - Programmable edge-sensitive interrupt triggering

## 2.20 LCD display controller (CLCD)

SPEAr320S has an integrated display controller able to directly interface a variety of color and monochrome LCD panels.

### Main features:

- Programmable resolution up to 1024 x 768 (XGA)
- Programmable timing parameters
- Support for TFT (thin film transistor) color displays
- Supports for STN (super twisted nematic) displays (single and dual panel) with 4- or 8-bit interfaces
- AC bias signal for STN and data enable signal for TFT panels
- Gray scaling algorithm

The set of supported pixel widths and formats for each display type is shown in [Table 4](#).

**Table 4. Pixel widths and formats available for different display types**

| Display   | 1 bpp                            | 2 bpp                            | 4 bpp                             | 8 bpp                           | 16 bpp                             | 24 bpp                 |
|-----------|----------------------------------|----------------------------------|-----------------------------------|---------------------------------|------------------------------------|------------------------|
| Color TFT | Palette of 2 colors over 64K     | Palette of 4 colors over 64K     | Palette of 16 colors over 64K     | Palette of 256 colors over 64K  | RGB 5:5:5 + intensity (64K colors) | RGB 8:8:8 (16M colors) |
| Color STN | Palette of 2 colors over 3375    | Palette of 4 colors over 3375    | Palette of 16 colors over 3375    | Palette of 256 colors over 3375 | RGB 4:4:4 (4096 colors)            | -                      |
| Mono STN  | Palette of 2 gray levels over 15 | Palette of 4 gray levels over 15 | Palette of 16 gray levels over 15 | Palette of 256 colors over 3375 | -                                  | -                      |

## 2.21 Touchscreen interface (TOUCHSCREEN)

SPEAr320S provides a toggling output signal (TOUCHSCREEN\_X) that can be connected to an external touchscreen panel. This interface operates in combination with the A/D converter (ADC). Two coordinates can be read by software from the ADC: one at the end of the high period and one at the end of the low period of TOUCHSCREEN\_X signal.

## 2.22 JPEG codec accelerator (JPGC)

SPEAr320S provides an integrated hardware accelerator for decoding and encoding standard JPEG images.

JPEG data streams to be decoded must be compliant with the interchange format syntax specified in the ISO/IEC 10918-1. The JFIF image file format is also supported through header processing.

The output format for decoding (and input format for encoding) is a MCU stream, not a conventional bitmap format like RGB. Displaying a decoded JPEG still picture would require further steps and algorithms like color space conversion and scaling.

### Main features:

- Compliance with the baseline JPEG standard (ISO/IEC 10918-1)
- Single-clock per pixel encoding/decoding
- Support for up to four channels of component color
- 8-bit/channel pixel depths
- Programmable quantization tables (up to four)
- Programmable Huffman tables (two AC and two DC)
- Programmable minimum coded unit (MCU)
- Configurable JPEG header processing
- Support for restart marker insertion
- Use of two DMA channels and two 8 x 32-bit FIFOs (local to the JPEG) for efficient transferring and buffering of encoded/decoded data from/to the Codec core.

## 2.23 Digital audio port (I2S)

The SPEAr320S integrates a digital audio port compliant to standard I2S (Philips) specifications.

### Main features:

- I2S master mode
- Stereo (2.0) playback and recording
- Support for standard sampling rates (8, 16, 32, 44.1, 48, 96, 192 kHz); the clock input is 24 MHz, so the rate precision depends on the chosen rate and divider.
- Support of a range of audio samples: 12 / 16 / 20 / 24/ 32 bits
- Programmable thresholds for internal FIFO queues
- Capability of using DMA transfer

## 2.24 Cryptographic co-processor (C3)

SPEAr320S provides an embedded cryptographic co-processor (C3). C3 is a high-performance instruction-driven DMA-based engine that can be used to accelerate the processing of security algorithms.

After its initial configuration by the main CPU, it runs in a completely autonomous way (DMA data in, data processing, DMA data out), until the completion of all the requested operations. C3 firmware is fetched from system memory.



**Main features:**

- Supported cryptographic algorithms:
  - Advanced encryption standard (AES) cipher in ECB, CBC, CTR modes
  - Data encryption standard (DES) cipher in ECB and CBC modes
  - SHA-1, HMAC-SHA-1, MD5, HMAC-MD5 digests
- Hardware chaining of cryptographic stages for optimized data flow when multiple algorithms are required to process the same set of data (for example, encryption and hashing on the fly)

## 2.25 System controller (SYSCTR)

The system controller provides an interface for controlling the operation of the overall system.

**Main features:**

- Power saving system mode control
- Crystal oscillator and PLL control
- Configuration of system response to interrupts
- Reset status capture and soft reset generation
- Watchdog and timer module clock enable

Using three mode control bits, the system controller switches the SPEAr320S to any of the four different modes: DOZE, SLEEP, SLOW and NORMAL.

- **SLEEP mode:** in this mode, the system clocks, HCLK and CLK, are disabled and the system controller clock, SCLK, is driven by a low-speed oscillator (nominally 32768 Hz). When either a FIQ or an IRQ interrupt is generated (through the VIC), the system enters DOZE mode. Additionally, the operating mode setting in the system control register automatically changes from SLEEP to DOZE.
- **DOZE mode:** in this mode, the system clocks, HCLK and CLK, and the system controller clock are driven by a crystal oscillator (24 MHz) or a low-frequency oscillator (32 KHz). The system controller moves into SLEEP mode from DOZE mode only when none of the mode control bits are set and the processor is in wait-for-interrupt state. If SLOW mode or NORMAL mode is required, the system moves into the XTAL control transition state to initialize the crystal oscillator.
- **SLOW mode:** during this mode, both the system clocks and the system controller clock are driven by the crystal oscillator. If NORMAL mode is selected, the system goes into the “PLL control” transition state. If neither the SLOW nor the NORMAL mode control bits are set, the system goes into the “Switch from XTAL” transition state.
- **NORMAL mode:** in NORMAL mode, both the system clocks and the system controller clock are driven by the PLL output. If the NORMAL mode control bit is not set, then the system goes into the “Switch from PLL” transition state.

### 2.25.1 Reset and clock generator

The reset and clock generator is a fully programmable block that generates all the clocks necessary to the chip.

The default operating clock frequencies are:

- Clock @ 333 MHz for the CPU.
- Clock @ 166 MHz for AHB bus and AHB peripherals.
- Clock @ 83 MHz for, APB bus and APB peripherals.
- Clock @ 333 MHz for DDR memory interface.

The default values give the maximum allowed clock frequencies. The clock frequencies are fully programmable through dedicated registers.

The reset and clock generator consists of 2 main parts:

- Multiclock generator block
- 3 internal PLLs

The multiclock generator block receives a reference signal (which is usually delivered by the PLL) and generates all clocks for SPEAr320S IPs according to dedicated programmable registers.

Each PLL uses an oscillator input of 24 MHz to generate a clock signal at a frequency corresponding at the highest of the group. This is the reference signal used by the multiclock generator block to obtain all the other requested clocks for the group. Its main feature is the electromagnetic interference reduction capability.

You can set up PLL1 and PLL2 in order to modulate the VCO with a triangular wave. The resulting signal has a spectrum (and power) spread over a small programmable range of frequencies centered on F0 (the VCO frequency), obtaining minimum electromagnetic emissions. This method replaces all the other traditional methods of EMI reduction, such as filtering, ferrite beads, chokes, adding power layers and ground planes to PCBs, metal shielding and so on. This offers important cost savings.

### 2.26 Vectored interrupt controller (VIC)

SPEAr320S integrates a vectored interrupt controller which provides a software interface to the interrupt system. In any system with an interrupt controller, the software has to determine the source that requests service and where its service routine is loaded. The VIC inside SPEAr320S does both of these in hardware. It supplies the starting address, or vector address, of the service routine corresponding to the highest priority requesting interrupt source.

As in any ARM9-based system, two levels of interrupts are available:

- fast interrupt requests (FIQ), for fast, low latency interrupt handling
- normal interrupt requests (IRQ), for more general interrupts

The interrupt inputs must be level sensitive, active HIGH, and held asserted until the interrupt service routine clears the interrupt. Edge-triggered interrupts are not compatible. The interrupt inputs do not have to be synchronous to HCLK. The VIC does not handle interrupt sources with transient behavior. For example, an interrupt is asserted and then de-asserted before software can clear the interrupt source. In this case, the CPU acknowledges the interrupt and obtains the vectored address for the interrupt from the VIC, assuming that no other interrupt has occurred to overwrite the vectored address. However, when a

transient interrupt occurs, the priority logic of the VIC is not set, and lower priority interrupts can interrupt the transient interrupt service routine, assuming interrupt nesting is permitted.

There are 32 interrupt lines. The VIC uses a bit position for each different interrupt source. The software can control each request line to generate software interrupts. There are 16 vectored interrupts. These interrupts can only generate an IRQ interrupt. The vectored and non-vectored IRQ interrupts provide an address for an interrupt service routine (ISR). The FIQ interrupt has the highest priority, followed by interrupt vector 0 to interrupt vector 15. Non-vectored IRQ interrupts have the lowest priority.

The specific interrupt map for the SPEAr320S device is documented in the companion reference manuals.

## 2.27 Watchdog timer (WDT)

The ARM watchdog module consists of a 32-bit down counter with a programmable time-out interval that has the capability to generate an interrupt and a reset signal on timing out. The watchdog module is intended to be used to apply a reset to a system in the event of a software failure.

## 2.28 Real-time clock (RTC)

The real-time clock provides an 1-second resolution clock. This keeps time when the system is inactive and can be used to wake the system up when a programmed alarm time is reached.

### Main features:

- Time-of-day clock in 24 hour mode
- Calendar
- Alarm capability
- Isolation mode, allowing RTC to work even if power is not supplied to the rest of the device.

## 2.29 DMA controller (DMAC)

SPEAr320S provides one DMA controller.

### Main features:

- Able to service up to 8 independent DMA channels for serial data transfers between single source and destination (for instance, memory-to-memory, memory-to-peripheral, peripheral to- memory, and peripheral-to-peripheral).
- Each DMA channel can support a unidirectional transfer, with internal four-word FIFO per channel.

## 2.30 General purpose timers (GPT)

SPEAr320S provides 6 general purpose timers.

**Main features:**

- Each timer provides a programmable 16-bit counter and a dedicated prescaler able to perform a clock division by 1 up to 256 (different input frequencies can be chosen through configuration registers, in the range from 3.96 Hz to 48 MHz)
- Operating modes:
  - Auto-reload mode: when a software-defined value is reached, an interrupt is triggered and the counter automatically restarts from zero
  - Single-shot mode: when a software-defined value is reached, an interrupt is triggered, the counter is stopped and the timer is disabled
- Capture capability (only for 4 timers)

## 2.31 Pulse width modulators (PWM)

SPEAr320S integrates 4 PWM (pulse width modulation) signal generators.

**Main features:**

- Prescaler to define the input clock frequency to each timer
- Programmable duty cycle from 0% to 100%
- Programmable pulse length

### 3 Pin description

This chapter provides a full description of the ball characteristics and the signal multiplexing of SPEAr320S device.

[Section 3.1](#) shows the pin/ball map of SPEAr320S.

[Section 3.2](#) lists the required external components to connect.

[Section 3.3](#) describes some dedicated pins, such as:

- [Clock, reset and 3V3 comparator pins](#)
- [Power supply pins](#)
- [Debug pins](#)
- [Non-multiplexed pins](#)

[Section 3.4](#) provides a complete description of the shared IO pins (PL\_GPIOs) and their configuration modes, as well as detailed information on all multiplexed signals, grouped by IP.

[Section 3.5](#) explains the available debug modes.

The following table defines the table headers and abbreviations used in this chapter.

**Table 5. Headers/abbreviations**

| Header                    | Description  | Abbreviations                               |
|---------------------------|--|---|
| <b>Group</b>              | Grouping of signals of the same type/functional block.   | –   |
| <b>Signal name</b>        | Name of signal multiplexed on each ball.   | –   |
| <b>Direction (Dir.)</b>   | Indicates the direction of the signal.   | I= Input<br>O= Output<br>IO= Input/output   |
| <b>PL_GPIO_# /Ball</b>    | PL_GPIO and ball number associated with each signal on the package.  | –   |
| <b>Configuration mode</b> | Indicates the available configuration mode among the following ones:<br>– Mode 1<br>– Mode 2<br>– Mode 3<br>– Mode 4<br>– Alternate function<br>– Extended mode<br>See <a href="#">Section 3.4.2</a> for the description of each mode. | –   |
| <b>Pin type</b>           | Pad type information   | PU= Pull Up<br>PD= Pull Down<br>GND= Ground |
| <b>Value</b>              | Indicates the electrical value on the ball.  | –   |



### 3.1 Pin/ball map

Figure 2. SPEAr320S pin/ball map

|          | 1                 | 2                | 3                              | 4                          | 5                | 6                | 7                | 8            | 9            | 10                  | 11               | 12               | 13            | 14                  | 15             | 16            | 17            |
|----------|-------------------|------------------|--------------------------------|----------------------------|------------------|------------------|------------------|--------------|--------------|---------------------|------------------|------------------|---------------|---------------------|----------------|---------------|---------------|
| <b>A</b> | PL_GPIO_13        | PL_GPIO_14       | PL_GPIO_19                     | PL_GPIO_23                 | PL_GPIO_26       | PL_GPIO_28       | PL_GPIO_29       | PL_GPIO_38   | PL_GPIO_39   | PL_GPIO_44          | PL_GPIO_46       | PL_GPIO_50       | PL_GPIO_55    | PL_GPIO_60          | PL_GPIO_62     | PL_GPIO_69    | PL_GPIO_73    |
| <b>B</b> | PL_GPIO_6         | PL_GPIO_9        | PL_GPIO_15                     | PL_GPIO_20                 | PL_GPIO_24       | PL_GPIO_27       | PL_GPIO_30       | PL_GPIO_37   | PL_GPIO_40   | PL_GPIO_45          | PL_GPIO_48       | PL_GPIO_52       | PL_GPIO_59    | PL_GPIO_65          | PL_GPIO_68     | PL_GPIO_72    | PL_GPIO_77    |
| <b>C</b> | PL_GPIO_4         | PL_GPIO_8        | PL_GPIO_10                     | PL_GPIO_17                 | PL_GPIO_21       | PL_GPIO_25       | PL_GPIO_31       | PL_GPIO_36   | PL_GPIO_41   | PL_GPIO_47          | PL_GPIO_49       | PL_GPIO_56       | PL_GPIO_63    | PL_GPIO_67          | PL_GPIO_70     | PL_GPIO_74    | PL_GPIO_81    |
| <b>D</b> | PL_GPIO_3         | PL_GPIO_5        | PL_GPIO_7                      | PL_GPIO_12                 | PL_GPIO_18       | PL_GPIO_22       | PL_GPIO_32       | PL_GPIO_35   | PL_GPIO_42   | PL_GPIO_51          | PL_GPIO_53       | PL_GPIO_58       | PL_GPIO_64    | PL_GPIO_71          | PL_GPIO_78     | PL_GPIO_80    | PL_GPIO_84    |
| <b>E</b> | RTC_XO            | RTC_XI           | PL_GPIO_1                      | PL_GPIO_2                  | PL_GPIO_11       | PL_GPIO_16       | PL_GPIO_33       | PL_GPIO_34   | PL_GPIO_43   | PL_GPIO_54          | PL_GPIO_57       | PL_GPIO_61       | PL_GPIO_66    | PL_GPIO_75          | PL_GPIO_82     | PL_GPIO_83    | PL_GPIO_86    |
| <b>F</b> | RTC_vdd1v5        | RTC_gnd          | PL_GPIO_0                      | DIGITAL_GNDBG_COMP         | digital_vdde 3v3 | digital_vdde 3v3 | digital_vdde 3v3 | vdd          | vdd          | digital_vdde 3v3    | digital_vdde 3v3 | digital_vdde 3v3 | PL_GPIO_76    | PL_GPIO_79          | PL_GPIO_85     | PL_GPIO_88    | PL_GPIO_89    |
| <b>G</b> | DITH_pll_vss_ana  | DITH_pll_vdd_ana | USB_DEVICE_VBUS                | DIGITAL_REXT               | digital_vdde 3v3 | gnd              | gnd              | gnd          | gnd          | gnd                 | gnd              | vdd              | PL_GPIO_87    | PL_GPIO_90          | PL_GPIO_91     | PL_GPIO_92    | PL_GPIO_93    |
| <b>H</b> | USB_HOST1_DP      | USB_HOST1_DM     | USB_HOST1_VBUS                 | USB_HOST0_OVERCUR          | vdd              | gnd              | gnd              | gnd          | gnd          | gnd                 | gnd              | vdd              | PL_GPIO_94    | PL_GPIO_95          | PL_GPIO_96     | PL_GPIO_97    | PL_CLK4       |
| <b>J</b> | USB_HOST1_vdd3v3  | gnd              | USB_HOST0_VBUS                 | USB_HOST1_OVERCUR          | vdd              | gnd              | gnd              | gnd          | gnd          | gnd                 | gnd              | digital_vdde 3v3 | DDR2_EN       | BOOT_SEL            | TEST_4         | PL_CLK3       | PL_CLK2       |
| <b>K</b> | USB_HOST0_DP      | USB_HOST0_DM     | USB_HOST1_vdd2v5               | USB_HOST0_vdd3v3           | USB_TXR_TUNE     | gnd              | gnd              | gnd          | gnd          | gnd                 | gnd              | digital_vdde 3v3 | TEST_3        | TEST_2              | TEST_1         | TEST_0        | PL_CLK1       |
| <b>L</b> | gnd               | USB_HOST0_vdd2v5 | gnd                            | USB_ANALOG_TEST            | gnd              | gnd              | gnd              | gnd          | gnd          | gnd                 | vdd              | digital_vdde 3v3 | TMS           | TDI                 | TDO            | nTRST         | TCK           |
| <b>M</b> | USB_DEVICE_DP     | USB_DEVICE_DM    | USB_HOST1_HOST0_DEVICE_Dvdd1v2 | dith_vdd2v5                | DDR_vdde1v8      | vdd              | vdd              | gnd          | gnd          | gnd                 | vdd              | digital_vdde 3v3 | SMI_DATAIN    | SMI_DATAOUT         | SMI_CS_0       | SMI_CS_1      | MRESET        |
| <b>N</b> | USB_DEVICE_vdd2v5 | gnd              | USB_DEVICE_vdd3v3              | dith_vss2v5                | DDR_vdde1v8      | DDR_vdde1v8      | DDR_vdde1v8      | DDR_vdde1v8  | DDR_vdde1v8  | DDR_vdde1v8         | DDR_vdde1v8      | ADC_agnd         | ADC_avdd      | ADC_VREFN           | AIN_1          | AIN_0         | SMI_CLK       |
| <b>P</b> | MCLK_XI           | MCLK_XO          | MCLK_GND                       | DDR_MEM_COMP2V5_GNDBG_COMP | DDR_MEM_ADDR_9   | DDR_MEM_ADDR_10  | DDR_MEM_BA_0     | DDR_MEM_BA_1 | DDR_MEM_CS_0 | DDR_MEM_VREF        | DDR_MEM_DQ_0     | DDR_MEM_DQ_6     | DDR_MEM_DQ_7  | ADC_VREFP           | AIN_4          | AIN_3         | AIN_2         |
| <b>R</b> | MCLK_VDD          | MCLK_VDD2V5      | MCLK_GNDSUB                    | DDR_MEM_COMP2V5_GNDBG_COMP | DDR_MEM_ADDR_8   | DDR_MEM_ADDR_11  | DDR_MEM_ADDR_14  | DDR_MEM_BA_2 | DDR_MEM_CS_1 | DDR_MEM_GATE_OPEN_0 | DDR_MEM_DQ_1     | DDR_MEM_DQ_5     | DDR_MEM_DQ_15 | DDR_MEM_GATE_OPEN_1 | AIN_7          | AIN_6         | AIN_5         |
| <b>T</b> | DDR_MEM_ADDR_1    | DDR_MEM_ADDR_0   | DDR_MEM_ODT_0                  | DDR_MEM_ODT_1              | DDR_MEM_ADDR_7   | DDR_MEM_ADDR_12  | DDR_MEM_WE       | DDR_MEM_CAS  | DDR_MEM_CLKP | nDDR_MEM_DQS_0      | DDR_MEM_DQ_2     | DDR_MEM_DQ_4     | DDR_MEM_DQ_14 | DDR_MEM_DM_1        | nDDR_MEM_DQS_1 | DDR_MEM_DQ_9  | DDR_MEM_DQ_8  |
| <b>U</b> | DDR_MEM_ADDR_2    | DDR_MEM_ADDR_3   | DDR_MEM_ADDR_4                 | DDR_MEM_ADDR_5             | DDR_MEM_ADDR_6   | DDR_MEM_ADDR_13  | DDR_MEM_CLKEN    | DDR_MEM_RAS  | DDR_MEM_CLKN | DDR_MEM_DQS_0       | DDR_MEM_DQ_3     | DDR_MEM_DM_0     | DDR_MEM_DQ_13 | DDR_MEM_DQ_12       | DDR_MEM_DQS_1  | DDR_MEM_DQ_11 | DDR_MEM_DQ_10 |

## 3.2 Required external components

Some pads require the use of an external component. Please follow the instructions below to ensure the proper functioning of the device:

1. DDR\_COMP\_1V8: place an external 121 k $\Omega$  resistor between ball P4 and ball R4
2. USB\_TX\_RTUNE: connect an external 43.2  $\Omega$  pull-down resistor to ball K5
3. DIGITAL\_REXT: place an external 121 k $\Omega$  resistor between ball G4 and ball F4
4. DITH\_VDD\_2V5: add a ferrite bead to ball M4

## 3.3 Dedicated pins description

### 3.3.1 Clock, reset and 3V3 comparator pins

**Table 6. MCLK, RTC, Reset and 3.3 V comparator pins description**

| Group                 | Signal name       | Description                  | Dir.  | Pin type   | Ball |
|-----------------------|-------------------|------------------------------|-------|--|------|
| Master clock (MCLK)   | MCLK_XI           | 24 MHz (typical) crystal in  | I     | Oscillator 2.5 V capable                         | P1   |
|                       | MCLK_XO           | 24 MHz (typical) crystal out | O     |  | P2   |
| Real-time clock (RTC) | RTC_XI            | 32 kHz crystal in            | I     | Oscillator 1V5 capable                           | E2   |
|                       | RTC_XO            | 32 kHz crystal out           | O     |  | E1   |
| Reset                 | MRESET            | Main reset                   | I     | TTL Schmitt trigger input buffer, 3.3 V tolerant | M17  |
| 3.3 V comparator      | DIGITAL_REXT      | Configuration                | O     | Analog, 3.3 V capable                            | G4   |
|                       | DIGITAL_GNDBGCOMP | Power                        | Power | Power  | F4   |

### 3.3.2 Power supply pins

**Table 7. Power supply pins description**

| Group          | Signal name                    | Value | Ball   |
|----------------|--------------------------------|-------|--|
| Digital ground | GND                            | 0 V   | G6 G7 G8 G9 G10 G11 H6 H7<br>H8 H9 H10 H11 J6 J7 J8 J9 J10<br>J11 K6 K7 K8 K9 K10 K11 L6 L7<br>L8 L9 L10 M8 M9 M10 |
|                | USB_HOST1_HOST0_DEVICE_DVSS    |       | L5   |
| Analog ground  | RTC_GND                        | 0 V   | F2   |
|                | DITH_PLL_VSS_ANA               |       | G1   |
|                | USB_HOST1_VSSA                 |       | J2   |
|                | USB_HOST0_VSSA                 |       | L1   |
|                | USB_COMMON_VSSAC               |       | L3   |
|                | USB_DEVICE_VSSA                |       | N2   |
|                | DITH_VSS2V5                    |       | N4   |
|                | MCLK_GND                       |       | P3   |
|                | MCLK_GNDSUB                    |       | R3   |
| ADC_AGND       | N12                            |       |  |
| IO             | DIGITAL_VDDE3V3                | 3.3 V | F5 F6 F7 F10 F11 F12 G5 J12<br>K12 L12 M12   |
| Core           | VDD                            | 1.2 V | F8 F9 G12 H5 H12 J5 L11 M6<br>M7 M11   |
| USB Host0 PHY  | USB_HOST0_VDD2V5               | 2.5 V | L2   |
|                | USB_HOST0_VDD3V3               | 3.3 V | K4   |
| USB Host1 PHY  | USB_HOST1_VDD2V5               | 2.5 V | K3   |
|                | USB_HOST1_VDD3V3               | 3.3 V | J1   |
| USB Device PHY | USB_DEVICE_VDD2V5              | 2.5 V | N1   |
|                | USB_DEVICE_VDD3V3              | 3.3 V | N3   |
|                | USB_HOST1_HOST0_DEVICE_DVDD1V2 | 1.2 V | M3   |
| OSCI (MCLK)    | MCLK_VDD                       | 1.2 V | R1   |
|                | MCLK_VDD2V5                    | 2.5 V | R2   |
| PLL1           | DITH_PLL_VDD_ANA               | 2.5 V | G2   |
| PLL2           | DITH_VDD_2V5                   | 2.5 V | M4   |
| DDR IO         | DDR_VDDE1V8                    | 1.8 V | M5 N5 N6 N7 N8 N9 N10 N11  |
| ADC            | ADC_AVDD                       | 2.5 V | N13  |
| OSCI (RTC)     | RTC_VDD1V5                     | 1.5 V | F1   |

*Note: All the VDD 2V5 power supplies are analog VDD.*



### 3.3.3 Debug pins

**Table 8. Debug pins description**

| Signal name | Description  | Dir. | Pin type   | Ball |
|-------------|--|------|--|------|
| TEST_0      | Debug mode configuration ports. See also <a href="#">Section Table 32.: Ball sharing during debug.</a> | I    | TTL input buffer, 3.3 V tolerant, PD                 | K16  |
| TEST_1      |  |      |  | K15  |
| TEST_2      |  |      |  | K14  |
| TEST_3      |  |      |  | K13  |
| TEST_4      |  |      |  | J15  |
| BOOT_SEL    | Reserved, to be fixed at high level  |      |  | J14  |
| nTRST       | Test reset input   | I    | TTL Schmitt trigger input buffer, 3.3 V tolerant, PU | L16  |
| TDO         | Test data output   | O    | TTL output buffer, 3.3 V capable 4 mA                | L15  |
| TCK         | Test clock   | I    | TTL Schmitt trigger input buffer, 3.3 V tolerant, PU | L17  |
| TDI         | Test data input  | I    |  | L14  |
| TMS         | Test mode select   | I    |  | L13  |

### 3.3.4 Non-multiplexed pins

**Table 9. SMI pins description**

| Signal name | Description              | Dir. | Pin type                             | Ball |
|-------------|--------------------------|------|--------------------------------------|------|
| SMI_DATAIN  | Serial Flash input data  | I    | TTL Input Buffer 3.3 V tolerant, PU  | M13  |
| SMI_DATAOUT | Serial Flash output data | O    | TTL output buffer 3.3 V capable 4 mA | M14  |
| SMI_CLK     | Serial Flash clock       | IO   |                                      | N17  |
| SMI_CS_0    | Serial Flash chip select | O    |                                      | M15  |
| SMI_CS_1    |                          |      |                                      | M16  |

**Table 10. USB pins description**

| Group      | Signal name       | Description            | Dir. | Pin type                                 | Ball |
|------------|-------------------|------------------------|------|--|------|
| USB Device | USB_DEVICE_DP     | USB Device D+          | IO   | Bidirectional analog buffer 5 V tolerant | M1   |
|            | USB_DEVICE_DM     | USB Device D-          |      |  | M2   |
|            | USB_DEVICE_VBUS   | USB Device VBUS        | I    | TTL input buffer 3.3 V tolerant, PD      | G3   |
| USB Host   | USB_HOST1_DP      | USB Host1 D+           | IO   | Bidirectional analog buffer 5 V tolerant | H1   |
|            | USB_HOST1_DM      | USB Host1 D-           |      |  | H2   |
|            | USB_HOST1_VBUS    | USB Host1 VBUS         | O    | TTL output buffer 3.3 V capable, 4 mA    | H3   |
|            | USB_HOST1_OVERCUR | USB Host1 Over-Current | I    | TTL input buffer 3.3 V tolerant, PD      | J4   |
|            | USB_HOST0_DP      | USB Host0 D+           | IO   | Bidirectional analog buffer 5 V tolerant | K1   |
|            | USB_HOST0_DM      | USB Host0 D-           |      |  | K2   |
|            | USB_HOST0_VBUS    | USB Host0 VBUS         | O    | TTL output buffer 3.3 V capable, 4 mA    | J3   |
|            | USB_HOST0_OVERCUR | USB Host0 Over-current | I    | TTL Input Buffer 3.3 V tolerant, PD      | H4   |
| USB        | USB_TXRTUNE       | Reference resistor     | O    | Analog                                   | K5   |
|            | USB_ANALOG_TEST   | Analog test output     | O    | Analog                                   | L4   |

**Table 11. ADC pins description**

| Signal name | Description                    | Dir. | Pin type                     | Ball |
|-------------|--------------------------------|------|------------------------------|------|
| AIN_0       | ADC analog input channel       | I    | Analog buffer 2.5 V tolerant | N16  |
| AIN_1       |                                |      |                              | N15  |
| AIN_2       |                                |      |                              | P17  |
| AIN_3       |                                |      |                              | P16  |
| AIN_4       |                                |      |                              | P15  |
| AIN_5       |                                |      |                              | R17  |
| AIN_6       |                                |      |                              | R16  |
| AIN_7       |                                |      |                              | R15  |
| ADC_VREFN   | ADC negative voltage reference |      |                              | N14  |
| ADC_VREFP   | ADC positive voltage reference |      |                              | P14  |

Table 12. DDR pins description

| Signal name    | Description                        | Dir. | Pin type                        | Ball |
|----------------|------------------------------------|------|---------------------------------|------|
| DDR_MEM_ADD_0  | Address Line                       | O    | SSTL_2/SSTL_18                  | T2   |
| DDR_MEM_ADD_1  |                                    |      |                                 | T1   |
| DDR_MEM_ADD_2  |                                    |      |                                 | U1   |
| DDR_MEM_ADD_3  |                                    |      |                                 | U2   |
| DDR_MEM_ADD_4  |                                    |      |                                 | U3   |
| DDR_MEM_ADD_5  |                                    |      |                                 | U4   |
| DDR_MEM_ADD_6  |                                    |      |                                 | U5   |
| DDR_MEM_ADD_7  |                                    |      |                                 | T5   |
| DDR_MEM_ADD_8  |                                    |      |                                 | R5   |
| DDR_MEM_ADD_9  |                                    |      |                                 | P5   |
| DDR_MEM_ADD_10 |                                    |      |                                 | P6   |
| DDR_MEM_ADD_11 |                                    |      |                                 | R6   |
| DDR_MEM_ADD_12 |                                    |      |                                 | T6   |
| DDR_MEM_ADD_13 |                                    |      |                                 | U6   |
| DDR_MEM_ADD_14 |                                    |      |                                 | R7   |
| DDR_MEM_BA_0   | Bank select                        | O    |                                 | P7   |
| DDR_MEM_BA_1   |                                    |      |                                 | P8   |
| DDR_MEM_BA_2   |                                    |      |                                 | R8   |
| DDR_MEM_RAS    | Row address strobe                 | O    |                                 | U8   |
| DDR_MEM_CAS    | Column address strobe              | O    |                                 | T8   |
| DDR_MEM_WE     | Write enable                       | O    |                                 | T7   |
| DDR_MEM_CLKEN  | Clock enable                       | O    |                                 | U7   |
| DDR_MEM_CLKP   | Differential clock                 | O    | Differential SSTL_2/<br>SSTL_18 | T9   |
| DDR_MEM_CLKN   |                                    |      |                                 | U9   |
| DDR_MEM_CS_0   | Chip select                        | O    | SSTL_2/ SSTL_18                 | P9   |
| DDR_MEM_CS_1   |                                    |      |                                 | R9   |
| DDR_MEM_ODT_0  | On-die termination enable<br>lines | IO   |                                 | T3   |
| DDR_MEM_ODT_1  |                                    |      |                                 | T4   |

Table 12. DDR pins description (continued)

| Signal name               | Description                   | Dir.  | Pin type                               | Ball            |     |
|---------------------------|-------------------------------|-------|--|-----------------|-----|
| DDR_MEM_DQ_0              | Data lines<br>(lower byte)    | IO    | SSTL_2/ SSTL_18                        | P11             |     |
| DDR_MEM_DQ_1              |                               |       |  | R11             |     |
| DDR_MEM_DQ_2              |                               |       |  | T11             |     |
| DDR_MEM_DQ_3              |                               |       |  | U11             |     |
| DDR_MEM_DQ_4              |                               |       |  | T12             |     |
| DDR_MEM_DQ_5              |                               |       |  | R12             |     |
| DDR_MEM_DQ_6              |                               |       |  | P12             |     |
| DDR_MEM_DQ_7              |                               |       |  | P13             |     |
| DDR_MEM_DQS_0             | Lower data strobe             | O     | Differential SSTL_2/<br>SSTL_18        | U10             |     |
| nDDR_MEM_DQS_0            |                               |       |  | T10             |     |
| DDR_MEM_DM_0              | Lower data mask               | O     | SSTL_2/ SSTL_18                        | U12             |     |
| DDR_MEM_GATE_OPEN_0       | Lower gate open               | IO    |  | R10             |     |
| DDR_MEM_DQ_8              | Data lines<br>(upper byte)    | IO    |  | SSTL_2/ SSTL_18 | T17 |
| DDR_MEM_DQ_9              |                               |       |  |                 | T16 |
| DDR_MEM_DQ_10             |                               |       |  |                 | U17 |
| DDR_MEM_DQ_11             |                               |       |  |                 | U16 |
| DDR_MEM_DQ_12             |                               |       |  |                 | U14 |
| DDR_MEM_DQ_13             |                               |       |  |                 | U13 |
| DDR_MEM_DQ_14             |                               |       | T13                                    |                 |     |
| DDR_MEM_DQ_15             |                               |       | R13                                    |                 |     |
| DDR_MEM_DQS_1             | Upper data strobe             | IO    | Differential SSTL_2/<br>SSTL_18        | U15             |     |
| nDDR_MEM_DQS_1            |                               |       |  | T15             |     |
| DDR_MEM_DM_1              | Upper data mask               | IO    | SSTL_2/ SSTL_18                        | T14             |     |
| DDR_MEM_GATE_OPEN_1       | Upper gate open               |       |  | R14             |     |
| DDR_MEM_VREF              | Reference voltage             | I     | Analog                                 | P10             |     |
| DDR_MEM_COMP2V5_GNDBGCOMP | Return for external resistors | Power | Power                                  | R4              |     |
| DDR_MEM_COMP2V5_REXT      | External resistor             | Power | Analog                                 | P4              |     |
| DDR2_EN                   | Configuration                 | I     | TTL Input Buffer 3.3 V<br>Tolerant, PU | J13             |     |

### 3.4 Shared IO pins (PL\_GPIOs)

The 98 PL\_GPIO and 4 PL\_CLK pins have the following characteristics:

- Output buffer: TTL 3.3 V capable up to 10 mA
- Input buffer: TTL, 3.3 V tolerant, selectable internal pull up/pull down (PU/PD)

The PL\_GPIOs can be configured in different modes. This allows SPEAr320S to be tailored for use in various applications like:

- Metering concentrators
- Large power supply controllers
- Small printers

#### 3.4.1 PL\_GPIO / PL\_CLK pins description

**Table 13. PL\_GPIO / PL\_CLK pins description**

| Group    | Signal name                | Ball                               | Dir. | Description  | Pin type   |
|----------|----------------------------|------------------------------------|------|--|--|
| PL_GPIOs | PL_GPIO_97...<br>PL_GPIO_0 | (See<br><a href="#">Table 15</a> ) | IO   | General purpose IO or multiplexed pins (see <a href="#">Table 15</a> ) | (See the introduction of <a href="#">Section 3.4</a> here above) |
|          | PL_CLK1...<br>PL_CLK4      |                                    |      | Programmable logic external clocks                                     |  |

*Note:* The I/O direction depends on the currently configured multiplexing option and can be different from the I/O direction at reset. Refer to [Table 15: PL\\_GPIO/PL\\_CLK multiplexing scheme and reset states](#).

#### 3.4.2 Extended mode: RMI automation networking mode

When Extended mode is selected the I/O functions can be selected individually from the columns of [Table 15](#) using 11 RAS\_iosel\_regx registers which provide 3-bit configuration fields for selecting the I/O functions on each of the 102 GPIO I/O pins. (see [Table 15: PL\\_GPIO/PL\\_CLK multiplexing scheme and reset states](#)).

This mode provides a fully flexible way of configuring the I/O functions for different applications. It is forward compatible with the 4 legacy configuration modes and features enhanced interrupt management with programmable edge polarity.

For example:

- 3 independent SSP synchronous serial ports (SPI, Microwire or TI protocol)
- 2 RMI interfaces
- Standard parallel port (SPP device implementation)
- 3 independent I2C interfaces
- 7 UARTs
  - 1 with hardware flow control (up to 3 Mbps)
  - 1 with hardware flow control (baud rate up to 7 Mbps)
  - 5 with software flow control (baud rate up to 7 Mbps)
- 4 PWM outputs

### 3.4.3 Alternate functions

Other peripheral functions are listed in the Alternate Functions column of [Table 13: PL\\_GPIO / PL\\_CLK pins description](#) and can be individually enabled/disabled configuring the bits of a dedicated control register.

### 3.4.4 Legacy configuration modes

This section describes the legacy operating modes created by using a selection of the embedded IPs. These 4 modes provide for backward-compatibility with existing SPEAr320 hardware applications. Mode 1 is the default mode for SPEAr320S.

The following modes can be selected by software through programming of dedicated configuration registers (see [Figure 3: Hierarchical multiplexing scheme](#)).

- [Mode 1: HMI automation mode](#)
- [Mode 2: MII automation networking mode](#)
- [Mode 3: Expanded automation mode](#)
- [Mode 4: Printer mode](#)

[Table 15](#) shows the IO functions available in each mode.

Mode 1 is the default mode for SPEAr320S.

#### Mode 1: HMI automation mode

In this example, HMI automation networking operating mode provides the following features with Mode 1 selected and alternate functions for UART0, SSP0 and I2C0 enabled. Other feature combinations are possible using different alternate functions.

- LCD interface (up to 1024x768, 24-bit LCD controller, TFT and STN panels)
- NAND Flash interface (8 bits, 4 chip selects)
- 2 CAN 2.0 interfaces
- 3 UARTs
  - 1 with hardware flow control (up to 3 Mbps)
  - 2 with software flow control (baud rate up to 7 Mbps)
- Touchscreen facilities
- 3 independent SSP synchronous serial ports (SPI, Microwire or TI protocol)
- 2 independent I2C interfaces
- GPIOs with interrupt capability
- SDIO interface supporting SPI, SD1, SD4 and SD8 mode
- 1 PWM output (PWM3)

### Mode 2: MII automation networking mode

In this example, MII automation networking operating mode provides the following features with Mode 2 selected and alternate functions for UART0, MII0, SSP0, I2C0 enabled. Other feature combinations are possible using different alternate functions.

- NAND Flash interface (8 bits, 4 chip selects)
- 2 CAN 2.0 interfaces
- 2 MII interfaces
- 7 UARTs
  - 1 with hardware flow control (up to 3 Mbps)
  - 6 with software flow control (baud rate up to 7 Mbps)
- 3 independent SSP synchronous serial ports (SPI, Microwire or TI protocol) with 3 independent CS.
- 2 independent I2C interfaces
- GPIOs with interrupt capability
- SDIO interface supporting SPI, SD1, SD4 and SD8 mode

### Mode 3: Expanded automation mode

In this example, Expanded automation operating mode provides the following features with Mode 3 selected and alternate functions for MII0, UART0, I2C0 and SSP0 enabled. Some features are mutually exclusive. Note that if UART0 alternate functions with software flow control are enabled, UART3/4/5 are available, but not if UART0 alternate functions are enabled with hardware flow control. If SSP0 alternate functions are enabled, PWM0/1/2/3 are not available. This is also the case for EMI with respect to the NAND Flash interface (FSMC). Other feature combinations are possible using different alternate functions.

- External memory interface (16 data bits, 24 address bits and 4 chip selects)
- FSMC NAND Flash interface (8-16 bits and 4 chip selects shared with EMI)
- 2 CAN 2.0 interfaces
- MII interface
- 6 UARTs
  - 1 with hardware flow control (up to 3 Mbps)
  - 1 with hardware flow control (baud rate up to 7 Mbps)
  - 4 with software flow control (baud rate up to 7 Mbps)
- 1 SSP port
- 2 independent I2C interfaces
- Up to 4 PWM outputs
- GPIOs with interrupt capabilities

**Mode 4: Printer mode**

In this example, Printer mode provides the following features with Mode 4 selected and alternate functions for UART0, I2C0 and SSP0 enabled. Other feature combinations are possible using different alternate functions.

- NAND Flash interface (8 bits, 4 chip selects)
- 4 PWM outputs
- 7 UARTs
  - 1 with hardware flow control (up to 3 Mbps)
  - 1 with hardware flow control (baud rate up to 7 Mbps)
  - 5 with software flow control (baud rate up to 7 Mbps)
- SDIO interface supporting SPI, SD1, SD4 and SD8 mode
- Standard parallel port (SPP device implementation)
- 2 independent SSP synchronous serial ports (SPI, Microwire or TI protocol)
- 2 independent I2C interfaces
- GPIOs with interrupt capabilities



### 3.4.5 Boot pins

The status of the boot pins is read at startup by the BootROM.

The H[7:0] pins are user-definable strapping option pins. The values of the pins are latched at startup and are readable from a register.

**Table 14. Boot pins description**

| B3 B2 B1 B0 | Boot device   |
|-------------|---|
| 0000        | USB Device  |
| 0001        | Ethernet MII0 (MAC address in I2C non-volatile memory)        |
| 0010        | Ethernet MII0 (MAC address in SPI non-volatile memory)        |
| 0011        | Serial NOR Flash (SMI interface)                              |
| 0100        | Parallel 8-bit NOR Flash (EMI interface)                      |
| 0101        | Parallel 16-bit NOR Flash (EMI interface)                     |
| 0110        | Parallel 8-bit NAND Flash (FSMC interface)                    |
| 0111        | Parallel 16-bit NAND Flash (FSMC interface)                   |
| 1010        | UART0   |
| 1011        | Bypass BootROM and boot from serial NOR Flash (SMI interface) |
| Other       | Reserved  |

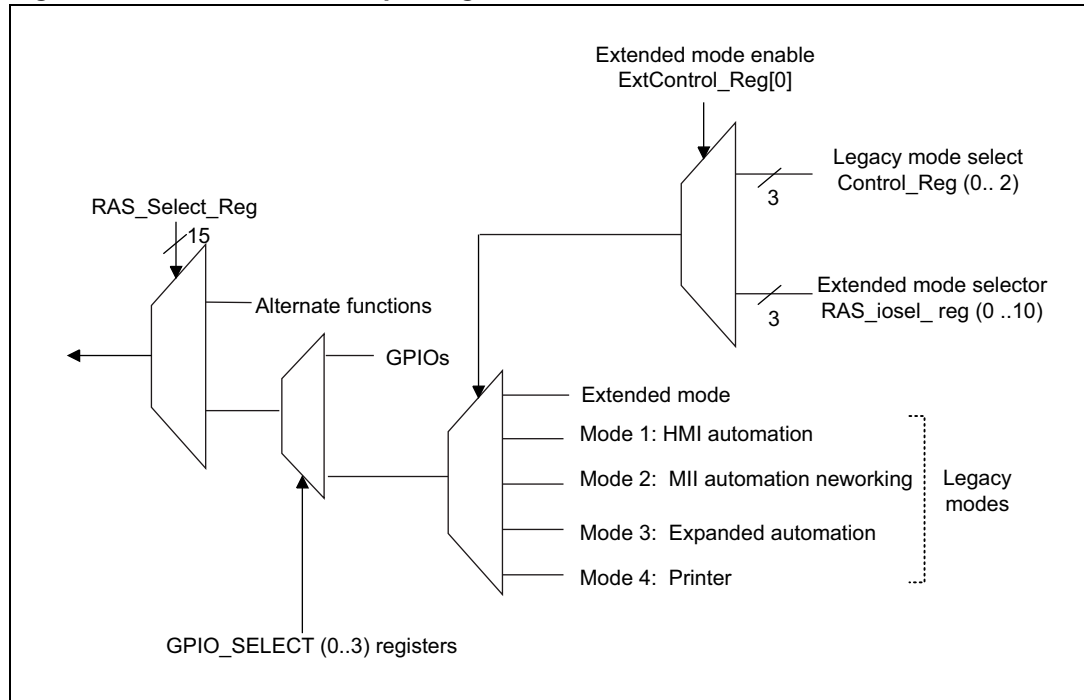
### 3.4.6 GPIOs

The PL\_GPIO pins can be used as software-controlled general purpose I/Os if they are not used by the interfaces of embedded IPs mapped on same pins.

### 3.4.7 Multiplexing scheme

To provide the best I/O multiplexing flexibility and the higher number of GPIOs for ARM controlled input-output function, the following hierarchical multiplexing scheme has been implemented.

**Figure 3. Hierarchical multiplexing scheme**



*Note:* 3 selection bits per pin are available in RAS\_iose1\_reg (0..10).



Table 15. PL\_GPIO/PL\_CLK multiplexing scheme and reset states

| PL_GPIO_# / ball number | Extended mode primary function (SW defined) | Alternate function (SW defined) | Full debug mode     | Reset state | Boot pins | Function in GPIO alternate mode | Legacy configuration mode (SW defined)     |            |         |           |
|-------------------------|---|---------------------------------|---------------------|-------------|-----------|---------------------------------|--|------------|---------|-----------|
|                         |   |                                 |                     |             |           |                                 | Mode 1 (Default configuration after reset) | Mode 2     | Mode 3  | Mode 4    |
| PL_GPIO_97/H16          | SSP1_MOSI                                   |                                 | ARM_TRACE_CLK       | OL          |           | GPIO_97                         | CLD0                                       | MII1_TXCLK | EMI_A0  | I2C2_SDA  |
| PL_GPIO_96/H15          | SSP1_CLK                                    |                                 | ARM_TRACE_PKT[A][0] | OL          |           | GPIO_96                         | CLD1                                       | MII1_TXD0  | EMI_A1  | I2C2_SCL  |
| PL_GPIO_95/H14          | SSP1_SS0                                    |                                 | ARM_TRACE_PKT[A][1] | OL          |           | GPIO_95                         | CLD2                                       | MII1_TXD1  | EMI_A2  | UART3_TX  |
| PL_GPIO_94/H13          | SSP1_MISO                                   |                                 | ARM_TRACE_PKT[A][2] | OL          |           | GPIO_94                         | CLD3                                       | MII1_TXD2  | EMI_A3  | UART3_RX  |
| PL_GPIO_93/G17          | SSP2_MOSI                                   |                                 | ARM_TRACE_PKT[A][3] | OL          |           | GPIO_93                         | CLD4                                       | MII1_TXD3  | EMI_A4  | UART4_TX  |
| PL_GPIO_92/G16          | SSP2_CLK                                    |                                 | ARM_TRACE_PKT[B][0] | OL          |           | GPIO_92                         | CLD5                                       | MII1_TXEN  | EMI_A5  | UART4_RX  |
| PL_GPIO_91/G15          | SSP2_SS0                                    |                                 | ARM_TRACE_PKT[B][1] | OL          |           | GPIO_91                         | CLD6                                       | MII1_TXER  | EMI_A6  | UART5_TX  |
| PL_GPIO_90/G14          | SSP2_MISO                                   |                                 | ARM_TRACE_PKT[B][2] | OL          |           | GPIO_90                         | CLD7                                       | MII1_RXCLK | EMI_A7  | UART5_RX  |
| PL_GPIO_89/F17          | PWM0  |                                 | ARM_TRACE_PKT[B][3] | OL          |           | GPIO_89                         | CLD8                                       | MII1_RXDV  | EMI_A8  | UART6_TX  |
| PL_GPIO_88/F16          | PWM1  |                                 | ARM_TRACE_SYNCA     | OL          |           | GPIO_88                         | CLD9                                       | MII1_RXER  | EMI_A9  | UART6_RX  |
| PL_GPIO_87/G13          | PWM2  |                                 | ARM_TRACE_SYNCB     | OL          |           | GPIO_87                         | CLD10                                      | MII1_RXD0  | EMI_A10 | 0         |
| PL_GPIO_86/E17          | PWM3  |                                 | ARM_PIPESTATA[0]    | OL          |           | GPIO_86                         | CLD11                                      | MII1_RXD1  | EMI_A11 | 0         |
| PL_GPIO_85/F15          | UART1_CTS                                   |                                 | ARM_PIPESTATA[1]    | OL          |           | GPIO_85                         | CLD12                                      | MII1_RXD2  | EMI_A12 | SPP_DATA0 |
| PL_GPIO_84/D17          | UART1_DTR                                   |                                 | ARM_PIPESTATA[2]    | OL          |           | GPIO_84                         | CLD13                                      | MII1_RXD3  | EMI_A13 | SPP_DATA1 |
| PL_GPIO_83/E16          | UART1_RI                                    |                                 | ARM_PIPESTATB[0]    | OL          |           | GPIO_83                         | CLD14                                      | MII1_COL   | EMI_A14 | SPP_DATA2 |
| PL_GPIO_82/E15          | UART1_DCD                                   |                                 | ARM_PIPESTATB[1]    | OL          |           | GPIO_82                         | CLD15                                      | MII1_CRS   | EMI_A15 | SPP_DATA3 |
| PL_GPIO_81/C17          | UART1_DSR                                   |                                 | ARM_PIPESTATB[2]    | OL          |           | GPIO_81                         | CLD16                                      | MII1_MDIO  | EMI_A16 | SPP_DATA4 |
| PL_GPIO_80/D16          | UART1_RTS                                   |                                 | ARM_TRACE_PKT[A][4] | OL          |           | GPIO_80                         | CLD17                                      | MII1_MDC   | EMI_A17 | SPP_DATA5 |
| PL_GPIO_79/F14          | UART_RS485_TX                               |                                 | ARM_TRACE_PKT[A][5] | OL          |           | GPIO_79                         | CLD18                                      | 0          | EMI_A18 | SPP_DATA6 |
| PL_GPIO_78/D15          | UART_RS485_RX                               |                                 | ARM_TRACE_PKT[A][6] | OL          |           | GPIO_78                         | CLD19                                      | 0          | EMI_A19 | SPP_DATA7 |
| PL_GPIO_77/B17          | UART_RS485_OE                               |                                 | ARM_TRACE_PKT[A][7] | OL          |           | GPIO_77                         | CLD20                                      | 0          | EMI_A20 | SPP_STRBn |
| PL_GPIO_76/F13          | I2C2_SDA                                    |                                 | ARM_TRACE_PKT[B][4] | OL          |           | GPIO_76                         | CLD21                                      | 0          | EMI_A21 | SPP_ACKn  |
| PL_GPIO_75/E14          | I2C2_SCL                                    |                                 | ARM_TRACE_PKT[B][5] | OL          |           | GPIO_75                         | CLD22                                      | 0          | EMI_A22 | SPP_BUSY  |



**Table 15. PL\_GPIO/PL\_CLK multiplexing scheme and reset states (continued)**

| PL_GPIO_# / ball number | Extended mode primary function (SW defined) | Alternate function (SW defined) | Full debug mode   | Reset state | Boot pins | Function in GPIO alternate mode | Legacy configuration mode (SW defined)     |               |                   |               |
|-------------------------|---|---------------------------------|-------------------|-------------|-----------|---------------------------------|--|---------------|-------------------|---------------|
|                         |   |                                 |                   |             |           |                                 | Mode 1 (Default configuration after reset) | Mode 2        | Mode 3            | Mode 4        |
| PL_GPIO_74/C16          | UART3_TX                                    |                                 | ARM_TRACE_PKT[B]6 | OL          |           | GPIO_74                         | CLD23                                      | 0             | EMI_A23           | SPP_PERROR    |
| PL_GPIO_73/A17          | UART3_RX                                    |                                 | ARM_TRACE_PKT[B]7 | OL          |           | GPIO_73                         | CLAC                                       | 0             | EMI_D8/ FSMC_D8   | SPP_SELECT    |
| PL_GPIO_72/B16          | UART4_TX                                    |                                 | Functional mode   | OL          |           | GPIO_72                         | CLFP                                       | 0             | EMI_D9/ FSMC_D9   | SPP_AUTOFDn   |
| PL_GPIO_71/D14          | UART4_RX                                    |                                 |                   | OL          |           | GPIO_71                         | CLLP                                       | 0             | EMI_D10/ FSMC_D10 | SPP_FAULTn    |
| PL_GPIO_70/C15          | UART5_TX                                    |                                 |                   | OL          |           | GPIO_70                         | CLLE                                       | 0             | EMI_D11/ FSMC_D11 | SPP_INITn     |
| PL_GPIO_69/A16          | UART5_RX                                    |                                 |                   | OL          |           | GPIO_69                         | CLPOWER                                    | 0             | EMI_WAIT          | SPP_SELINn    |
| PL_GPIO_68/B15          | SSP1_MOSI                                   |                                 |                   | IPU         |           | GPIO_68                         | FSMC_D0                                    | FSMC_D0       | EMI_D0/ FSMC_D0   | FSMC_D0       |
| PL_GPIO_67/C14          | SSP1_CLK                                    |                                 |                   | IPU         |           | GPIO_67                         | FSMC_D1                                    | FSMC_D1       | EMI_D1/ FSMC_D1   | FSMC_D1       |
| PL_GPIO_66/E13          | SSP1_SS0                                    |                                 |                   | IPU         |           | GPIO_66                         | FSMC_D2                                    | FSMC_D2       | EMI_D2/ FSMC_D2   | FSMC_D2       |
| PL_GPIO_65/B14          | SSP1_MISO                                   |                                 |                   | IPU         |           | GPIO_65                         | FSMC_D3                                    | FSMC_D3       | EMI_D3/ FSMC_D3   | FSMC_D3       |
| PL_GPIO_64/D13          | SSP2_MOSI                                   |                                 |                   | IPU         |           | GPIO_64                         | FSMC_D4                                    | FSMC_D4       | EMI_D4/ FSMC_D4   | FSMC_D4       |
| PL_GPIO_63/C13          | SSP2_CLK                                    |                                 |                   | IPU         |           | GPIO_63                         | FSMC_D5                                    | FSMC_D5       | EMI_D5/ FSMC_D5   | FSMC_D5       |
| PL_GPIO_62/A15          | SSP2_SS0                                    |                                 |                   | IPU         | H7        | GPIO_62                         | FSMC_D6                                    | FSMC_D6       | EMI_D6/ FSMC_D6   | FSMC_D6       |
| PL_GPIO_61/E12          | SSP2_MISO                                   |                                 |                   | IPU         | H6        | GPIO_61                         | FSMC_D7                                    | FSMC_D7       | EMI_D7/ FSMC_D7   | FSMC_D7       |
| PL_GPIO_60/A14          | PWM0  |                                 |                   | IPU         | H5        | GPIO_60                         | FSMC_ADDR_LE                               | FSMC_ADDR_LE  | FSMC_ADDR_LE      | FSMC_ADDR_LE  |
| PL_GPIO_59/B13          | PWM1  |                                 |                   | IPU         | H4        | GPIO_59                         | FSMC_WE                                    | FSMC_WE       | EMI_WE/ FSMC_WE   | FSMC_WE       |
| PL_GPIO_58/D12          | PWM2  |                                 |                   | IPU         | H3        | GPIO_58                         | FSMC_RE                                    | FSMC_RE       | EMI_OE/ FSMC_RE   | FSMC_RE       |
| PL_GPIO_57/E11          | PWM3  |                                 |                   | IPU         | H2        | GPIO_57                         | FSMC_CMD_LE                                | FSMC_CMD_LE   | FSMC_CMD_LE       | FSMC_CMD_LE   |
| PL_GPIO_56/C12          |   |                                 |                   | IPU         | H1        | GPIO_56                         | FSMC_RDY /BSY                              | FSMC_RDY/ BSY | FSMC_RDY/BSY      | FSMC_RDY/ BSY |
| PL_GPIO_55/A13          |   |                                 |                   | IPU         | H0        | GPIO_55                         | FSMC_CS0                                   | FSMC_CS0      | EMI_CE0/ FSMC_CS0 | FSMC_CS0      |
| PL_GPIO_54/E10          |   |                                 |                   | IPU         | B3        | GPIO_54                         | FSMC_CS1                                   | FSMC_CS1      | EMI_CE1/ FSMC_CS1 | FSMC_CS1      |
| PL_GPIO_53/D11          | UART3_TX                                    |                                 |                   | IPU         | B2        | GPIO_53                         | FSMC_CS2                                   | FSMC_CS2      | EMI_CE2/ FSMC_CS2 | FSMC_CS2      |



Table 15. PL\_GPIO/PL\_CLK multiplexing scheme and reset states (continued)

| PL_GPIO_# / ball number | Extended mode primary function (SW defined) | Alternate function (SW defined) | Full debug mode | Reset state | Boot pins | Function in GPIO alternate mode | Legacy configuration mode (SW defined)     |                     |                   |           |
|-------------------------|---|---------------------------------|-----------------|-------------|-----------|---------------------------------|--|---------------------|-------------------|-----------|
|                         |   |                                 |                 |             |           |                                 | Mode 1 (Default configuration after reset) | Mode 2              | Mode 3            | Mode 4    |
| PL_GPIO_52/B12          | UART3_RX                                    |                                 | Functional mode | IPU         | B1        | GPIO_52                         | FSMC_CS3                                   | FSMC_CS3            | EMI_CE_3/FSMC_CS3 | FSMC_CS3  |
| PL_GPIO_51/D10          | SSP1_MOSI                                   |                                 |                 | IPU         | B0        | GPIO_51                         | SD_CD                                      | SD_CD               | EMI_BYTEN0        | SD_CD     |
| PL_GPIO_50/A12          | SSP1_CLK                                    | TMR_CPTR4                       |                 | IPU         |           | GPIO_50                         | SD_DAT7                                    | SD_DAT7             | EMI_BYTEN1        | SD_DAT7   |
| PL_GPIO_49/C11          | SSP1_SS0                                    | TMR_CPTR3                       |                 | IPU         |           | GPIO_49                         | SD_DAT6                                    | SD_DAT6             | EMI_D12/FSMC_D12  | SD_DAT6   |
| PL_GPIO_48/B11          | SSP1_MISO                                   | TMR_CPTR2                       |                 | IPU         |           | GPIO_48                         | SD_DAT5                                    | SD_DAT5             | EMI_D13/FSMC_D13  | SD_DAT5   |
| PL_GPIO_47/C10          | SSP2_MOSI                                   | TMR_CPTR1                       |                 | IPU         |           | GPIO_47                         | SD_DAT4                                    | SD_DAT4             | EMI_D14/FSMC_D14  | SD_DAT4   |
| PL_GPIO_46/A11          | SSP2_CLK                                    | TMR_CLK4                        |                 | OL          |           | GPIO_46                         | SD_DAT3                                    | SD_DAT3             | EMI_D15/FSMC_D15  | SD_DAT3   |
| PL_GPIO_45/B10          | SSP2_SS0                                    | TMR_CLK3                        |                 | OL          |           | GPIO_45                         | SD_DAT2                                    | SD_DAT2             | UART1_DCD         | SD_DAT2   |
| PL_GPIO_44/A10          | SSP2_MISO                                   | TMR_CLK2                        |                 | OL          |           | GPIO_44                         | SD_DAT1                                    | SD_DAT1             | UART1_DSR         | SD_DAT1   |
| PL_GPIO_43/E9           | PWM0  | TMR_CLK1                        |                 | OL          |           | GPIO_43                         | SD_DAT0                                    | SD_DAT0             | UART1_RTS         | SD_DAT0   |
| PL_GPIO_42/D9           | PWM1  | UART0_DTR                       |                 | OH          |           | GPIO_42                         | I2S_RX                                     | I2S_RX              | UART3_TX          | 0         |
| PL_GPIO_41/C9           | PWM2  | UART0_RI                        |                 | IPD         |           | GPIO_41                         | I2S_TX                                     | I2S_TX              | UART3_RX          | 0         |
| PL_GPIO_40/B9           | PWM3  | UART0_DSR                       |                 | IPD         |           | GPIO_40                         | I2S_LR                                     | I2S_LR              | UART4_TX          | 0         |
| PL_GPIO_39/A9           | SSP1_MOSI                                   | UART0_DCD                       |                 | IPD         |           | GPIO_39                         | I2S_CLK                                    | I2S_CLK             | UART4_RX          | 0         |
| PL_GPIO_38/A8           | SSP1_CLK                                    | UART0_CTS                       |                 | IPD         |           | GPIO_38                         | PWM0                                       | PWM0                | UART5_TX          | 0         |
| PL_GPIO_37/B8           | SSP1_SS0                                    | UART0_RTS                       |                 | OH          |           | GPIO_37                         | PWM1                                       | PWM1                | UART5_RX          | 0         |
| PL_GPIO_36/C8           | SSP1_MISO                                   | SSP0_CS4                        |                 | OH          |           | GPIO_36                         | TOUCHSCREEN X                              | 0                   | UART1_CTS         | UART1_CTS |
| PL_GPIO_35/D8           | SSP2_MOSI                                   | SSP0_CS3                        |                 | OH          |           | GPIO_35                         | audio_over_samp_clk                        | audio_over_samp_clk | UART1_DTR         | UART1_DTR |
| PL_GPIO_34/E8           | SSP2_CLK                                    | SSP0_CS2                        |                 | OH          |           | GPIO_34                         | SD_LED / PWM2                              | SD_LED / PWM2       | UART1_RI          | UART1_RI  |
| PL_GPIO_33/E7           | SSP2_SS0                                    | basGPIO5                        |                 | IPU         |           | GPIO_33                         | CAN0_TX                                    | CAN0_TX             | CAN0_TX           | UART1_DCD |
| PL_GPIO_32/D7           | SSP2_MISO                                   | basGPIO4                        |                 | IPU         |           | GPIO_32                         | CAN0_RX                                    | CAN0_RX             | CAN0_RX           | UART1_DSR |
| PL_GPIO_31/C7           | PWM0  | basGPIO3                        |                 | IPU         |           | GPIO_31                         | CAN1_TX                                    | CAN1_TX             | CAN1_TX           | UART1_RTS |
| PL_GPIO_30/B7           | PWM1  | basGPIO2                        |                 | IPU         |           | GPIO_30                         | CAN1_RX                                    | CAN1_RX             | CAN1_RX           | 0         |



**Table 15. PL\_GPIO/PL\_CLK multiplexing scheme and reset states (continued)**

| PL_GPIO_# / ball number | Extended mode primary function (SW defined) | Alternate function (SW defined) | Full debug mode | Reset state | Boot pins | Function in GPIO alternate mode | Legacy configuration mode (SW defined)     |          |          |           |
|-------------------------|---|---------------------------------|-----------------|-------------|-----------|---------------------------------|--|----------|----------|-----------|
|                         |   |                                 |                 |             |           |                                 | Mode 1 (Default configuration after reset) | Mode 2   | Mode 3   | Mode 4    |
| PL_GPIO_29/A7           | PWM2  | basGPIO1                        | Functional mode | IPU         |           | GPIO_29                         | UART1_TX                                   | UART1_TX | UART1_TX | UART1_TX  |
| PL_GPIO_28/A6           | PWM3  | basGPIO0                        |                 | IPU         |           | GPIO_28                         | UART1_RX                                   | UART1_RX | UART1_RX | UART1_RX  |
| PL_GPIO_27/B6           | RMII0_TXD0                                  | MII0_TXCLK                      |                 | IPU         |           | GPIO_27                         | Reserved                                   | 0        | Reserved | Reserved  |
| PL_GPIO_26/A5           | RMII0_RXD0                                  | MII0_TXD0                       |                 | OL          |           | GPIO_26                         | Reserved                                   | 0        | Reserved | Reserved  |
| PL_GPIO_25/C6           | RMII1_TXD0                                  | MII0_TXD1                       |                 | OL          |           | GPIO_25                         | Reserved                                   | 0        | 0        | Reserved  |
| PL_GPIO_24/B5           | RMII1_RXD0                                  | MII0_TXD2                       |                 | OL          |           | GPIO_24                         | Reserved                                   | 0        | 0        | Reserved  |
| PL_GPIO_23/A4           | RMII1_TX_EN                                 | MII0_TXD3                       |                 | OL          |           | GPIO_23                         | Reserved                                   | 0        | Reserved | Reserved  |
| PL_GPIO_22/D6           | RMII_REF_CLK                                | MII0_TXEN                       |                 | OL          |           | GPIO_22                         | Reserved                                   | 0        | Reserved | Reserved  |
| PL_GPIO_21/C5           | RMII1_TXD1                                  | MII0_TXER                       |                 | OL          |           | GPIO_21                         | Reserved                                   | 0        | Reserved | Reserved  |
| PL_GPIO_20/B4           | RMII1_RXD1                                  | MII0_RXCLK                      |                 | IPU         |           | GPIO_20                         | SSP1_MOSI                                  | I2C2_SDA | 0        | SSP1_MOSI |
| PL_GPIO_19/A3           | RMII1_CRS_DV                                | MII0_RXDV                       |                 | IPU         |           | GPIO_19                         | SSP1_CLK                                   | I2C2_SCL | 0        | SSP1_CLK  |
| PL_GPIO_18/D5           | RMII1_RX_ER                                 | MII0_RXER                       |                 | IPU         |           | GPIO_18                         | SSP1_SS0                                   | 0        | 0        | SSP1_SS0  |
| PL_GPIO_17/C4           | RMII0_TXD1                                  | MII0_RXD0                       |                 | IPU         |           | GPIO_17                         | SSP1_MISO                                  | 0        | 0        | SSP1_MISO |
| PL_GPIO_16/E6           | RMII0_TX_EN                                 | MII0_RXD1                       |                 | IPU         |           | GPIO_16                         | SSP2_MOSI                                  | UART3_TX | 0        | 0         |
| PL_GPIO_15/B3           | RMII0_RXD1                                  | MII0_RXD2                       |                 | IPU         |           | GPIO_15                         | SSP2_CLK                                   | UART3_RX | PWM0     | PWM0      |
| PL_GPIO_14/A2           | RMII0_CRS_DV                                | MII0_RXD3                       |                 | IPU         |           | GPIO_14                         | SSP2_SS0                                   | UART4_TX | PWM1     | PWM1      |
| PL_GPIO_13/A1           | RMII0_RX_ER                                 | MII0_COL                        |                 | IPU         |           | GPIO_13                         | SSP2_MISO                                  | UART4_RX | PWM2     | PWM2      |
| PL_GPIO_12/D4           | SD_CD                                       | MII0_CRS                        |                 | IPU         |           | GPIO_12                         | PWM3                                       | 0        | PWM3     | PWM3      |
| PL_GPIO_11/E5           | RMII_MDC                                    | MII0_MDC                        |                 | OL          |           | GPIO_11                         | Reserved                                   | 0        | Reserved | Reserved  |
| PL_GPIO_10/C3           | RMII_MDIO                                   | MII0_MDIO                       |                 | IPD         |           | GPIO_10                         | Reserved                                   | 0        | Reserved | Reserved  |
| PL_GPIO_9/B2            | I2C1_SDA                                    | SSP0_MOSI                       |                 | IPU         |           | GPIO_9                          | 0  | UART3_TX | PWM0     | 0         |
| PL_GPIO_8/C2            | I2C1_SCL                                    | SSP0_CLK                        |                 | OL          |           | GPIO_8                          | 0  | UART3_RX | PWM1     | 0         |
| PL_GPIO_7/D3            | UART1_CTS                                   | SSP0_SS0                        |                 | OH          |           | GPIO_7                          | 0  | UART4_TX | PWM2     | 0         |
| PL_GPIO_6/B1            | UART1_DTR                                   | SSP0_MISO                       |                 | IPU         |           | GPIO_6                          | 0  | UART4_RX | PWM3     | 0         |

Table 15. PL\_GPIO/PL\_CLK multiplexing scheme and reset states (continued)

| PL_GPIO_# / ball number | Extended mode primary function (SW defined) | Alternate function (SW defined) | Full debug mode | Reset state | Boot pins | Function in GPIO alternate mode | Legacy configuration mode (SW defined)     |          |          |          |
|-------------------------|---|---------------------------------|-----------------|-------------|-----------|---------------------------------|--|----------|----------|----------|
|                         |   |                                 |                 |             |           |                                 | Mode 1 (Default configuration after reset) | Mode 2   | Mode 3   | Mode 4   |
| PL_GPIO_5/D2            | UART1_RI                                    | I2C0_SDA                        | Functional mode | IPU         |           | GPIO_5                          | 0  | UART5_TX | 0        | 0        |
| PL_GPIO_4/C1            | UART1_DCD                                   | I2C0_SCL                        |                 | IPU         |           | GPIO_4                          | 0  | UART5_RX | 0        | 0        |
| PL_GPIO_3/D1            | UART1_DSR                                   | UART0_RX                        |                 | IPD         |           | GPIO_3                          | I2C2_SDA                                   | UART6_TX | 0        | 0        |
| PL_GPIO_2/E4            | UART1_RTS                                   | UART0_TX                        |                 | OH          |           | GPIO_2                          | I2C2_SCL                                   | UART6_RX | 0        | 0        |
| PL_GPIO_1/E3            | I2C2_SDA                                    | IrDA_RX                         |                 | IPU         |           | GPIO_1                          | UART2_TX                                   | UART2_TX | UART2_TX | UART2_TX |
| PL_GPIO_0/F3            | I2C2_SCL                                    | IrDA_TX                         |                 | OL          |           | GPIO_0                          | UART2_RX                                   | UART2_RX | UART2_RX | UART2_RX |
| PL_CLK1/K17             | UART3_TX                                    | PL_CLK1                         |                 | OL          |           | GPIO_98                         | CLCP                                       | 0        | I2C1_SDA | SD_LED   |
| PL_CLK2/J17             | UART3_RX                                    | PL_CLK2                         |                 | OL          |           | GPIO_99                         | SD_CLK                                     | SD_CLK   | I2C1_SCL | SD_CLK   |
| PL_CLK3/J16             | UART4_TX                                    | PL_CLK3                         |                 | IPU         |           | GPIO_100                        | SD_WP                                      | SD_WP    | 0        | SD_WP    |
| PL_CLK4/H17             | UART4_RX                                    | PL_CLK4                         | IPU             |             | GPIO_101  | SD_CMD                          | SD_CMD                                     | 0        | SD_CMD   |          |

- Note:
- 1 [Table 15](#) cells filled with '0' or '1' are unused and unless otherwise configured as Alternate function or GPIO, the corresponding pin is held at low or high level respectively by the internal logic.
  - 2 Pins shared by EMI and FSMC: Depending on the AHB address to be accessed the pins are used for EMI or FSMC transfers.
  - 3 Reset state definition: the state of each pin during reset and after reset release. Device is in configuration mode 1 (default state) : OH= Output high level, OL output low level, IPU = input pull up, IPD = input pull down.
  - 4 Full debug mode: refer to [Table 32: Ball sharing during debug](#) for details on debug mode selection.
  - 5 Functional mode definition: in functional mode the I/O works as configured by the application (depending on settings for Configuration mode 1- 4/Extended mode/Alternate function).
  - 6 Refer to [Table 16: Table shading reference for Table 15 multiplexing scheme](#) for colors and shading used in [Table 15](#) cells to identify pin groups



**Table 16. Table shading reference for Table 15 multiplexing scheme**

| Shading        | Pin group                               |
|----------------|---|
| FSMC           | FSMC pins: NAND Flash                   |
| EMI            | EMI pins                                |
| CLCD           | Color LCD controller pins               |
| Touchscreen    | Touchscreen pins                        |
| UART           | UART pins                               |
| CAN            | CAN pins                                |
| Ethernet MAC   | MII/RMII Ethernet MAC pins              |
| SD/SDIO/MMC    | SD card controller pins                 |
| PWM generators | Pulse-width modulator timer module pins |
| GPT            | Timer pins                              |
| IrDa           | IrDa pins                               |
| SSP            | SSP pins                                |
| I2C            | I2C pins                                |
| SPP            | Standard parallel port pins             |
| I2S            | I2S pins                                |



### 3.4.8 Multiplexed signals description

This section provides a description of the multiplexed signals present in SPEAr320S device, grouped by IP.

**Table 17. FSMC signals description**

| Signal name  | Description                        | Dir.        | PL_GPIO_# /Ball | Configuration mode   |
|--------------|------------------------------------|-------------|-----------------|----------------------|
| FSMC_ADDR_LE | Address latch enable (active high) | O           | PL_GPIO_60/A14  | 1, 2, 3, 4, Extended |
| FSMC_CMD_LE  | Command latch enable (active high) | O           | PL_GPIO_57/E11  | 1, 2, 3, 4, Extended |
| FSMC_CS0     | Chip enable (active low)           | O           | PL_GPIO_55/A13  | 1, 2, 3, 4, Extended |
| FSMC_CS1     |                                    |             | PL_GPIO_54/E10  | 1, 2, 3, 4, Extended |
| FSMC_CS2     |                                    |             | PL_GPIO_53/D11  | 1, 2, 3, 4, Extended |
| FSMC_CS3     |                                    |             | PL_GPIO_52/B12  | 1, 2, 3, 4, Extended |
| FSMC_D0      | Data lines                         | IO          | PL_GPIO_68/B15  | 1, 2, 3, 4, Extended |
| FSMC_D1      |                                    |             | PL_GPIO_67/C14  | 1, 2, 3, 4, Extended |
| FSMC_D2      |                                    |             | PL_GPIO_66/E13  | 1, 2, 3, 4, Extended |
| FSMC_D3      |                                    |             | PL_GPIO_65/B14  | 1, 2, 3, 4, Extended |
| FSMC_D4      |                                    |             | PL_GPIO_64/D13  | 1, 2, 3, 4, Extended |
| FSMC_D5      |                                    |             | PL_GPIO_63/C13  | 1, 2, 3, 4, Extended |
| FSMC_D6      |                                    |             | PL_GPIO_62/A15  | 1, 2, 3, 4, Extended |
| FSMC_D7      |                                    |             | PL_GPIO_61/E12  | 1, 2, 3, 4, Extended |
| FSMC_D8      |                                    |             | PL_GPIO_73/A17  | 3, Extended          |
| FSMC_D9      |                                    |             | PL_GPIO_72/B16  | 3, Extended          |
| FSMC_D10     |                                    |             | PL_GPIO_71/D14  | 3, Extended          |
| FSMC_D11     |                                    |             | PL_GPIO_70/C15  | 3, Extended          |
| FSMC_D12     |                                    |             | PL_GPIO_49/C11  | 3, Extended          |
| FSMC_D13     |                                    |             | PL_GPIO_48/B11  | 3, Extended          |
| FSMC_D14     |                                    |             | PL_GPIO_47/C10  | 3, Extended          |
| FSMC_D15     | PL_GPIO_46/A11                     | 4, Extended |                 |                      |
| FSMC_RDY/BSY | Wait signal (active low)           | I           | PL_GPIO_56/C12  | 1, 2, 3, 4, Extended |
| FSMC_RE      | Read enable (active low)           | O           | PL_GPIO_58/D12  | 1, 2, 3, 4, Extended |
| FSMC_WE      | Write enable (active low)          | O           | PL_GPIO_59/B13  | 1, 2, 3, 4, Extended |

**Table 18. EMI signals description**

| Signal name | Description   | Dir.        | PL_GPIO_# /Ball | Configuration mode |
|-------------|---|-------------|-----------------|--------------------|
| EMI_A0      | Address bus   | O           | PL_GPIO_97/H16  | 3, Extended        |
| EMI_A1      |   |             | PL_GPIO_96/H15  | 3, Extended        |
| EMI_A2      |   |             | PL_GPIO_95/H14  | 3, Extended        |
| EMI_A3      |   |             | PL_GPIO_94/H13  | 3, Extended        |
| EMI_A4      |   |             | PL_GPIO_93/G17  | 3, Extended        |
| EMI_A5      |   |             | PL_GPIO_92/G16  | 3, Extended        |
| EMI_A6      |   |             | PL_GPIO_91/G15  | 3, Extended        |
| EMI_A7      |   |             | PL_GPIO_90/G14  | 3, Extended        |
| EMI_A8      |   |             | PL_GPIO_89/F17  | 3, Extended        |
| EMI_A9      |   |             | PL_GPIO_88/F16  | 3, Extended        |
| EMI_A10     |   |             | PL_GPIO_87/G13  | 3, Extended        |
| EMI_A11     |   |             | PL_GPIO_86/E17  | 3, Extended        |
| EMI_A12     |   |             | PL_GPIO_85/F15  | 3, Extended        |
| EMI_A13     |   |             | PL_GPIO_84/D17  | 3, Extended        |
| EMI_A14     |   |             | PL_GPIO_83/E16  | 3, Extended        |
| EMI_A15     |   |             | PL_GPIO_82/E15  | 3, Extended        |
| EMI_A16     |   |             | PL_GPIO_81/C17  | 3, Extended        |
| EMI_A17     |   |             | PL_GPIO_80/D16  | 3, Extended        |
| EMI_A18     |   |             | PL_GPIO_79/F14  | 3, Extended        |
| EMI_A19     |   |             | PL_GPIO_78/D15  | 3, Extended        |
| EMI_A20     |   |             | PL_GPIO_77/B17  | 3, Extended        |
| EMI_A21     |   |             | PL_GPIO_76/F13  | 3, Extended        |
| EMI_A22     |   |             | PL_GPIO_75/E14  | 3, Extended        |
| EMI_A23     | PL_GPIO_74/C16  | 3, Extended |                 |                    |
| EMI_BYTEN0  | Byte_enables are provided to validate the data present on the bus when high data is valid.        | IO          | PL_GPIO_51/D10  | 3, Extended        |
| EMI_BYTEN1  |   |             | PL_GPIO_50/A12  | 3, Extended        |
| EMI_CE0     | EMI Chip selects, derived from internal address decoding (kept disabled during NAND_Flash cycles) | O           | PL_GPIO_55/A13  | 3, Extended        |
| EMI_CE1     |   |             | PL_GPIO_54/E10  | 3, Extended        |
| EMI_CE2     |   |             | PL_GPIO_53/D11  | 3, Extended        |
| EMI_CE3     |   |             | PL_GPIO_52/B12  | 3, Extended        |

Table 18. EMI signals description (continued)

| Signal name | Description  | Dir. | PL_GPIO_# /Ball | Configuration mode |
|-------------|--|------|-----------------|--------------------|
| EMI_D0      | Data bus   | O    | PL_GPIO_68/B15  | 3, Extended        |
| EMI_D1      |  |      | PL_GPIO_67/C14  | 3, Extended        |
| EMI_D2      |  |      | PL_GPIO_66/E13  | 3, Extended        |
| EMI_D3      |  |      | PL_GPIO_65/B14  | 3, Extended        |
| EMI_D4      |  |      | PL_GPIO_64/D13  | 3, Extended        |
| EMI_D5      |  |      | PL_GPIO_63/C13  | 3, Extended        |
| EMI_D6      |  |      | PL_GPIO_62/A15  | 3, Extended        |
| EMI_D7      |  |      | PL_GPIO_61/E12  | 3, Extended        |
| EMI_D8      |  |      | PL_GPIO_73/A17  | 3, Extended        |
| EMI_D9      |  |      | PL_GPIO_72/B16  | 3, Extended        |
| EMI_D10     |  |      | PL_GPIO_71/D14  | 3, Extended        |
| EMI_D11     |  |      | PL_GPIO_70/C15  | 3, Extended        |
| EMI_D12     |  |      | PL_GPIO_49/C11  | 3, Extended        |
| EMI_D13     |  |      | PL_GPIO_48/B11  | 3, Extended        |
| EMI_D14     |  |      | PL_GPIO_47/C10  | 3, Extended        |
| EMI_D15     |  |      | PL_GPIO_46/A11  | 3, Extended        |
| EMI_OE      | Data output enable for read cycles, target device must open its data bus with this signal.   | O    | PL_GPIO_58/D12  | 3, Extended        |
| EMI_WAIT    | Transfer acknowledge signal, used by the cycle target to slow down the cycle (must be pulled up on the bus for targets that do not need it).<br><i>Note: This is an optional signal.</i> | I    | PL_GPIO_69/A16  | 3, Extended        |
| EMI_WE      | Write strobe, data are ready on EMI_ADB before its falling edge and after the rising edge.   | O    | PL_GPIO_59/B13  | 3, Extended        |

Table 19. CLCD signals description

| Signal name | Description  | Dir. | PL_GPIO_# /Ball | Configuration mode |
|-------------|--|------|-----------------|--------------------|
| CLAC        | STN AC bias drive or TFT data enable output                              | O    | PL_GPIO_73/A17  | 1, Extended        |
| CLCP        | LCD panel clock  | O    | PL_CLK1/K17     | 1, Extended        |
| CLD0        | LCD panel data   | O    | PL_GPIO_97/H16  | 1, Extended        |
| CLD1        |  |      | PL_GPIO_96/H15  |                    |
| CLD2        |  |      | PL_GPIO_95/H14  |                    |
| CLD3        |  |      | PL_GPIO_94/H13  |                    |
| CLD4        |  |      | PL_GPIO_93/G17  |                    |
| CLD5        |  |      | PL_GPIO_92/G16  |                    |
| CLD6        |  |      | PL_GPIO_91/G15  |                    |
| CLD7        |  |      | PL_GPIO_90/G14  |                    |
| CLD8        |  |      | PL_GPIO_89/F17  |                    |
| CLD9        |  |      | PL_GPIO_88/F16  |                    |
| CLD10       |  |      | PL_GPIO_87/G13  |                    |
| CLD11       |  |      | PL_GPIO_86/E17  |                    |
| CLD12       |  |      | PL_GPIO_85/F15  |                    |
| CLD13       |  |      | PL_GPIO_84/D17  |                    |
| CLD14       |  |      | PL_GPIO_83/E16  |                    |
| CLD15       |  |      | PL_GPIO_82/E15  |                    |
| CLD16       |  |      | PL_GPIO_81/C17  |                    |
| CLD17       |  |      | PL_GPIO_80/D16  |                    |
| CLD18       |  |      | PL_GPIO_79/F14  |                    |
| CLD19       |  |      | PL_GPIO_78/D15  |                    |
| CLD20       |  |      | PL_GPIO_77/B17  |                    |
| CLD21       |  |      | PL_GPIO_76/F13  |                    |
| CLD22       |  |      | PL_GPIO_75/E14  |                    |
| CLD23       |  |      | PL_GPIO_74/C16  |                    |
| CLFP        | Frame pulse (STN)/ vertical synchronization pulse (TFT)                  | O    | PL_GPIO_72/B16  | 1, Extended        |
| CLLE        | Line end signal  | O    | PL_GPIO_70/C15  | 1, Extended        |
| CLLP        | Line synchronization pulse (STN)/ horizontal synchronization pulse (TFT) | O    | PL_GPIO_71/D14  | 1, Extended        |
| CLPOWER     | LCD panel power enable   | O    | PL_GPIO_69/A16  | 1, Extended        |

**Table 20. Touchscreen signal description**

| Signal name   | Description               | Dir. | PL_GPIO_# /Ball | Configuration mode |
|---------------|---------------------------|------|-----------------|--------------------|
| TOUCHSCREEN X | Touchscreen select signal | O    | PL_GPIO_36/C8   | 1, Extended        |

**Table 21. UART signals description**

| Signal name  | Description                                   | Dir. | PL_GPIO_# /Ball | Configuration mode |
|--------------|---|------|-----------------|--------------------|
| <b>UART0</b> |   |      |                 |                    |
| UART0_CTS    | UART0 clear to send modem status input        | I    | PL_GPIO_38/A8   | Alternate function |
| UART0_DCD    | UART0 data carrier detect modem status input  | I    | PL_GPIO_39/A9   | Alternate function |
| UART0_DSR    | UART0 data set ready modem status input       | I    | PL_GPIO_40/B9   | Alternate function |
| UART0_DTR    | UART0 data terminal ready modem status output | O    | PL_GPIO_42/D9   | Alternate function |
| UART0_RI     | UART0 ring indicator modem status input       | I    | PL_GPIO_41/C9   | Alternate function |
| UART0_RTS    | UART0 request to send modem status output     | O    | PL_GPIO_37/B8   | Alternate function |
| UART0_RX     | UART0 received serial data input              | I    | PL_GPIO_3/D1    | Alternate function |
| UART0_TX     | UART0 transmitted serial data output          | O    | PL_GPIO_2/E4    | Alternate function |
| <b>UART1</b> |   |      |                 |                    |
| UART1_CTS    | UART1 clear to send modem status input        | I    | PL_GPIO_36/C8   | 3, 4, Extended     |
|              |   |      | PL_GPIO_85/F15  | Extended mode      |
|              |   |      | PL_GPIO_7/D3    |                    |
| UART1_DCD    | UART1 data carrier detect modem status input  | I    | PL_GPIO_45/B10  | 3, Extended        |
|              |   |      | PL_GPIO_33/E7   | 4, Extended        |
|              |   |      | PL_GPIO_4/C1    | Extended mode      |
|              |   |      | PL_GPIO_82/E15  |                    |
| UART1_DSR    | UART1 data set ready modem status input       | I    | PL_GPIO_44/A10  | 3, Extended        |
|              |   |      | PL_GPIO_32/D7   | 4, Extended        |
|              |   |      | PL_GPIO_3/D1    | Extended mode      |
|              |   |      | PL_GPIO_81/C17  |                    |
| UART1_DTR    | UART1 data terminal ready modem status output | O    | PL_GPIO_35/D8   | 3, 4, Extended     |
|              |   |      | PL_GPIO_84/D17  | Extended mode      |
|              |   |      | PL_GPIO_6/B1    |                    |
| UART1_RI     | UART1 ring indicator modem status input       | I    | PL_GPIO_34/E8   | 3, 4, Extended     |
|              |   |      | PL_GPIO_83/E16  | Extended mode      |
|              |   |      | PL_GPIO_5/D2    |                    |

**Table 21. UART signals description (continued)**

| Signal name  | Description                               | Dir. | PL_GPIO_# /Ball | Configuration mode   |
|--------------|---|------|-----------------|----------------------|
| UART1_RTS    | UART1 request to send modem status output | O    | PL_GPIO_43/E9   | 3, Extended          |
|              |   |      | PL_GPIO_31/C7   | 4, Extended          |
|              |   |      | PL_GPIO_80/D16  | Extended mode        |
|              |   |      | PL_GPIO_2/E4    |                      |
| UART1_RX     | UART1 received serial data input          | I    | PL_GPIO_28/A6   | 1, 2, 3, 4, Extended |
| UART1_TX     | UART1 transmitted serial data output      | O    | PL_GPIO_29/A7   | 1, 2, 3, 4, Extended |
| <b>UART2</b> |   |      |                 |                      |
| UART2_RX     | UART2 received serial data input          | I    | PL_GPIO_0/F3    | 1, 2, 3, 4, Extended |
| UART2_TX     | UART2 transmitted serial data output      | O    | PL_GPIO_1/E3    | 1, 2, 3, 4, Extended |
| <b>UART3</b> |   |      |                 |                      |
| UART3_RX     | UART3 received serial data input          | I    | PL_GPIO_15/B3   | 2, Extended          |
|              |   |      | PL_GPIO_8/C2    |                      |
|              |   |      | PL_GPIO_41/C9   | 3, Extended          |
|              |   |      | PL_GPIO_94/H13  | 4, Extended          |
|              |   |      | PL_GPIO_73/A17  | Extended mode        |
|              |   |      | PL_GPIO_52/B12  |                      |
| PL_CLK2/J17  |   |      |                 |                      |
| UART3_TX     | UART3 transmitted serial data output      | O    | PL_GPIO_16/E6   | 2, Extended          |
|              |   |      | PL_GPIO_9/B2    |                      |
|              |   |      | PL_GPIO_42/D9   | 3, Extended          |
|              |   |      | PL_GPIO_95/H14  | 4, Extended          |
|              |   |      | PL_GPIO_74/C16  | Extended mode        |
|              |   |      | PL_GPIO_53/D11  |                      |
| PL_CLK1/K17  |   |      |                 |                      |
| <b>UART4</b> |   |      |                 |                      |
| UART4_RX     | UART4 received serial data input          | I    | PL_GPIO_13/A1   | 2, Extended          |
|              |   |      | PL_GPIO_6/B1    |                      |
|              |   |      | PL_GPIO_39/A9   | 3, Extended          |
|              |   |      | PL_GPIO_92/G16  | 4, Extended          |
|              |   | I    | PL_GPIO_71/D14  | Extended mode        |
|              |   |      | PL_CLK4/H17     |                      |

**Table 21. UART signals description (continued)**

| Signal name       | Description                               | Dir. | PL_GPIO_# /Ball | Configuration mode |
|-------------------|---|------|-----------------|--------------------|
| UART4_TX          | UART4 transmitted serial data output      | O    | PL_GPIO_14/A2   | 2, Extended        |
|                   |   |      | PL_GPIO_7/D3    |                    |
|                   |   |      | PL_GPIO_40/B9   | 3, Extended        |
|                   |   |      | PL_GPIO_93/G17  | 4, Extended        |
|                   |   |      | PL_GPIO_72/B16  | Extended mode      |
| PL_CLK3/J16       |   |      |                 |                    |
| <b>UART5</b>      |   |      |                 |                    |
| UART5_RX          | UART5 received serial data input          | I    | PL_GPIO_4/C1    | 2, Extended        |
|                   |   |      | PL_GPIO_37/B8   | 3, Extended        |
|                   |   |      | PL_GPIO_90/G14  | 4, Extended        |
|                   |   |      | PL_GPIO_69/A16  | Extended mode      |
| UART5_TX          | UART5 transmitted serial data output      | O    | PL_GPIO_5/D2    | 2, Extended        |
|                   |   |      | PL_GPIO_38/A8   | 3, Extended        |
|                   |   |      | PL_GPIO_91/G15  | 4, Extended        |
|                   |   |      | PL_GPIO_70/C15  | Extended mode      |
| <b>UART6</b>      |   |      |                 |                    |
| UART6_RX          | UART6 received serial data input          | I    | PL_GPIO_2/E4    | 2, Extended        |
|                   |   |      | PL_GPIO_88/F16  | 4, Extended        |
| UART6_TX          | UART6 transmitted serial data output      | O    | PL_GPIO_3/D1    | 2, Extended        |
|                   |   |      | PL_GPIO_89/F17  | 4, Extended        |
| <b>UART/RS485</b> |   |      |                 |                    |
| UART_RS485_TX     | UART/RS485 transmitted serial data output | O    | PL_GPIO_79/F14  | Extended mode      |
| UART_RS485_RX     | UART/RS485 received serial data output    | I    | PL_GPIO_78/D15  | Extended mode      |
| UART_RS485_OE     | UART/RS485 data output enable             | O    | PL_GPIO_77/B17  | Extended mode      |

**Table 22. CAN signals description**

| Signal name | Description                  | Dir. | PL_GPIO_# /Ball | Configuration mode |
|-------------|------------------------------|------|-----------------|--------------------|
| <b>CAN0</b> |                              |      |                 |                    |
| CAN0_RX     | CAN0 receiver data input     | I    | PL_GPIO_32/D7   | 1, 2, 3, Extended  |
| CAN0_TX     | CAN0 transmitter data output | O    | PL_GPIO_33/E7   | 1, 2, 3, Extended  |
| <b>CAN1</b> |                              |      |                 |                    |
| CAN1_RX     | CAN1 receiver data input     | I    | PL_GPIO_30/B7   | 1, 2, 3, Extended  |
| CAN1_TX     | CAN1 transmitter data output | O    | PL_GPIO_31/C7   | 1, 2, 3, Extended  |

**Table 23. MMC-SD/SDIO controller signals description**

| Signal name | Description   | Dir. | PL_GPIO_# /Ball | Configuration mode |
|-------------|---|------|-----------------|--------------------|
| SD_CD       | Card detection for single slot (active low)                                   | I    | PL_GPIO_51/D10  | 1, 2, 4, Extended  |
|             |   |      | PL_GPIO_12/D4   | Extended mode      |
| SD_CLK      | Clock to external card  | O    | PL_CLK2/J17     | 1, 2, 4, Extended  |
| SD_CMD      | Command line  | IO   | PL_CLK4/H17     | 1, 2, 4, Extended  |
| SD_DAT0     | Data line   | IO   | PL_GPIO_43/E9   | 1, 2, 4, Extended  |
| SD_DAT1     |   |      | PL_GPIO_44/A10  | 1, 2, 4, Extended  |
| SD_DAT2     |   |      | PL_GPIO_45/B10  | 1, 2, 4, Extended  |
| SD_DAT3     |   |      | PL_GPIO_46/A11  | 1, 2, 4, Extended  |
| SD_DAT4     |   |      | PL_GPIO_47/C10  | 1, 2, 4, Extended  |
| SD_DAT5     |   |      | PL_GPIO_48/B11  | 1, 2, 4, Extended  |
| SD_DAT6     |   |      | PL_GPIO_49/C11  | 1, 2, 4, Extended  |
| SD_DAT7     |   |      | PL_GPIO_50/A12  | 1, 2, 4, Extended  |
| SD_LED      | Cautions the user not to remove the card while the SD card is being accessed. | O    | PL_GPIO_34/E8   | 1, 2, Extended     |
|             |   |      | PL_CLK1/K17     | 4, Extended        |
| SD_WP       | SD card write protect (active low)  | I    | PL_CLK3/J16     | 1, 2, 4, Extended  |

**Table 24. PWM signals description**

| Signal name | Description         | Dir. | PL_GPIO_# /Ball | Configuration mode |
|-------------|---------------------|------|-----------------|--------------------|
| PWM0        | PWM0 output channel | O    | PL_GPIO_38/A8   | 1, 2, Extended     |
|             |                     |      | PL_GPIO_15/B3   | 3, 4, Extended     |
|             |                     |      | PL_GPIO_9/B2    | 3, Extended        |
|             |                     |      | PL_GPIO_89/F17  | Extended mode      |
|             |                     |      | PL_GPIO_60/A14  |                    |
|             |                     |      | PL_GPIO_43/E9   |                    |
| PWM1        | PWM1 output channel | O    | PL_GPIO_37/B8   | 1, 2, Extended     |
|             |                     |      | PL_GPIO_14/A2   | 3, 4, Extended     |
|             |                     |      | PL_GPIO_8/C2    | 3, Extended        |
|             |                     |      | PL_GPIO_88/F16  | Extended mode      |
|             |                     |      | PL_GPIO_59/B13  |                    |
|             |                     |      | PL_GPIO_42/D9   |                    |
|             |                     |      | PL_GPIO_30/B7   |                    |



**Table 24. PWM signals description (continued)**

| Signal name | Description         | Dir. | PL_GPIO_# /Ball | Configuration mode |
|-------------|---------------------|------|-----------------|--------------------|
| PWM2        | PWM2 output channel | O    | PL_GPIO_34/E8   | 1, 2, Extended     |
|             |                     |      | PL_GPIO_13/A1   | 3, 4, Extended     |
|             |                     |      | PL_GPIO_7/D3    | 3, Extended        |
|             |                     |      | PL_GPIO_87/G13  | Extended mode      |
|             |                     |      | PL_GPIO_58/D12  |                    |
|             |                     |      | PL_GPIO_41/C9   |                    |
|             |                     |      | PL_GPIO_29/A7   |                    |
| PWM3        | PWM3 output channel | O    | PL_GPIO_12/D4   | 1, 3, 4, Extended  |
|             |                     |      | PL_GPIO_6/B1    | 3, Extended        |
|             |                     |      | PL_GPIO_86/E17  | Extended mode      |
|             |                     |      | PL_GPIO_57/E11  |                    |
|             |                     |      | PL_GPIO_40/B9   |                    |
|             |                     |      | PL_GPIO_28/A6   |                    |

**Table 25. GPT signals description**

| Signal name | Description  | Dir. | PL_GPIO_# /Ball | Configuration mode |
|-------------|--|------|-----------------|--------------------|
| TMR_CLK1    | This clock toggles each time the timer interrupt goes active.      | O    | PL_GPIO_43/E9   | Alternate function |
| TMR_CLK2    |  |      | PL_GPIO_44/A10  | Alternate function |
| TMR_CLK3    |  |      | PL_GPIO_45/B10  | Alternate function |
| TMR_CLK4    |  |      | PL_GPIO_46/A11  | Alternate function |
| TMR_CPTR1   | Asynchronous signal provided for the measurement of timing signals | I    | PL_GPIO_47/C10  | Alternate function |
| TMR_CPTR2   |  |      | PL_GPIO_48/B11  | Alternate function |
| TMR_CPTR3   |  |      | PL_GPIO_49/C11  | Alternate function |
| TMR_CPTR4   |  |      | PL_GPIO_50/A12  | Alternate function |

**Table 26. IrDA signals description**

| Signal name | Description                  | Dir. | PL_GPIO_# /Ball | Configuration mode |
|-------------|------------------------------|------|-----------------|--------------------|
| IrDA_RX     | IrDA receiver data input     | I    | PL_GPIO_1/E3    | Alternate function |
| IrDA_TX     | IrDA transmitter data output | O    | PL_GPIO_0/F3    | Alternate function |

Table 27. SSP signals description

| Signal name | Description  | Dir. | PL_GPIO_# /Ball | Configuration mode |
|-------------|--|------|-----------------|--------------------|
| <b>SSP0</b> |  |      |                 |                    |
| SSP0_CS2    | Slave select (used only in master mode)                                | O    | PL_GPIO_34/E8   | Alternate function |
| SSP0_CS3    | Slave select (used only in master mode)                                | O    | PL_GPIO_35/D8   | Alternate function |
| SSP0_CS4    | Slave select (used only in master mode)                                | O    | PL_GPIO_36/C8   | Alternate function |
| SSP0_CLK    | SSP clock. It is used as output in master mode as input in slave mode. | IO   | PL_GPIO_8/C2    | Alternate function |
| SSP0_MISO   | Master input slave output  | IO   | PL_GPIO_6/B1    | Alternate function |
| SSP0_MOSI   | Master output slave input  | IO   | PL_GPIO_9/B2    | Alternate function |
| SSP0_SS0    | SSP frame output (master mode), input (slave mode)                     | IO   | PL_GPIO_7/D3    | Alternate function |
| <b>SSP1</b> |  |      |                 |                    |
| SSP1_CLK    | SSP clock. It is used as output in master mode as input in slave mode. | IO   | PL_GPIO_19/A3   | 1, 4, Extended     |
|             |  |      | PL_GPIO_96/H15  | Extended mode      |
|             |  |      | PL_GPIO_67/C14  |                    |
|             |  |      | PL_GPIO_50/A12  |                    |
| SSP1_MISO   | Master input slave output  | IO   | PL_GPIO_17/C4   | 1, 4, Extended     |
|             |  |      | PL_GPIO_94/H13  | Extended mode      |
|             |  |      | PL_GPIO_65/B14  |                    |
|             |  |      | PL_GPIO_48/B11  |                    |
| SSP1_MOSI   | Master output slave input  | IO   | PL_GPIO_20/B4   | 1, 4, Extended     |
|             |  |      | PL_GPIO_97/H16  | Extended mode      |
|             |  |      | PL_GPIO_68/B15  |                    |
|             |  |      | PL_GPIO_51/D10  |                    |
| SSP1_SS0    | SSP frame output (master mode), input (slave mode)                     | IO   | PL_GPIO_18/D5   | 1, 4, Extended     |
|             |  |      | PL_GPIO_95/H14  | Extended mode      |
|             |  |      | PL_GPIO_66/E13  |                    |
|             |  |      | PL_GPIO_49/C11  |                    |
| <b>SSP2</b> |  |      |                 |                    |

Table 27. SSP signals description (continued)

| Signal name | Description  | Dir. | PL_GPIO_# /Ball | Configuration mode |
|-------------|--|------|-----------------|--------------------|
| SSP2_CLK    | SSP clock. It is used as output in master mode as input in slave mode. | IO   | PL_GPIO_15/B3   | 1, Extended        |
|             |  |      | PL_GPIO_92/G16  | Extended mode      |
|             |  |      | PL_GPIO_63/C13  |                    |
|             |  |      | PL_GPIO_46/A11  |                    |
|             |  |      | PL_GPIO_34/E8   |                    |
| SSP2_MISO   | Master input slave output  | IO   | PL_GPIO_13/A1   | 1, Extended        |
|             |  |      | PL_GPIO_90/G14  | Extended mode      |
|             |  |      | PL_GPIO_61/E12  |                    |
|             |  |      | PL_GPIO_44/A10  |                    |
|             |  |      | PL_GPIO_32/D7   |                    |
| SSP2_MOSI   | Master output slave input  | IO   | PL_GPIO_16/E6   | 1, Extended        |
|             |  |      | PL_GPIO_47/C10  | Extended mode      |
|             |  |      | PL_GPIO_35/D8   |                    |
|             |  |      | PL_GPIO_16/E6   |                    |
|             |  |      | PL_GPIO_93/G17  |                    |
|             |  |      | PL_GPIO_64/D13  |                    |
| SSP2_SS0    | SSP frame output (master mode), input (slave mode)                     | IO   | PL_GPIO_14/A2   | 1, Extended        |
|             |  |      | PL_GPIO_91/G15  | Extended mode      |
|             |  |      | PL_GPIO_62/A15  |                    |
|             |  |      | PL_GPIO_45/B10  |                    |
|             |  |      | PL_GPIO_33/E7   |                    |

Table 28. I2C signals description

| Signal name | Description             | Dir. | PL_GPIO_# /Ball | Configuration mode |
|-------------|-------------------------|------|-----------------|--------------------|
| <b>I2C0</b> |                         |      |                 |                    |
| I2C0_SCL    | I2C0 input/output clock | IO   | PL_GPIO_4/C1    | Alternate function |
| I2C0_SDA    | I2C0 input/output data  | IO   | PL_GPIO_5/D2    | Alternate function |
| <b>I2C1</b> |                         |      |                 |                    |
| I2C1_SCL    | I2C1 input/output clock | IO   | PL_CLK2/J17     | 3, Extended        |
|             |                         |      | PL_GPIO_8/C2    | Extended mode      |
| I2C1_SDA    | I2C1 input/output data  | IO   | PL_CLK1/K17     | 3, Extended        |
|             |                         |      | PL_GPIO_9/B2    | Extended mode      |
| <b>I2C2</b> |                         |      |                 |                    |
| I2C2_SCL    | I2C2 input/output clock | IO   | PL_GPIO_2/E4    | 1, Extended        |
|             |                         |      | PL_GPIO_19/A3   | 2, Extended        |
|             |                         |      | PL_GPIO_96/H15  | 4, Extended        |
|             |                         |      | PL_GPIO_75/E14  | Extended mode      |
|             |                         |      | PL_GPIO_0/F3    |                    |
| I2C2_SDA    | I2C2 input/output data  | IO   | PL_GPIO_3/D1    | 1, Extended        |
|             |                         |      | PL_GPIO_20/B4   | 2, Extended        |
|             |                         |      | PL_GPIO_97/H16  | 4, Extended        |
|             |                         |      | PL_GPIO_76/F13  | Extended mode      |
|             |                         |      | PL_GPIO_1/E3    |                    |

Table 29. I2S signals description

| Signal name         | Description   | Dir. | PL_GPIO_# /Ball | Configuration mode |
|---------------------|---|------|-----------------|--------------------|
| audio_over_samp_clk | Audio oversampling clock. This is the clock that I2S_CLK derives from. The interfacing digital-to-analog converter (DAC) can use this clock to (over)sample the I2S data. | O    | PL_GPIO_35/D8   | 1, 2, Extended     |
| I2S_CLK             | I2S clock   | O    | PL_GPIO_39/A9   | 1, 2, Extended     |
| I2S_LR              | I2S word select   | O    | PL_GPIO_40/B9   | 1, 2, Extended     |
| I2S_RX              | I2S receive data  | I    | PL_GPIO_42/D9   | 1, 2, Extended     |
| I2S_TX              | I2S transmit data   | O    | PL_GPIO_41/C9   | 1, 2, Extended     |

Table 30. SPP signals description

| Signal name | Description   | Dir. | PL_GPIO_# /Ball | Configuration mode |
|-------------|---|------|-----------------|--------------------|
| SPP_ACKn    | The peripheral pulses this line low when it has received the previous data and is ready to receive more data. The rising edge of SPP_ACKn can be enabled to interrupt the host. | O    | PL_GPIO_76/F13  | 4, Extended        |
| SPP_AUTOFDn | Usage of this line varies. Most printers will perform a line feed after each carriage return when this line is low, and carriage returns only when this line is high.           | I    | PL_GPIO_72/B16  | 4, Extended        |
| SPP_BUSY    | The peripheral drives this signal high to indicate that it is not ready to receive data.  | O    | PL_GPIO_75/E14  | 4, Extended        |
| SPP_DATA0   | SPP unidirectional data lines   | O    | PL_GPIO_85/F15  | 4, Extended        |
| SPP_DATA1   |   |      | PL_GPIO_84/D17  | 4, Extended        |
| SPP_DATA2   |   |      | PL_GPIO_83/E16  | 4, Extended        |
| SPP_DATA3   |   |      | PL_GPIO_82/E15  | 4, Extended        |
| SPP_DATA4   |   |      | PL_GPIO_81/C17  | 4, Extended        |
| SPP_DATA5   |   |      | PL_GPIO_80/D16  | 4, Extended        |
| SPP_DATA6   |   |      | PL_GPIO_79/F14  | 4, Extended        |
| SPP_DATA7   |   |      | PL_GPIO_78/D15  | 4, Extended        |
| SPP_FAULTn  | Usage of this line varies. Peripherals usually drive this line low when an error condition exists.  | O    | PL_GPIO_71/D14  | 4, Extended        |
| SPP_INITn   | This line is held low for a minimum of 50 $\mu$ s to reset the printer and clear the print buffer.  | I    | PL_GPIO_70/C15  | 4, Extended        |
| SPP_PERROR  | Usage of this line varies. Printers typically drive this signal high during a paper empty condition.  | O    | PL_GPIO_74/C16  | 4, Extended        |
| SPP_SELECT  | The peripheral drives this signal high when it is selected and ready for data transfer.   | O    | PL_GPIO_73/A17  | 4, Extended        |
| SPP_SELINn  | The host drives this line low to select the peripheral.   | I    | PL_GPIO_69/A16  | 4, Extended        |
| SPP_STRBn   | Data is valid during an active low pulse on this line.  | I    | PL_GPIO_77/B17  | 4, Extended        |

Table 31. Ethernet signals description

| Signal name | Description   | Dir. | PL_GPIO_# / ball number | Configuration mode (see <a href="#">Section 3.4.2</a> ) |
|-------------|---|------|-------------------------|---|
| <b>MII0</b> |   |      |                         |   |
| MII0_COL    | PHY collision<br>This signal is asserted by the PHY when a collision is detected on the medium. This signal is not synchronous to any clock. (Active high)  | I    | PL_GPIO_13/A1           | Alternate function                                      |
| MII0_CRS    | PHY CRS<br>This signal is asserted by the PHY when either the transmit or receive medium is not idle. The PHY deasserts this signal when both transmit and receive medium are idle. This signal is not synchronous to any clock. (Active high)  | I    | PL_GPIO_12/D4           | Alternate function                                      |
| MII0_MDC    | Management data clock<br>The MAC provides timing reference for the MAC_MDIO signal through this aperiodic clock. The maximum frequency of this clock is 2.5 MHz. This clock is generated from the application clock (HCLK) via a clock divider. | O    | PL_GPIO_11/E5           | Alternate function                                      |
| MII0_MDIO   | Management data input/output  | IO   | PL_GPIO_10/C3           | Alternate function                                      |
| MII0_RXCLK  | Reception clock<br>This is the reception clock (25/2.5 MHz in 100M/10Mbps) provided by the external PHY for MII interfaces. The MII0_RXDn signals that the Ethernet controller receives are synchronous to this clock.                          | I    | PL_GPIO_20/B4           | Alternate function                                      |
| MII0_RXD0   | PHY receive data<br>These bits provide the MII receive data nibble. The validity of the data is qualified with MII0_RXDV and MII0_RXER.   | I    | PL_GPIO_17/C4           | Alternate function                                      |
| MII0_RXD1   |   |      | PL_GPIO_16/E6           | Alternate function                                      |
| MII0_RXD2   |   |      | PL_GPIO_15/B3           | Alternate function                                      |
| MII0_RXD3   |   |      | PL_GPIO_14/A2           | Alternate function                                      |
| MII0_RXDV   | PHY receive data valid<br>When high, indicates that the data on the MII0_RXDn bus is valid. It remains asserted continuously from the first recovered byte/nibble of the frame through the final recovered byte/nibble.                         | I    | PL_GPIO_19/A3           | Alternate function                                      |
| MII0_RXER   | PHY receive error<br>When high, indicates an error or carrier extension in the received frame on the MII0_RXDn bus.   | I    | PL_GPIO_18/D5           | Alternate function                                      |

**Table 31. Ethernet signals description (continued)**

| Signal name | Description   | Dir.   | PL_GPIO_# / ball number | Configuration mode (see <a href="#">Section 3.4.2</a> ) |
|-------------|---|--|-------------------------|---|
| MII0_TXCLK  | Transmission clock<br>This is the transmission clock (25/2.5 MHz in 100 M/10 Mbps) provided by the external PHY for the MII interface. All the MII0_TXDn signals generated by the MAC are synchronous to this clock.  | I  | PL_GPIO_27/B6           | Alternate function                                      |
| MII0_TXD0   | PHY transmit data.  | O  | PL_GPIO_26/A5           | Alternate function                                      |
| MII0_TXD1   | These bits provide the MII transmit data nibble. The validity of the data is qualified with MII0_TXEN and MII0_TXER.  |  | PL_GPIO_25/C6           | Alternate function                                      |
| MII0_TXD2   |   |  | PL_GPIO_24/B5           | Alternate function                                      |
| MII0_TXD3   |   |  | PL_GPIO_23/A4           | Alternate function                                      |
| MII0_TXEN   |   | PHY transmit data enable<br>When high, it indicates that valid data is being transmitted on the MII0_TXDn bus. | O                       | PL_GPIO_22/D6   |
| MII0_TXER   | PHY transmit error<br>When high, indicates a transmit error or carrier extension on the MII0_TXDn bus.  | O  | PL_GPIO_21/C5           | Alternate function                                      |
| <b>MII1</b> |   |  |                         |   |
| MII1_COL    | PHY collision<br>This signal is asserted by the PHY when a collision is detected on the medium. This signal is not synchronous to any clock. (Active high)  | I  | PL_GPIO_83/E16          | 2, Extended   |
| MII1_CRS    | PHY CRS<br>This signal is asserted by the PHY when either the transmit or receive medium is not idle. The PHY deasserts this signal when both transmit and receive medium are idle. This signal is not synchronous to any clock. (Active high)                                  | I  | PL_GPIO_82/E15          | 2, Extended   |
| MII1_MDC    | Management data clock<br>The MAC provides timing reference for the MII1_MDIO signal through this aperiodic clock. The maximum frequency of this clock is 2.5 MHz. This clock is generated inside the Ethernet controller from the application clock (HCLK) via a clock divider. | O  | PL_GPIO_80/D16          | 2, Extended   |
| MII1_MDIO   | Management data input/output  | IO   | PL_GPIO_81/C17          | 2, Extended   |
| MII1_RXCLK  | This is the reception clock (25/2.5 MHz in 100M/10Mbps) provided by the external PHY for MII interfaces. All MII1_RXDn signals that the Ethernet controller receives are synchronous to this clock.   | I  | PL_GPIO_90/G14          | 2, Extended   |

Table 31. Ethernet signals description (continued)

| Signal name        | Description  | Dir. | PL_GPIO_# / ball number | Configuration mode (see Section 3.4.2) |
|--------------------|--|------|-------------------------|--|
| MII1_RXD0          | PHY receive data<br>These bits provide the MII receive data nibble. The validity of the data is qualified with MII1_RXDV and MII1_RXER.  | I    | PL_GPIO_87/G13          | 2, Extended                            |
| MII1_RXD1          |  |      | PL_GPIO_86/E17          | 2, Extended                            |
| MII1_RXD2          |  |      | PL_GPIO_85/F15          | 2, Extended                            |
| MII1_RXD3          |  |      | PL_GPIO_84/D17          | 2, Extended                            |
| MII1_RXDV          | PHY receive data valid<br>When high, indicates that the data on the MII1_RXDn bus is valid. It remains asserted continuously from the first recovered byte/nibble of the frame through the final recovered byte/nibble.                          | I    | PL_GPIO_89/F17          | 2, Extended                            |
| MII1_RXER          | PHY receive error<br>When high, indicates an error or carrier extension in the received frame on the MII1_RXDn bus.  | I    | PL_GPIO_88/F16          | 2, Extended                            |
| MII1_TXCLK         | Transmission clock<br>This is the transmission clock (25/2.5 MHz in 100M/10Mbps) provided by the external PHY for the MII. All the MII transmission signals generated by the MAC are synchronous to this clock.                                  | I    | PL_GPIO_97/H16          | 2, Extended                            |
| MII1_TXD0          | PHY transmit data.<br>These bits provide the MII transmit data nibble. The validity of the data is qualified with MII1_TXEN and MII1_TXER.   | O    | PL_GPIO_96/H15          | 2, Extended                            |
| MII1_TXD1          |  |      | PL_GPIO_95/H14          | 2, Extended                            |
| MII1_TXD2          |  |      | PL_GPIO_94/H13          | 2, Extended                            |
| MII1_TXD3          |  |      | PL_GPIO_93/G17          | 2, Extended                            |
| MII1_TXEN          | PHY transmit data enable<br>When high, indicates that valid data is being transmitted on the MII1_TXDn bus.  | O    | PL_GPIO_92/G16          | 2, Extended                            |
| MII1_TXER          | PHY transmit error<br>When high, indicates a transmit error or carrier extension on the MII1_TXDn bus.   | O    | PL_GPIO_91/G15          | 2, Extended                            |
| <b>RMII0/RMII1</b> |  |      |                         |  |
| RMII_MDC           | Management data clock<br>The MAC provides timing reference for the RMII_MDIO signal through this aperiodic clock. The maximum frequency of this clock is 2.5 MHz. This clock is generated from the application clock (HCLK) via a clock divider. | O    | PL_GPIO_11/E5           | Extended mode                          |
| RMII_MDIO          | Management data input/output   | IO   | PL_GPIO_10/C3           | Extended mode                          |
| RMII_REF_CLK       | 50 MHz reference clock input for RMII interface  | I    | PL_GPIO_22/D6           | Extended mode                          |



Table 31. Ethernet signals description (continued)

| Signal name  | Description   | Dir. | PL_GPIO_# / ball number | Configuration mode (see <a href="#">Section 3.4.2</a> ) |
|--------------|---|------|-------------------------|---|
| RMII0_CRS_DV | PHY receive data valid<br>Contains the CRS (carrier sense) and data valid information of the receive interface. | I    | PL_GPIO_14/A2           | Extended mode   |
| RMII0_RX_ER  | PHY receive error   | I    | PL_GPIO_13/A1           | Extended mode   |
| RMII0_RXD0   | PHY receive data  | I    | PL_GPIO_26/A5           | Extended mode   |
| RMII0_RXD1   | These bits provide the RMII receive data. The validity of the data is qualified with RMII0_CRS_DV.              |      | PL_GPIO_15/B3           | Extended mode   |
| RMII0_TX_EN  | PHY transmit data enable<br>When high, indicates that valid data is being transmitted on the RMII_TXDn bus      | O    | PL_GPIO_16/E6           | Extended mode   |
| RMII0_TXD0   | PHY transmit data   | O    | PL_GPIO_27/B6           | Extended mode   |
| RMII0_TXD1   | These bits provide the RMII transmit data. The validity of the data is qualified with RMII0_TX_EN.              |      | PL_GPIO_17/C4           | Extended mode   |
| RMII1_CRS_DV | PHY receive data valid<br>Contains the crs and data valid information of the receive interface.                 | I    | PL_GPIO_19/A3           | Extended mode   |
| RMII1_RX_ER  | PHY receive error   | I    | PL_GPIO_18/D5           | Extended mode   |
| RMII1_RXD0   | PHY receive data  | I    | PL_GPIO_24/B5           | Extended mode   |
| RMII1_RXD1   | These bits provide the RMII receive data. The validity of the data is qualified with RMII1_CRS_DV.              |      | PL_GPIO_20/B4           | Extended mode   |
| RMII1_TX_EN  | PHY transmit data enable<br>When high, it indicates that valid data is being transmitted on the RMII_TXDn bus.  | O    | PL_GPIO_23/A4           | Extended mode   |
| RMII1_TXD0   | PHY transmit data   | O    | PL_GPIO_25/C6           | Extended mode   |
| RMII1_TXD1   | These bits provide the RMII transmit data. The validity of the data is qualified with RMII1_TX_EN.              |      | PL_GPIO_21/C5           | Extended mode   |

### 3.5 PL\_GPIO and PL\_CLK pin sharing for debug and test modes

In some cases the PL\_GPIO and PL\_CLK pins may be used in different ways for debugging purposes. There are four different cases (see also [Table 32](#)):

1. Case 0 - All the PL\_GPIO and PL\_CLK get values from Boundary scan registers during Ex-test instruction of JTAG . Typically, this configuration is used to verify the correctness of the soldering process during the production flow. The pad (PL\_GPIO or PL\_CLK) is driven by the Boundary Scan Register, and disconnected from the I/O function used in functional mode.
2. Case 1 - All the PL\_GPIO and PL\_CLK maintain their original meaning and the JTAG Interface is disconnected from the processor.
3. Case 2 - All the PL\_GPIO and PL\_CLK maintain their original meaning but the JTAG Interface is connected to the processor. This configuration is useful during the development phase, but offers only “static” debug.
4. Case 3 - Some PL\_GPIOs, as shown in [Table 32](#) below, are used to connect the ETM9 lines to an external box. This configuration is typically used only during the development phase. It offers a very powerful debug capability. When the processor reaches a breakpoint it is possible, by analyzing the trace buffer, to understand the reason why the processor has reached the break.

**Table 32. Ball sharing during debug**

| Signals                              | Case 0 - boundary scan | Case 1 - no debug | Case 2 - static debug | Case 3 - full debug   |
|--------------------------------------|------------------------|-------------------|-----------------------|---|
| TEST_0                               | 0                      | 0                 | 1                     | 0   |
| TEST_1                               | 0                      | 0                 | 0                     | 1   |
| TEST_2                               | 0                      | 1                 | 1                     | 1   |
| TEST_3                               | 0                      | 1                 | 1                     | 1   |
| TEST_4                               | 1                      | 0                 | 0                     | 0   |
| nTRST                                | nTRST_bscan            | nc                | nTRST_ARM             | nTRST_ARM   |
| TCK                                  | TCK_bscan              | nc                | TCK_ARM               | TCK_ARM   |
| TMS                                  | TSM_bscan              | nc                | TMS_ARM               | TMS_ARM   |
| TDI                                  | TDI_bscan              | nc                | TDI_ARM               | TDI_ARM   |
| TDO                                  | TDO_bscan              | nc                | TDO_ARM               | TDO_ARM   |
| PL_GPIOxxx/<br>PL_CLKx<br>(all pins) | Used for boundary scan | Functional mode   | Functional mode       | PL_GPIO97-<br>PL_GPIO73 used for debug, Refer to <a href="#">Table 15: PL_GPIO/PL_CLK multiplexing scheme and reset states on page 43</a> |

## 4 Electrical characteristics

### 4.1 Absolute maximum ratings

This product contains devices to protect the inputs against damage due to high/low static voltages. However, it is advisable to take normal precaution to avoid application of any voltage higher/lower than the specified maximum/minimum rated voltages.

**Caution:** Stresses above those listed in [Table 33](#) may cause permanent damage to the device. Exposure to maximum rating conditions for extended periods may affect device reliability.

**Table 33. Absolute maximum ratings**

| Symbol        | Parameter                             | Min   | Max  | Unit |
|---------------|---------------------------------------|-------|------|------|
| $V_{DD\ 1.2}$ | Supply voltage for the core           | - 0.3 | 1.44 | V    |
| $V_{DD\ 3.3}$ | Supply voltage for the I/Os           | - 0.3 | 3.9  | V    |
| $V_{DD\ 2.5}$ | Supply voltage for the analog blocks  | - 0.3 | 3    | V    |
| $V_{DD\ 1.8}$ | Supply voltage for the DRAM interface | - 0.3 | 2.16 | V    |
| $V_{DD\ RTC}$ | RTC supply voltage                    | -0.3  | 2.16 | V    |
| $T_{STG}$     | Storage temperature                   | -55   | 150  | °C   |

### 4.2 Maximum power consumption

*Note:* These values take into consideration the worst cases of process variation and voltage range and must be used to design the power supply section of the board.

**Table 34. Maximum power consumption**

| Symbol               | Description   | Max | Unit |
|----------------------|---|-----|------|
| $I_{DD(1.2Vsupply)}$ | Current consumption of $V_{DD\ 1.2}$ supply voltage for the core                          | 400 | mA   |
| $I_{DD(1.8Vsupply)}$ | Current consumption of $V_{DD\ 1.8}$ supply voltage for the DRAM interface <sup>(1)</sup> | 150 | mA   |
| $I_{DD(RTC)}$        | Current consumption of RTC supply voltage   | 8   | μA   |
| $I_{DD(2.5Vsupply)}$ | Current consumption of 2.5V supply voltage for the analog blocks                          | 30  | mA   |
| $I_{DD(3.3Vsupply)}$ | Current consumption of 3.3V supply voltage for the I/Os <sup>(2)</sup>                    | 12  | mA   |
| $P_D$                | Maximum power consumption <sup>(3)</sup>  | 870 | mW   |

1. Peak current with Linux memory test (50% write and 50% read) plus DMA reading memory.
2. With 30 logic channels connected to the device and simultaneously switching at 10 MHz.
3. Based on bench measurements for worst case silicon under worst case operating conditions. Devices tested with operating system running, CPU and DDR2 running at 333 MHz, DDR2 driven by PLL2, SDRAM and all on-chip peripherals and internal modules enabled.
 

1.2 V current and power are primarily dependent on the applications running and the use of internal chip functions (DMA, USB, Ethernet, and so on).

3.3 V current and power are primarily dependent on the capacitive loading, frequency, and utilization of the external buses.

### 4.3 Recommended operating conditions

To ensure proper operation of the device, it is highly recommended to follow the conditions shown in the following table.

**Table 35. Recommended operating conditions**

| Symbol              | Parameter                          | Min  | Typ | Max  | Unit |
|---------------------|------------------------------------|------|-----|------|------|
| V <sub>DD</sub> 1.2 | Supply voltage for the core        | 1.14 | 1.2 | 1.3  | V    |
| V <sub>DD</sub> 3.3 | Supply voltage for the I/Os        | 3    | 3.3 | 3.6  | V    |
| V <sub>DD</sub> 2.5 | PLL supply voltage <sup>(1)</sup>  | 2.25 | 2.5 | 2.75 | V    |
| V <sub>DD</sub> 2.5 | Oscillator supply voltage          | 2.25 | 2.5 | 2.75 | V    |
| V <sub>DD</sub> 1.8 | Supply voltage for DRAM interface  | 1.70 | 1.8 | 1.9  | V    |
| V <sub>DD</sub> RTC | RTC supply voltage                 | 1.3  | 1.5 | 1.8  | V    |
| T <sub>A</sub>      | Ambient temperature <sup>(2)</sup> | -40  | –   | 85   | °C   |
| T <sub>J</sub>      | Junction temperature               | -40  | –   | 125  | °C   |

1. For power supply filtering it is required to add an external ferrite inductor.
2. T<sub>A</sub> to be considered under JEDEC51 conditions or equivalent ones.

### 4.4 Overshoot and undershoot

This product can support the following values of overshoot and undershoot.

**Table 36. Overshoot and undershoot specifications**

| Parameter   | 3V3 I/Os | 2V5 I/Os | 1V8 I/Os |
|---|----------|----------|----------|
| Amplitude   | 500 mV   | 500 mV   | 500 mV   |
| Ratio of overshoot (or undershoot) duration with respect to pulse width | 1/3      | 1/3      | 1/3      |

If the amplitude of the overshoot/undershoot increases (decreases), the ratio of overshoot/undershoot width to the pulse width decreases (increases). The formula relating the two is:

$$\text{Amplitude of OS/US} = 0.75 \cdot (1 - \text{ratio of OS (or US) duration with respect to pulse width})$$

*Note:* The value of overshoot/undershoot should not exceed the value of 0.5 V. However, the duration of the overshoot/undershoot can be increased by decreasing its amplitude.

## 4.5 3.3V I/O characteristics

The 3.3 V I/Os are compliant with JEDEC standard JESD8b.

**Table 37. Low voltage TTL DC input specification (3 V < V<sub>DD</sub> < 3.6 V)**

| Symbol            | Parameter                  | Min | Max | Unit |
|-------------------|----------------------------|-----|-----|------|
| V <sub>IL</sub>   | Low level input voltage    |     | 0.8 | V    |
| V <sub>IH</sub>   | High level input voltage   | 2   |     | V    |
| V <sub>hyst</sub> | Schmitt trigger hysteresis | 300 | 800 | mV   |

**Table 38. Low voltage TTL DC output specification (3 V < V<sub>DD</sub> < 3.6 V)**

| Symbol          | Parameter                 | Test condition                         | Min                   | Max | Unit |
|-----------------|---------------------------|--|-----------------------|-----|------|
| V <sub>OL</sub> | Low level output voltage  | I <sub>OL</sub> = X mA <sup>(1)</sup>  |                       | 0.3 | V    |
| V <sub>OH</sub> | High level output voltage | I <sub>OH</sub> = -X mA <sup>(1)</sup> | V <sub>DD</sub> - 0.3 |     | V    |

1. Maximum current load (IOL) = 10 mA for PL\_GPIO and PL\_CLK pins. For the IOL max value of dedicated pins, refer to [Chapter 3: Pin description](#).

**Table 39. Pull-up and pull-down characteristics**

| Symbol          | Parameter                       | Test condition                        | Min | Max | Unit |
|-----------------|---------------------------------|---------------------------------------|-----|-----|------|
| R <sub>PU</sub> | Equivalent pull-up resistance   | V <sub>I</sub> = 0 V                  | 29  | 67  | kΩ   |
| R <sub>PD</sub> | Equivalent pull-down resistance | V <sub>I</sub> = V <sub>DDE</sub> 3V3 | 29  | 103 | kΩ   |

## 4.6 Clocking parameters

### 4.6.1 Master clock (MCLK)

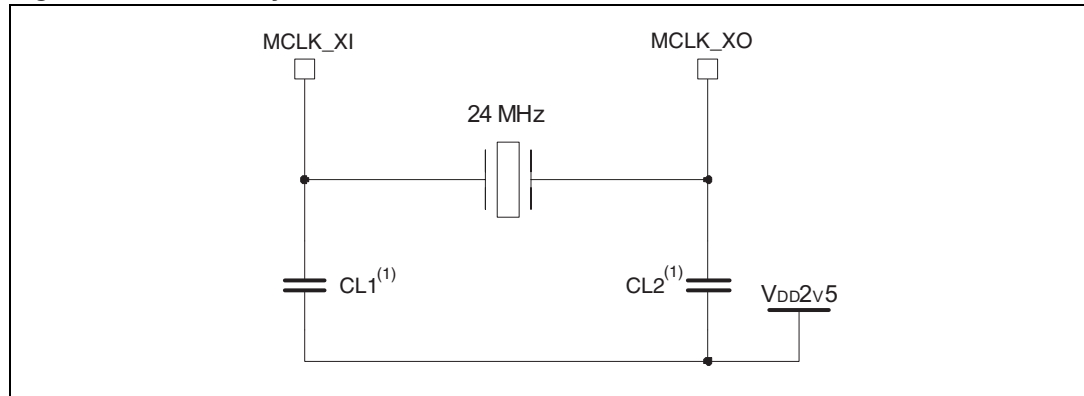
#### MCLK generated from a crystal oscillator

**Table 40. MCLK oscillator characteristics**

| Symbol              | Parameter                    | Conditions                          | Min  | Typ               | Max               | Unit |
|---------------------|------------------------------|-------------------------------------|------|-------------------|-------------------|------|
| f <sub>osc_in</sub> | Oscillator frequency         |                                     |      | 24 <sup>(1)</sup> | 33 <sup>(2)</sup> | MHz  |
| ESR                 | Equivalent series resistance |                                     |      |                   | 50                | Ω    |
| gm                  | Oscillator transconductance  | Startup                             | 19.8 | 28.5              |                   | mA/V |
| t <sub>SU</sub>     | Startup time                 | Stabilized power on MCLK_VDD2V5 pin |      |                   | 2 <sup>(3)</sup>  | ms   |

1. A frequency of 24 MHz is mandatory to obtain the required frequencies for all clocks generated by the USB PLL (PLL3).
2. At Max freq = 33 MHz the ESR value has to be less than 20 Ω.
3. Startup time simulated with a 30 MHz crystal.

**Figure 4. MCLK crystal connection**



1. C<sub>L1</sub> and C<sub>L2</sub> are the load capacitors.

The value of the capacitors depends on the type of the selected crystal. To calculate the value of the load capacitance, use the formula given below.

**Formula**

$$C_L = \frac{C_{L1} \times C_{L2}}{C_{L1} + C_{L2}} + C_s$$

Where C<sub>L1</sub> and C<sub>L2</sub> are the load capacitors and C<sub>S</sub> is the circuit stray capacitance.

In our application:

$$C_{L1} = C_{L2} = C_{ext}$$

This implies:

$$C_{\text{ext}} = (C_L - C_S) * 2$$

**Example:**

For this example, a Rakon XTAL003342 24 MHz oscillator has been used.

For the Rakon XTAL003342 crystal,  $C_L = 12$  pF

With  $C_S = \sim 3$  pF, we have:  $C_{\text{ext}} = C_{L1} = CL2 = 18$  pF

**MCLK generated from an external clock source**

**Table 41. MCLK external user clock source characteristics**

| Symbol   | Parameter                            | Conditions  | Min                     | Typ               | Max                     | Unit          |
|--|--------------------------------------|---|-------------------------|-------------------|-------------------------|---------------|
| $f_{\text{MCLK\_XI}}$  | External clock source frequency      |   | No limitation           | 24 <sup>(1)</sup> | 33                      | MHz           |
| $V_{\text{MCLK\_XIH}}$   | MCLK_XI input pin high level voltage |   | MCLK_VDD2V5 - 0.3       |                   | MCLK_VDD2V5             | V             |
| $V_{\text{MCLK\_XIL}}$   | MCLK_XI input pin low level voltage  |   | MCLK_GNDSUB             |                   | 0.3                     | V             |
| $\text{DuCy}_{(\text{MCLK\_XI})}$                                  | Duty cycle <sup>(2)</sup>            |   | 40                      |                   | 60                      | %             |
| $t_{\text{r}(\text{MCLK\_XI})}$<br>$t_{\text{f}(\text{MCLK\_XI})}$ | MCLK_XI input rise and fall time     |   | -5% of the clock period |                   | +5% of the clock period | %             |
| $C_{\text{IN}(\text{MCLK\_XI})}$                                   | MCLK_XI input capacitance            |   |                         | 7                 |                         | pF            |
| $I_{\text{L}(\text{MCLK\_XI})}$                                    | MCLK_XI input leakage current        | $\text{MCLK\_GNDSUB} \leq V_{\text{IN}} \leq \text{MCLK\_VDD2V5}$ |                         |                   | $\pm 1$                 | $\mu\text{A}$ |

1. A frequency of 24 MHz is mandatory to obtain the required operating frequency for all clocks generated by the USB PLL (PLL3).
2. An initial delay of  $1 \mu\text{s} + 2048 f_{\text{MCLK\_XI}}$  cycles occurs for duty cycle detection and internal clock availability.

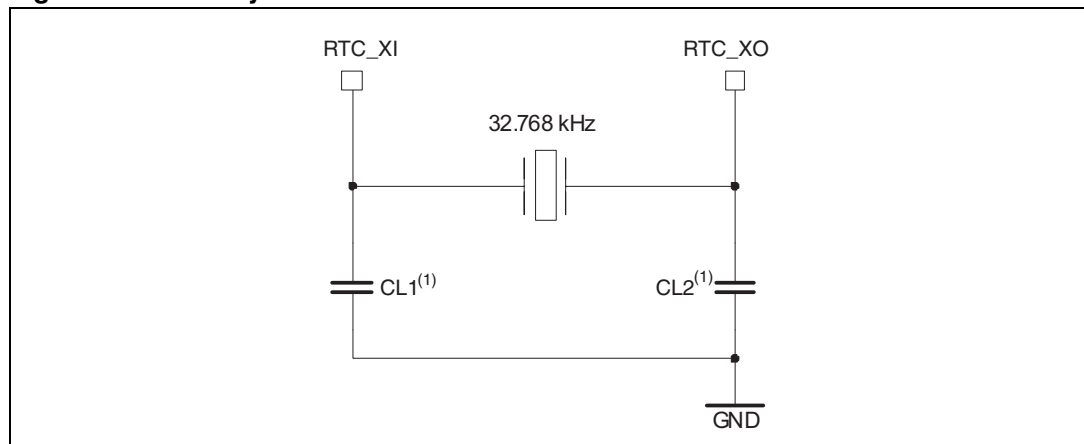
### 4.6.2 Real-time clock (RTC)

#### RTC clock generated from a crystal oscillator

**Table 42. RTC oscillator characteristics**

| Symbol              | Parameter                    | Condition                          | Min | Typ    | Max   | Unit                       |
|---------------------|------------------------------|------------------------------------|-----|--------|-------|----------------------------|
| f <sub>OSC_IN</sub> | Oscillator frequency         |                                    |     | 32.768 |       | kHz                        |
| ESR                 | Equivalent series resistance |                                    |     |        | 6000  | Ω                          |
| gm                  | Oscillator transconductance  | Startup                            | 5   |        |       | μA/V                       |
| t <sub>SU</sub>     | Startup time                 | Stabilized power on RTC_VDD1V5 pin |     |        | 17000 | f <sub>OSC_IN</sub> cycles |

**Figure 5. RTC crystal connection**



1. C<sub>L1</sub> and C<sub>L2</sub> are the load capacitors.

The value of the capacitors depends on the type of the selected crystal. To calculate the value of the load capacitance, use the formula given below.

**Formula**

$$C_L = \frac{C_{L1} \times C_{L2}}{C_{L1} + C_{L2}} + C_s$$

Where C<sub>L1</sub> and C<sub>L2</sub> are the load capacitors and C<sub>S</sub> is the circuit stray capacitance.

In our application:

$$C_{L1} = C_{L2} = C_{ext}$$

This implies:

$$C_{ext} = (C_L - C_s) * 2$$



**Example:**

For this example, a Fox Electronics, NC26LF-327 32.768 kHz oscillator has been used.

For the Fox Electronics, NC26LF-327 crystal,  $C_L = 12.5$  pF

With  $C_S = \sim 0.1$  pF, we have:  $C_{ext} = C_{L1} = CL2 = 24.8$  pF=22 pF

**RTC clock generated from an external clock source****Table 43. RTC external user clock source characteristics**

| Symbol                               | Parameter                           | Condition                               | Min              | Typ    | Max        | Unit    |
|--------------------------------------|-------------------------------------|---|------------------|--------|------------|---------|
| $f_{RTC\_XI}$                        | External clock source frequency     |   |                  | 32.768 |            | kHz     |
| $V_{RTC\_XIH}$                       | RTC_XI input pin high level voltage |   | RTC_VDD1V5 - 0.2 |        | RTC_VDD1V5 | V       |
| $V_{RTC\_XIL}$                       | RTC_XI input pin low level voltage  |   | RTC_GND          |        | 0.2        | V       |
| $DuCy_{(RTC\_XI)}$                   | Duty cycle                          |   | 40               |        | 60         | %       |
| $t_{r(RTC\_XI)}$<br>$t_{f(RTC\_XI)}$ | RTC_XI input rise and fall time     |   |                  |        | 50         | ns      |
| $C_{IN(RTC\_XI)}$                    | RTC_XI input capacitance            |   |                  | 5      |            | pF      |
| $I_{L(RTC\_XI)}$                     | RTC_XI input leakage                | $RTC\_GND \leq V_{IN} \leq RTC\_VDD1V5$ |                  |        | $\pm 1$    | $\mu A$ |

## 4.7 LPDDR and DDR2 pin characteristics

**Table 44. DC characteristics**

| Symbol     | Parameter                | Test condition | Min             | Max              | Unit |
|------------|--------------------------|----------------|-----------------|------------------|------|
| $V_{IL}$   | Low level input voltage  | SSTL18         | -0.3            | $V_{REF}-0.125$  | V    |
| $V_{IH}$   | High level input voltage | SSTL18         | $V_{REF}+0.125$ | $V_{DDE}1V8+0.3$ | V    |
| $V_{hyst}$ | Input voltage hysteresis |                | 200             |                  | mV   |

**Table 45. Driver characteristics**

| Symbol | Parameter        | Min | Typ | Max | Unit     |
|--------|------------------|-----|-----|-----|----------|
| $R_O$  | Output impedance |     | 45  |     | $\Omega$ |

**Table 46. On-die termination**

| Symbol | Parameter  | Min | Typ | Max | Unit     |
|--------|--|-----|-----|-----|----------|
| RT1    | Termination value of resistance for on die termination |     | 75  |     | $\Omega$ |
| RT2    | Termination value of resistance for on die termination |     | 150 |     | $\Omega$ |

**Table 47. Reference voltage**

| Symbol      | Parameter                   | Min              | Typ               | Max              | Unit |
|-------------|-----------------------------|------------------|-------------------|------------------|------|
| $V_{REFIN}$ | Voltage applied to core/pad | $0.49 * V_{DDE}$ | $0.500 * V_{DDE}$ | $0.51 * V_{DDE}$ | V    |

## 4.8 ADC pin characteristics

**Table 48. ADC pin characteristics**

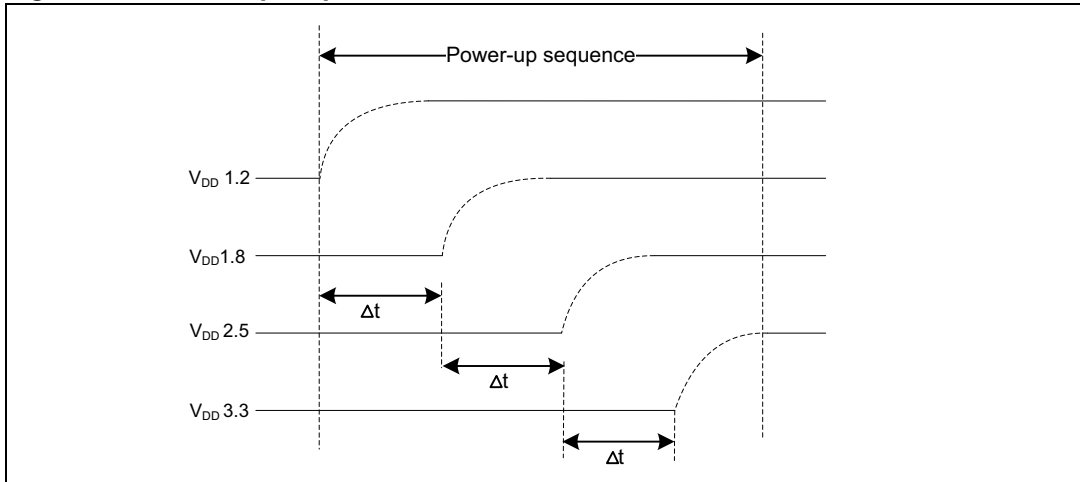
| Symbol                | Parameters  | Min               | Typ | Max               | Unit             |
|-----------------------|---|-------------------|-----|-------------------|------------------|
| $f_{\text{ADC\_CLK}}$ | ADC_CLK frequency   | 3                 |     | 14                | MHz              |
| $V_{\text{DD}}$       | ADC supply voltage  |                   |     | 2.5               | V                |
| $V_{\text{REFP}}$     | Positive reference voltage                                  |                   |     | 2.5               | V                |
| $V_{\text{REFN}}$     | Negative reference voltage                                  | 0                 |     |                   | V                |
| $V_{\text{IREF}}$     | Internal reference voltage                                  | 1.95              | 2   | 2.05              | V                |
| $t_{\text{STARTUP}}$  | Startup time  |                   | 50  |                   | $\mu\text{s}$    |
| $V_{\text{AIN}}$      | Input range (absolute)                                      | AGND - 0.3        |     | AVDD - 0.3        | V                |
|                       | Conversion range  | $V_{\text{REFN}}$ |     | $V_{\text{REFP}}$ | V                |
| $C_{\text{AIN}}$      | Input capacitance   | 5                 | 6.4 | 8                 | pF               |
| $R_{\text{AIN}}$      | Input mux resistance (total equivalent sampling resistance) | 1.5               | 2   | 2.5               | $\text{K}\Omega$ |
| $t_{\text{CONV}}$     | Conversion time ( $f_{\text{ADC\_CLK}}=14\text{ MHz}$ )     |                   |     | 1                 | $\mu\text{s}$    |
|                       | Conversion time   | 13                |     |                   | ADC_CLK cycles   |
| INL                   | Integral linearity error                                    |                   |     | $\pm 1$           | LSB              |
| DNL                   | Differential linearity error                                |                   |     | $\pm 1$           | LSB              |

### 4.9 Power-up sequence

It is recommended to power up the power supplies in the order shown in [Figure 6](#).

V<sub>DD</sub> 1.2 is brought up first, followed by V<sub>DD</sub> 1.8, then V<sub>DD</sub> 2.5 and finally V<sub>DD</sub> 3.3. The minimum time ( $\Delta t$ ) between each power up is  $>0 \mu s$ .

**Figure 6. Power-up sequence**



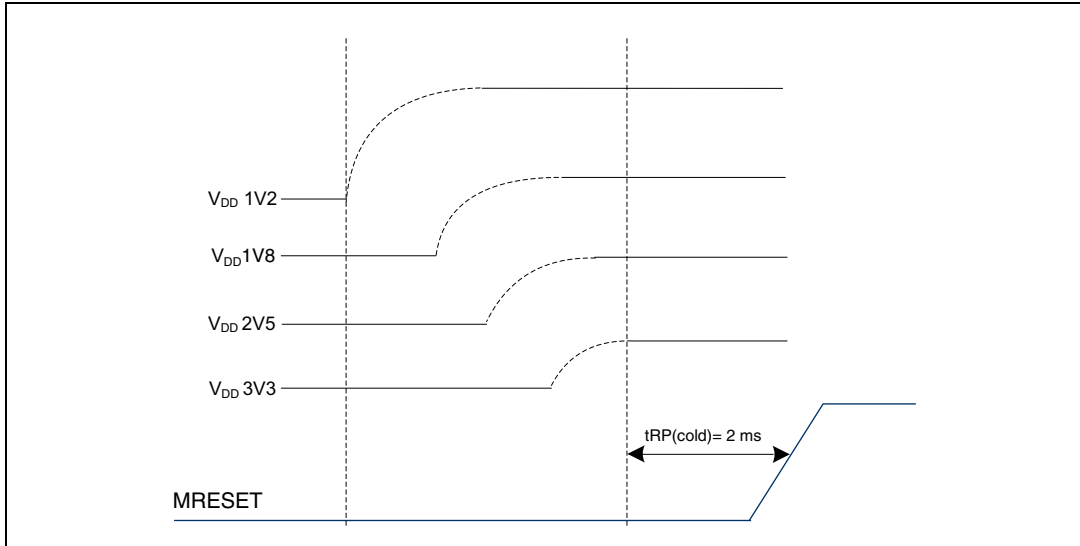
### 4.10 Power-down sequence

All power supplies can be shut down at the same time.

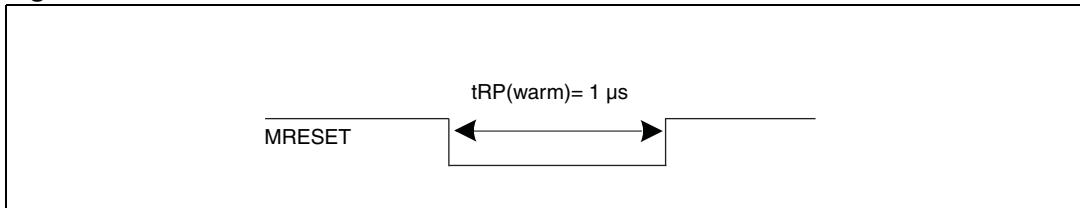
### 4.11 Reset release

The master reset (MRESET) must be released after all the power supplies are stable and for a time interval of 2 ms, which is the start-up time of the main oscillator, and must be asserted low for at least 1  $\mu$ s for warm reset.

**Figure 7. Cold reset release**



**Figure 8. Warm reset release**



Note: See also: [Section 5.2: Reset timing characteristics on page 78](#).

## 5 Timing requirements

This chapter provides the timing requirements for the synchronous and asynchronous IPs present in SPEAr320S.

The signal transition levels used for timing measurements are:  $0.2 \cdot VDD$  and  $0.8 \cdot VDD$ .

### 5.1 External interrupt timing characteristics

In legacy modes, all the interrupts are high-level triggered. In extended mode, interrupt trigger polarity is programmable as rising or falling edge.

**Table 49. PL\_GPIO external interrupt input timing**

| Symbol | Description                                   | Min | Unit |
|--------|---|-----|------|
| tINT   | Minimum width for rising edge interrupt pulse | 24  | ns   |

### 5.2 Reset timing characteristics

**Table 50. Reset timing characteristics**

| Symbol    | Description  | Min | Unit    |
|-----------|--|-----|---------|
| tRP(cold) | MRESET pin active low state duration for cold reset (startup time from all supplies up and stable).<br>See <a href="#">Figure 7: Cold reset release on page 77</a> | 2   | ms      |
| tRP(warm) | MRESET pin active low state duration for warm reset (minimum pulse width able to reset the device).<br>See <a href="#">Figure 8: Warm reset release on page 77</a> | 1   | $\mu$ s |

*Note:* Warm reset can be triggered by software by writing any value to the system controller SYSSTAT register.

### 5.3 CAN timing characteristics

The nominal CAN bit time allows a delay Prop\_Seg to compensate for the physical delay times. For details refer to *RM0319, Reference manual, SPEAr320S architecture and functionality*.

[Table 51](#) specifies the delay for the CAN I/O pads.

$\text{Prop\_Seg} \geq 2 * \text{max node output delay} + \text{bus line delay} + \text{node input delay}$

**Table 51. CAN timing characteristics**

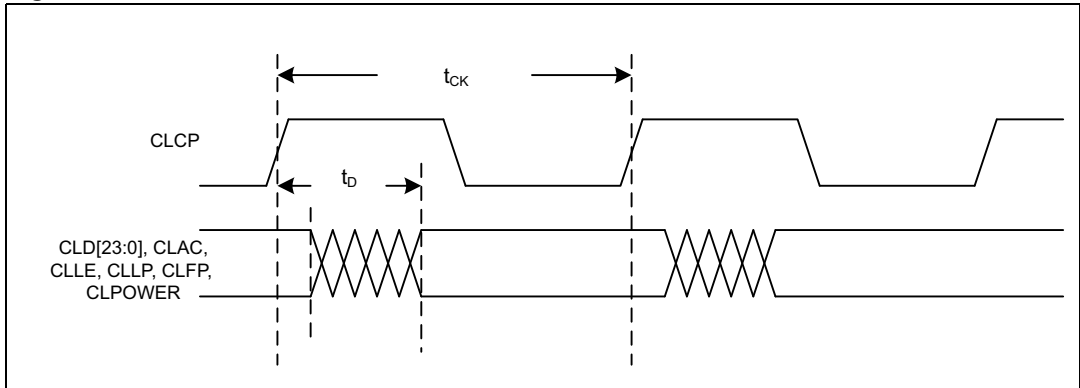
| Symbol      | Description                      | Max  | Unit |
|-------------|----------------------------------|------|------|
| $t_{d(RX)}$ | CAN0_RX (PL_GPIO32) input delay  | 5.03 | ns   |
|             | CAN1_RX (PL_GPIO30) input delay  | 6.2  | ns   |
| $t_{d(TX)}$ | CAN0_TX (PL_GPIO33) output delay | 9.55 | ns   |
|             | CAN1_TX (PL_GPIO31) output delay | 10.2 | ns   |

### 5.4 CLCD timing characteristics

The CLCD has a wide variety of configurations, and the parameters change accordingly.

The timing characterization is performed assuming an output load capacitance of 10 pF on all outputs.

**Figure 9. CLCD waveform**



**Table 52. CLCD timing requirements**

| Symbol   | Description                    | Min   | Max   | Unit |
|----------|--------------------------------|-------|-------|------|
| $t_{CK}$ | CLCP clock period              | 20.83 | 41.66 | ns   |
| $t_D$    | CLCP to CLCD output data delay | 1     | 9.5   |      |



## 5.5 DDR2/LPDDR timing characteristics

The timing parameters listed below are defined by the JEDEC Standard for DDR memories. DDR memories whose parameters are within the ranges defined in [Table 53](#), [Table 54](#) and [Table 55](#) can be interfaced with SPEAr320S.

Read cycle timing apply to DQS and DQ input to SPEAr. Write cycle timings refer to DQS and DQ output to SPEAr.

The timing characterization is performed assuming an output load capacitance of 10 pF on all the DDR pads.

### 5.5.1 DDR2/LPDDR read cycle timing characteristics

Figure 10. DDR2/LPDDR read cycle waveform

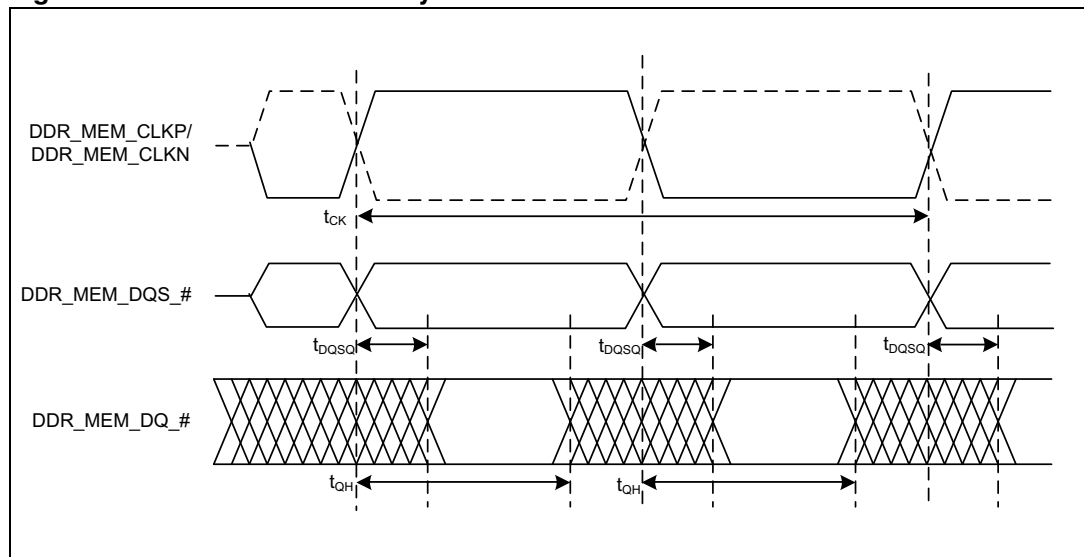


Table 53. DDR2/LPDDR read cycle timing requirements

| Symbol     | Description  | Min              | Max              | Unit |
|------------|--|------------------|------------------|------|
| $t_{ck}$   | DDR_MEM_CLKP/CLKN cycle time when interfacing DDR2 memory        | 3                |                  | ns   |
|            | LPDDR DDR_MEM_CLKP/CLKN cycle time when interfacing LPDDR memory | 6                |                  |      |
| $t_{DQSQ}$ | DQS to DQ input setup time                                       | 0                | $0.25t_{CK}+0.4$ |      |
| $t_{QH}$   | DQS to DQ input hold time  | $0.25t_{CK}+0.7$ | $0.5t_{CK}$      |      |

### 5.5.2 DDR2/LPDDR write cycle timing characteristics

Figure 11. DDR2/LPDDR write cycle waveform

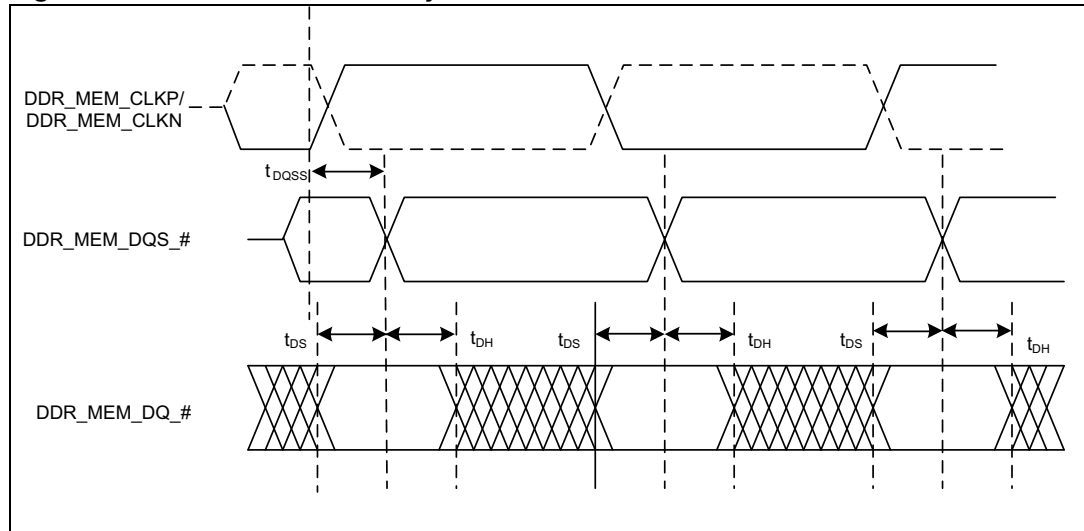


Table 54. DDR2/LPDDR write cycle timing requirements

| Symbol     | Description                                      | Min  | Max                 | Unit |
|------------|--|------|---------------------|------|
| $t_{DQSS}$ | Positive DQS latching edge to associated CK edge | -0.5 | 0.5                 | ns   |
| $t_{DS}$   | DQ & DQM output setup time relative to DQS       | 0    | $0.25t_{CK} - 0.76$ |      |
| $t_{DH}$   | DQ & DQM output hold time relative to DQS        | 0    | $0.25t_{CK} - 0.84$ |      |

### 5.5.3 DDR2/LPDDR command timing characteristics

Figure 12. DDR2/LPDDR command waveform

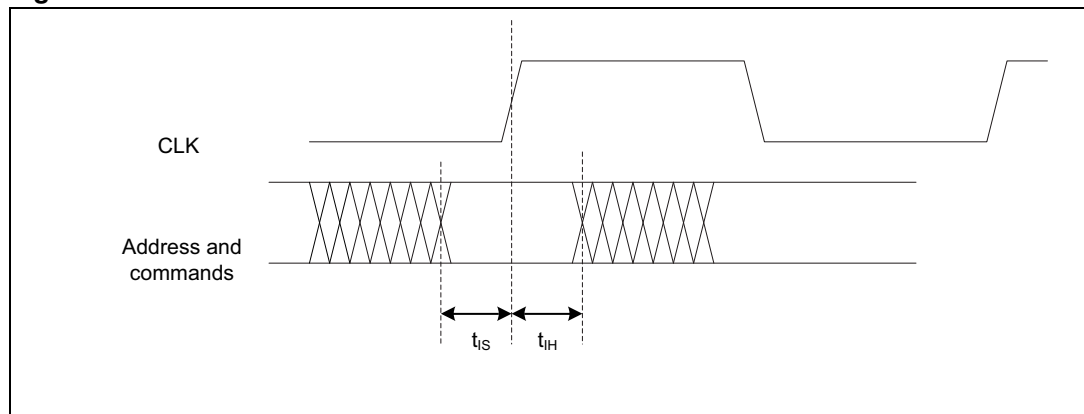
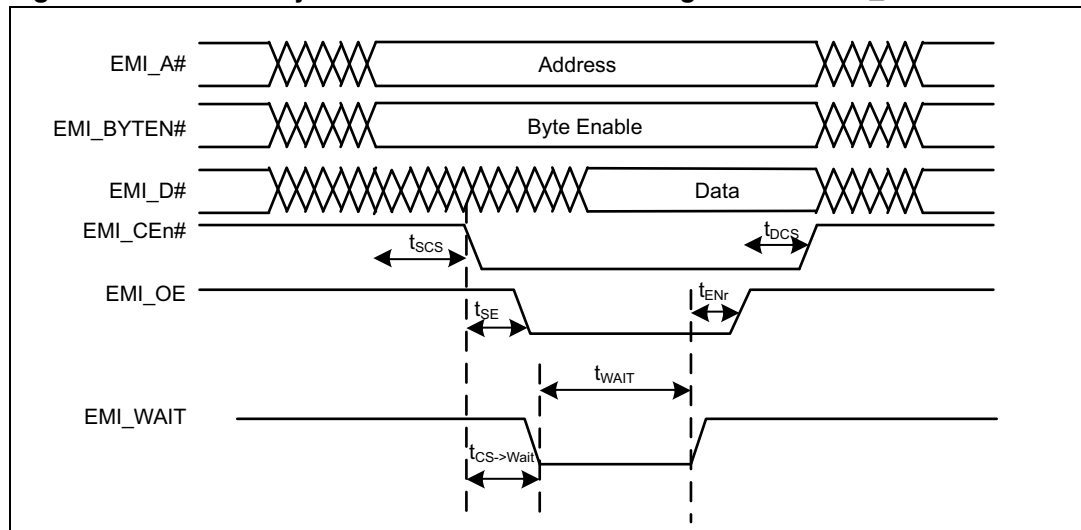


Table 55. DDR2/LPDDR command timing requirements

| Symbol   | Description                           | Min | Max                | Unit |
|----------|---------------------------------------|-----|--------------------|------|
| $t_{IS}$ | Address and control output setup time | 0   | $0.5t_{CK} - 0.5$  | ns   |
| $t_{IH}$ | Address and control output hold time  | 0   | $0.5t_{CK} - 0.59$ |      |

### 5.6 EMI timing characteristics

**Figure 13. EMI read cycle waveform with acknowledgement on EMI\_WAIT**



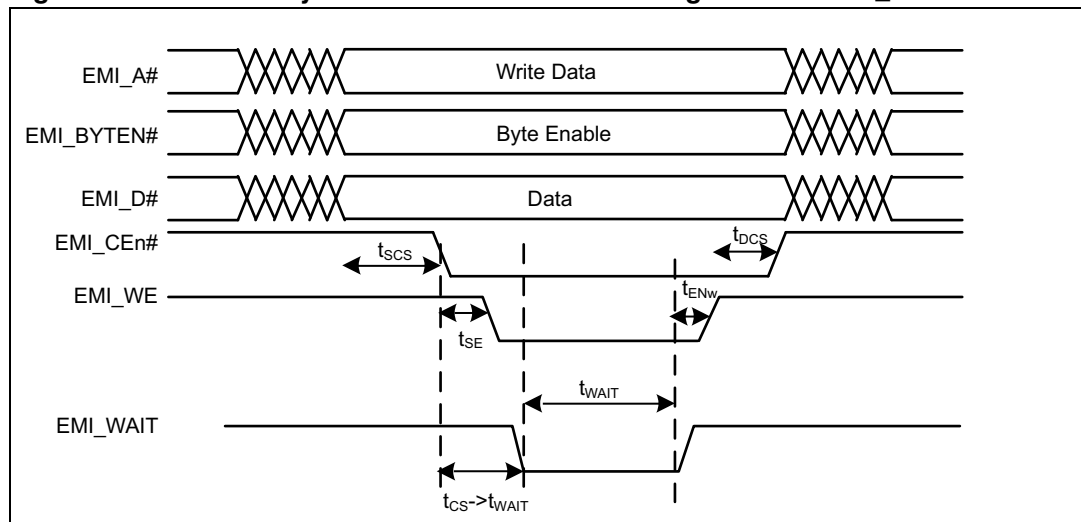
Note: The values of  $t_{SE}$ ,  $t_{ENr}$ ,  $t_{DCS}$ ,  $t_{SCS}$  are programmable via the EMI registers.

**Table 56. EMI timing requirements for read cycle with acknowledgement on WAIT**

| Symbol                    | Min            |
|---------------------------|----------------|
| $t_{CS \rightarrow Wait}$ | $t_{HCLK}$     |
| $t_{WAIT}$                | $4 * t_{HCLK}$ |

Note: Values in [Table 56](#) refer to the common internal source clock which has a period of  $t_{HCLK} = 6 \text{ ns}$ .

**Figure 14. EMI write cycle waveform with acknowledgement on EMI\_WAIT**



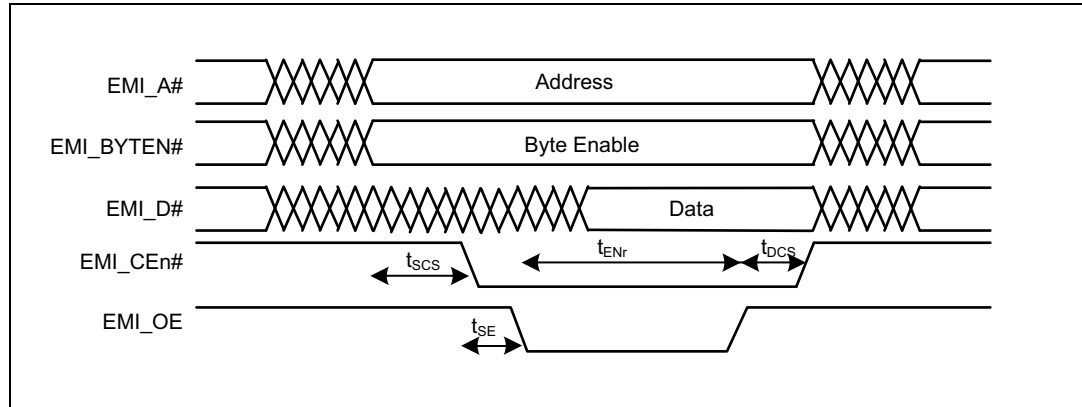
Note: The values of  $t_{SE}$ ,  $t_{ENw}$ ,  $t_{DCS}$ ,  $t_{SCS}$  are programmable via the EMI registers.

**Table 57. EMI timing requirements for write cycle with acknowledgement on WAIT**

| Symbol                    | Min            |
|---------------------------|----------------|
| $t_{CS \rightarrow Wait}$ | $t_{HCLK}$     |
| $t_{WAIT}$                | $4 * t_{HCLK}$ |

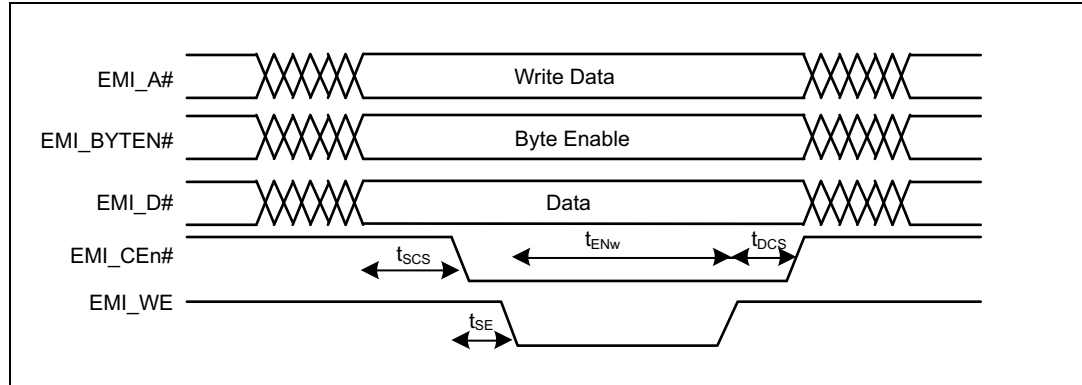
Note: Values in Table 57 refer to the common internal source clock which has a period of  $t_{HCLK} = 6\text{ ns}$ .

**Figure 15. EMI read cycle waveform without acknowledgement on EMI\_WAIT**



Note: The values of  $t_{SE}$ ,  $t_{ENr}$ ,  $t_{DCS}$ ,  $t_{SCS}$  are programmable via the EMI registers.

**Figure 16. EMI write cycle waveform without acknowledgement on EMI\_WAIT**



Note: The values of  $t_{SE}$ ,  $t_{ENw}$ ,  $t_{DCS}$ ,  $t_{SCS}$  are programmable via the EMI registers.

**Table 58. EMI signals timing requirements**

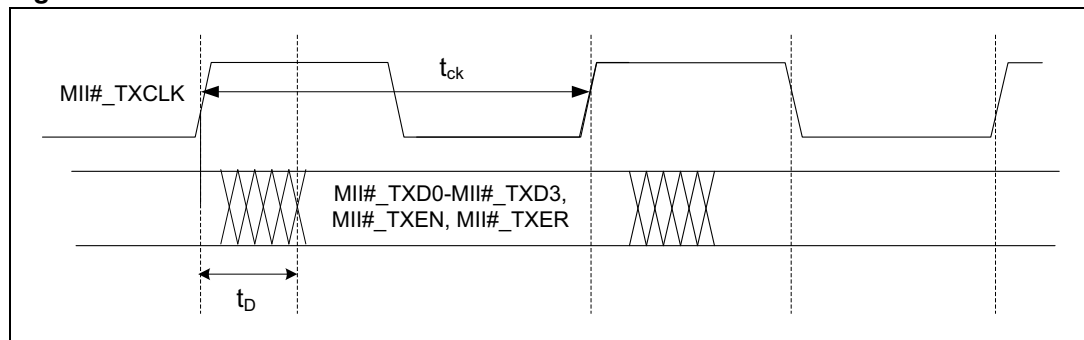
| Direction | Signal name    | Max      | Min      | Unit |
|-----------|----------------|----------|----------|------|
| Output    | EMI_A0-EMI_A23 | 8.612293 | 1.93584  | ns   |
|           | EMD0-EMID15    | 9.471291 | 2.260195 |      |
|           | EMI_CE0        | 8.764648 | 2.90581  |      |
|           | EMI_CE1        | 7.977348 | 2.636304 |      |
|           | EMI_CE2        | 9.027624 | 2.930175 |      |
|           | EMI_CE3        | 9.29631  | 3.006315 |      |
|           | EMI_BYTEN0     | 9.554388 | 3.092855 |      |
|           | EMI_BYTEN1     | 9.233592 | 3.038856 |      |
|           | EMI_RE         | 8.193018 | 2.680564 |      |
|           | EMI_WE         | 8.172619 | 2.80189  |      |
| Input     | EMI_D0-EMI_D15 | 10.8188  | 1.30245  |      |

## 5.7 Ethernet MII timing characteristics

The timing characterization is performed assuming an output load capacitance of 5 pF on the MII TX clock (MII#\_TXCLK) and 10 pF on the other pads.

### 5.7.1 MII transmit timing characteristics

**Figure 17. MII TX waveform**



**Table 59. MII TX timing requirements**

| Symbol   | Description                         | Min  | Max   | Unit |
|----------|-------------------------------------|------|-------|------|
| $t_{CK}$ | MII#_TXCLK clock period             | 40   | 40    | ns   |
| $t_D$    | MII#_TXCLK to MII output data delay | 3.34 | 11.86 |      |

*Note:* To calculate the  $t_{SETUP}$  value for the PHY, you have to consider the next  $t_{CK}$  rising edge, so you have to apply the following formula:  $t_{SETUP} = t_{CK} - t_{max}$

### 5.7.2 MII receive timing characteristics

Figure 18. MII RX waveform

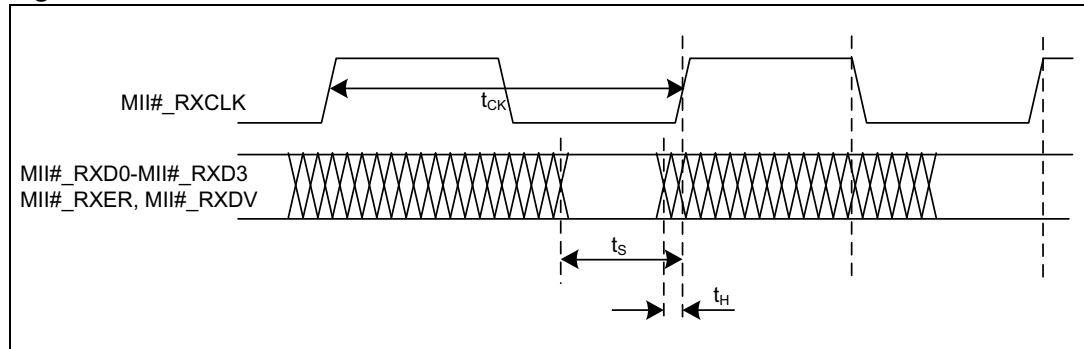


Table 60. MII RX timing requirements

| Symbol   | Description                                 | Min  | Max | Unit |
|----------|---|------|-----|------|
| $t_{CK}$ | MII#_TXCLK clock period                     | 40   | 40  | ns   |
| $t_S$    | Setup time requirement for MII receive data | 12.5 |     |      |
| $t_H$    | Hold time requirement for MII receive data  | -2   |     |      |

### 5.7.3 MDC/MDIO timing characteristics

Figure 19. MDC waveform

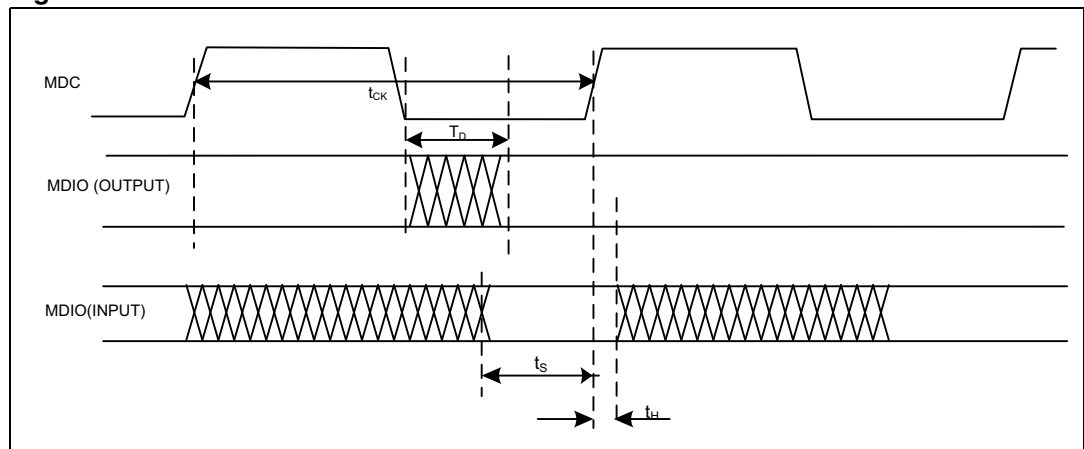


Table 61. MDC timing requirements

| Symbol   | Description                              | Min   | Max   | Unit |
|----------|--|-------|-------|------|
| $t_{CK}$ | MDC clock period                         | 614.4 | 614.4 | ns   |
| $t_D$    | Falling edge of MDC to MDIO output delay | -2.4  | 0.64  |      |
| $t_S$    | Setup time requirement for MDIO input    | 9.6   |       |      |
| $t_H$    | Hold time requirement for MDIO input     | -6.6  |       |      |

Note: When MDIO is used as output the data are launched on the falling edge of the clock as shown in Figure 19.

## 5.8 Ethernet RMIi timing characteristics

### 5.8.1 RMIi transmit timing characteristics

Figure 20. RMIi TX waveform

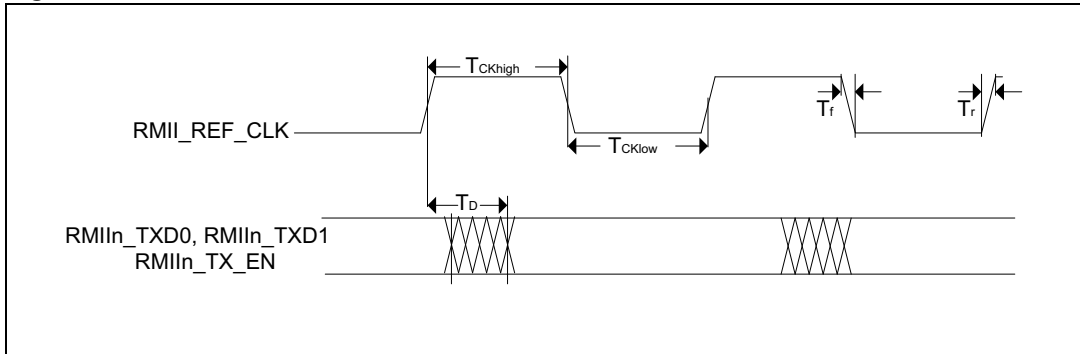
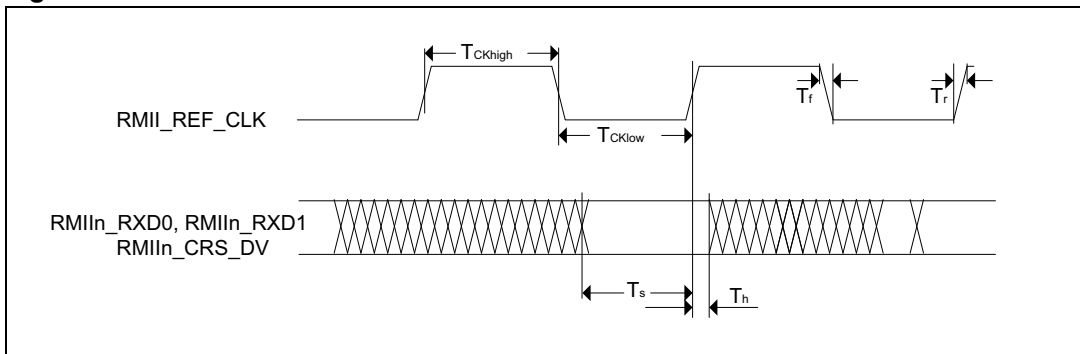


Table 62. RMIi TX timing requirements

| Symbol   | Description                     | Min  | Max   | Unit |
|----------|---------------------------------|------|-------|------|
| $t_{CK}$ | RMIi_REF_CLK period             | 20   |       | ns   |
| $t_D$    | Clock to RMIi0_TXD output delay | 4.28 | 15.65 |      |
|          | Clock to RMIi1_TXD output delay | 4.20 | 15.45 |      |

### 5.8.2 RMIi receive timing characteristics

Figure 21. RMIi RX waveform



**Table 63. RMI1 RX timing requirements**

| Symbol   | Description                                   | Min   | Max | Unit |
|----------|---|-------|-----|------|
| $t_{CK}$ | RMII_REF_CLK period                           | 20    |     | ns   |
| $t_S$    | Setup time requirement for RMII0 receive data | 4.9   |     |      |
|          | Setup time requirement for RMII1 receive data | 5     |     |      |
| $t_H$    | Hold time requirement for RMII0 receive data  | 0.1   |     |      |
|          | Hold time requirement for RMII1 receive data  | -0.09 |     |      |

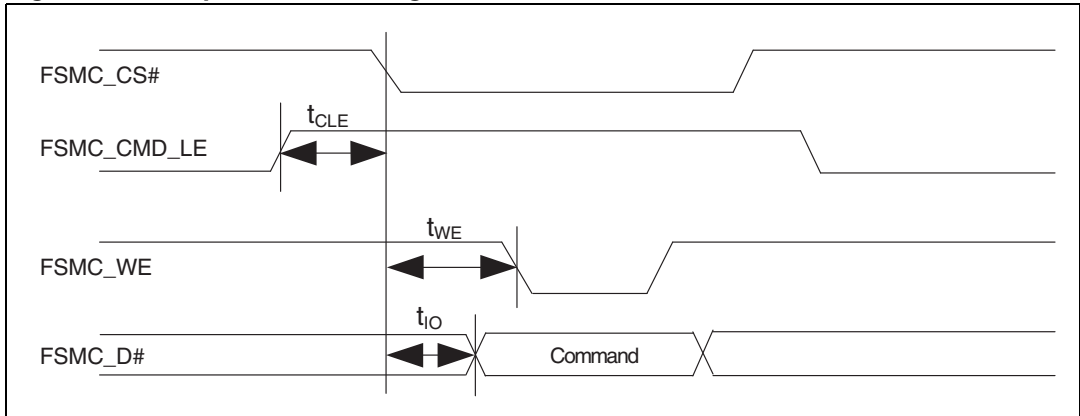


### 5.9 FSMC timing characteristics

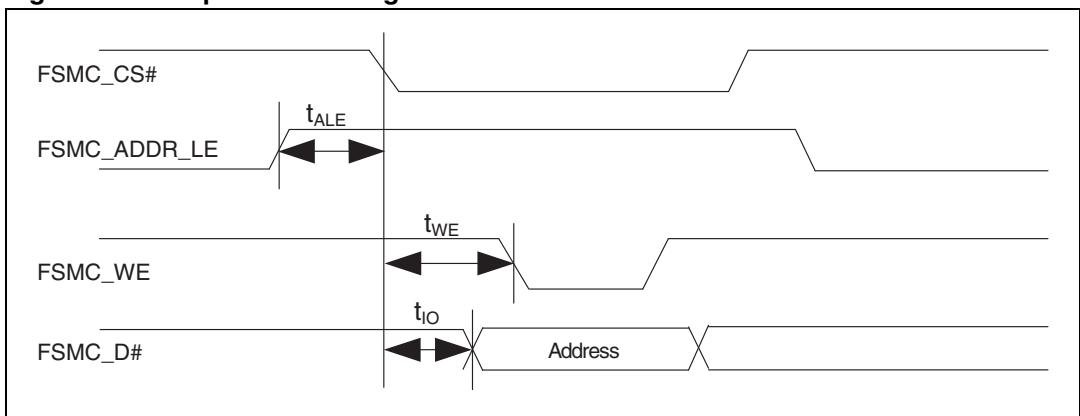
The FSMC present in SPEAr320S can interface external parallel NAND Flash memories.

The timing characterization is performed using primetime assuming an output load capacitance of 3 pF on the data, 15 pF on FSMC\_CSx, FSMC\_RE and FSMC\_WE and 10 pF on FSMC\_ADDR\_LE and FSMC\_CMD\_LE.

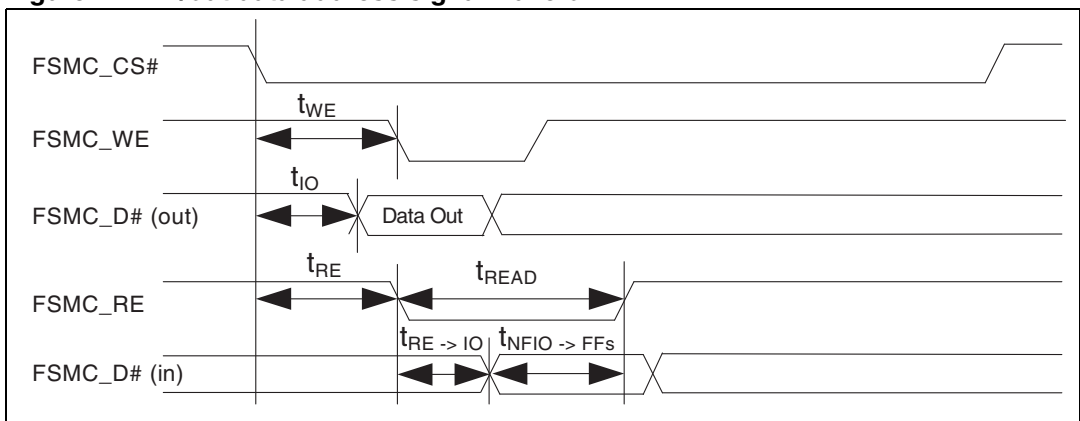
**Figure 22. Output command signal waveform**



**Figure 23. Output address signal waveform**



**Figure 24. In/out data address signal waveform**



**Table 64. FSMC timing requirements**

| Symbol                           | Min                                     | Max                                     |
|----------------------------------|---|---|
| t <sub>CLE</sub>                 | -3.9                                    | 2.8                                     |
| t <sub>ALE</sub>                 | -4.2                                    | 2.6                                     |
| t <sub>WE</sub> <sup>(1)</sup>   | $((Tset+1) * t_{HCLK}) - 3 \text{ ns}$  | $((Tset+1) * t_{HCLK}) + 3 \text{ ns}$  |
| t <sub>RE</sub> <sup>(1)</sup>   | $((Tset+1) * t_{HCLK}) - 3 \text{ ns}$  | $((Tset+1) * t_{HCLK}) + 3 \text{ ns}$  |
| t <sub>IO</sub> <sup>(2)</sup>   | $((Thiz +1) * t_{HCLK}) - 3 \text{ ns}$ | $((Thiz +1) * t_{HCLK}) + 3 \text{ ns}$ |
| t <sub>READ</sub> <sup>(3)</sup> | $((Twait+1) * t_{HCLK})$                |   |

1. Programmable by the Tset bits in the FSMC registers.
2. Programmable by the Thiz bits in the FSMC registers.
3. Programmable by the Twait bits in the FSMC registers.

*Note:* Values in [Table 64](#) refer to the common internal source clock which has a period of t<sub>HCLK</sub> = 6 ns.

**Table 65. FSMC signals timing requirements**

| Direction | Signal name      | Max       | Min      | Data path width | Unit |
|-----------|------------------|-----------|----------|-----------------|------|
| Output    | FSMC_CMD_LE      | 10.57     | 3.1      |                 | ns   |
|           | FSMC_ADDR_LE     | 9.5       | 2.8      |                 |      |
|           | FSMC_WE          | 8.5       | 2.9      |                 |      |
|           | FSMC_RE          | 8.4       | 2.75     |                 |      |
|           | FSMC_CS0         | 9.165836  | 3.07661  |                 |      |
|           | FSMC_CS1         | 8.473722  | 2.81431  |                 |      |
|           | FSMC_CS2         | 9.172739  | 3.02958  |                 |      |
|           | FSMC_CS3         | 9.808426  | 3.21934  |                 |      |
|           | FSMC_D7-FSMC_D0  | 7.710164  | 2.298715 | 8-bit           |      |
|           | FSMC_D15-FSMC_D8 | 9.301547  | 2.420165 | 8-bit           |      |
|           | FSMC_D15-FSMC_D0 | 9.301547  | 2.298715 | 16-bit          |      |
| Input     | FSMC_RDY/BUSY    | 6.88      | 1.7      |                 |      |
|           | FSMC_D7-FSMC_D0  | 8.8809    | 1.18356  | 8-bit           |      |
|           | FSMC_D15-FSMC_D8 | 10.875302 | 1.37802  | 8-bit           |      |
|           | FSMC_D15-FSMC_D0 | 10.875302 | 1.18356  | 16-bit          |      |

## 5.10 GPIO/XGPIO timing characteristics

For edge-sensitive signals, the interrupt line is sampled by flip flops clocked by PCLK for GPIOs and HCLK for XGPIOs, the APB and AHB clocks, normally running at 83 MHz and 166 MHz respectively.

The minimum pulse width required for interrupt detection on signal edge is:

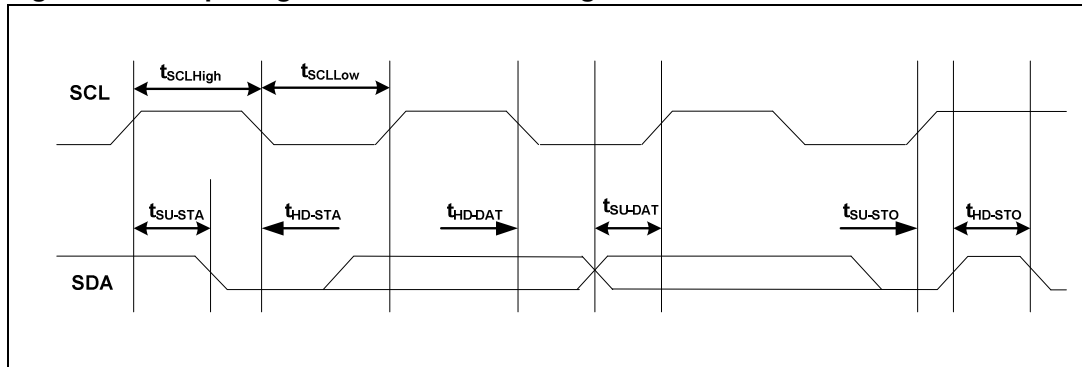
$3 \cdot T_{PCLK}$  (36 ns at 83 MHz) for GPIO

$3 \cdot T_{HCLK}$  (18 ns at 166 MHz) for XGPIO

## 5.11 I<sup>2</sup>C timing characteristics

The timing characterization is performed using primetime assuming an output load capacitance of 10 pF on SCL and SDA.

**Figure 25. Output signal waveform for I<sup>2</sup>C signals**



The timings of the high and low level of SCL ( $t_{SCLHigh}$  and  $t_{SCLLow}$ ) are programmable.

The clock-to-output data delay is:

- MIN (T(clk+data)min) = 5.9
- MAX (T(clk+data)max) = 15

The timings shown in [Figure 25](#) depend on the programmed value of  $t_{SCLHigh}$  and  $t_{SCLLow}$ . The values listed in [Table 66](#) to [Table 68](#) have been calculated using the minimum programmable values of :

- High-speed mode: IC\_HS\_SCL\_HCNT= 19 and IC\_HS\_SCL\_LCNT= 53 registers
- Fast-speed mode: IC\_FS\_SCL\_HCNT= 99 and IC\_FS\_SCL\_LCNT= 215 registers
- Standard-speed mode: IC\_SS\_SCL\_HCNT= 664 and IC\_SS\_SCL\_LCNT= 780 registers

These minimum values depend on the AHB clock frequency, which is 166 MHz.

- Note:**
- 1 A device may internally require a hold time of at least 300 ns for the SDA signal (referred to the  $V_{IHmin}$  of the SCL signal) to bridge the undefined region of the falling edge of SCL (Please refer to the I<sup>2</sup>C Bus Specification v3-0 Jun 2007). However, the SDA data hold time in the I<sup>2</sup>C controller of SPEAr320S is one-clock cycle based (6 ns with the HCLK clock at 166 MHz). This time may be insufficient for some slave devices. A few slave devices may not receive the valid address due to the lack of SDA hold time and will not acknowledge even if the address is valid. If the SDA data hold time is insufficient, an error may occur.
  - 2 **Workaround:** If a device needs more SDA data hold time than one clock cycle, an RC delay circuit is needed on the SDA line as illustrated in [Figure 26](#).

Figure 26. RC delay circuit

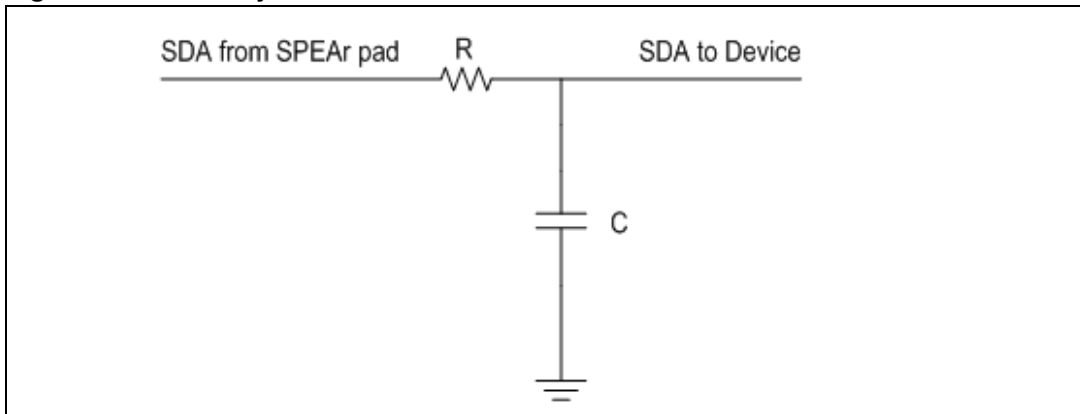


Table 66. I<sup>2</sup>C timing requirements in high-speed mode

| Parameter           | Min  | Unit |
|---------------------|------|------|
| t <sub>SU-STA</sub> | 140  | ns   |
| t <sub>HD-STA</sub> | 325  |      |
| t <sub>SU-DAT</sub> | 300  |      |
| t <sub>HD-DAT</sub> | 1    |      |
| t <sub>SU-STO</sub> | 620  |      |
| t <sub>HD-STO</sub> | 4745 |      |

Table 67. I<sup>2</sup>C timing requirements in fast-speed mode

| Parameter           | Min  | Unit |
|---------------------|------|------|
| t <sub>SU-STA</sub> | 620  | ns   |
| t <sub>HD-STA</sub> | 602  |      |
| t <sub>SU-DAT</sub> | 1270 |      |
| t <sub>HD-DAT</sub> | 1    |      |
| t <sub>SU-STO</sub> | 620  |      |
| t <sub>HD-STO</sub> | 4745 |      |

Table 68. I<sup>2</sup>C timing requirements in standard-speed mode

| Parameter           | Min  | Unit |
|---------------------|------|------|
| t <sub>SU-STA</sub> | 4718 | ns   |
| t <sub>HD-STA</sub> | 3992 |      |
| t <sub>SU-DAT</sub> | 4660 |      |
| t <sub>HD-DAT</sub> | 1    |      |
| t <sub>SU-STO</sub> | 4010 |      |
| t <sub>HD-STO</sub> | 4745 |      |

### 5.12 I2S timing characteristics

Figure 27. I2S waveform

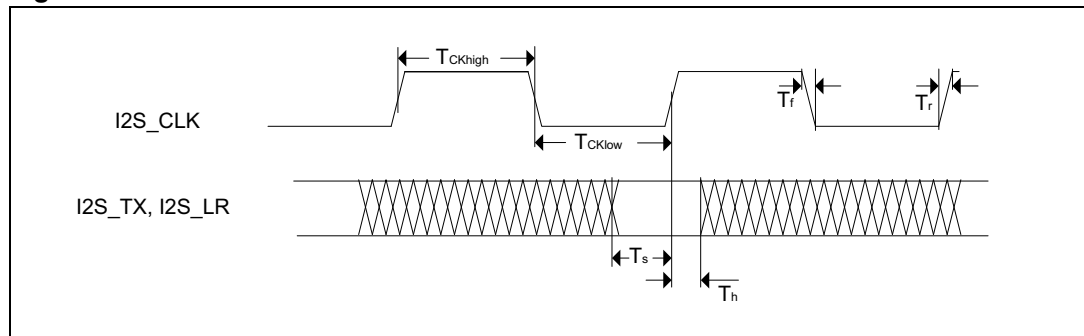


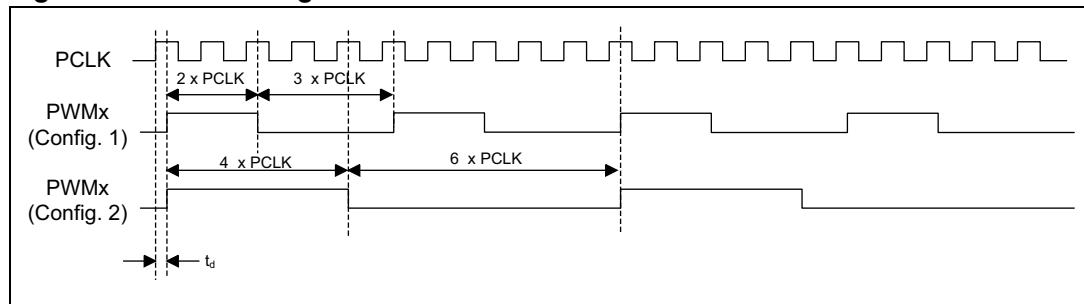
Table 69. I2S timing requirements

| Symbol   | Description                        | Min | Max | Unit |
|----------|------------------------------------|-----|-----|------|
| $t_{CK}$ | I2S_CLK clock period               | 40  |     | ns   |
| $t_D$    | I2S_CLK to I2S_TX output delay     | 3.8 | 9   |      |
| $t_S$    | Setup time requirement for I2S_CLK | 6   |     |      |
| $t_H$    | Hold time requirement for I2S_CLK  | 1   |     |      |

### 5.13 PWM timing characteristics

This section describes the timing characteristics of the four PWM generators. [Figure 28](#) shows two PWM waveforms in two example configurations programmed using the PWM registers.

Figure 28. PWM timing waveforms



**Config. 1:** Prescaler<sub>x</sub> = 0, Duty\_reg\_x = 2, Period\_Reg\_x = 4.

**Config. 2:** Prescaler<sub>x</sub> = 1, Duty\_reg\_x = 2, Period\_Reg\_x = 4.

**Calculations** (in PLCK periods):

$$PWMxDuty = (Prescaler_x + 1) * Duty\_reg\_x$$

$$PWMx\ Period = (Prescaler_x + 1) * (Period\_Reg\_x = 1)$$

Table 70. PWM timing characteristics

| Symbol | Parameter   | PWM Channel | External pin | Min | Max  | Unit |
|--------|---|-------------|--------------|-----|------|------|
| $t_d$  | PWM path delay from PWM internal output to output on external pin | PWM1        | PL_GPIO_9    | 4.1 | 14.3 | ns   |
|        |   |             | PL_GPIO_15   | 3.9 | 13.7 |      |
|        |   |             | PL_GPIO_31   | 4.3 | 15.1 |      |
|        |   |             | PL_GPIO_38   | 4.2 | 14.6 |      |
|        |   |             | PL_GPIO_43   | 4.0 | 14.3 |      |
|        |   |             | PL_GPIO_60   | 4.0 | 13.8 |      |
|        |   | PWM2        | PL_GPIO_89   | 3.4 | 10.4 |      |
|        |   |             | PL_GPIO_8    | 4.3 | 15.2 |      |
|        |   |             | PL_GPIO_14   | 4.0 | 14.3 |      |
|        |   |             | PL_GPIO_30   | 4.3 | 15.0 |      |
|        |   |             | PL_GPIO_37   | 4.2 | 15.0 |      |
|        |   |             | PL_GPIO_42   | 4.2 | 14.5 |      |
|        |   | PWM3        | PL_GPIO_59   | 4.2 | 13.8 |      |
|        |   |             | PL_GPIO_88   | 3.3 | 11.0 |      |
|        |   |             | PL_GPIO_7    | 4.4 | 15.1 |      |
|        |   |             | PL_GPIO_13   | 4.5 | 15.8 |      |
|        |   |             | PL_GPIO_29   | 4.3 | 15.3 |      |
|        |   |             | PL_GPIO_34   | 4.5 | 15.8 |      |
|        |   | PWM4        | PL_GPIO_41   | 3.9 | 13.8 |      |
|        |   |             | PL_GPIO_58   | 4.1 | 14.2 |      |
|        |   |             | PL_GPIO_87   | 3.4 | 11.5 |      |
|        |   |             | PL_GPIO_6    | 4.2 | 14.7 |      |
|        |   |             | PL_GPIO_12   | 4.0 | 13.9 |      |
|        |   |             | PL_GPIO_28   | 4.5 | 15.3 |      |
|        |   |             | PL_GPIO_40   | 4.3 | 15.1 |      |
|        |   |             | PL_GPIO_57   | 4.4 | 15.3 |      |
|        |   |             | PL_GPIO_86   | 3.5 | 11.9 |      |

### 5.14 SD timing characteristics

Figure 29. SD timing waveform

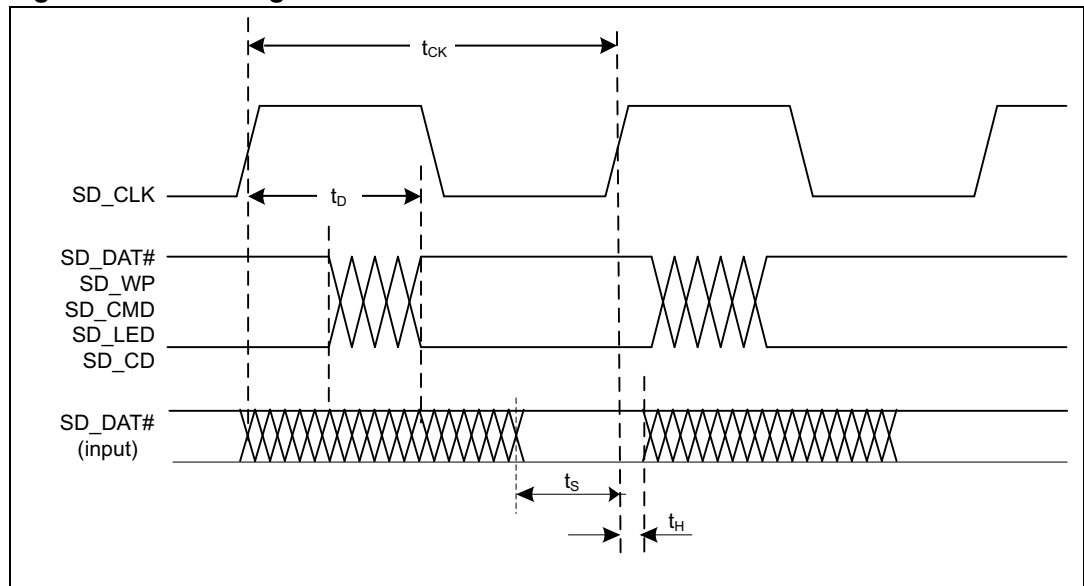


Table 71. SD timing requirements (high-speed mode, 48 MHz)

| Symbol   | Description                          | Min   | Max | Unit |
|----------|--------------------------------------|-------|-----|------|
| $t_{CK}$ | SD_CLK clock period                  | 20.8  | –   | ns   |
| $t_D$    | SD_CLK to SD output delay            | -1.60 | 10  |      |
| $t_S$    | Setup time requirement for SD inputs | 7.35  |     |      |
| $t_H$    | Hold time requirement for SD inputs  | 0.19  |     |      |

Table 72. SD timing requirements (full-speed mode, 24 MHz)

| Symbol        | Description                          | Min   | Max | Unit |
|---------------|--------------------------------------|-------|-----|------|
| $t_{CK}$      | SD_CLK clock period                  | 41.6  | –   | ns   |
| $t_{ck-half}$ | SD_CLK half period                   | 20.8  |     |      |
| $t_D$         | SD_CLK to SD output delay            | -0.40 | 10  |      |
| $t_S$         | Setup time requirement for SD inputs | 7.35  |     |      |
| $t_H$         | Hold time requirement for SD inputs  | 0.19  |     |      |

Note: In full-speed mode, the frequency is 24 MHz (41.6 ns). The data is launched at the falling edge of the 24 MHz clock and captured on the clock's rising edge (the effective available time is always 20.8 ns)



### 5.15 SMI timing characteristics

Figure 30. SMI input/output waveform

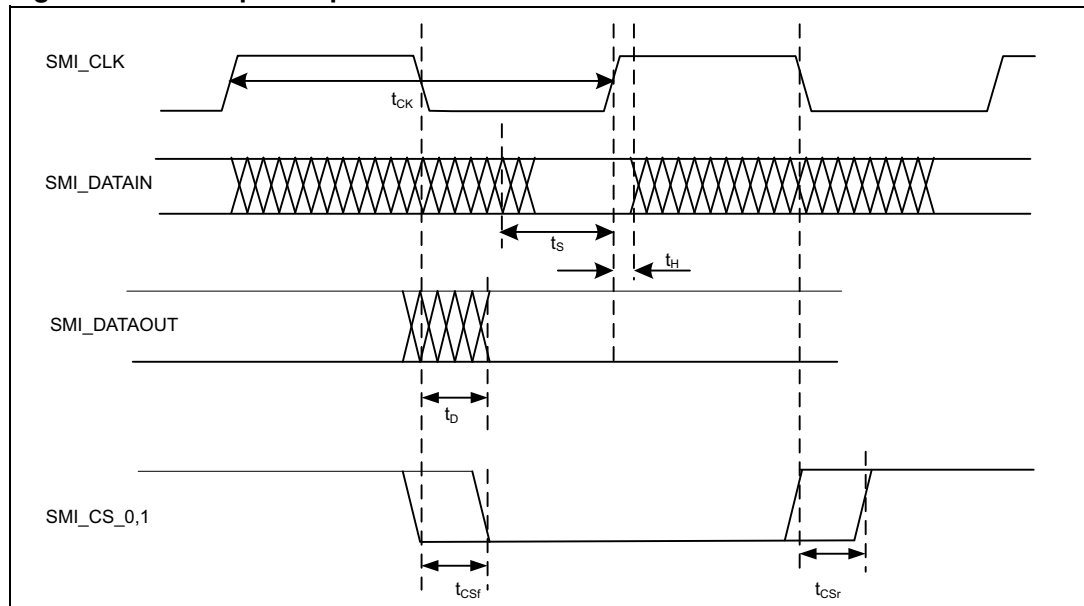


Table 73. SMI timing requirements

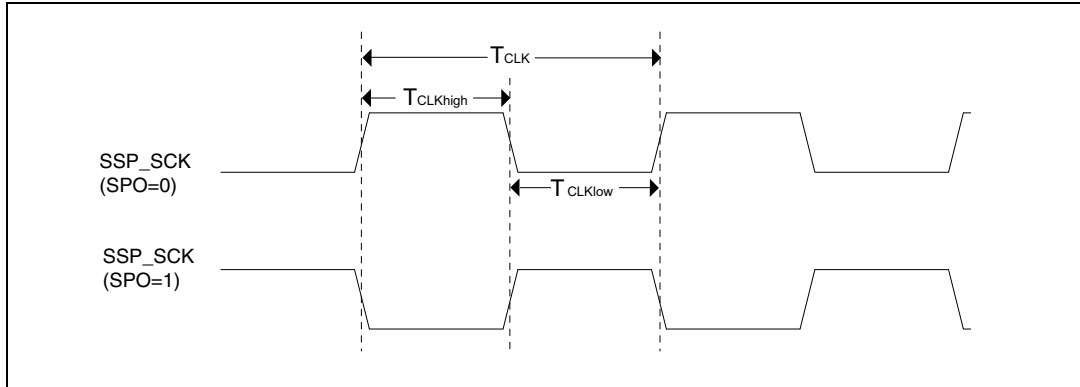
| Symbol    | Description  | Min   | Max  | Unit |
|-----------|--|-------|------|------|
| $t_{CK}$  | SMI clock period   | 20    | 50   | ns   |
| $t_D$     | SMI_CLK to SMI_DATAOUT output delay  | -2.96 | 3.05 |      |
| $t_S$     | Setup requirement for SMI_DATAIN   | 8.05  |      |      |
| $t_H$     | Hold requirement for SMI_DATAIN  | -2.53 |      |      |
| $t_{CSf}$ | Minimum and maximum delay of falling edge of SMI_CS_0 , 1 with regard to SMI_CLK | -3.0  | 2.9  |      |
| $t_{CSr}$ | Minimum and maximum delay of rising edge of SMI_CS_0 , 1 with regard to SMI_CLK  | -2.8  | 2.8  |      |

### 5.16 SSP timing characteristics

This section describes the timing characteristics of the synchronous serial port.

*Note:* The characterization of the SSP has been done using the SPI protocol.

**Figure 31. SSP\_SCK waveform**



The clock polarity parameter (SPO) indicates the state of the clock signal when it is idle. This can be programmed in the SSPCR0 register.

- SPO= 0 The clock idle state is low.
- SPO= 1 The clock idle state is high.

#### 5.16.1 SPI master mode timings

SSP\_SCK is the SPI output clock.

$T_{PCLK}$  is the clock period of the PCLK internal clock.

**Figure 32. SPI master mode external timing waveform (SPH= 0, SPO =0)**

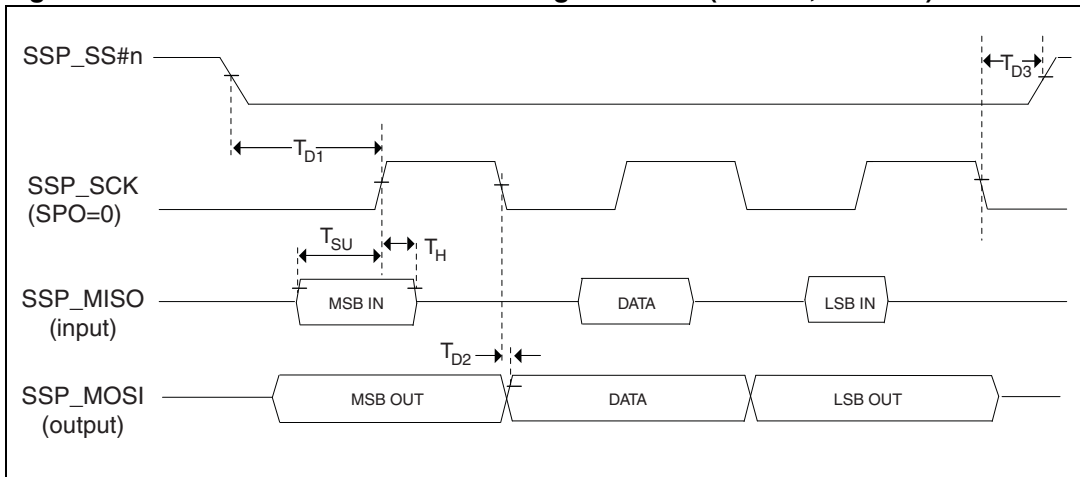


Table 74. SPI master mode timing characteristics (SPH = 0, SPO=0)

| Symbol          | Parameters   |      | Min                            | Max                             | Unit |
|-----------------|--|------|--------------------------------|---------------------------------|------|
| T <sub>SU</sub> | Setup time, MISO (input) valid before SSP_SCK (output) rising edge               | SSP0 | 7.8                            |                                 | ns   |
|                 |  | SSP1 | 16                             |                                 |      |
|                 |  | SSP2 | 15.55                          |                                 |      |
| T <sub>H</sub>  | Hold time, MISO (input) valid after SSP_SCK (output) rising edge                 | SSP0 | -2.7                           |                                 | ns   |
|                 |  | SSP1 | -4                             |                                 |      |
|                 |  | SSP2 | -4.6                           |                                 |      |
| T <sub>D1</sub> | Delay time, SSP_SS#n (output) falling edge to first SSP_SCK (output) rising edge | SSP0 | T <sub>SSP_SCK</sub> -10       | T <sub>SSP_SCK</sub> -3         | ns   |
|                 |  | SSP1 | T <sub>SSP_SCK</sub> -6.4      | T <sub>SSP_SCK</sub> -0.9       |      |
|                 |  | SSP2 | T <sub>SSP_SCK</sub> -5.87     | T <sub>SSP_SCK</sub> -0.03      |      |
| T <sub>D2</sub> | Delay time, SSP_SCK (output) falling edge to MOSI (output) transition            | SSP0 | 2.7                            | 9.5                             | ns   |
|                 |  | SSP1 | 0.57                           | 5.34                            |      |
|                 |  | SSP2 | 0.2                            | 5.53                            |      |
| T <sub>D3</sub> | Delay time, SSP_SCK (output) falling edge to SSP_SS#n (output) rising edge       | SSP0 | (T <sub>SSP_SCK</sub> /2)+ 3   | (T <sub>SSP_SCK</sub> /2) +8    | ns   |
|                 |  | SSP1 | (T <sub>SSP_SCK</sub> /2)+ 0.9 | (T <sub>SSP_SCK</sub> /2) +6.4  |      |
|                 |  | SSP2 | (T <sub>SSP_SCK</sub> /2)-0.03 | (T <sub>SSP_SCK</sub> /2) +5.87 |      |

Figure 33. SPI master mode external timing waveform (SPH= 0, SPO =1 )

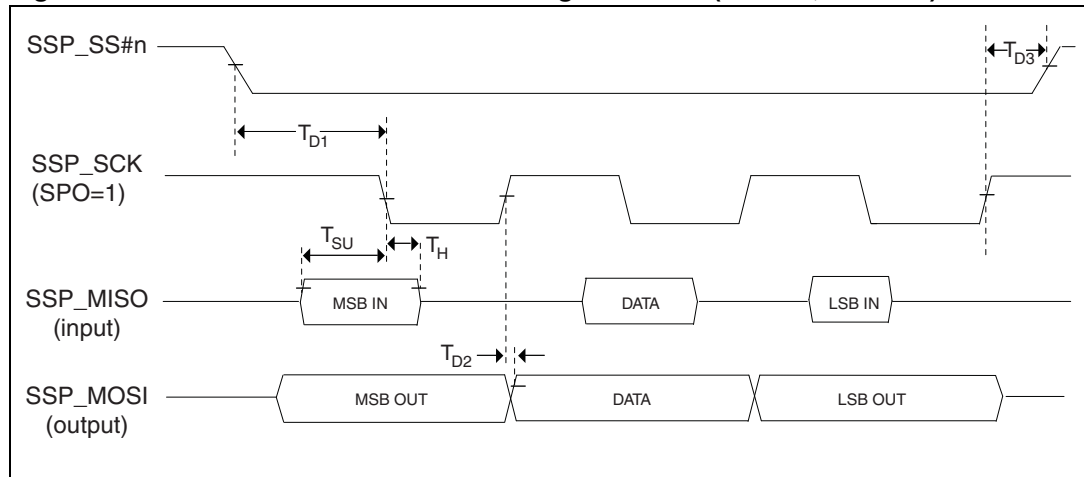


Table 75. SPI master mode timing characteristics (SPH = 0, SPO=1)

| Symbol          | Parameters  |      | Min                            | Max                             | Unit |
|-----------------|---|------|--------------------------------|---------------------------------|------|
| T <sub>SU</sub> | Setup time, MISO (input) valid before SSP_SCK (output) falling edge               | SSP0 | 7.8                            |                                 | ns   |
|                 |   | SSP1 | 16                             |                                 |      |
|                 |   | SSP2 | 15.55                          |                                 |      |
| T <sub>H</sub>  | Hold time, MISO (input) valid after SSP_SCK (output) falling edge                 | SSP0 | -2.7                           |                                 | ns   |
|                 |   | SSP1 | -4                             |                                 |      |
|                 |   | SSP2 | -4.6                           |                                 |      |
| T <sub>D1</sub> | Delay time, SSP_SS#n (output) falling edge to first SSP_SCK (output) falling edge | SSP0 | T <sub>SSP_SCK</sub> -10       | T <sub>SSP_SCK</sub> -3         | ns   |
|                 |   | SSP1 | T <sub>SSP_SCK</sub> -6.4      | T <sub>SSP_SCK</sub> -0.9       |      |
|                 |   | SSP2 | T <sub>SSP_SCK</sub> -5.87     | T <sub>SSP_SCK</sub> -0.03      |      |
| T <sub>D2</sub> | Delay time, SSP_SCK (output) rising edge to MOSI (output) transition              | SSP0 | 2.7                            | 9.5                             | ns   |
|                 |   | SSP1 | 0.57                           | 5.34                            |      |
|                 |   | SSP2 | 0.2                            | 5.53                            |      |
| T <sub>D3</sub> | Delay time, SSP_SCK (output) rising edge to SSP_SS#n (output) rising edge         | SSP0 | (T <sub>SSP_SCK</sub> /2)+ 3   | (T <sub>SSP_SCK</sub> /2) +8    | ns   |
|                 |   | SSP1 | (T <sub>SSP_SCK</sub> /2)+ 0.9 | (T <sub>SSP_SCK</sub> /2) +6.4  |      |
|                 |   | SSP2 | (T <sub>SSP_SCK</sub> /2)-0.03 | (T <sub>SSP_SCK</sub> /2) +5.87 |      |

Figure 34. SPI master mode external timing waveform (SPH = 1, SPO = 0)

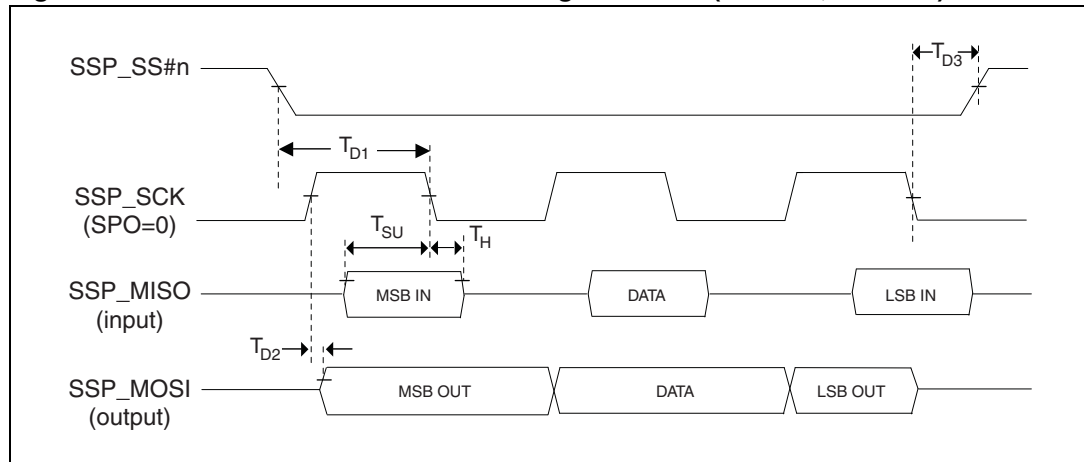


Table 76. SPI master mode timing characteristics (SPH = 1, SPO=0)

| Symbol          | Parameters  |      | Min                            | Max                            | Unit |
|-----------------|---|------|--------------------------------|--------------------------------|------|
| T <sub>SU</sub> | Setup time, MISO (input) valid before SSP_SCK (output) falling edge               | SSP0 | 7.8                            |                                | ns   |
|                 |   | SSP1 | 16                             |                                |      |
|                 |   | SSP2 | 15.55                          |                                |      |
| T <sub>H</sub>  | Hold time, MISO (input) valid after SSP_SCK (output) falling edge                 | SSP0 | -2.7                           |                                | ns   |
|                 |   | SSP1 | -4                             |                                |      |
|                 |   | SSP2 | -4.6                           |                                |      |
| T <sub>D1</sub> | Delay time, SSP_SS#n (output) falling edge to first SSP_SCK (output) falling edge | SSP0 | (T <sub>SSP_SCK</sub> /2)-10   | (T <sub>SSP_SCK</sub> /2)-3    | ns   |
|                 |   | SSP1 | (T <sub>SSP_SCK</sub> /2)-6.4  | (T <sub>SSP_SCK</sub> /2)-0.9  |      |
|                 |   | SSP2 | (T <sub>SSP_SCK</sub> /2)-5.87 | (T <sub>SSP_SCK</sub> /2)-0.03 |      |
| T <sub>D2</sub> | Delay time, SSP_SCK (output) rising edge to MOSI (output) transition              | SSP0 | 2.7                            | 9.5                            | ns   |
|                 |   | SSP1 | 0.57                           | 5.34                           |      |
|                 |   | SSP2 | 0.2                            | 5.53                           |      |
| T <sub>D3</sub> | Delay time, SSP_SCK (output) rising edge to SSP_SS#n (output) rising edge         | SSP0 | T <sub>SSP_SCK</sub> + 3       | (T <sub>SSP_SCK</sub> + 10)    | ns   |
|                 |   | SSP1 | T <sub>SSP_SCK</sub> + 0.9     | (T <sub>SSP_SCK</sub> + 6.4)   |      |
|                 |   | SSP2 | T <sub>SSP_SCK</sub> - 0.03    | T <sub>SSP_SCK</sub> + 5.87    |      |

Figure 35. SPI master mode external timing waveform (SPH = 1, SPO = 1)

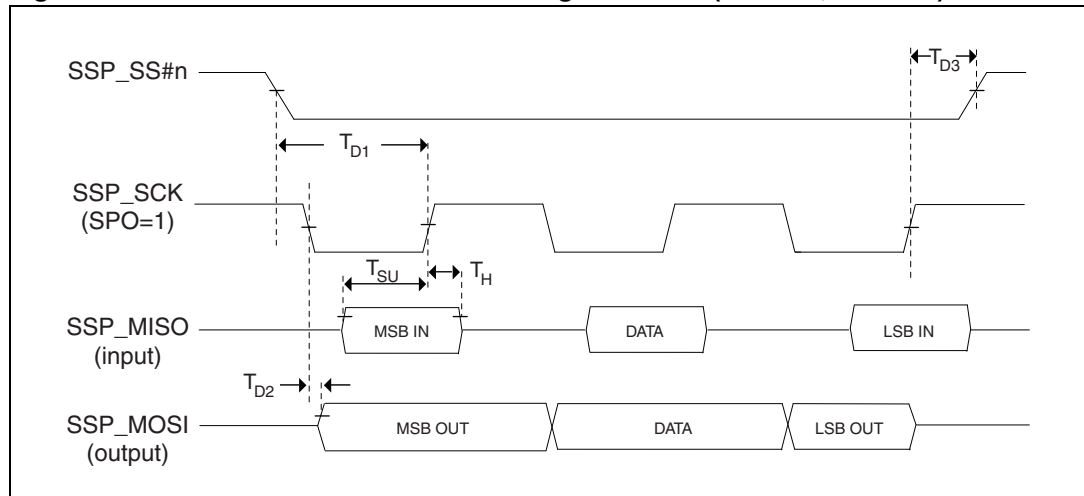


Table 77. SPI master mode timing characteristics (SPH = 1, SPO=1)

| Symbol          | Parameters   | Min  | Max                            | Unit                           |    |
|-----------------|--|------|--------------------------------|--------------------------------|----|
| T <sub>SU</sub> | Setup time, MISO (input) valid before SSP_SCK (output) rising edge               | SSP0 | 7.8                            | ns                             |    |
|                 |  | SSP1 | 16                             |                                |    |
|                 |  | SSP2 | 15.55                          |                                |    |
| T <sub>H</sub>  | Hold time, MISO (input) valid after SSP_SCK (output) rising edge                 | SSP0 | -2.7                           | ns                             |    |
|                 |  | SSP1 | -4                             |                                |    |
|                 |  | SSP2 | -4.6                           |                                |    |
| T <sub>D1</sub> | Delay time, SSP_SS#n (output) falling edge to first SSP_SCK (output) rising edge | SSP0 | (T <sub>SSP_SCK</sub> /2)-10   | (T <sub>SSP_SCK</sub> /2)-3    | ns |
|                 |  | SSP1 | (T <sub>SSP_SCK</sub> /2)-6.4  | (T <sub>SSP_SCK</sub> /2)-0.9  |    |
|                 |  | SSP2 | (T <sub>SSP_SCK</sub> /2)-5.87 | (T <sub>SSP_SCK</sub> /2)-0.03 |    |
| T <sub>D2</sub> | Delay time, SSP_SCK (output) falling edge to MOSI (output) transition            | SSP0 | 2.7                            | 9.5                            | ns |
|                 |  | SSP1 | 0.57                           | 5.34                           |    |
|                 |  | SSP2 | 0.2                            | 5.53                           |    |
| T <sub>D3</sub> | Delay time, SSP_SCK (output) rising edge to SSP_SS#n (output) rising edge        | SSP0 | T <sub>SSP_SCK</sub> + 3       | (T <sub>SSP_SCK</sub> + 10)    | ns |
|                 |  | SSP1 | T <sub>SSP_SCK</sub> + 0.9     | (T <sub>SSP_SCK</sub> + 6.4)   |    |
|                 |  | SSP2 | T <sub>SSP_SCK</sub> - 0.03    | T <sub>SSP_SCK</sub> + 5.87    |    |

### 5.16.2 SPI slave mode timings

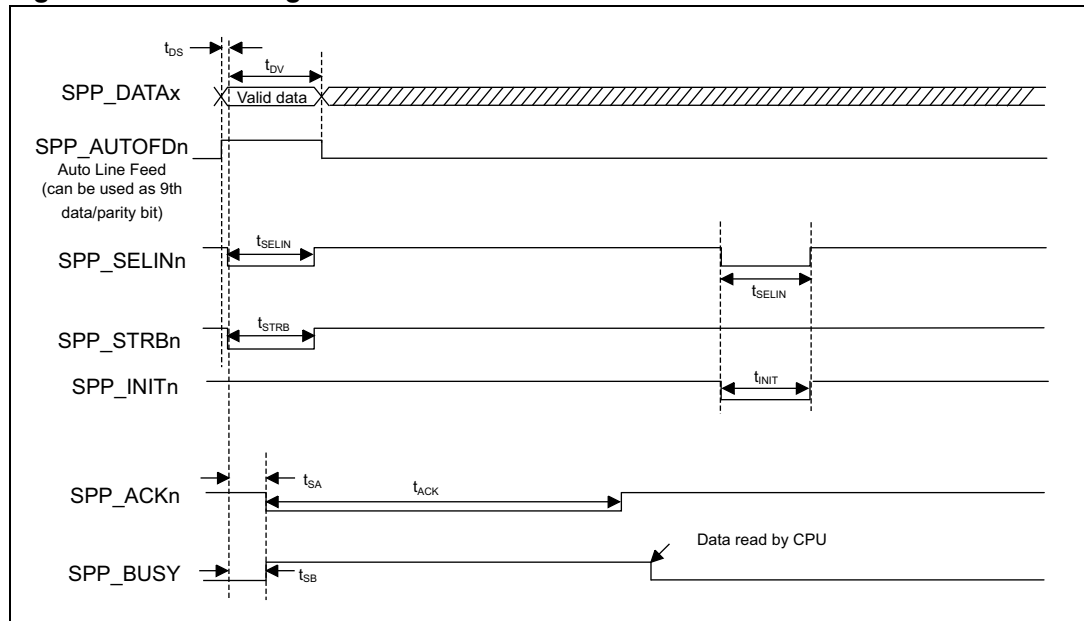
**Table 78. SSP timing characteristics (slave mode)**

| Symbol             | Parameters                    | Min                | Max                    | Unit |
|--------------------|-------------------------------|--------------------|------------------------|------|
| $T_{SSP\_CLK}$     | SSP_CLK_IN input clock period | $T_{PCLK} * 12$    | $254 * 256 * T_{PCLK}$ | ns   |
| $T_{SSP\_CLKHigh}$ | SSP_SCK high pulse            | $T_{SSP\_CLK} / 2$ |                        |      |
| $T_{SSP\_CLKLow}$  | SSP_SCK low pulse             | $T_{SSP\_CLK} / 2$ |                        |      |
| $T_{SU}$           | Data input setup time         | $4 * T_{PCLK}$     |                        |      |
| $T_H$              | Data input hold time          | 0                  |                        |      |
| $T_D$              | Data output delay             | $3 * T_{PCLK}$     | $4 * T_{PCLK}$         |      |

### 5.17 SPP timing characteristics

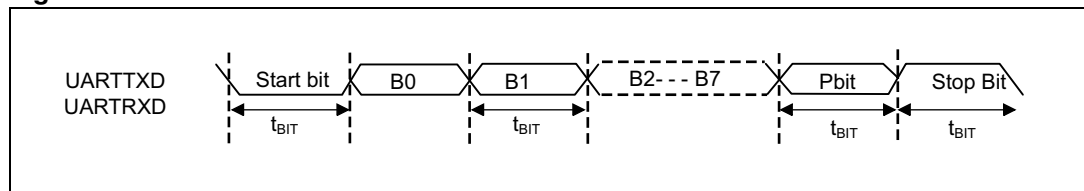
This section describes the timing characteristics of the standard parallel port (SPP).

**Figure 36. SPP timing waveform**



### 5.18 UART timing characteristics

**Figure 37. UART transmit and receive waveform**



**Table 79. UART transmit timing characteristics**

| Symbol                | Parameters  | Min  | Max  | Unit |
|-----------------------|---|--|--|------|
| $f_{\text{baudrate}}$ | UART1 .. UART6 baud rate  |  | 6 <sup>(1)</sup>                                 | Mbps |
|                       | UART0 baud rate   |  | 3  |      |
| $t_{\text{BIT}}$      | UART duration of transmit data bit (B0..B7), Parity bit (Pbit), Start bit, Stop bits <sup>(2)</sup> | $1/f_{\text{baudrate}} - t_{\text{UARTCLK}} - 1$ | $1/f_{\text{baudrate}} + t_{\text{UARTCLK}} + 1$ | ns   |

1. Maximum baudrate = 6 Mbps provided that UARTCLK is within a frequency range greater than 96 MHz and less than 5/3 PCLK.
2.  $t_{\text{UARTCLK}} = 1/f_{\text{UARTCLK}}$  with  $f_{\text{UARTCLK}}$  in MHz

**Table 80. UART receive timing characteristics**

| Symbol           | Parameter  | Conditions        | Min  | Max  | Unit |
|------------------|--|-------------------|--|--|------|
| $t_{\text{BIT}}$ | Pulse duration of receive data (B0 ..B7), Parity bit (Pbit), Start bit, Stop bits <sup>(1)</sup> | Baudrate = 6 Mbps | $1/f_{\text{baudrate}} - (t_{\text{UARTCLK}}/2)$       | $1/f_{\text{baudrate}} + (t_{\text{UARTCLK}}/2)$     | ns   |
|                  |  |                   | $1/f_{\text{baudrate}} - 1/(16 * f_{\text{baudrate}})$ | $1/f_{\text{baudrate}} + (16 * f_{\text{baudrate}})$ | ns   |

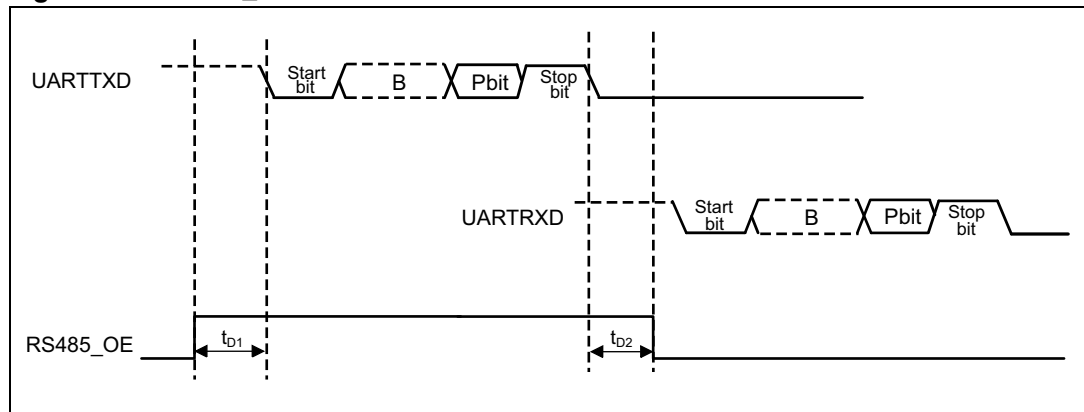
1. The time margin is with respect to a single bit accumulation and not with respect to the whole UART frame. The start bit is sampled after the 8th baud cycle after a low is detected at input, Subsequently, each bit is sampled at consecutive 16 baud cycles.

The above min. and max. values allow a deviation of  $\pm 1$  baud cycle in a single bit time. The accumulated deviation of a UART character frame must not exceed  $3/(16 * f_{\text{baudrate}})$ .

For information related to baud rate generation refer to:

- [Section 2.12: Asynchronous serial ports \(UART\)](#)
- *RM0321, Reference manual, SPEAr320S address map and registers*

**Figure 38. RS485\_OE transmit and receive waveform**





**Table 81. RS485\_OE transmit and receive timing characteristics**

| Symbol   | Parameters  | Min | Max | Unit |
|----------|---|-----|-----|------|
| $t_{D1}$ | Delay from OE enable till UART first bit transmission | 500 |     | ns   |
| $t_{D2}$ | Delay from UART last bit transmission till OE enable  | 900 |     | ns   |

- Note:
- 1 The time value depends upon the CPU frequency to write and read registers.
  - 2 It also depends on the UART clock frequency used to set its flag register bit to indicate the end of transmission.

For example:

For  $t_{D2}$ , the above values are with respect to 83 MHz PCLK and UARTCLK 83 MHz.

## 6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

**Table 82. LFBGA289 (15 x 15 x 1.7 mm) mechanical data**

| Dim. | mm     |        |        | inches |        |        |
|------|--------|--------|--------|--------|--------|--------|
|      | Min.   | Type   | Max.   | Min.   | Type   | Max.   |
| A    |        |        | 1.700  |        |        | 0.0669 |
| A1   | 0.270  |        |        | 0.0106 |        |        |
| A2   |        | 0.985  |        |        | 0.0387 |        |
| A3   |        | 0.200  |        |        | 0.0078 |        |
| A4   |        |        | 0.800  |        |        | 0.0315 |
| b    | 0.450  | 0.500  | 0.550  | 0.0177 | 0.0197 | 0.0217 |
| D    | 14.850 | 15.000 | 15.150 | 0.5846 | 0.5906 | 0.5965 |
| D1   |        | 12.800 |        |        | 0.5039 |        |
| E    | 14.850 | 15.000 | 15.150 | 0.5846 | 0.5906 | 0.5965 |
| E1   |        | 12.800 |        |        | 0.5039 |        |
| e    |        | 0.800  |        |        | 0.0315 |        |
| F    |        | 1.100  |        |        | 0.0433 |        |
| ddd  |        |        | 0.200  |        |        | 0.0078 |
| eee  |        |        | 0.150  |        |        | 0.0059 |
| fff  |        |        | 0.080  |        |        | 0.0031 |

Figure 39. LFBGA289 package dimensions

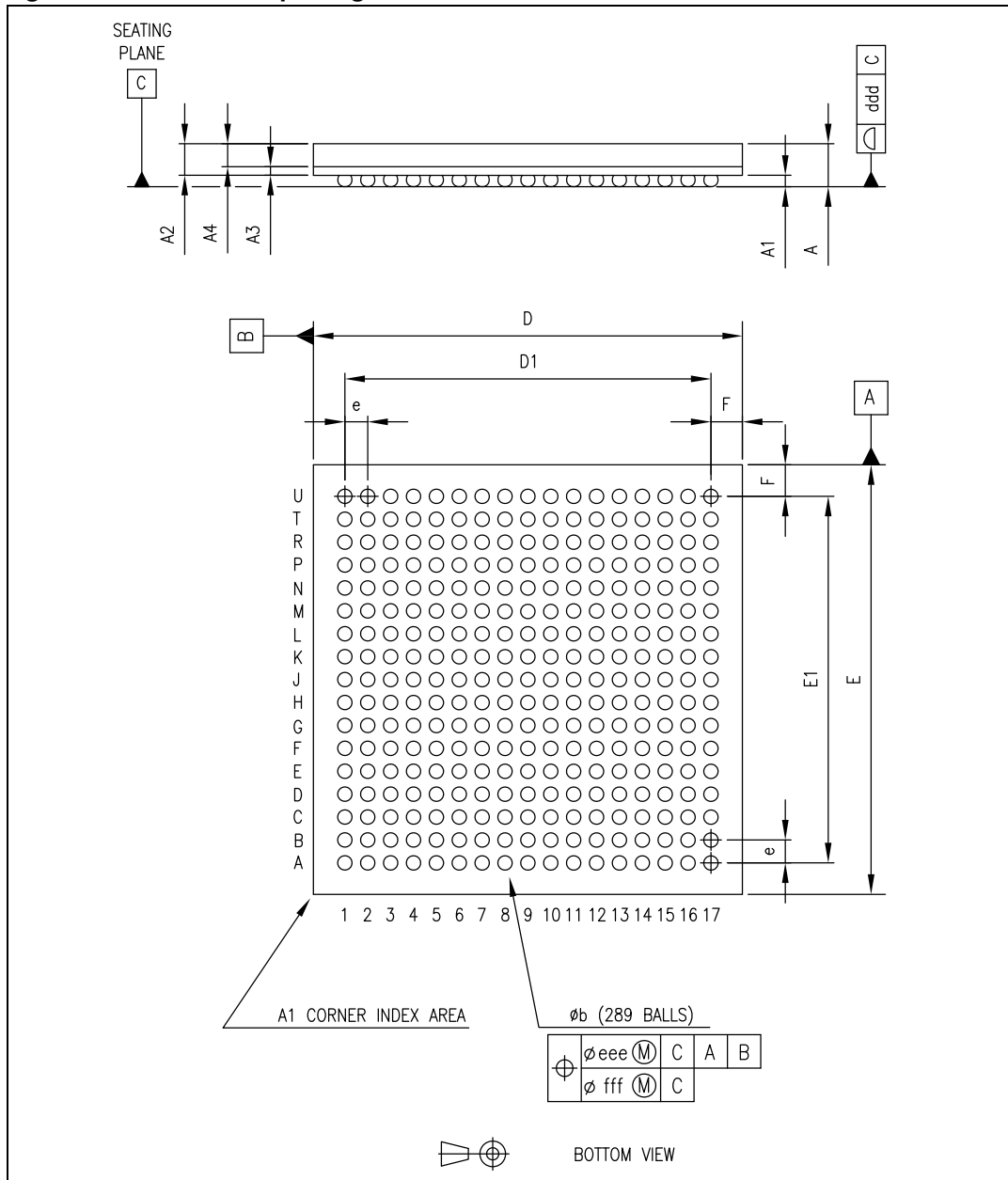


Table 83. LFBGA289 package thermal characteristics

| Symbol              | Parameter   | Value | Unit |
|---------------------|---|-------|------|
| $\Theta_{JA}^{(1)}$ | Thermal resistance junction-to-ambient              | 30    | °C/W |
| $\Theta_{JB}$       | Thermal resistance junction-to-board                | 21    |      |
| $\Theta_{JC}$       | Thermal resistance junction-to-case                 | 13.5  |      |
| $\Psi_{JC}$         | Junction-to-case thermal characterisation parameter | 0.48  |      |

1. Measured on JESD51 2s2p test board.

## Appendix A Acronyms

**Table 84. List of acronyms**

| Acronym | Definition                                       |
|---------|--|
| ADC     | Analog-to-digital converter                      |
| AES     | Advanced encryption standard                     |
| AHB     | AMBA high speed bus                              |
| AMBA    | Advanced microcontroller bus architecture        |
| APB     | Advanced peripheral bus                          |
| BIST    | Built-In self test                               |
| CAN     | Controller area network                          |
| CBC     | Cipher block chaining                            |
| CMOS    | Complimentary metal-oxide semiconductor          |
| CPU     | Central processing unit                          |
| CRC     | Cyclic redundancy check                          |
| DDR     | Double data rate                                 |
| DES     | Data encryption standard                         |
| DLL     | Delay locked loop (when applied to DDR memories) |
| DMA     | Direct memory access                             |
| EMI     | External memory interface                        |
| ETM     | Embedded trace macrocell                         |
| FIFO    | First-in-first-out                               |
| FIQ     | Fast interrupt request                           |
| FPGA    | Field programmable gate array                    |
| FSMC    | Flexible static memory controller                |
| GB      | Giga bytes                                       |
| GPIO    | General purpose input / output                   |
| HLOS    | High-level operating system                      |
| HMI     | Human machine interface                          |
| HW      | Hardware   |
| IrDA    | Infrared data association                        |
| IRQ     | Interrupt request                                |
| JPEG    | Joint photographic experts group                 |
| JTAG    | Joint test action group                          |
| KB      | Kilo bytes                                       |
| LCD     | Liquid color display                             |

**Table 84. List of acronyms (continued)**

| <b>Acronym</b> | <b>Definition</b>                           |
|----------------|---|
| LSB            | Least significant bit                       |
| MAC            | Media access control                        |
| MB             | Mega bytes                                  |
| MCU            | Microcontroller unit                        |
| MD5            | Message digest 5                            |
| MII            | Media independent interface                 |
| MMU            | Memory management unit                      |
| MSB            | Most significant bit                        |
| PHY            | Physical (device, transceiver, layer)       |
| PLL            | Phase locked loop                           |
| PWM            | Pulse width modulation                      |
| RAM            | Random access memory                        |
| RAS            | Reconfigurable array subsystem              |
| RF             | Radio frequency                             |
| RFU            | Reserved for future use                     |
| RISC           | Reduced instruction set computing           |
| RMI            | Reduced media independent interface         |
| ROM            | Read only memory                            |
| RTC            | Real-time clock                             |
| RTOS           | Real-time operating system                  |
| RX             | Receive                                     |
| SHA-1          | Secure hash algorithm                       |
| SMI            | Serial memory interface                     |
| SoC            | System-on-chip                              |
| SPI            | Serial peripheral interface                 |
| SPP            | Standard parallel port                      |
| SRAM           | Static RAM                                  |
| SSP            | Synchronous serial port                     |
| SW             | Software                                    |
| TCM            | Tightly coupled memory                      |
| TFT            | Thin film transistor, a display technology  |
| TX             | Transmit                                    |
| UART           | Universal asynchronous receiver transmitter |
| USB            | Universal serial bus                        |

**Table 84. List of acronyms (continued)**

| Acronym | Definition                    |
|---------|-------------------------------|
| VIC     | Vectored interrupt controller |
| WDT     | Watchdog timer                |

## Revision history

**Table 85. Document revision history**

| Date        | Revision | Changes  |
|-------------|----------|--|
| 5-Apr-2012  | 1        | Initial release.   |
| 27-Sep-2012 | 2        | <p><i>Figure 1: SPEAr320S architectural block diagram</i>: Replaced “4 KB SRAM” by “8 KB SRAM”.</p> <p><i>Section 2.2: Internal memories (BootROM/SRAM)</i>: Added “Boot from UART0” and “Boot from Ethernet MII0” to the list of bootstrap modes.</p> <p><i>Section 2.25: System controller (SYSCTR)</i>: Replaced “a low-speed oscillator” by “a crystal oscillator (24 MHz) or a low-frequency oscillator (32 KHz)” in Doze mode description.</p> <p><i>Table 32: Ball sharing during debug</i>: modified the configuration for pins TEST_2, TEST_3 and TEST_4.</p> <p><i>Section 3.4.2: Extended mode: RMI automation networking mode</i> revised descriptions of each mode.</p> <p><i>Section 3.4.5: Boot pins</i> added description of H[7:0] pins Ethernet MII0 boot and bypass mode.</p> <p>Updated <i>Figure 3: Hierarchical multiplexing scheme</i></p> <p>Added note on I/O direction below <i>Table 13: PL_GPIO / PL_CLK pins description</i></p> <p>Chaged order of columns and added reset states to <i>Table 15: PL_GPIO/PL_CLK multiplexing scheme and reset states</i></p> <p>Added <i>Section 3.5: PL_GPIO and PL_CLK pin sharing for debug and test modes</i></p> <p><i>Table 8: Debug pins description</i>:</p> <ul style="list-style-type: none"> <li>– Replaced “Test configuration ports” by “Debug mode configuration ports”</li> <li>– Deleted “For functional mode, they have to be set to zero” for pins TEST_0 to TEST_4.</li> <li>– Added a cross-reference.</li> <li>– Added bypass mode to <i>Table 14: Boot pins description</i></li> </ul> <p><i>Section 4.6: Clocking parameters</i>:</p> <ul style="list-style-type: none"> <li>– Added <i>Table 40: MCLK oscillator characteristics</i> and new <i>Section : MCLK generated from a crystal oscillator</i>.</li> </ul> <p>Added <i>Table 42: RTC oscillator characteristics</i> and new <i>Section : RTC clock generated from an external clock source</i>. <i>Section 4.11: Reset release</i>:</p> <ul style="list-style-type: none"> <li>– Updated the introduction.</li> <li>– Renamed and updated <i>Figure 7: Cold reset release</i>.</li> <li>– Added new <i>Figure 8: Warm reset release</i>.</li> </ul> <p><i>Table 50: Reset timing characteristics</i>: added new row for warm reset.</p> |

Table 85. Document revision history (continued)

| Date        | Revision   | Changes   |
|-------------|------------|---|
| 27-Sep-2012 | 2 (cont'd) | <p>Added <a href="#">Section 5.3: CAN timing characteristics</a></p> <p>Updated <a href="#">Section 5.5: DDR2/LPDDR timing characteristics</a></p> <p><a href="#">Section 5.7.3: MDC/MDIO timing characteristics</a>, corrected td min</p> <p>Updated <a href="#">Table 62: RMI TX timing requirements</a></p> <p><a href="#">Section 5.11: I2C timing characteristics</a> added note and diagram of RC circuit.</p> <p>Added <a href="#">Section 5.13: PWM timing characteristics</a></p> <p>Added <a href="#">Section 5.18: UART timing characteristics</a></p> <p><a href="#">Table 83: LFBGA289 package thermal characteristics</a>:</p> <ul style="list-style-type: none"> <li>– Modified <math>\Theta_{JA}</math>, <math>\Theta_{JB}</math>, <math>\Theta_{JC}</math> values.</li> <li>– Added <math>\Psi_{JC}</math> value.</li> </ul> |



**Please Read Carefully:**

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST's terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

**UNLESS OTHERWISE SET FORTH IN ST'S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.**

**UNLESS EXPRESSLY APPROVED IN WRITING BY TWO AUTHORIZED ST REPRESENTATIVES, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS "AUTOMOTIVE GRADE" MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER'S OWN RISK.**

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2012 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

[www.st.com](http://www.st.com)

