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CONTINUITY OF SPECIFICATIONS

There is no change to this document as a result of offering the device as a Cypress product. Any changes that have been made are the result of normal document improvements and are noted in the document history page, where supported. Future revisions will occur when appropriate, and changes will be noted in a document history page.

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BCM43243

Single-Chip IEEE 802.11 a/b/g/n 2×2 MAC/Baseband/Radio

GENERAL DESCRIPTION

The Broadcom® BCM43243 is a single-chip device for wireless media systems. It integrates a MAC, baseband, and radio that support IEEE 802.11 a/b/g and 2×2 IEEE 802.11n, and uses USB 2.0 as the WLAN host interface.

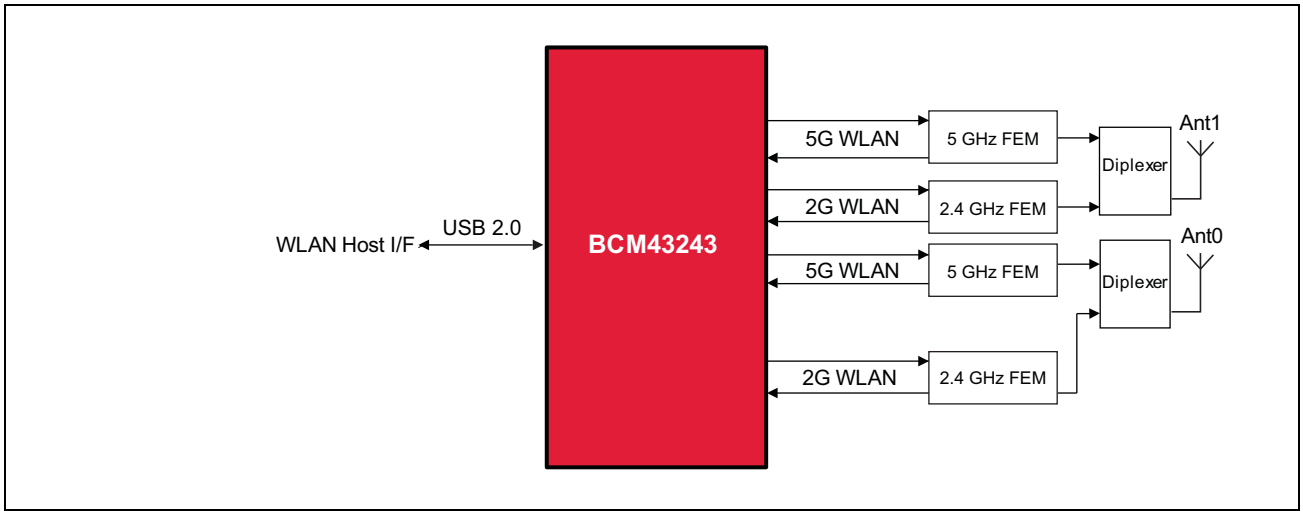
The BCM43243 takes advantage of the high throughput and extended range of the Broadcom second-generation MIMO solution. With MIMO, the information is sent and received over two or more antennas simultaneously using the same frequency band, providing greater range and higher throughput, while maintaining compatibility with legacy IEEE 802.11a/b/g devices. This is accomplished through a combination of enhanced MAC and PHY implementations, including spatial multiplexing modes in the transmitter and receiver and advanced digital signal processing techniques that improve receive sensitivity. The BCM43243 architecture, with its fully integrated dual-band radio transceiver, supports 2 × 2 antennas. It also supports 20 MHz and 40 MHz channels, allowing for PHY Layer throughput up to 300 Mbps.

GENERAL DESCRIPTION

Using advanced design techniques and process technology to reduce active and standby power, the BCM43243 is designed to address the needs of media-embedded applications that require minimal power consumption and compact size.

The BCM43243 includes a Power Management Unit (PMU) that simplifies the system power topology and allows for direct operation with a 3.3V or 5V supply, which provides flexibility. The BCM43243 includes power saving schemes such as single-core listen (OCL), single-core demodulation of SISO/STBC packets, and dynamic maximum likelihood (ML) demapping (which is based on channel conditions).

Figure 1: Functional Block Diagram



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FEATURES

IEEE 802.11x Features

- Single-band 2.4 GHz IEEE 802.11 b/g/n or dual-band 2.4 GHz and 5 GHz IEEE 802.11 a/b/g/n.
- Hardware support for virtual simultaneous dual-band operation with switching times less than 1 ms.
- Dual-stream IEEE 802.11n support for 20 MHz and 40 MHz channels provides PHY layer rates up to 300 Mbps for typical upper-layer throughput up to 200 Mbps.
- IEEE 802.11n STBC (space-time block coding) in both TX and RX for improved range and power efficiency.
- Integrated 2.4 GHz and 5 GHz power amplifiers as well as six RF control signals to control external RF switches or LNAs.
- Internal fractional nPLL allows support for a wide range of reference clock frequencies.
- Standard high-speed USB 2.0 host interface.
- Integrated ARM® Cortex-M3™ processor and on-chip memory for complete WLAN subsystem functionality, minimizing the need to wake up the applications processor (AP) for standard WLAN functions. (This allows for further minimization of power consumption, while maintaining the ability to field-upgrade with future features. On-chip memory includes 544 KB SRAM and 640 KB ROM.)
- OneDriver™ software architecture for easy migration from existing embedded WLAN devices as well as future devices.
- Advanced power topology allows for very low active and standby power.

FEATURES

General Features

- Programmable dynamic power management.
- 3072-bit OTP for storing board parameters.
- 16 general-purpose I/Os (GPIOs).
- FCFBGA package (10 mm × 10 mm, 0.4 mm pitch) allows low-cost 4-layer PCB design with no hidden vias.

Security

- WPA™ and WPA2™ (Personal) support for powerful encryption and authentication.
- AES and TKIP in hardware for faster data encryption and IEEE 802.11i compatibility.
- Reference WLAN subsystem provides Cisco® Compatible Extensions (CCX, CCX 2.0, CCX 3.0, CCX 4.0, CCX 5.0).
- Reference WLAN subsystem provides Wi-Fi Protected Setup (WPS).
- Worldwide regulatory support.

Revision History

Revision	*Date*	*Change Description*
43243-DS100-R	04/16/15	Initial release

Broadcom Corporation
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Irvine, CA 92617

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About This Document

Purpose and Audience

This data sheet provides details about the functional, operational, and electrical characteristics of the Broadcom BCM43243. It is intended for hardware design, application, and OEM engineers.

Acronyms and Abbreviations

In most cases, acronyms and abbreviations are defined on first use.

For a comprehensive list of acronyms and other terms used in Broadcom documents, go to: http://www.broadcom.com/press/glossary.php.

Document Conventions

The following conventions may be used in this document:

Convention	*Description*
Bold	User input and actions: for example, type **exit**, click **OK,** press **Alt+C**
`Monospace`	Code: `#include <iostream>` HTML: `<td rowspan = 3>` Command line commands and parameters: `wl [-l] <command>`
< >	Placeholders for *required* elements: enter your <username> or `wl <command>`
[ ]	Indicates *optional* command-line parameters: `wl [-l]` Indicates bit and byte ranges (inclusive): [0:3] or [7:0]

Technical Support

Broadcom provides customer access to a wide range of information, including technical documentation, schematic diagrams, product bill of materials, PCB layout information, and software updates through its customer support portal (https://support.broadcom.com). For a CSP account, contact your Sales or Engineering support representative.

In addition, Broadcom provides other product support through its Downloads & Support site (http://www.broadcom.com/support/).

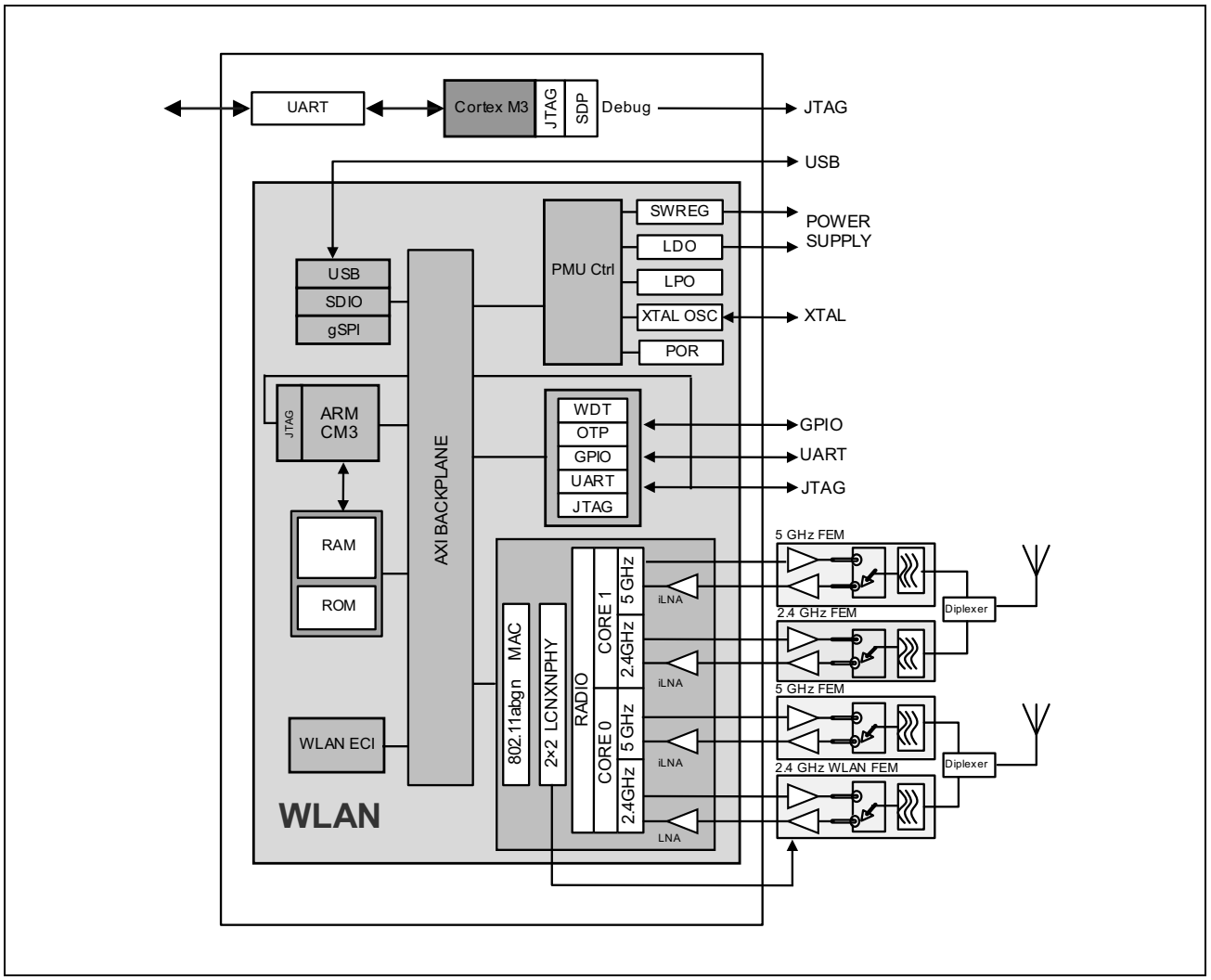
Section 1: Overview

Overview

The Broadcom BCM43243 is a single-chip IEEE 802.11 a/b/g and 2 × 2 IEEE 802.11n device for wireless media systems that integrates the MAC, baseband, and radio. BCM43243-based designs require few external components, provide size, form, and functional design flexibility, and can be produced in mass volumes at minimal cost.

Comprehensive power management circuitry and software ensure the system can meet the needs of media devices that require minimal power consumption and reliable operation. Figure 2 shows the interconnect of all the major physical blocks in the BCM43243 and their associated external interfaces, which are described in greater detail in the following sections.

Figure 2: BCM43243 Block Diagram



Features

The BCM43243 supports the following features:

- IEEE 802.11a/b/g/n dual-band radio—virtual simultaneous dual-band operation
- On-chip WLAN driver execution capable of supporting IEEE 802.11 functionality
- Single- and dual-antenna support
- WLAN high-speed USB 2.0 host interface

Standards Compliance

The BCM43243 supports the following standards:

- IEEE 802.11n—Handheld Device Class (Section 11)
- IEEE 802.11a, IEEE 802.11b, and IEEE 802.11g
- IEEE 802.11d
- IEEE 802.11h
- IEEE 802.11i

The BCM43243 supports the following future drafts/standards:

- IEEE 802.11r—Fast Roaming (between APs)
- IEEE 802.11k—Resource Management
- IEEE 802.11w—Secure Management Frames
- IEEE 802.11 Extensions:
  - IEEE 802.11e QoS Enhancements (as per the WMM® specification is already supported)
  - IEEE 802.11h 5 GHz Extensions
  - IEEE 802.11i MAC Enhancements
  - IEEE 802.11r Fast Roaming Support
  - IEEE 802.11k Radio Resource Measurement
- Security:
  - WLAN authentication and privacy infrastructure (WAPI)
  - WEP
  - WPA™ Personal
  - WPA2™ Personal
  - WMM
  - WMM-PS (U-APSD)
  - WMM-SA
  - AES (Hardware Accelerator)
  - TKIP (HW Accelerator)
  - CKIP (SW Support)

- Proprietary Protocols:
  - CCXv2, CCXv3, CCXv4, and CCXv5
  - WFAEC

Section 2: Power Supplies and Power Management

Power Supply Topology

One buck regulator, multiple LDO regulators, and a Power Management Unit (PMU) are integrated into the BCM43243. All regulators are programmable via the PMU. These blocks simplify power supply design for WLAN functions in embedded designs. Regulator inputs and outputs are brought out to pins on the BCM43243. This allows maximum flexibility for the system designer to choose which of the BCM43243 integrated regulators to use.

A 3.3V regulated supply can be used, with all additional voltages being provided by the regulators in the BCM43243.

The WL_REG_ON signal is used to power-up the regulators and take the respective section out of reset. The CBUCK, CLDO, and LNLDOs power up when any of the reset signals are deasserted. All regulators are powered down only when WL_REG_ON is deasserted. The CLDO and LNLDOs may be turned off/on based on the dynamic demands of the digital baseband.

The BCM43243 allows for an extremely low power-consumption mode by completely shutting down the CBUCK, CLDO, and LNDLO regulators. When in this state, LPLDO1 and LPLDO2 (which are low-power linear regulators that are supplied by the system VDDIO supply) provide the BCM43243 with all the voltages it requires, further reducing leakage currents.

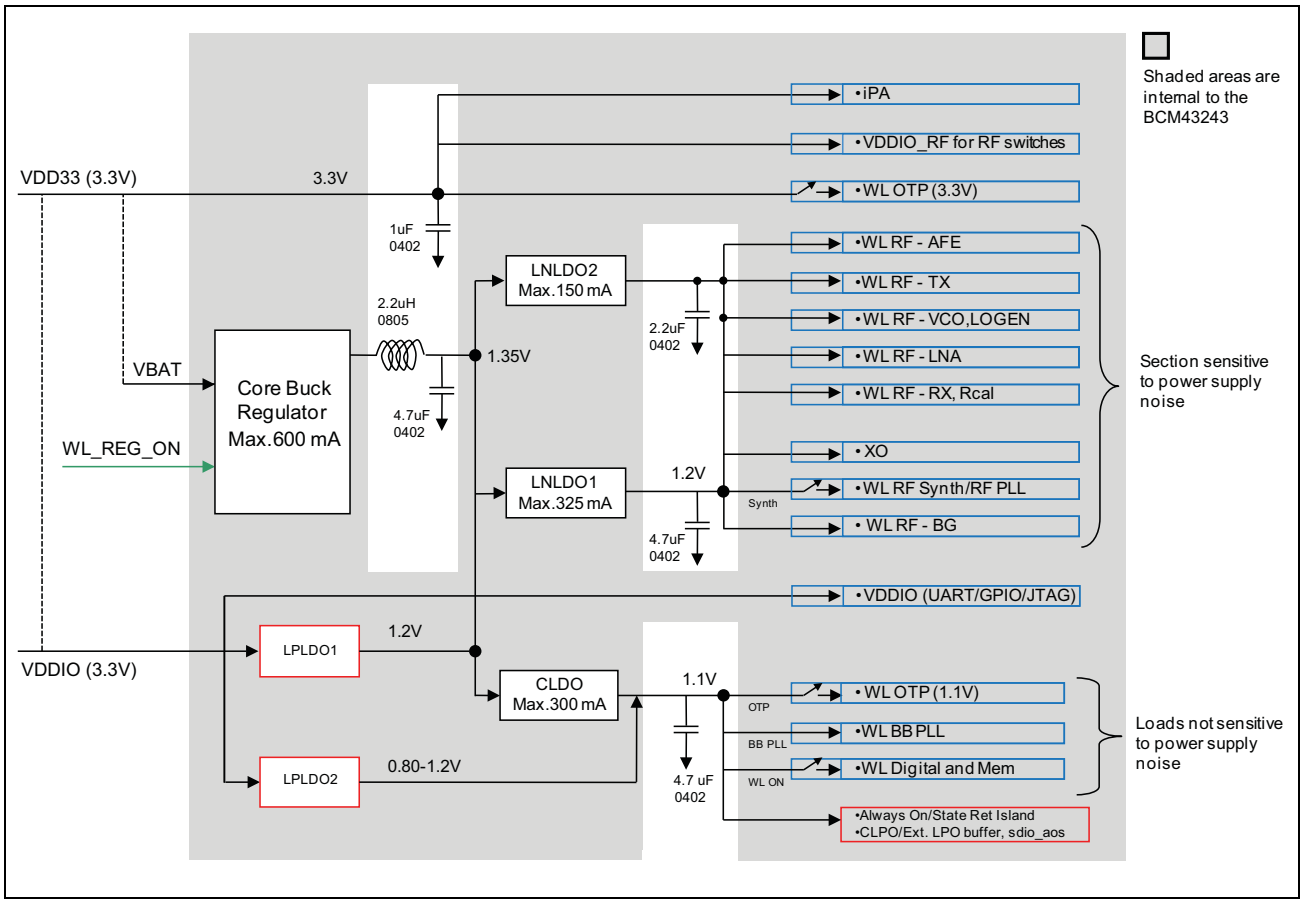
BCM43243 PMU Features

The BCM43243 PMU supplies the following voltages:

- 3.0V to 5.25V (VBAT) down to 1.35 × Vout
- 1.35V to 1.2 × Vout (150 mA and 325 mA maximum) LNLDOs
- 1.35V to 1.2 × Vout (300 mA maximum) CLDO
- Additional internal LDOs (not externally accessible)

Figure 3 on page 14 shows the regulators and a typical power topology. In this example, VDD33 is an external regulated supply at 3.3V ±10%. Input to the Core Buck regulator (VBAT) can be tied to VDD33. VDDIO can also be provided by VDD33.

Figure 3: Typical Power Topology



WLAN Power Management

All areas of the chip design are optimized to minimize power consumption. Silicon processes and cell libraries were chosen to reduce leakage current and supply voltages. Additionally, the BCM43243 integrated RAM is a high Vt memory with dynamic clock control. The dominant supply current consumed by the RAM is leakage current only. Additionally, the BCM43243 includes an advanced WLAN power management unit (PMU) sequencer. The PMU sequencer provides significant power savings by putting the BCM43243 into various power management states appropriate to the current environment and activities that are being performed.

The BCM43243 WLAN power states are described as follows:

- Active mode—All WLAN blocks in the BCM43243 are powered up and fully functional with active carrier sensing and frame transmission and receiving. All required regulators are enabled and put in the most efficient mode based on the load current. Clock speeds are dynamically adjusted by the PMU sequencer.
- Power-down mode—The BCM43243 is effectively powered off by shutting down all internal regulators. The chip is brought out of this mode by external logic, reenabling the internal regulators.

PMU Sequencing

The PMU sequencer is responsible for minimizing system power consumption. It enables and disables various system resources based on a computation of the required resources and a table that describes the relationship between resources and the time needed to enable and disable them.

Resource requests may come from several sources: clock requests from cores, the minimum resources defined in the ResourceMin register, and the resources requested by any active resource request timers. The PMU sequencer maps clock requests into a set of resources required to produce the requested clocks.

Each resource is in one of four states: enabled, disabled, transition_on, and transition_off and has a timer that contains 0 when the resource is enabled or disabled and a non-zero value in the transition states. The timer is loaded with the time_on or time_off value of the resource when the PMU determines that the resource must be enabled or disabled. That timer decrements on each 32.768 kHz PMU clock. When it reaches 0, the state changes from transition_off to disabled or transition_on to enabled. If the time_on value is 0, the resource can go immediately from disabled to enabled. Similarly, a time_off value of 0 indicates that the resource can go immediately from enabled to disabled. The terms enable sequence and disable sequence refer to either the immediate transition or the timer load-decrement sequence.

During each clock cycle, the PMU sequencer performs the following actions:

- Computes the required resource set based on requests and the resource dependency table.
- Decrements all timers whose values are non zero. If a timer reaches 0, the PMU clears the ResourcePending bit for the resource and inverts the ResourceState bit.
- Compares the request with the current resource status and determines which resources must be enabled or disabled.
- Initiates a disable sequence for each resource that is enabled, no longer being requested, and has no powered-up dependents.
- Initiates an enable sequence for each resource that is disabled, is being requested, and has all of its dependencies enabled.

Power-Up/Power-Down/Reset Circuits

The BCM43243 has a signal, WL_REG_ON, that enables or disables the WLAN circuits and the internal regulator blocks, allowing the host to control power consumption. For timing diagrams of these signals and the required power-up sequences, see Section 14: “Power-Up Sequence and Timing,” on page 73.

The WL_REG_ON signal is used by the PMU to power up the WLAN section. When this pin is high, the regulators are enabled and the WLAN section is out of reset. When this pin is low, the WLAN section is in reset. If WL_REG_ON is low, the regulators are disabled. This pin has an internal 200 kΩ pull-down resistor that is enabled by default. It can be disabled through programming.

Section 3: Frequency References

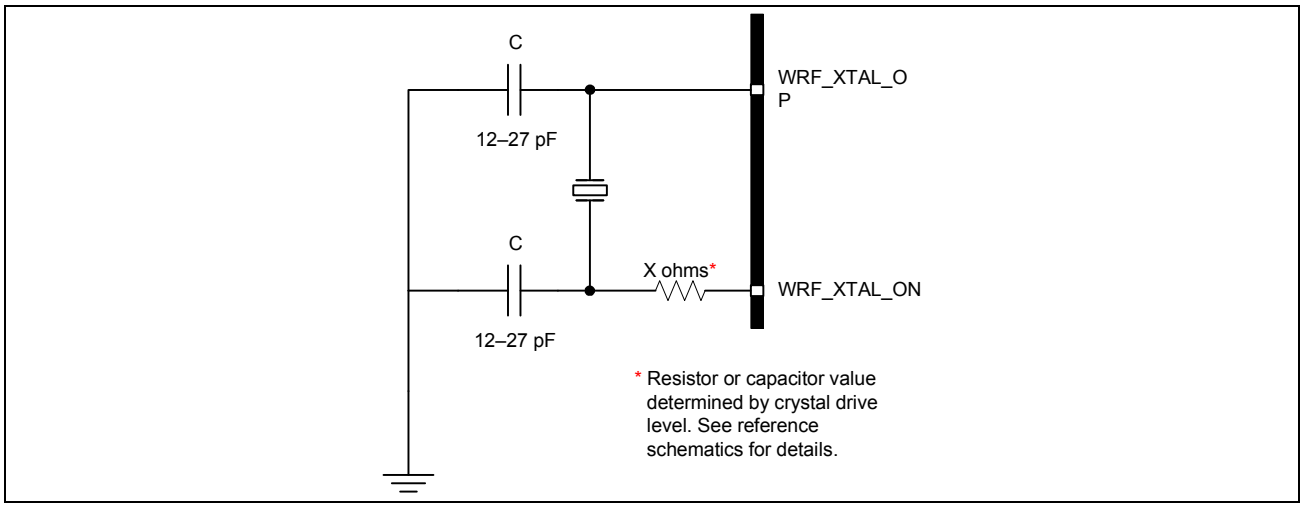
An external crystal is used for generating all radio frequencies and normal operation clocking. As an alternative, an external frequency reference driven by a temperature-compensated crystal oscillator (TCXO) signal may be used. In addition, a low-power oscillator (LPO) is provided for lower power mode timing.

Note: The crystal and TCXO implementations have different power supplies (WRF_XTAL_VDD1P2 for crystal, WRF_TCXO_VDD for TCXO).

Crystal Interface and Clock Generation

The BCM43243 can use an external crystal to provide a frequency reference. The recommended configuration for the crystal oscillator including all external components is shown in Figure 4. Consult the reference schematics for the latest configuration.

Figure 4: Recommended Oscillator Configuration



A fractional-N synthesizer in the BCM43243 generates the radio frequencies, clocks, and data/packet timing, enabling it to operate using a wide selection of frequency references.

The default frequency reference is a 37.4 MHz crystal or TCXO. The signal characteristics for the crystal interface are listed in Table 1 on page 19.

Note: The fractional-N synthesizer can support alternative reference frequencies. Frequencies other than the default, however, require support to be added in the driver plus additional extensive system testing. Contact Broadcom for further details.

TCXO

As an alternative to a crystal, an external precision TCXO can be used as the frequency reference, provided that it meets the Phase Noise requirements listed in Table 1. When the clock is provided by an external TCXO, there are two possible connection methods, shown in Figure 5 and Figure 6:

1. If the TCXO is dedicated to driving the BCM43243, it should be connected to the WRF_XTAL_OP pin through an external 1000 pF coupling capacitor, as shown in Figure 5. The internal clock buffer connected to this pin will be turned OFF when the BCM43243 goes into sleep mode. When the clock buffer turns ON and OFF there will be a small impedance variation. Power must be supplied to the WRF_XTAL_VDD1P2 pin.
2. For 2.4 GHz operation only, an alternative is to DC-couple the TCXO to the WRF_TCXO_CK pin, as shown in Figure 6. Use this method when the same TCXO is shared with other devices and a change in the input impedance is not acceptable because it may cause a frequency shift that cannot be tolerated by the other device sharing the TCXO. This pin is connected to a clock buffer powered from WRF_TCXO_VDD. If the power supply to this buffer is always on (even in sleep mode), the clock buffer is always on, thereby ensuring a constant input impedance in all states of the device. The maximum current drawn from WRF_TCXO_VDD is approximately 500 µA.

Figure 5: Recommended Circuit to Use with an External Dedicated TCXO

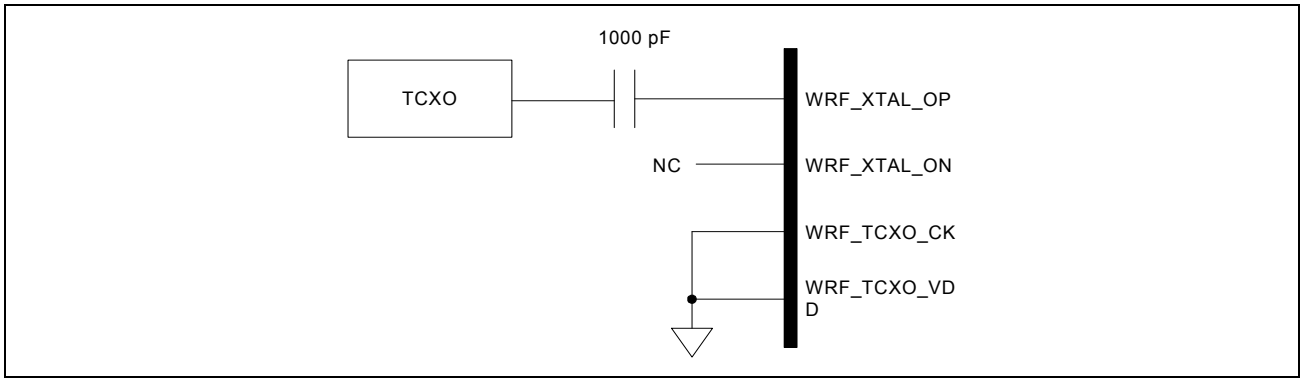


Figure 6: Recommended Circuit to Use with an External Shared TCXO

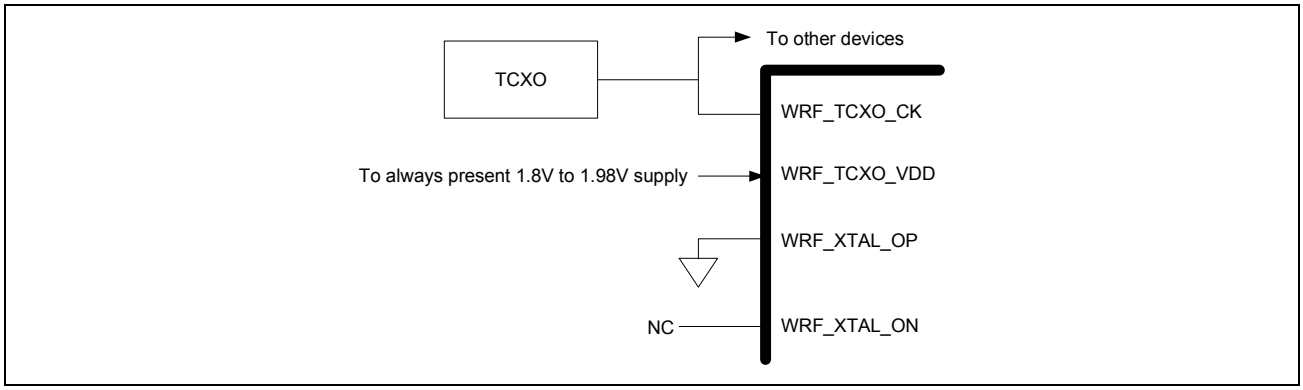


Table 1: Crystal Oscillator and External Clock – Requirements and Performance

		Crystal[a]			External Frequency Reference[b c]			
Parameter	**Conditions/Notes**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Units**
Frequency	–	–	37.4	–	–	–	–	MHz
Crystal load capacitance	–	–	12	–	–	–	–	pF
ESR	–	–	–	60	–	–	–	Ω
Drive level	External crystal specification requirement	200	–	–	–	–	–	µW
Input impedance (WRF_XTAL_OP)	Resistive	–	–	–	12k	17k	–	Ω
	Capacitive	–	–	–	–	–	6	pF
Input impedance (WRF_TCXO_IN)	Resistive	–	–	–	17k	31k	–	Ω
	Capacitive	–	–	–	–	–	2	pF
WRF_XTAL_OP Input low level	DC-coupled digital signal	–	–	–	0	–	0.2	V
WRF_XTAL_OP Input high level	DC-coupled digital signal	–	–	–	1.0	–	1.26	V
WRF_XTAL_OP input voltage (see Figure 5)	AC-coupled analog signal	–	–	–	400	–	1200	mV_{p-p}
WRF_TCXO_IN Input voltage (see Figure 6)	DC-coupled analog signal	–	–	–	400	–	2500	mV_{p-p}
Frequency tolerance Initial + over temp.	Without trimming	–20	–	20	–20	–	20	ppm
Duty cycle	37.4 MHz clock	–	–	–	40	50	60	%
Phase Noise (IEEE 802.11b/g)	37.4 MHz clock at 10 kHz offset	–	–	–	–	–	–131	dBc/Hz
	37.4 MHz clock at 100 kHz or higher offset	–	–	–	–	–	–138	dBc/Hz
Phase Noise (IEEE 802.11a)	37.4 MHz clock at 10 kHz offset	–	–	–	–	–	–139	dBc/Hz
	37.4 MHz clock at 100 kHz or higher offset	–	–	–	–	–	–146	dBc/Hz
Phase Noise (IEEE 802.11n, 2.4 GHz	37.4 MHz clock at 10 kHz offset	–	–	–	–	–	–136	dBc/Hz
	37.4 MHz clock at 100 kHz or higher offset	–	–	–	–	–	–143	dBc/Hz
Phase Noise (IEEE 802.11n, 5 GHz)	37.4 MHz clock at 10 kHz offset	–	–	–	–	–	–144	dBc/Hz
	37.4 MHz clock at 100 kHz or higher offset	–	–	–	–	–	–151	dBc/Hz

a. (Crystal) Use WRF_XTAL_OP and WRF_XTAL_ON, internal power to pin WRF_XTAL_VDD1P2.
b. (TCXO) See "TCXO" on page 18 for alternative connection methods.
c. For a clock reference other than 37.4 MHz, 20 × log10(f/ 37.4) dB should be added to the limits, where f = the reference clock frequency in MHz.

Section 4: WLAN Global Functions

WLAN CPU and Memory Subsystem

The BCM43243 includes an integrated ARM Cortex-M3™ processor with internal RAM and ROM. The ARM Cortex-M3 processor is a low-power processor that features low gate count, low interrupt latency, and low-cost debug. It is intended for deeply embedded applications that require fast interrupt response features. The processor implements the ARM architecture v7-M with support for Thumb®-2 instruction set. ARM Cortex-M3 delivers 30% more performance gain over ARM7TDMI.

At 0.19 µW/MHz, the Cortex-M3 is the most power-efficient general-purpose microprocessor available, outperforming 8- and 16-bit devices on MIPS/µW. It supports integrated sleep modes.

ARM Cortex-M3 uses multiple technologies to reduce cost through improved memory utilization, reduced pin overhead, and reduced silicon area. ARM Cortex-M3 supports independent buses for Code and Data access (ICode/DCode and System buses). ARM Cortex-M3 supports extensive debug features including real time trace of program execution.

On-chip memory for the CPU includes 544 KB RAM and 640 KB ROM.

One-Time Programmable Memory

Various hardware configuration parameters may be stored in an internal 3072-bit One-Time Programmable (OTP) memory, which is read by the system software after device reset. In addition, customer-specific parameters including the system vendor ID and the MAC address can be stored, depending on the specific board design.

The initial state of all bits in an unprogrammed OTP device is 0. After any bit is programmed to a 1, it cannot be reprogrammed to 0. The entire OTP array can be programmed in a single write cycle using a utility provided with the Broadcom WLAN manufacturing test tools. Alternatively, multiple write cycles can be used to selectively program specific bytes, but only bits which are still in the 0 state can be altered during each programming cycle.

Prior to OTP programming, all values should be verified using the appropriate editable nvram.txt file, which is provided with the reference board design package.

GPIO Interface

The BCM43243 has 13 general-purpose I/O (GPIO) that can be used to connect to various external devices.

Upon power-up and reset, these pins become tristated. Subsequently, they can be programmed to be either input or output pins via the GPIO control register. An internal (programmable) pull-up/pull-down resistor is included on each GPIO.

UART Interface

One UART interface can be enabled by software as an alternate function on pins UART_RX (muxed on GPIO_6) and UART_TX (muxed on GPIO_7). Provided primarily for debugging during development, this UART enables the BCM43243 to operate as RS-232 data termination equipment (DTE) for exchanging and managing data with other serial devices. It is compatible with the industry standard 16550 UART, and it provides a FIFO size of 64 × 8 in each direction.

JTAG Interface

The BCM43243 supports the IEEE 1149.1 JTAG boundary scan standard for performing device package and PCB assembly testing during manufacturing. In addition, the JTAG interface allows Broadcom to assist customers by using proprietary debug and characterization test tools during board bring-up. Therefore, it is highly recommended to provide access to the JTAG pins by means of test points or a header on all PCB designs.

The JTAG interface (multiplexed on the GPIO pins) is enabled when the JTAG_SEL pin is asserted high. The JTAG to GPIO signal mapping is as follows:

- TCK GPIO_2
- TMS GPIO_3
- TDI GPIO_4
- TDO GPIO_5

Section 5: USB Interface

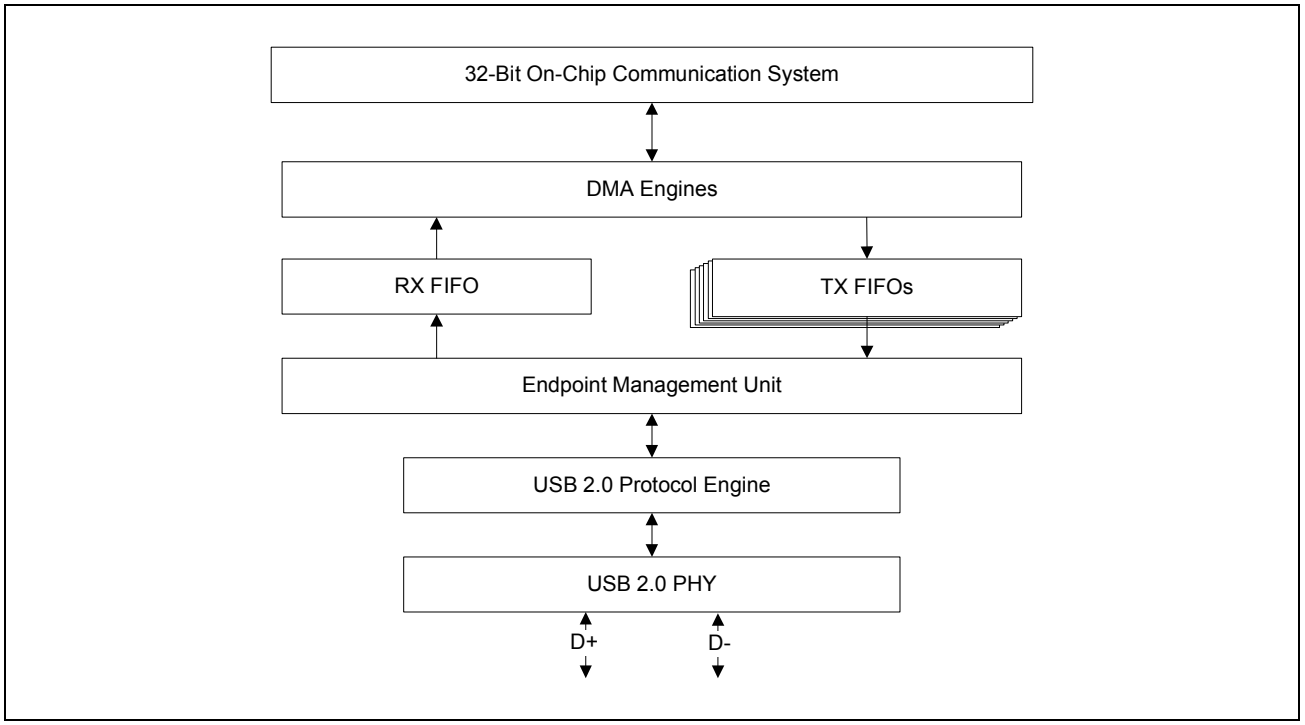
WLAN USB 2.0 Interface

The BCM43243 USB interface can be set to operate as a USB 2.0 port. Features include the following:

- A USB 2.0 protocol engine that supports the following:
  - A Parallel Interface Engine (PIE) between packet buffers and USB transceiver
  - Up to nine endpoints, including Configurable Control Endpoint 0
- Separate endpoint packet buffers with a 512-byte FIFO buffer each
- Host-to-device communication for bulk, control, and interrupt transfers
- Configuration and status registers

Figure 7 shows the blocks in the device core.

Figure 7: WLAN USB 2.0 Host Interface Block Diagram



The USB 2.0 PHY handles the USB protocol and the serial signaling interface between the host and device. It is primarily responsible for data transmission and recovery. On the transmit side, data is encoded, along with a clock, using the NRZI scheme with bit stuffing to ensure that the receiver detects a transition in the data stream. A SYNC field that precedes each packet enables the receiver to synchronize the data and clock recovery circuits. On the receive side, the serial data is deserialized, unstuffed, and checked for errors. The recovered data and clock are then shifted to the clock domain that is compatible with the internal bus logic.

The endpoint management unit contains the PIE control logic and the endpoint logic. The PIE interfaces between the packet buffers and the USB transceiver. It handles packet identification (PID), USB packets, and transactions.

The endpoint logic contains nine uniquely addressable endpoints. These endpoints are the source or sink of communication flow between the host and the device. Endpoint zero is used as a default control port for both the input and output directions. The USB system software uses this default control method to initialize and configure the device information and allows USB status and control access. Endpoint zero is always accessible after a device is attached, powered, and reset.

Endpoints are supported by 512-byte FIFO buffers, one for each IN endpoint and one shared by all OUT endpoints. Both TX and RX data transfers support a DMA burst of 4, which guarantees low latency and maximum throughput performance. The RX FIFO can never overflow by design. The maximum USB packet size cannot be more than 512 bytes.

Section 6: Wireless LAN MAC and PHY

MAC Features

The BCM43243 WLAN media access controller (MAC) supports features specified in the IEEE 802.11 base standard, and amended by IEEE 802.11n. The salient features are listed below:

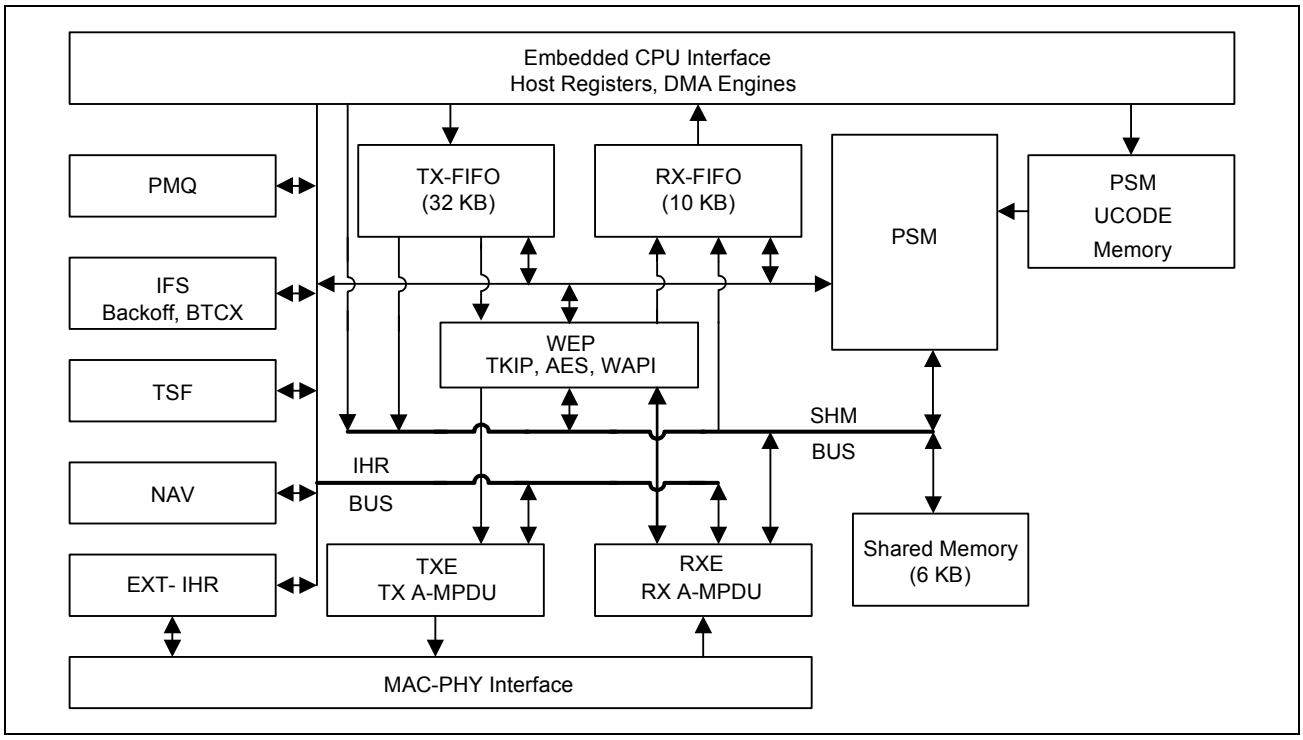
- Transmission and reception of aggregated MPDUs (A-MPDU)
- Support for power management schemes, including WMM power-save, power-save multipoll (PSMP) and multiphase PSMP operation
- Support for immediate ACK and Block-ACK policies
- Interframe space timing support, including RIFS
- Support for RTS/CTS and CTS-to-self frame sequences for protecting frame exchanges
- Back-off counters in hardware for supporting multiple priorities as specified in the WMM specification
- Timing synchronization function (TSF), network allocation vector (NAV) maintenance, and target beacon transmission time (TBTT) generation in hardware
- Hardware offload for AES-CCMP, legacy WPA TKIP, legacy WEP ciphers, WAPI, and support for key management
- Programmable independent basic service set (IBSS) or infrastructure basic service set functionality
- Statistics counters for MIB support

MAC Description

The BCM43243 WLAN MAC is designed to support high-throughput operation with low-power consumption. In addition, several power saving modes have been implemented that allow the MAC to consume very little power while maintaining network-wide timing synchronization. The architecture diagram of the MAC is shown in Figure 8 on page 25.

The following sections provide an overview of the important modules in the MAC.

Figure 8: WLAN MAC Architecture



PSM

The programmable state machine (PSM) is a microcoded engine, which provides most of the low-level control to the hardware, to implement the IEEE 802.11 specification. It is a microcontroller that is highly optimized for flow control operations, which are predominant in implementations of communication protocols. The instruction set and fundamental operations are simple and general, which allows algorithms to be optimized until very late in the design process. It also allows for changes to the algorithms to track evolving IEEE 802.11 specifications.

The PSM fetches instructions from the microcode memory. It uses the shared memory to obtain operands for instructions, as a data store, and to exchange data between both the host and the MAC data pipeline (via the SHM bus). The PSM also uses a scratch-pad memory (similar to a register bank) to store frequently accessed and temporary variables.

The PSM exercises fine-grained control over the hardware engines by programming internal hardware registers (IHR). These IHRs are colocated with the hardware functions they control and are accessed by the PSM via the IHR bus.

The PSM fetches instructions from the microcode memory using an address determined by the program counter, instruction literal, or a program stack. For ALU operations the operands are obtained from shared memory, scratch-pad, IHRs, or instruction literals, and the results are written into the shared memory, scratch-pad, or IHRs.

There are two basic branch instructions: conditional branches and ALU based branches. To better support the many decision points in the IEEE 802.11 algorithms, branches can depend on either a readily available signals from the hardware modules (branch condition signals are available to the PSM without polling the IHRs), or the results of ALU operations.

WEP

The wired equivalent privacy (WEP) engine encapsulates all the hardware accelerators to perform the encryption and decryption, as well as MIC computation and verification. The accelerators implement the following cipher algorithms: legacy WEP, WPA TKIP, WPA2 AES-CCMP.

The PSM determines, based on the frame type and association information, the appropriate cipher algorithm to be used. It supplies the keys to the hardware engines from an on-chip key table. The WEP interfaces with the TXE to encrypt and compute the MIC on transmit frames, and the RXE to decrypt and verify the MIC on receive frames.

TXE

The transmit engine (TXE) constitutes the transmit data path of the MAC. It coordinates the DMA engines to store the transmit frames in the TXFIFO. It interfaces with WEP module to encrypt frames and transfers the frames across the MAC-PHY interface at the appropriate time determined by the channel access mechanisms.

The data received from the DMA engines are stored in transmit FIFOs. The MAC supports multiple logical queues to support traffic streams that have different QoS priority requirements. The PSM uses the channel access information from the IFS module to schedule a queue from which the next frame is transmitted. Once the frame is scheduled, the TXE hardware transmits the frame based on a precise timing trigger received from the IFS module.

The TXE module also contains the hardware that allows the rapid assembly of MPDUs into an A-MPDU for transmission. The hardware module aggregates the encrypted MPDUs by adding appropriate headers and pad delimiters as needed.

RXE

The receive engine (RXE) constitutes the receive data path of the MAC. It interfaces with the DMA engine to drain the received frames from the RXFIFO. It transfers bytes across the MAC-PHY interface and interfaces with the WEP module to decrypt frames. The decrypted data is stored in the RXFIFO.

The RXE module contains programmable filters that are programmed by the PSM to accept or filter frames based on several criteria such as receiver address, BSSID, and certain frame types.

The RXE module also contains the hardware required to detect A-MPDUs, parse the headers of the containers, and disaggregate them into component MPDUS.

IFS

The IFS module contains the timers required to determine interframe space timing including RIFS timing. It also contains multiple backoff engines required to support prioritized access to the medium as specified by WMM.

The interframe spacing timers are triggered by the cessation of channel activity on the medium, as indicated by the PHY. These timers provide precise timing to the TXE to begin frame transmission. The TXE uses this information to send response frames or perform transmit frame-bursting (RIFS or SIFS separated, as within a TXOP).

The backoff engines (for each access category) monitor channel activity, in each slot duration, to determine whether to continue or pause the backoff counters. When the backoff counters reach 0, the TXE gets notified, so that it may commence frame transmission. In the event of multiple backoff counters decrementing to 0 at the same time, the hardware resolves the conflict based on policies provided by the PSM.

The IFS module also incorporates hardware that allows the MAC to enter a low-power state when operating under the IEEE power save mode. In this mode, the MAC is in a suspended state with its clock turned off. A sleep timer, whose count value is initialized by the PSM, runs on a slow clock and determines the duration over which the MAC remains in this suspended state. Once the timer expires the MAC is restored to its functional state. The PSM updates the TSF timer based on the sleep duration ensuring that the TSF is synchronized to the network.

TSF

The timing synchronization function (TSF) module maintains the TSF timer of the MAC. It also maintains the target beacon transmission time (TBTT). The TSF timer hardware, under the control of the PSM, is capable of adopting timestamps received from beacon and probe response frames in order to maintain synchronization with the network.

The TSF module also generates trigger signals for events that are specified as offsets from the TSF timer, such as uplink and downlink transmission times used in PSMP.

NAV

The network allocation vector (NAV) timer module is responsible for maintaining the NAV information conveyed through the duration field of MAC frames. This ensures that the MAC complies with the protection mechanisms specified in the standard.

The hardware, under the control of the PSM, maintains the NAV timer and updates the timer appropriately based on received frames. This timing information is provided to the IFS module, which uses it as a virtual carrier-sense indication.

MAC-PHY Interface

The MAC-PHY interface consists of a data path interface to exchange RX/TX data from/to the PHY. In addition, there is a programming interface, which can be controlled either by the host or by the PSM to configure and control the PHY.

WLAN PHY Description

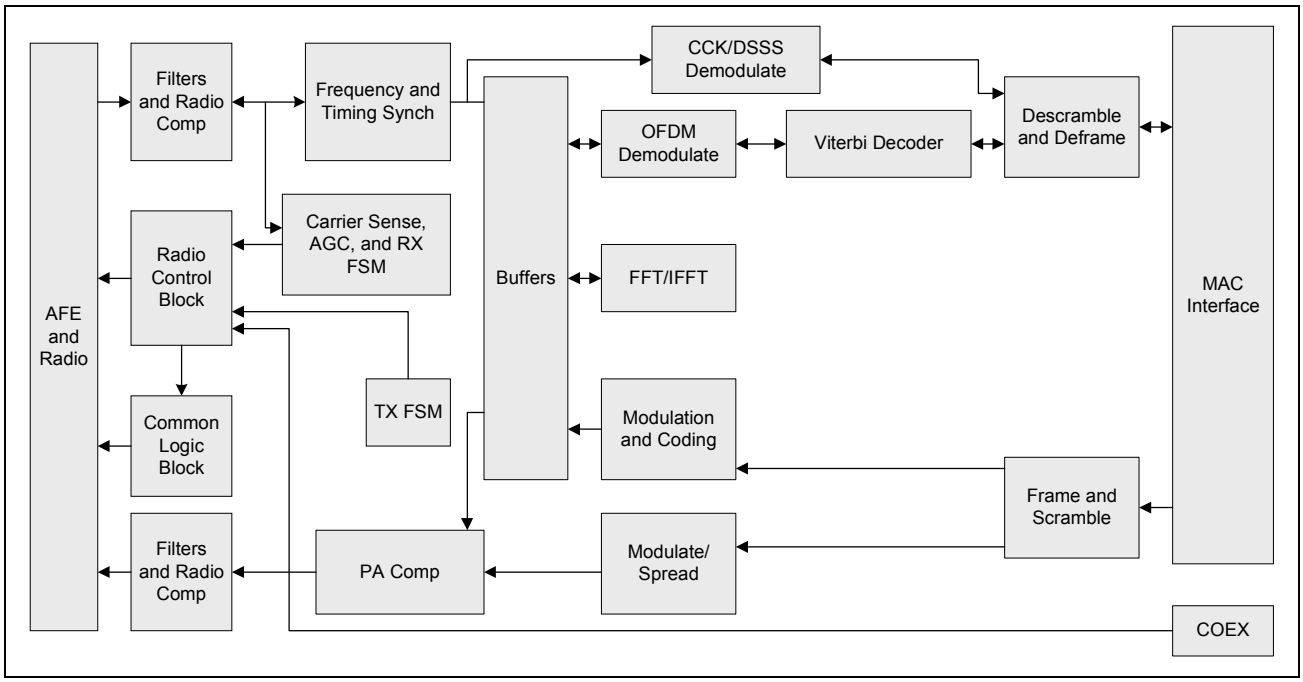
The BCM43243 supports IEEE 802.11a/b/g/n dual-stream to provide maximum data rates up to 300 Mbps.

The PHY has been designed to work with interference, radio nonlinearity, and impairments. It incorporates efficient implementations of the filters, FFT and Viterbi decoder algorithms. Efficient algorithms have been designed to achieve maximum throughput and reliability, including algorithms for carrier sense/rejection, frequency/phase/timing acquisition and tracking, channel estimation and tracking. The PHY receiver also contains a robust IEEE 802.11b demodulator. The PHY carrier sense has been tuned to provide high throughput for IEEE 802.11g/11b hybrid networks.

PHY Features

- Supports IEEE 802.11a, 11b, 11g, and 11n dual-stream PHY standards
- IEEE 802.11n dual-stream operation in 20 MHz and 40 MHz channels
- Supports Optional Short GI and Green Field modes in TX and RX
- Supports optional space-time block code (STBC) receive of two space-time streams
- Supports IEEE 802.11h/k for worldwide operation
- Advanced algorithms for low power, enhanced sensitivity, range, and reliability
- Supports power saving schemes such as single-core listen (OCL), single-core demodulation of SISO/ STBC packets based on RSSI, and dynamic ML turn-off based on RSSI
- Automatic gain control scheme for blocking and non blocking application scenario for cellular applications
- Closed-loop transmit power control
- Digital RF chip calibration algorithms to handle CMOS RF chip non-idealities
- On-the-fly channel frequency and transmit power selection
- Supports per packet RX antenna diversity for IEEE 802.11b PHY rates.
- Designed to meet FCC and other worldwide regulatory requirements
- TX LDPC for improved range and power efficiency
- Hardware support for faster switch times between channels/bands

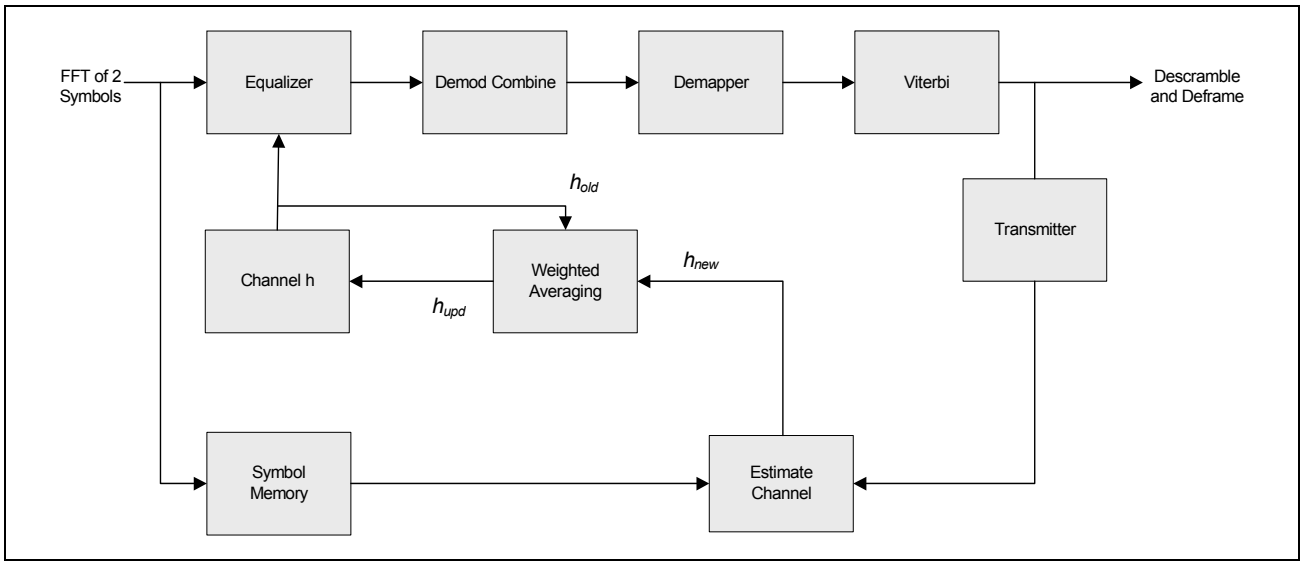
Figure 9: WLAN PHY Block Diagram



The PHY is capable of fully calibrating the RF front end to extract the highest performance. On power-up, the PHY performs a full suite of calibration to correct for IQ mismatch and local oscillator leakage. The PHY also performs periodic calibration to compensate for any temperature related drift thus maintaining high-performance over time. A closed loop transmit control algorithm maintains the output power to required level with capability control TX power on a per packet basis.

One of the key feature of the PHY is two space-time stream receive capability. The STBC scheme can obtain diversity gains by using multiple transmit antennas in AP (Access Point) in a fading channel environment, without increasing the complexity at the STA. Details of the STBC receive are shown in the block diagram in Figure 10 on page 30.

Figure 10: STBC Receive Block Diagram



In STBC mode, symbols are processed in pairs. Equalized output symbols are linearly combined and decoded. Channel estimate is refined on every pair of symbols using the received symbols and reconstructed symbols.

Section 7: WLAN Radio Subsystem

The BCM43243 includes an integrated dual-band WLAN RF transceiver that has been optimized for use in 2.4 GHz and 5 GHz Wireless LAN systems (but not both simultaneously). It has been designed to provide low-power, low-cost, and robust communications for applications operating in the globally available 2.4 GHz unlicensed ISM or 5 GHz U-NII bands. The transmit and receive sections include all on-chip filtering, mixing, and gain control functions.

Up to 11 RF control signals are available to drive the external RF switches and support external power amplifiers and low noise amplifiers for each band. See the reference board schematics for further details.

Receiver Path

The BCM43243 has a wide dynamic range, direct conversion receiver. It employs high order on-chip channel filtering to ensure reliable operation in the noisy 2.4 GHz ISM band or the entire 5 GHz U-NII band. Control signals are available that can support the use of optional external low noise amplifiers (LNA), which can increase the receive sensitivity by several dB.

Transmit Path

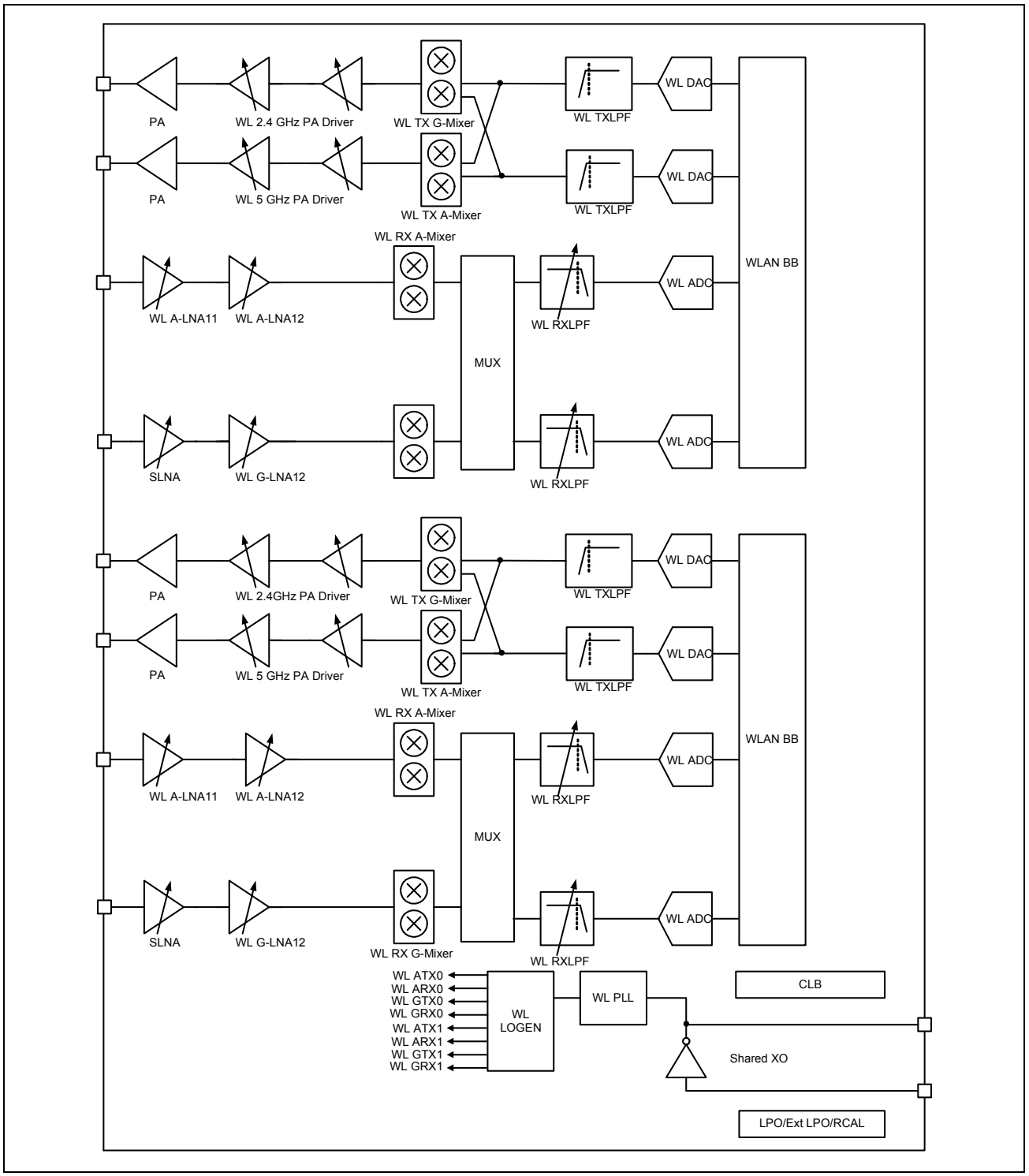
Baseband data is modulated and upconverted to the 2.4 GHz ISM or 5 GHz U-NII bands, respectively.

Linear on-chip power amplifiers are included for both 2.4 GHz and 5 GHz. Closed loop power control is also provided, as are spare RF control signals that can be used to support external RF switches for either or both bands.

Calibration

The BCM43243 features dynamic and automatic on-chip calibration to continually compensate for temperature and process variation across components. This enables the BCM43243 to be used in high-volume applications, because calibration routines are not required during manufacturing testing. These calibration routines are performed periodically in the course of normal radio operation. Examples of some of the automatic calibration algorithms are baseband filter calibration for optimum transmit and receive performance and LOFT calibration for carrier leakage reduction. In addition, I/Q Calibration, R Calibration, and VCO Calibration are performed on-chip.

Figure 11: Radio Functional Block Diagram



Section 8: Pinouts and Signal Descriptions

Ball Map

The BCM43243 ball map (top view) is defined in Figure 12 through Figure 15 on page 36.

Figure 12: FCFBGA Ball Map, Top View, 1 of 4—A1 through M12

	1	2	3	4	5	6	7	8	9	10	11	12
A	VSS	NC		NC		NC	NC		NC		RF_SW_CTRL_6	
B	VSS	VSS	NC	NC	NC	NC	VSS	NC	NC		RF_SW_CTRL_7	RF_SW_CTRL_5
C	NC	NC										
D		NC										
E	NC	NC			NC		VSS	VSS	NC	NC	VSS	GMODE_EXT_LNA_PU_CORE0
F		NC			NC							
G	NC	NC			RSVD							
H		VSS			NC							
J	RSVD	RSVD						GND		OTP_VDD33		
K	RSVD	GND			RSVD			GND		RSVD	VDDIO_RF	
L		RSVD			GND					RSVD	VDD	
M	NC	GND			GND			GND	GND	VSS		

Figure 13: FCFBGA Ball Map, Top View, 2 of 4—A13 through M23

13	14	15	16	17	18	19	20	21	22	23	
RF_SW_CTRL_3		GPIO_7		GPIO_8		GPIO_6		GPIO_3		GPIO_0	A
RF_SW_CTRL_1	RF_SW_CTRL_4	RF_SW_CTRL_2	RF_SW_CTRL_0	GPIO_2	JTAG_SEL	GPIO_12	GPIO_9	GPIO_4	GPIO_5	GPIO_1	B
									SR_VLX	SR_VLX	C
									SR_PVSS	SR_PVSS	D
AMODE_EXT_LNA_PU_CORE0		EXT_XTAL_PU							SR_PVSS	SR_PVSS	E
						PMU_AVSS			SR_VDDBATP5V	SR_VDDBATP5V	F
									SR_VDDBATA5V	SR_VDDBATA5V	G
									VOUT_CLDO	VOUT_CLDO	H
	GPIO_11		WLREG_ON			VOUT_LNLDO2			VOUT_LNLDO1	VOUT_LNLDO1	J
GPIO_10	VSS		VDDIO			VSS			LDO_VDD1P5	LDO_VDD1P5	K
VDD	VDD		RSVD			GND			VSS	VSS	L
	VDD		VSS			MONPLL			AVDD33		M

Figure 14: FCFBGA Ball Map, Top View, 3 of 4—N1 through AC12

N		RSVD			GND				GND			VDD
P	NC	GND			GND			GND		VSS		VDD
R	WRF_RFIN_2G _CORE0	RGND			RGND		RGND	RGND	RGND	RGND	VSS	VSS
T	RGND	RGND			RGND		RGND	RGND		RGND	RGND	
U	WRF_PAOUT_2G _CORE0	RGND			WRF_RX2G _VDD1P2_CORE0			RGND			RGND	
V	RGND	RGND			RGND			RGND	RGND		RGND	
W	WRF_PADRV2G _VDD3P3_CORE0	RGND			RGND	RGND	RGND	WRF_GPIO_OUT	RGND	WRF_AFE_VDD1P2 _CORE0	RGND	WRF_RX2G_VDD1P2 _CORE1
Y	RGND	RGND										
AA	WRF_PA_VDD3P3 _CORE0	RGND										
AB	WRF_PADRV5G _VDD3P3_CORE0	RGND	RGND	RGND	RGND	WRF_TX_VDD1P2 _CORE0	RGND	WRF_RX5G _VDD1P2_CORE0	RGND	WRF_TX_VDD1P2 _CORE1	RGND	RGND
AC	RGND	WRF_PAOUT _5G_CORE0	RGND	WRF_RFIN _5G_CORE0	RGND	RGND	WRF_VCO _VDD1P2		WRF_SYNTH _VDD1P2	RGND	WRF_RFIN _2G_CORE1	RGND
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**

Figure 15: FCFBGA Ball Map, Top View, 4 of 4—N13 through AC23

	VDD					AVDD_BBPLL			RREF	DP	N
VDD	VDD	VSS	VSS			VDDIO_RF			VSS	DM	P
VSS	VSS	VSS				AMODE_EXT_LNA _PU_CORE1			MONCDR	DVSS	R
RGND	RGND		RGND	WRF_XTAL _CAB_GND1P2		VSS			VSS		T
RGND			RGND			WRF_XTAL _CAB_GND1P2			GMODE_EXT_LNA _PU_CORE1	RF_SW_CTRL_8	U
RGND		RGND	RGND			WRF_XTAL _CAB_GND1P2			VSS	VSS	V
RGND	WRF_AFE_VDD1P2 _CORE1	RGND	RGND	WRF_RX5G _VDD1P2_CORE1	RGND	WRF_XTAL _CAB_GND1P2			WRF_TCXO _VDD1P8	WRF_XTAL _CAB_XON	W
									WRF_TCXO _CKIN2V		Y
									WRF_XTAL _CAB_GND1P2	WRF_XTAL _CAB_XOP	AA
RGND	RGND	RGND	RGND	RGND	RGND	RGND	RGND	WRF_XTAL _CAB_GND1P2	WRF_XTAL _CAB_GND1P2	WRF_XTAL _CAB_GND1P2	AB
WRF_PAOUT _2G_CORE1	WRF_PADRV2G _VDD3P3_CORE1	WRF_PA _VDD3P3_CORE1	WRF_PADRV5G _VDD3P3_CORE1	WRF_PAOUT _5G_CORE1	RGND	WRF_RFIN _5G_CORE1	RGND	WRF_XTAL _CAB_GND1P2	WRF_XTAL _CAB_VDD1P2	WRF_XTAL _CAB_GND1P2	AC
13	14	15	16	17	18	19	20	21	22	23	

Pin List—Ordered By Pin Number

Table 2 lists the pins numerically by pin number.

Table 2: Pin List By Pin Number

Pin	Name
A1	VSS
A2	NC
A4	NC
A6	NC
A7	NC
A9	NC
A11	RF_SW_CTRL_6
A13	RF_SW_CTRL_3
A15	GPIO_7
A17	GPIO_8
A19	GPIO_6
A21	GPIO_3
A23	GPIO_0
B1	VSS
B2	VSS
B3	NC
B4	NC
B5	NC
B6	NC
B7	VSS
B8	NC
B9	NC
B11	RF_SW_CTRL_7
B12	RF_SW_CTRL_5
B13	RF_SW_CTRL_1
B14	RF_SW_CTRL_4
B15	RF_SW_CTRL_2
B16	RF_SW_CTRL_0
B17	GPIO_2
B18	JTAG_SEL
B19	GPIO_12
B20	GPIO_9
B21	GPIO_4
B22	GPIO_5
B23	GPIO_1
C1	NC
C2	NC
C22	SR_VLX
C23	SR_VLX
D2	NC_D2
D22	SR_PVSS
D23	SR_PVSS
E1	NC
E2	NC
E5	NC
E7	VSS
E8	VSS
E9	NC
E10	NC
E11	VSS
E12	GMODE_EXT_LNA_PU_CORE0
E13	AMODE_EXT_LNA_PU_CORE0
E15	EXT_XTAL_PU
E22	SR_PVSS
E23	SR_PVSS
F2	NC
F5	NC
F19	PMU_AVSS
F22	SR_VDDBATP5V
F23	SR_VDDBATP5V
G1	NC
G2	NC
G5	RSVD
G22	SR_VDDBATA5V
G23	SR_VDDBATA5V
H2	VSS
H5	RSVD
H22	VOUT_CLDO
H23	VOUT_CLDO
J1	RSVD

Pin	Name
J2	RSVD
J8	GND
J10	OTP_VDD33
J14	GPIO_11
J16	WL_REG_ON
J19	VOUT_LNLDO2
J22	VOUT_LNLDO1
J23	VOUT_LNLDO1
K1	RSVD
K2	GND
K5	RSVD
K8	GND
K10	RSVD
K11	VDDIO_RF
K13	GPIO_10
K14	VSS
K16	VDDIO
K19	VSS
K22	LDO_VDD1P5
K23	LDO_VDD1P5
L2	RSVD
L5	GND
L10	RSVD
L11	VDD
L13	VDD
L14	VDD
L16	RSVD
L19	GND
L22	VSS
L23	VSS
M1	NC
M2	GND
M5	GND
M8	GND
M9	GND
M10	VSS
M14	VDD
M16	VSS
M19	MONPLL
M22	AVDD33

Pin	Name
N2	RSVD
N5	GND
N9	GND
N12	VDD
N14	VDD
N19	AVDD_BBPLL
N22	RREF
N23	DP
P1	NC
P2	GND
P5	GND
P8	GND
P10	VSS
P12	VDD
P13	VDD
P14	VDD
P15	VSS
P16	VSS
P19	VDDIO_RF
P22	VSS
P23	DM
R1	WRF_RFIN_2G_CORE0
R2	RGND
R5	RGND
R7	RGND
R8	RGND
R9	RGND
R10	RGND
R11	VSS
R12	VSS
R13	VSS
R14	VSS
R15	VSS
R19	AMODE_EXT_LNA_PU_CORE1
R22	MONCDR
R23	GND
T1	RGND
T2	RGND
T5	RGND
T7	RGND

Pin	Name
T8	RGND
T10	RGND
T11	RGND
T13	RGND
T14	RGND
T16	RGND
T17	WRF_XTAL_CAB_GND1P2
T19	VSS
T22	VSS
U1	WRF_PAOUT_2G_CORE0
U2	RGND
U5	WRF_RX2G_VDD1P2_CORE0
U8	RGND
U11	RGND
U13	RGND
U16	RGND
U19	WRF_XTAL_CAB_GND1P2
U22	GMODE_EXT_LNA_PU_CORE1
U23	RF_SW_CTRL_8
V1	RGND
V2	RGND
V5	RGND
V8	RGND
V9	RGND
V11	RGND
V13	RGND
V15	RGND
V16	RGND
V19	WRF_XTAL_CAB_GND1P2
V22	VSS
V23	VSS
W1	WRF_PADRV2G_VDD3P3_CORE0
W2	RGND
W5	RGND
W6	RGND
W7	RGND
W8	WRF_GPIO_OUT
W9	RGND
W10	WRF_AFE_VDD1P2_CORE0
W11	RGND

Pin	Name
W12	WRF_RX2G_VDD1P2_CORE1
W13	RGND
W14	WRF_AFE_VDD1P2_CORE1
W15	RGND
W16	RGND
W17	WRF_RX5G_VDD1P2_CORE1
W18	RGND
W19	WRF_XTAL_CAB_GND1P2
W22	WRF_TCXO_VDD1P8
W23	WRF_XTAL_CAB_XON
Y1	RGND
Y2	RGND
Y22	WRF_TCXO_CKIN2V
AA1	WRF_PA_VDD3P3_CORE0
AA2	RGND
AA22	WRF_XTAL_CAB_GND1P2
AA23	WRF_XTAL_CAB_XOP
AB1	WRF_PADRV5G_VDD3P3_CORE0
AB2	RGND
AB3	RGND
AB4	RGND
AB5	RGND
AB6	WRF_TX_VDD1P2_CORE0
AB7	RGND
AB8	WRF_RX5G_VDD1P2_CORE0
AB9	RGND
AB10	WRF_TX_VDD1P2_CORE1
AB11	RGND
AB12	RGND
AB13	RGND
AB14	RGND
AB15	RGND
AB16	RGND
AB17	RGND
AB18	RGND
AB19	RGND
AB20	RGND
AB21	WRF_XTAL_CAB_GND1P2
AB22	WRF_XTAL_CAB_GND1P2
AB23	WRF_XTAL_CAB_GND1P2

Pin	*Name*
AC1	RGND
AC2	WRF_PAOUT_5G_CORE0
AC3	RGND
AC4	WRF_RFIN_5G_CORE0
AC5	RGND
AC6	RGND
AC7	WRF_VCO_VDD1P2
AC9	WRF_SYNTH_VDD1P2
AC10	RGND
AC11	WRF_RFIN_2G_CORE1
AC12	RGND
AC13	WRF_PAOUT_2G_CORE1
AC14	WRF_PADRV2G_VDD3P3_CORE1
AC15	WRF_PA_VDD3P3_CORE1
AC16	WRF_PADRV5G_VDD3P3_CORE1
AC17	WRF_PAOUT_5G_CORE1
AC18	RGND
AC19	WRF_RFIN_5G_CORE1
AC20	RGND
AC21	WRF_XTAL_CAB_GND1P2
AC22	WRF_XTAL_CAB_VDD1P2
AC23	WRF_XTAL_CAB_GND1P2

Pin List—Listed Alphabetically By Pin Name

Table 3 lists the pins alphabetically by pin name.

Table 3: Alphabetical Pin List By Pin Name

Name	Pin
AMODE_EXT_LNA_PU_CORE0	E13
AMODE_EXT_LNA_PU_CORE1	R19
AVDD33	M22
AVDD_BBPLL	N19
DM	P23
DP	N23
EXT_XTAL_PU	E15
GMODE_EXT_LNA_PU_CORE0	E12
GMODE_EXT_LNA_PU_CORE1	U22
GND	J8
GND	K2
GND	K8
GND	L5
GND	L19
GND	M2
GND	M5
GND	M8
GND	M9
GND	N5
GND	N9
GND	P2
GND	P5
GND	P8
GND	R23
GPIO_0	A23
GPIO_1	B23
GPIO_2	B17
GPIO_3	A21
GPIO_4	B21
GPIO_5	B22
GPIO_6	A19
GPIO_7	A15
GPIO_8	A17
GPIO_9	B20
GPIO_10	K13
GPIO_11	J14
GPIO_12	B19
JTAG_SEL	B18
LDO_VDD1P5	K22
LDO_VDD1P5	K23
MONCDR	R22
MONPLL	M19
NC	A2
NC	A4
NC	A6
NC	A7
NC	A9
NC	B3
NC	B4
NC	B5
NC	B6
NC	B8
NC	B9
NC	C1
NC	C2
NC	D2
NC	E1
NC	E2
NC	E5
NC	E9
NC	E10
NC	F2
NC	F5
NC	G1
NC	G2
NC	M1
NC	P1
OTP_VDD33	J10
PMU_AVSS	F19
RF_SW_CTRL_0	B16

Name	Pin
RF_SW_CTRL_1	B13
RF_SW_CTRL_2	B15
RF_SW_CTRL_3	A13
RF_SW_CTRL_4	B14
RF_SW_CTRL_5	B12
RF_SW_CTRL_6	A11
RF_SW_CTRL_7	B11
RF_SW_CTRL_8	U23
RGND	R2
RGND	R5
RGND	R7
RGND	R8
RGND	R9
RGND	R10
RGND	T1
RGND	T2
RGND	T5
RGND	T7
RGND	T8
RGND	T10
RGND	T11
RGND	T13
RGND	T14
RGND	T16
RGND	U2
RGND	U8
RGND	U11
RGND	U13
RGND	U16
RGND	V1
RGND	V2
RGND	V5
RGND	V8
RGND	V9
RGND	V11
RGND	V13
RGND	V15
RGND	V16
RGND	W2
RGND	W5
RGND	W6
RGND	W7
RGND	W9
RGND	W11
RGND	W13
RGND	W15
RGND	W16
RGND	W18
RGND	Y1
RGND	Y2
RGND	AA2
RGND	AB2
RGND	AB3
RGND	AB4
RGND	AB5
RGND	AB7
RGND	AB9
RGND	AB11
RGND	AB12
RGND	AB13
RGND	AB14
RGND	AB15
RGND	AB16
RGND	AB17
RGND	AB18
RGND	AB19
RGND	AB20
RGND	AC1
RGND	AC3
RGND	AC5
RGND	AC6
RGND	AC10
RGND	AC12
RGND	AC18
RGND	AC20
RREF	N22
RSVD	G5
RSVD	H5
RSVD	J1
RSVD	J2

Name	Pin
RSVD	K1
RSVD	K5
RSVD	K10
RSVD	L2
RSVD	L10
RSVD	L16
RSVD	N2
SR_PVSS	D22
SR_PVSS	D23
SR_PVSS	E22
SR_PVSS	E23
SR_VDDBATA5V	G22
SR_VDDBATA5V	G23
SR_VDDBATP5V	F22
SR_VDDBATP5V	F23
SR_VLX	C22
SR_VLX	C23
VDD	L11
VDD	L13
VDD	L14
VDD	M14
VDD	N12
VDD	N14
VDD	P12
VDD	P13
VDD	P14
VDDIO	K16
VDDIO_RF	K11
VDDIO_RF	P19
VOUT_CLDO	H22
VOUT_CLDO	H23
VOUT_LNLDO1	J22
VOUT_LNLDO1	J23
VOUT_LNLDO2	J19
VSS	A1
VSS	B1
VSS	B2
VSS	B7
VSS	E7
VSS	E8

Name	Pin
VSS	E11
VSS	H2
VSS	K14
VSS	K19
VSS	L22
VSS	L23
VSS	M10
VSS	M16
VSS	P10
VSS	P15
VSS	P16
VSS	P22
VSS	R11
VSS	R12
VSS	R13
VSS	R14
VSS	R15
VSS	T19
VSS	T22
VSS	V22
VSS	V23
WL_REG_ON	J16
WRF_AFE_VDD1P2_CORE0	W10
WRF_AFE_VDD1P2_CORE1	W14
WRF_GPIO_OUT	W8
WRF_PADRV2G_VDD3P3_CORE0	W1
WRF_PADRV2G_VDD3P3_CORE1	AC14
WRF_PADRV5G_VDD3P3_CORE0	AB1
WRF_PADRV5G_VDD3P3_CORE1	AC16
WRF_PAOUT_2G_CORE0	U1
WRF_PAOUT_2G_CORE1	AC13
WRF_PAOUT_5G_CORE0	AC2
WRF_PAOUT_5G_CORE1	AC17
WRF_PA_VDD3P3_CORE0	AA1
WRF_PA_VDD3P3_CORE1	AC15
WRF_RFIN_2G_CORE0	R1
WRF_RFIN_2G_CORE1	AC11
WRF_RFIN_5G_CORE0	AC4
WRF_RFIN_5G_CORE1	AC19
WRF_RX2G_VDD1P2_CORE0	U5

Name	*Pin*
WRF_RX2G_VDD1P2_CORE1	W12
WRF_RX5G_VDD1P2_CORE0	AB8
WRF_RX5G_VDD1P2_CORE1	W17
WRF_SYNTH_VDD1P2	AC9
WRF_TCXO_CKIN2V	Y22
WRF_TCXO_VDD1P8	W22
WRF_TX_VDD1P2_CORE0	AB6
WRF_TX_VDD1P2_CORE1	AB10
WRF_VCO_VDD1P2	AC7
WRF_XTAL_CAB_GND1P2	T17
WRF_XTAL_CAB_GND1P2	U19
WRF_XTAL_CAB_GND1P2	V19
WRF_XTAL_CAB_GND1P2	W19
WRF_XTAL_CAB_GND1P2	AA22
WRF_XTAL_CAB_GND1P2	AB21
WRF_XTAL_CAB_GND1P2	AB22
WRF_XTAL_CAB_GND1P2	AB23
WRF_XTAL_CAB_GND1P2	AC21
WRF_XTAL_CAB_GND1P2	AC23
WRF_XTAL_CAB_VDD1P2	AC22
WRF_XTAL_CAB_XON	W23
WRF_XTAL_CAB_XOP	AA23

Signal Descriptions

The signal name, type, and description of each pin in the BCM43243 is listed in Table 4. The Type indicates pin direction (I/O = bidirectional, I = input, O = output) and the internal pull-up/pull-down characteristics (PU = weak internal pull-up resistor and PD = weak internal pull-down resistor), if any.

Table 4: FCFBGA Signal Descriptions

Signal Name	FCFBGA Ball #	Type	Description
WLAN Radio Pins			
AVDD_BBPLL	N19	I	Baseband PLL supply
WRF_XTAL_CAB_XON	W23	O	XTAL output
WRF_XTAL_CAB_XOP	AA23	I	XTAL input
WRF_RFIN_2G_CORE1	AC11	I	2.4G RF input core 1
WRF_RFIN_5G_CORE1	AC19	I	5G RF input core 1
WRF_GPIO_OUT	W8	O	WLAN Radio GPIO
WRF_TCXO_CKIN2V	Y22	I	TCXO buffered input. When not using a TCXO this pin should be connected to ground.
WRF_SYNTH_VDD1P2	AC9	I	Clock and miscellaneous supplies
WRF_TCXO_VDD1P8	W22		
WRF_VCO_VDD1P2	AC7		
WRF_XTAL_CAB_VDD1P2	AC22		
WRF_XTAL_CAB_GND1P2	T17, U19, V19, W19, AA22, AB21, AB22, AB23, AC21, AC23	I	Clock and miscellaneous grounds
WRF_AFE_VDD1P2_CORE1	W14	I	WLAN core 1 radio supplies
WRF_PADRV2G_VDD3P3_CORE1	AC14		
WRF_PADRV5G_VDD3P3_CORE1	AC16		
WRF_TX_VDD1P2_CORE1	AB10		
WRF_RX2G_VDD1P2_CORE1	W12		
WRF_RX5G_VDD1P2_CORE1	W17		
WRF_RFIN_2G_CORE0	R1	I	2.4G RF input core 0
WRF_RFIN_5G_CORE0	AC4	I	5G RF input core 0
WRF_PAOUT_2G_CORE0	U1	O	2.4 GHz RF output for Core 0
WRF_PAOUT_2G_CORE1	AC13	O	2.4 GHz RF output for Core 1
WRF_PAOUT_5G_CORE0	AC2	O	5 GHz RF output for Core 0
WRF_PAOUT_5G_CORE1	AC17	O	5 GHz RF output for Core 1

Table 4: FCFBGA Signal Descriptions (Cont.)

Signal Name	FCFBGA Ball #	Type	Description
WRF_AFE_VDD1P2_CORE0	W10	I	WLAN core 0 radio supplies
WRF_PADRV2G_VDD3P3_CORE0	W1		
WRF_PADRV5G_VDD3P3_CORE0	AB1		
WRF_TX_VDD1P2_CORE0	AB6		
WRF_RX2G_VDD1P2_CORE0	U5		
WRF_RX5G_VDD1P2_CORE0	AB8		
WRF_PA_VDD3P3_CORE1	AC15	I	WLAN PA Supplies (Core 1)
WRF_PA_VDD3P3_CORE0	AA1	I	WLAN PA Supplies (Core 0)
WLAN Digital Pins			
RF_SW_CTRL_0	B16	O	WLAN RF switch control outputs
RF_SW_CTRL_1	B13		
RF_SW_CTRL_2	B15		
RF_SW_CTRL_3	A13		
RF_SW_CTRL_4	B14		
RF_SW_CTRL_5	B12		
RF_SW_CTRL_6	A11		
RF_SW_CTRL_7	B11		
RF_SW_CTRL_8	U23		
GMODE_EXT_LNA_PU_CORE0	E12	O	2.4G external LNA control core 0
AMODE_EXT_LNA_PU_CORE0	E13	O	5G external LNA control core 0
GMODE_EXT_LNA_PU_CORE1	U22	O	2.4G external LNA control core 1
AMODE_EXT_LNA_PU_CORE1	R19	O	5G external LNA control core 1
GPIO_11	J14	I/O	WLAN GPIO
GPIO_10	K13	I/O	WLAN GPIO
GPIO_9	B20	I/O	WLAN GPIO
GPIO_8	A17	I/O	WLAN GPIO
GPIO_7	A15	I/O	WLAN GPIO
GPIO_12	B19	I/O	This pin can be programmed to be a GPIO or the JTAG TRST_L signal.
GPIO_6	A19	I/O	WLAN GPIO
GPIO_5	B22	I/O	This pin can be programmed to be a GPIO or the JTAG TDO signal.
GPIO_4	B21	I/O	This pin can be programmed to be a GPIO or the JTAG TDI signal.
GPIO_3	A21	I/O	This pin can be programmed to be a GPIO or the JTAG TMS signal.
GPIO_2	B17	I/O	This pin can be programmed to be a GPIO or the JTAG TCK signal.
GPIO_1	B23	I/O	This pin can be programmed to be a GPIO or AP_READY.

Table 4: FCFBGA Signal Descriptions (Cont.)

Signal Name	FCFBGA Ball #	Type	Description
GPIO_0	A23	I/O	This pin can be programmed to be a GPIO or a WLAN_HOST_WAKE output indicating that host wake-up should be performed.
JTAG_SEL	B18	I	JTAG select. The JTAG interface (multiplexed on the GPIO pins) is enabled when this pin is asserted high.
EXT_XTAL_PU	E15	O	External Xtal oscillator power-up signal
VDD	L11, L13, L14, M14, N12, N14, P12–P14	I	Digital always-on core supply
OTP_VDD33	J10	I	3.3V OTP power supply
VDDIO	K16	I	3.3V I/O supply
VDDIO_RF	K11, P19	I	3.3V RF control I/O supply
VSS	A1, B1, B2, B7, E7, E8, E11, H2, K14, K19, L22, L23, M10, M16, P10, P15, P16, P22, R11–R15, T19, T22, V22, V23	I	Core ground
RGND	R2, R5, R7–R10, T1, T2, T5, T7, T8, T10, T11, T13, T14, T16, U2, U8, U11, U13, U16, V1, V2, V5, V8, V9, V11, V13, V15, V16, W2, W5–7, W9, W11, W13, W15, W16, W18, Y1, Y2, AA2, AB2–AB5, AB7, AB9, AB11–AB20, AC1, AC3, AC5, AC6, AC10, AC12, AC18, AC20	I	WLAN Radio ground
WLAN USB Pins			
DP	N23	–	Data+
DM	P23	–	Data–
MONCDR	R22	–	USB 2.0 debug
MONPLL	M19	–	USB 2.0 debug
RREF	N22	–	USB 2.0 reference resistor
AVDD33	M22	–	USB 2.0 3.3V supply
PMU Pins			

Table 4: FCFBGA Signal Descriptions (Cont.)

Signal Name	*FCFBGA Ball #*	*Type*	*Description*
SR_PVSS	D22, D23, E22, E23	I	Switcher ground
SR_VDDBATA5V	G22, G23	I	Battery voltage input for band-gap and LDO3P3
SR_VDDBATP5V	F22, F23	I	Battery voltage input for the CBUCK switcher
SR_VLX	C22, C23	O	Switcher output (1.35V default)
LDO_VDD1P5	K22, K23	I	LDO input for CLDO, LNLDO1, and LNLDO2. Also voltage feedback input for CBUCK. (1.35V default)
WL_REG_ON	J16	I	Used by PMU to power up or power down the internal BCM43243 regulators used by the WLAN section. Also, when deasserted, this pin holds the WLAN section in reset. This pin has an internal 200 kΩ pull-down resistor that is enabled by default. It can be disabled through programming.
PMU_AVSS	F19	I	PMU ground
VOUT_LNLDO1	J22, J23	O	1.2V LNLDO1 output
VOUT_LNLDO2	J19	O	1.2V LNLDO2 output
VOUT_CLDO	H22, H23	O	1.2V Digital core LDO output
Ground Pins			
GND	J8, K2, K8, L5, L19, M2, M5, M8, M9, N5, N9, P2, P5, P8, R23	–	Connect to ground.
No-Connect Pins			
NC	A2, A4, A6, A7, A9, B3, B4, B5, B6, B8, B9, C1, C2, D2, E1, E2, E5, E9, E10, F2, F5, G1, G2, M1, P1	–	No-connect
Reserved Pins			
RSVD	L16	–	Reserved. Connect a 0Ω pull-down resistor to this pin.
RSVD	H5, J8, K2, K8, L5, L19, M2, M5, M8, M9, N5, N9, P2, P5, P8, R23	–	Reserved. Connect to ground.
RSVD	J1, J2, K1, K5, L2	–	Reserved. Connects to VOUT_LNLDO2.
RSVD	K10, L10		Reserved. Connects to VOUT_CLDO
RSVD	G5, N2	–	Reserved. Connect these pins to 3.3V.

WLAN GPIO Signals and Strapping Options

The pins listed in Table 5 are sampled at power-on reset (POR) to determine various operating modes. Sampling occurs a few milliseconds after an internal POR or deassertion of the external POR. After the POR, each pin assumes the GPIO or alternative function specified in the signal descriptions table. Each strapping option pin has an internal pull-up (PU) or pull-down (PD) resistor that determines the default mode. To change the mode, connect an external PU resistor to VDDIO or a PD resistor to GND, using a 10 kΩ resistor or less.

Note: Refer to the reference board schematics for more information.

Table 5: WLAN GPIO Functions and Strapping Options

Pin Name(s)	FCFBGA Pin	Function	Default	Description
GPIO_6, AMODE_EXT_LNA_PU_CORE0	A19 E13	strap_host_ifc_2 strap_host_ifc_1	00	The 2 strap pins strap_host_ifc_[2:1] together select the host interface to enable: 00: Normal USB 01: Bootloader-less USB
GPIO_7	A15	OTPEnabled	1	When this bit is 0, the OTP memory is not powered up by default.
GPIO_8	A17	SFlash Present	0	SFlash present strap
GPIO_9	B20	ARM Remap[0]	1	0: Boot from SRAM, ARM held in reset. 1: Boot from ROM by remapping the ARM core exception vectors, with the ARM held in reset.
GPIO_10	K13	SFlash type	0	Type of sflash used: 1 = Atmel®, 0 = ST®
GPIO_0, GPIO_1	A23 B23	ResourceInitMode[1:0]	10	00: PMU to power up to ILP clock available (no backplane clock). 01: Power up to ILP clock request. 10: ALP clock available. 11: HT clock available. This field may not be set to 11 for implementations using an oscillator running at other than 30 MHz because the PLL must be reprogrammed before it is enabled.
EXT_XTAL_PU	E15	strap_ext_xtal_pu_pol	0	This strap defines the output polarity of the ext_xtal_pu signal. 0 = Active high output polarity. 1 = Active low output polarity.

I/O States

The following notations are used in Table 6:

- I: Input signal
- O: Output signal
- I/O: Input/Output signal
- PU = Pulled up
- PD = Pulled down
- NoPull = Neither pulled up nor pulled down

Table 6: I/O States

Name	*I/O*	*Keeper*	*Active Mode*	*Low Power State/Sleep (All Power Present)*	*Power-down (WL_REG_ON Held Low)*	*Out-of-Reset; Before SW Download (WL_REG_ON High)*	*WL_REG_ON High and VDDIOs Are Present*	*Power Rail*
WL_REG_ON	I	N	Input; PD (pull-down can be disabled)	Input; PD (pull-down can be disabled)	Input; PD (of 200K)	Input; PD (of 200K)	Input; PD (of 200K)	–
GPIO_0	I/O	Y	Input/Output; PU, PD, NoPull (programmable [Default: PD])	Input/Output; PU, PD, NoPull (programmable [Default: PD])	High-Z, NoPull	Input; PD	Input; PD	WL_VDDIO
GPIO_1	I/O	Y	Input/Output; PU, PD, NoPull (programmable [Default: PU])	Input/Output; PU, PD, NoPull (programmable [Default: PU])	High-Z, NoPull	Input; PU	Input; PU	WL_VDDIO
GPIO_2	I/O	Y	Input/Output; PU, PD, NoPull (programmable [Default: PU])	Input/Output; PU, PD, NoPull (programmable [Default: PU])	High-Z, NoPull	Input; PU	Input; PU	WL_VDDIO
GPIO_3	I/O	Y	Input/Output; PU, PD, NoPull (programmable [Default: PU])	Input/Output; PU, PD, NoPull (programmable [Default: PU])	High-Z, NoPull	Input; PU	Input; PU	WL_VDDIO
GPIO_4	I/O	Y	Input/Output; PU, PD, NoPull (programmable [Default: noPull])	Input/Output; PU, PD, NoPull (programmable [Default: noPull])	High-Z, NoPull	Input; noPull	Input; NoPull	WL_VDDIO
GPIO_5	I/O	Y	Input/Output; PU, PD, NoPull (programmable [Default: PU])	Input/Output; PU, PD, NoPull (programmable [Default: PU])	High-Z, NoPull	Input; PU	Input; PU	WL_VDDIO
GPIO_6	I/O	Y	Input/Output; PU, PD, NoPull (programmable [Default: PD])	Input/Output; PU, PD, NoPull (programmable [Default: PD])	High-Z, NoPull	Input; PD	Input; PD	WL_VDDIO

Table 6: I/O States (Cont.)

Name	I/O	Keeper	Active Mode	Low Power State/Sleep (All Power Present)	Power-down (WL_REG_ON Held Low)	Out-of-Reset; Before SW Download (WL_REG_ON High)	WL_REG_ON High and VDDIOs Are Present	Power Rail

Note:

1. Keeper column: N=pad has no keeper. Y=pad has a keeper. Keeper is always active except in Power-down state.
2. If there is no keeper, and it is an input and there is Nopull, then the pad should be driven to prevent leakage due to floating pad (SDIO_CLK, for example).
3. In the Power-down state (xx_REG_ON=0): High-Z; NoPull => the pad is disabled because power is not supplied.

Section 9: DC Characteristics

Note: Values in this data sheet are design goals and are subject to change based on the results of device characterization.

Absolute Maximum Ratings

Caution! The absolute maximum ratings in Table 7 indicate levels where permanent damage to the device can occur, even if these limits are exceeded for only a brief duration. Functional operation is not guaranteed under these conditions. Operation at absolute maximum conditions for extended periods can adversely affect long-term reliability of the device.

Table 7: Absolute Maximum Ratings

Rating	*Symbol*	*Value*	*Unit*
DC supply voltage for I/O	VDDIO	–0.5 to 3.8	V
DC supply voltage for RF	VDDRF	–0.5 to 1.32	V
DC supply voltage for core	VDDC	–0.5 to 1.32	V
DC supply voltage for RF I/Os and PA driver supply	VDDIO_RF	–0.5 to 3.8	V
DC supply voltage for battery-supplied pins	SR_VDDBATA5V (VBAT)	–0.5 to 5.25	V
DC input supply voltage for CLDO and LNLDO1	–	–0.5 to 2.1	V
WRF_TCXO_VDD	–	–0.5 to 1.98	V
Maximum undershoot voltage for I/O	$V_{undershoot}$	–0.5	V
Maximum Junction Temperature	T_j	125	°C

Environmental Ratings

The environmental ratings are shown in Table 8.

Table 8: Environmental Ratings

Characteristic	*Value*	*Units*	*Conditions/Comments*
Ambient Temperature (T_A)	0 to +70	°C	Functional operation[a]
Storage Temperature	–40 to +125	°C	–
Relative Humidity	Less than 60	%	Storage
	Less than 85	%	Operation

a. Functionality is guaranteed but specifications require derating at extreme temperatures; see the specification tables for details.

Electrostatic Discharge Specifications

Extreme caution must be exercised to prevent electrostatic discharge (ESD) damage. Proper use of wrist and heel grounding straps to discharge static electricity is required when handling these devices. Always store unused material in its antistatic packaging.

Table 9: ESD Specifications

Pin Type	*Symbol*	*Condition*	*ESD Rating*	*Unit*
ESD, Handling Reference: NQY00083, Section 3.4, Group D9, Table B	ESD_HAND_HBM	Human body model contact discharge per JEDEC EID/JESD22-A114	1000	V
Machine Model (MM)	ESD_HAND_MM	Machine model contact	75	V
CDM	ESD_HAND_CDM	Charged device model contact discharge per JEDEC EIA/JESD22-C101	500	V

Recommended Operating Conditions and DC Characteristics

Caution! Functional operation is not guaranteed outside of the limits shown in Table 10 and operation outside these limits for extended periods can adversely affect long-term reliability of the device.

Table 10: Recommended Operating Conditions and DC Characteristics

Parameter	Symbol	Value			Unit
		Minimum	Typical	Maximum	
DC supply voltage	VDD33	3.0	3.3	3.6	V
DC supply voltage	VDDIO	3.0	3.3	3.6	V
DC supply voltage for CBUCK	VBAT	3.0	3.3	5.25	V
DC supply voltage for core	VDD	1.14	1.2	1.26	V
DC supply voltage for RF blocks in chip	VDDRF	1.14	1.2	1.26	V
DC supply voltage for TCXO input buffer	WRF_TCXO_VDD	1.62	1.8	1.98	V
Other Digital I/O Pins					
For VDDIO = 3.3V:					
Input high voltage	VIH	2.00	–	–	V
Input low voltage	VIL	–	–	0.80	V
Output high voltage @ 2 mA	VOH	VDDIO – 0.4	–	–	V
Output Low Voltage @ 2 mA	VOL	–	–	0.40	V
RF Switch Control Output Pins					
For VDDIO_RF = 3.3V:					
Output High Voltage @ 2 mA	VOH	VDDIO – 0.4	–	–	V
Output Low Voltage @ 2 mA	VOL	–	–	0.40	V
Input capacitance	C_{IN}	–	–	5	pF

Section 10: WLAN RF Specifications

Introduction

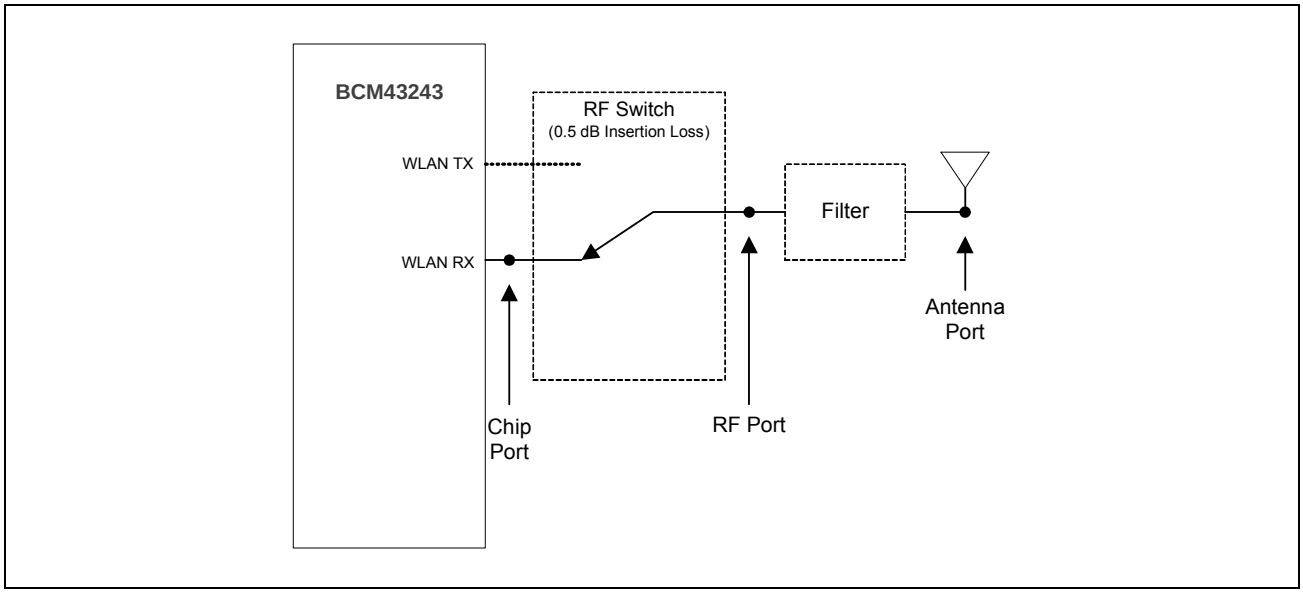
The BCM43243 includes an integrated dual-band direct conversion radio that supports either the 2.4 GHz band or the 5 GHz band. This section describes the RF characteristics of the 2.4 GHz and 5 GHz portions of the radio.

Note: Values in this data sheet are design goals and are subject to change based on the results of device characterization.

Unless otherwise stated, limit values apply for the conditions specified in Table 8: “Environmental Ratings,” on page 53 and Table 10: “Recommended Operating Conditions and DC Characteristics,” on page 54. Typical values apply for the following conditions:

- VDD33 = 3.3V ± 10% (VBAT tied to VDD33)
- Ambient temperature +25°C

Figure 16: Port Locations



Note: All WLAN specifications are measured at the chip port, unless otherwise specified.

2.4 GHz Band General RF Specifications

Table 11: 2.4 GHz Band General RF Specifications

Item	Condition	Minimum	Typical	Maximum	Unit
TX/RX switch time	Including TX ramp down	–	–	5	µs
RX/TX switch time	Including TX ramp up	–	–	2	µs
Power-up and power-down ramp time	DSSS/CCK modulations	–	–	< 2	µs

WLAN 2.4 GHz Receiver Performance Specifications

Note: The specifications in Table 12 are measured at the chip port, unless otherwise specified.

Table 12: WLAN 2.4 GHz Receiver Performance Specifications

Parameter	Condition/Notes	Minimum	Typical	Maximum	Unit
Frequency range	–	2400	–	2500	MHz
SISO RX sensitivity (8% PER for 1024 octet PSDU)	1 Mbps DSSS	–	–99.0	–	dBm
	2 Mbps DSSS	–	–96.0	–	dBm
	5.5 Mbps DSSS	–	–94.2	–	dBm
	11 Mbps DSSS	–	–90.4	–	dBm
SISO RX sensitivity (10% PER for 1024 octet PSDU)	6 Mbps OFDM	–	–94.0	–	dBm
	9 Mbps OFDM	–	–93.1	–	dBm
	12 Mbps OFDM	–	–91.7	–	dBm
	18 Mbps OFDM	–	–89.6	–	dBm
	24 Mbps OFDM	–	–85.6	–	dBm
	36 Mbps OFDM	–	–83	–	dBm
	48 Mbps OFDM	–	–77.7	–	dBm
	54 Mbps OFDM	–	–76.5	–	dBm
MIMO RX sensitivity (10% PER for 1024 octet PSDU)	6 Mbps OFDM	–	–95.0	–	dBm/core
	9 Mbps OFDM	–	–94.2	–	dBm/core
	12 Mbps OFDM	–	–93.5	–	dBm/core
	18 Mbps OFDM	–	–92.6	–	dBm/core
	24 Mbps OFDM	–	–88.6	–	dBm/core
	36 Mbps OFDM	–	–86	–	dBm/core
	48 Mbps OFDM	–	–81.1	–	dBm/core
	54 Mbps OFDM	–	–80.1	–	dBm/core

Table 12: WLAN 2.4 GHz Receiver Performance Specifications (Cont.)

Parameter	Condition/Notes		Minimum	Typical	Maximum	Unit
SISO RX sensitivity (10% PER for 4096 octet PSDU)[a]. Defined for default parameters: GF, 800 ns GI, and non-STBC.	20 MHz channel spacing for all MCS rates					
	MCS 7		–	–73.9	–	dBm
	MCS 6		–	–75.6	–	dBm
	MCS 5		–	–77	–	dBm
	MCS 4		–	–81.4	–	dBm
	MCS 3		–	–84.5	–	dBm
	MCS 2		–	–88.3	–	dBm
	MCS 1		–	–90.5	–	dBm
	MCS0		–	–92.5	–	dBm
MIMO RX sensitivity (10% PER for 4096 octet PSDU)[a]. Defined for default parameters: GF, 800 ns GI, and non-STBC.	20 MHz channel spacing for all MCS rates					
	MCS 15		–	–70.4	–	dBm (total)
	MCS 8		–	–90.1	–	dBm (total)
	MCS 7		–	–76.9	–	dBm/core
	MCS 6		–	–78.6	–	dBm/core
	MCS 5		–	–80	–	dBm/core
	MCS 4		–	–84.4	–	dBm/core
	MCS 3		–	–87.5	–	dBm/core
	MCS 2		–	–91.1	–	dBm/core
	MCS 1		–	–93.2	–	dBm/core
	MCS0		–	–94.0	–	dBm/core
Blocking level for 1 dB RX Sensitivity degradation (without external filtering)[b]	776–794 MHz	CDMA2000	–20	–	–	dBm
	824–849 MHz[c]	cdmaOne	–24.5	–	–	dBm
	824–849 MHz	GSM850	–20	–	–	dBm
	880–915 MHz	E-GSM	–18	–	–	dBm
	1710–1785 MHz	GSM1800	–20	–	–	dBm
	1850–1910 MHz	GSM1800	–22	–	–	dBm
	1850–1910 MHz	cdmaOne	–32	–	–	dBm
	1850–1910 MHz	WCDMA	–29	–	–	dBm
	1920–1980 MHz	WCDMA	–32	–	–	dBm
In-band static CW jammer immunity (fc – 8 MHz < fcw < + 8 MHz)	RX PER < 1%, 54 Mbps OFDM, 1000 octet PSDU for: (RxSense + 23 dB < Rxlevel < max input level)		–80	–	–	dBm
Input In-Band IP3	Maximum LNA gain		–	–15.5	–	dBm
	Minimum LNA gain		–	–1.5	–	dBm
Maximum receive level @ 2.4 GHz	@ 1, 2 Mbps (8% PER, 1024 octets)		–3.5	–	–	dBm
	@ 5.5, 11 Mbps (8% PER, 1024 octets)		–9.5	–	–	dBm
	@ 6–54 Mbps (10% PER, 1024 octets)		–19.5	–	–	dBm
	@ MCS0–7 rates (10% PER, 4095 octets)		–19.5	–	–	dBm

Table 12: WLAN 2.4 GHz Receiver Performance Specifications (Cont.)

Parameter	Condition/Notes		Minimum	Typical	Maximum	Unit
LPF 3 dB Bandwidth	–		9	–	10	MHz
Adjacent channel rejection-DSSS (Difference between interfering and desired signal at 8% PER for 1024 octet PSDU with desired signal level as specified in Condition/Notes)	***Desired and interfering signal 30 MHz apart***					
	1 Mbps DSSS	–74 dBm	35	–	–	dB
	2 Mbps DSSS	–74 dBm	35	–	–	dB
	Desired and interfering signal 25 MHz apart					
	5.5 Mbps DSSS	–70 dBm	35	–	–	dB
	11 Mbps DSSS	–70 dBm	35	–	–	dB
Adjacent channel rejection-OFDM (Difference between interfering and desired signal (25 MHz apart) at 10% PER for 1024 octet PSDU with desired signal level as specified in Condition/Notes)	6 Mbps OFDM	–79 dBm	16	–	–	dB
	9 Mbps OFDM	–78 dBm	15	–	–	dB
	12 Mbps OFDM	–76 dBm	13	–	–	dB
	18 Mbps OFDM	–74 dBm	11	–	–	dB
	24 Mbps OFDM	–71 dBm	8	–	–	dB
	36 Mbps OFDM	–67 dBm	4	–	–	dB
	48 Mbps OFDM	–63 dBm	0	–	–	dB
	54 Mbps OFDM	–62 dBm	–1	–	–	dB
Adjacent channel rejection MCS0–7 (Difference between interfering and desired signal (25 MHz apart) at 10% PER for 4096 octet PSDU with desired signal level as specified in Condition/Notes)	MCS7	–61 dBm	–2	–	–	dB
	MCS6	–62 dBm	–1	–	–	dB
	MCS5	–63 dBm	0	–	–	dB
	MCS4	–67 dBm	4	–	–	dB
	MCS3	–71 dBm	8	–	–	dB
	MCS2	–74 dBm	11	–	–	dB
	MCS1	–76 dBm	13	–	–	dB
	MCS0	–79 dBm	16	–	–	dB
Maximum receiver gain	–	–	–	105	–	dB
Gain control step	–	–	–	3	–	dB
RSSI accuracy[d]	Range –95 dBm to –30 dBm		–5	–	5	dB
	Range above –30 dBm		–8	–	8	dB
Return loss	Z_o = 50Ω, across the dynamic range		6	10	–	dB
Receiver cascaded noise figure	At maximum gain		–	3.5	–	dB

a. Sensitivity degradations for alternate settings in MCS modes. MM: 0.5 dB drop, SGI: 2 dB drop, and STBC: 0.75 dB drop.
b. The cellular standard listed for each band indicates the type of modulation used to generate the interfering signal in that band for the purpose of this test. It is not intended to indicate any specific usage of each band in any specific country.
c. The blocking levels are valid for channels 1 to 11. (For higher channels, the performance may be lower due to third harmonic signals (3 × 824 MHz) falling within band.)
d. The minimum and maximum values shown have a 95% confidence level.

WLAN 2.4 GHz Transmitter Performance Specifications

Note: The specifications in Table 13 are measured at the chip port output, unless otherwise specified.

Table 13: WLAN 2.4 GHz Transmitter Performance Specifications[a]

Parameter	Condition/Notes		Minimum	Typical	Maximum	Unit
Frequency range	–		2400	–	2500	MHz
Harmonic level (at –5 dBm with 100% duty cycle)	4.8–5.0 GHz	2nd harmonic	–	–	TBD	dBm/ 1 MHz
	7.2–7.5 GHz	3rd harmonic	–	–	TBD	dBm/ 1 MHz
OFDM EVM	OFDM, 64 QAM	0 dBm	–	–31	–	dB
OFDM EVM	OFDM, 64 QAM	–3 dBm	–	–33.9	–	dB
OFDM EVM	MCS7	–6 dBm	–	–35	–	dB
TX power at chip port for highest power level setting at 25°C, VDD33 = 3.3V, spectral mask and EVM compliance[b]	IEEE 802.11b: 1 Mbps		–	19.0	–	dBm
	IEEE 802.11g: 6 Mbps		–	22.5	–	dBm
	IEEE 802.11g: 54 Mbps @ 25 dB EVM, SISO + CDD		–	18.5	–	dBm
	MCS7: HT20 @ 28 dB EVM, SISO + CDD		–	17.0	–	dBm
	MCS7: HT40 @ 28 dB EVM, SISO + CDD		–	17.0	–	dBm
Phase noise	37.4 MHz crystal, integrated from 10 kHz to 10 MHz		–	0.5	–	Degrees
TX power control dynamic range	–		10	–	–	dB
Carrier suppression	–		15	–	–	dBc
Gain control step	–		–	0.25	–	dB
Return loss at chip port TX	Z_o = 50Ω		4	6	–	dB

a. All power targets are measured at the chip output and were measured using revision 6 reference boards.
b. Derate by 1 dB for PA_Vdd supply (direct supply to PA) of 3V.

WLAN 5 GHz Receiver Performance Specifications

Note: The specifications in Table 14 are measured at the chip port input, unless otherwise specified.

Table 14: WLAN 5 GHz Receiver Performance Specifications

Parameter	Condition/Notes	Minimum	Typical	Maximum	Unit
Frequency range	–	4900	–	5845	MHz
SISO RX sensitivity (10% PER for 1000 octet PSDU)	6 Mbps OFDM	–	–92.4	–	dBm
	9 Mbps OFDM	–	–91.1	–	dBm
	12 Mbps OFDM	–	–89.7	–	dBm
	18 Mbps OFDM	–	–87.6	–	dBm
	24 Mbps OFDM	–	–83.6	–	dBm
	36 Mbps OFDM	–	–81	–	dBm
	48 Mbps OFDM	–	–76.2	–	dBm
	54 Mbps OFDM	–	–75.1	–	dBm
MIMO RX sensitivity (10% PER for 1000 octet PSDU)	6 Mbps OFDM	–	–93.5	–	dBm/core
	9 Mbps OFDM	–	–88.3	–	dBm/core
	12 Mbps OFDM	–	–86.7	–	dBm/core
	18 Mbps OFDM	–	–84.5	–	dBm/core
	24 Mbps OFDM	–	–80.8	–	dBm/core
	36 Mbps OFDM	–	–78	–	dBm/core
	48 Mbps OFDM	–	–73.4	–	dBm/core
	54 Mbps OFDM	–	–78.0	–	dBm/core
SISO RX sensitivity (10% PER for 4096 octet PSDU) Defined for default parameters: GF, 800 ns GI, and non-STBC.	20 MHz channel spacing for all MCS rates				
	MCS 7	–	–71.9	–	dBm
	MCS 6	–	–73.6	–	dBm
	MCS 5	–	–75	–	dBm
	MCS 4	–	–79.4	–	dBm
	MCS 3	–	–82.5	–	dBm
	MCS 2	–	–86.3	–	dBm
	MCS 1	–	–88.5	–	dBm
	MCS 0	–	–90.5	–	dBm

Table 14: WLAN 5 GHz Receiver Performance Specifications (Cont.)

Parameter	Condition/Notes	Minimum	Typical	Maximum	Unit
MIMO RX sensitivity (10% PER for 4096 octet PSDU) Defined for default parameters: GF, 800 ns GI, and non-STBC.	20 MHz channel spacing for all MCS rates				
	MCS 15	–	–69.0	–	dBm (total)
	MCS 8	–	–89.0	–	dBm (total)
	MCS 7	–	–74.9	–	dBm/core
	MCS 6	–	–76.6	–	dBm/core
	MCS 5	–	–78	–	dBm/core
	MCS 4	–	–82.4	–	dBm/core
	MCS 3	–	–85.5	–	dBm/core
	MCS 2	–	–89.3	–	dBm/core
	MCS 1	–	–91.2	–	dBm/core
	MCS 0	–	–92.5	–	dBm/core
SISO RX sensitivity (10% PER for 4096 octet PSDU) Defined for default parameters: GF, 800 ns GI, and non-STBC.	40 MHz channel spacing for all MCS rates				
	MCS 7	–	–69.4	–	dBm
	MCS 6	–	–71.1	–	dBm
	MCS 5	–	–72.5	–	dBm
	MCS 4	–	–77	–	dBm
	MCS 3	–	–80	–	dBm
	MCS 2	–	–83.8	–	dBm
	MCS 1	–	–86	–	dBm
	MCS 0	–	–88.1	–	dBm
MIMO RX sensitivity (10% PER for 4096 octet PSDU) Defined for default parameters: GF, 800 ns GI, and non-STBC.	40 MHz channel spacing for all MCS rates				
	MCS 15	–	–67.0	–	dBm (total)
	MCS 8	–	–86.5	–	dBm (total)
	MCS 7	–	–71.9	–	dBm/core
	MCS 6	–	–73.7	–	dBm/core
	MCS 5	–	–75.1	–	dBm/core
	MCS 4	–	–79.6	–	dBm/core
	MCS 3	–	–82.7	–	dBm/core
	MCS 2	–	–86.5	–	dBm/core
	MCS 1	–	–88.6	–	dBm/core
	MCS 0	–	–90.4	–	dBm/core
Input In-Band IP3	Maximum LNA gain	–	–15.5	–	dBm
	Minimum LNA gain	–	–1.5	–	dBm
Maximum receive level @ 5.24 GHz	@ 6, 9, 12 Mbps	–29.5	–	–	dBm
	@ 18, 24, 36, 48, 54 Mbps	–29.5	–	–	dBm
LPF 3 dB bandwidth	–	9	–	18	MHz

Table 14: WLAN 5 GHz Receiver Performance Specifications (Cont.)

Parameter	Condition/Notes		Minimum	Typical	Maximum	Unit
Adjacent channel rejection (Difference between interfering and desired signal (20 MHz apart) at 10% PER for 1000 octet PSDU with desired signal level as specified in Condition/Notes)	6 Mbps OFDM	–79 dBm	16	–	–	dB
	9 Mbps OFDM	–78 dBm	15	–	–	dB
	12 Mbps OFDM	–76 dBm	13	–	–	dB
	18 Mbps OFDM	–74 dBm	11	–	–	dB
	24 Mbps OFDM	–71 dBm	8	–	–	dB
	36 Mbps OFDM	–67 dBm	4	–	–	dB
	48 Mbps OFDM	–63 dBm	0	–	–	dB
	54 Mbps OFDM	–62 dBm	–1	–	–	dB
	65 Mbps OFDM	–61 dBm	–2	–	–	dB
Alternate adjacent channel rejection (Difference between interfering and desired signal (40 MHz apart) at 10% PER for 1000[a] octet PSDU with desired signal level as specified in Condition/Notes)	6 Mbps OFDM	–78.5 dBm	32	–	–	dB
	9 Mbps OFDM	–77.5 dBm	31	–	–	dB
	12 Mbps OFDM	–75.5 dBm	29	–	–	dB
	18 Mbps OFDM	–73.5 dBm	27	–	–	dB
	24 Mbps OFDM	–70.5 dBm	24	–	–	dB
	36 Mbps OFDM	–66.5 dBm	20	–	–	dB
	48 Mbps OFDM	–62.5 dBm	16	–	–	dB
	54 Mbps OFDM	–61.5 dBm	15	–	–	dB
	65 Mbps OFDM	–60.5 dBm	14	–	–	dB
Maximum receiver gain	–		–	100	–	dB
Gain control step	–		–	3	–	dB
RSSI accuracy[b]	Range –98 dBm to –30 dBm		–5	–	5	dB
	Range above –30 dBm		–8	–	8	dB
Return loss	Z_o = 50Ω		6	10	–	dB
Receiver cascaded noise figure	At maximum gain		–	5.0	–	dB

a. For 65 Mbps, the size is 4096.
b. The minimum and maximum values shown have a 95% confidence level.

WLAN 5 GHz Transmitter Performance Specifications

Note: The specifications in Table 15 are measured at the chip port, unless otherwise specified.

Table 15: WLAN 5 GHz Transmitter Performance Specifications[a]

Parameter	Condition/Notes		Min.	Typ.	Max.	Unit
Frequency range	–		4900	–	5845	MHz
Harmonic level (at –5 dBm)	9.8–11.570 GHz	2nd harmonic	–	TBD	–	dBm/ MHz
OFDM EVM	OFDM, 64 QAM	0 dBm	–	–30.4	–	dB
OFDM EVM	OFDM, 64 QAM	–3 dBm	–	–32.7	–	dB
OFDM EVM	MCS7	–6 dBm	–	–33.6	–	dB
TX power at chip port for highest power level setting at 25°C, VDD33 = 3.3V, spectral mask and EVM compliance[b]	IEEE 802.11a 6 Mbps, SISO+CDD, low subband,		–	20.0	–	dBm
	IEEE 802.11a 6 Mbps, SISO+CDD, mid subband,		–	19.5	–	dBm
	IEEE 802.11a 6 Mbps, SISO+CDD, high subband,		–	19.0	–	dBm
	IEEE 802.11a 54 Mbps @ 25 dB EVM, SISO+CDD, low subband		–	17.5	–	dBm
	IEEE 802.11a 54 Mbps @ 25 dB EVM, SISO+CDD, mid subband		–	16.5	–	dBm
	IEEE 802.11a 54 Mbps @ 25 dB EVM, SISO+CDD, high subband		–	16.5	–	dBm
	MCS7 HT20 @ 28 dB EVM, SISO+CDD, low subband		–	16.5	–	dBm
	MCS7 HT20 @ 28 dB EVM, SISO+CDD, mid subband		–	15.5	–	dBm
	MCS7 HT20 @ 28 dB EVM, SISO+CDD, high subband		–	15.5	–	dBm
	MCS7 HT40 @ 28 dB EVM, SISO+CDD, low subband		–	16.5	–	dBm
	MCS7 HT40 @ 28 dB EVM, SISO+CDD, mid subband		–	15.5	–	dBm
	MCS7 HT40 @ 28 dB EVM, SISO+CDD, high subband		–	15.5	–	dBm
Phase noise	37.4 MHz crystal, Integrated from 10 kHz to 10 MHz		–	0.7	–	Degrees
TX power control dynamic range	–		20	–	–	dB
Carrier suppression	–		15	–	–	dBc
Gain control step	–		–	0.25	–	dB
Return loss	Z_o = 50Ω		–	6	–	dB

a. All power targets are measured at the chip output and were measured using revision 6 reference boards.
b. Derate by 1.2 dB for PA_Vdd supply (direct supply to PA) of 3V.

General Spurious Emissions Specifications

Table 16: General Spurious Emissions Specifications

Parameter	*Condition/Notes*		*Min.*	*Typ.*	*Max.*	*Unit*
Frequency range	–		TBD	TBD	TBD	MHz
General Spurious Emissions						
TX emissions	30 MHz < f < 1 GHz	RBW = 100 kHz	TBD	TBD	TBD	dBm
	1 GHz < f < 12.75 GHz	RBW = 1 MHz	TBD	TBD	TBD	dBm
	1.8 GHz < f < 1.9 GHz	RBW = 1 MHz	TBD	TBD	TBD	dBm
	5.15 GHz < f < 5.3 GHz	RBW = 1 MHz	TBD	TBD	TBD	dBm
RX/standby emissions	30 MHz < f < 1 GHz	RBW = 100 kHz	TBD	TBD	TBD	dBm
	1 GHz < f < 12.75 GHz	RBW = 1 MHz	TBD	TBD	TBD	dBm
	1.8 GHz < f < 1.9 GHz	RBW = 1 MHz	TBD	TBD	TBD	dBm
	5.15 GHz < f < 5.3 GHz	RBW = 1 MHz	TBD	TBD	TBD	dBm

Section 11: Internal Regulator Electrical Specifications

Note: Values in this data sheet are design goals and are subject to change based on the results of device characterization.

Functional operation is not guaranteed outside of the specification limits provided in this section.

Core Buck Switching Regulator

Table 17: Core Buck Switching Regulator (CBUCK) Specifications

Specification	Notes	Min.	Typ.	Max.	Units
Input supply voltage	DC voltage range inclusive of disturbances (VBAT).	3.0	3.3	5.25	V
PWM mode switching frequency	Forced PWM without FLL enabled	2.8	4	5.2	MHz
	Forced PWM with FLL enabled	3.6	4	4.4	MHz
PWM output current	–	–	–	600	mA
Output current limit	Peak inductor current	1100	1400	–	mA
Output voltage range	Programmable, 30 mV steps Default = 1.35V	1.2	1.35	1.5	V
PWM output voltage DC accuracy	Includes load and line regulation. Forced PWM mode	–4	–	4	%
PWM ripple voltage, static	Measure with 20 MHz bandwidth limit. Static Load. Max. ripple based on VBAT = 3.3V, Vout = 1.35V, Fsw = 4 MHz, 2.2 µH inductor L > 1.05 µH, Cap+Board total-ESR < 20 MΩ, Cout > 1.9 µF, ESL < 200 pH	–	7	20	mVpp
PWM mode peak efficiency	Peak Efficiency at 200 mA load Vout = 1.35V, VBAT = 3.3V at 25°C, Fsw = 4 MHz 2.2 µH inductor 0806 with DCR = 0.11Ω ±25% and ACR <1Ω at 4 MHz	78	84	–	%
PFM mode efficiency	10 mA load current Vout = 1.35V, VBAT = 3.3V at 25°C, Cap+Board total-ESR < 20 MΩ, Cout = 4.7 µF, ESL < 200 pH FLL = OFF 0603-size, L = 2.2 µH, DCR = 240 MΩ ±25%, ACR < 2Ω	67	77	–	%

Table 17: Core Buck Switching Regulator (CBUCK) Specifications (Cont.)

Specification	Notes	Min.	Typ.	Max.	Units
LPOM efficiency	1 mA load current, Vout = 1.35V, VBAT = 3.3V at 25°C, Cap+Board total-ESR < 20 MΩ, Cout = 4.7 µF, ESL < 200 pH FLL = OFF L = 2.2 µH, DCR = 240 MΩ ±25%, ACR < 2Ω	55	65	–	%
Start-up time from power down	VDDIO already ON and steady. Time from REG_ON rising edge to CLDO reaching 1.2V	–	674	850	µs
External inductor	0806 with DCR = 0.11Ω ±25% and ACR <1Ω	–	2.2	–	µH
External output capacitor	Ceramic, X5R, 0402, ESR <30 MΩ at 4 MHz, ±20%, 6.3V	2[a]	4.7	–	µF
External input capacitor	For SR_VDDBATP5V pin, Ceramic, X5R, 0603, ESR < 30 MΩ at 4 MHz, ±20%, 6.3V, 4.7 µF	0.67[a]	4.7	–	µF
Input supply voltage ramp-up time	0 to 4.3V	40	–	–	µs

a. Minimum capacitor value refers to the residual capacitor value after taking into account the part-to-part tolerance, DC-bias, temperature, and aging.

CLDO

Table 18: CLDO Specifications

Specification	*Notes*	*Min.*	*Typ.*	*Max.*	*Units*
Input supply voltage, V_{in}	Min. $V_{in} = V_o + 0.15V = 1.35V$ (for Vo = 1.2V) dropout voltage requirement must be met under maximum load.	1.2	1.35	1.5	V
Output current	–	0.2	–	300	mA
Output voltage, V_o	Programmable in 25 mV steps. Default = 1.2.V	1.1	1.2	1.275	V
Dropout voltage	At max load	–	–	150	mV
Output voltage DC accuracy	Includes line/load regulation	–4	–	+4	%
Quiescent Current	No load	–	20		µA
	Max. load	–	2100	–	µA
Line regulation	V_{in} from (V_o + 0.15V) to 1.5V, maximum load	–	–	5	mV/V
Load regulation	Load from 1 mA to 300 mA; $V_{in} \geq (V_o + 0.15V)$	–	0.025	0.045	mV/mA
PSRR	@1 kHz, Vin ≥ V_o + 0.15V, C_o = 4.7 µF	20	–		dB
Start-up time of PMU	VDDIO up and steady. Time from the REG_ON rising edge to the CLDO reaching 99% of V_o	–	550	850	µs
LDO turn-on time	LDO turn-on time when rest of the chip is up	–	–	180	µs
External output capacitor, C_o	Total ESR: 5 mΩ–240 mΩ	1.32[a]	4.7	–	µF
External input capacitor	Only use an external input capacitor at the VDD_LDO pin if it is not supplied from CBUCK output.	–	1	2.2	µF

a. Minimum capacitor value refers to the residual capacitor value after taking into account the part-to-part tolerance, DC-bias, temperature, and aging.

LNLDO1

Table 19: LNLDO1 Specifications

Specification	*Notes*	*Min.*	*Typ.*	*Max.*	*Units*
Input supply voltage , Vin	Min. $V_{in} = V_o$ +0.15V = 1.35V (for V_o = 1.2V) dropout voltage requirement must be met under maximum load.	1.2	1.35	1.5	V
Output current	–	0.2	–	325	mA
Output voltage, V_o	Programmable in 25 mV steps. Default = 1.2V	1.1	1.2	1.275	V
Dropout voltage	At maximum load	–	–	150	mV
Output voltage DC accuracy	includes Line/Load regulation	–4	–	+4	%
Quiescent current	No load	–	88	–	µA
	Max. load	–	2100	–	µA
Line regulation	V_{in} from (V_o + 0.15V) to 1.5V, 300 mA load	–	–	+5	mV/V
Load regulation	Load from 1 mA to 300 mA; $V_{in} \geq (V_o + 0.15V)$	–	0.025	0.045	mV/mA
Output noise	@30 kHz, 60–325 mA load C_o = 4.7 µF @100 kHz, 60–325 mA load C_o = 4.7 µF	–	–	60 30	nV/rt Hz nV/rt Hz
PSRR	@ 1kHz, Input > 1.35V, C_o= 4.7 µF, V_o = 1.2V	20	–	–	dB
Start-up time of PMU	VDDIO up and steady. Time from REG_ON rise edge to LNLDO1 reaching 99% of V_o	–	550	850	µs
LDO turn-on time	LDO turn-on time when rest of chip is up	–	–	180	µs
External output capacitor, C_o	Total ESR (trace/capacitor): 5 mΩ–240 mΩ	1.32[a]	4.7	–	µF
External input capacitor	Only use an external input capacitor at the VDD_LDO pin if it is not supplied from CBUCK output.	–	1	2.2	µF

a. Minimum capacitor value refers to the residual capacitor value after taking into account the part-to-part tolerance, DC-bias, temperature, and aging.

LNLDO2

Table 20: LNLDO2 Specifications

Specification	Notes	Min.	Typ.	Max.	Units
Input supply voltage, Vin	Min. Vin = V_o + 0.15V = 1.35V (for V_o = 1.2V) dropout voltage requirement must be met under maximum load.	1.2	1.35	1.5	V
Output current	–	–	–	150	mA
Output voltage, V_o	Programmable in 25 mV steps. Default = 1.2V	1.1	1.2	1.275	V
Dropout voltage	At maximum load	–	–	150	mV
Output voltage DC accuracy	includes Line/Load regulation	–4	–	+4	%
Quiescent current	No load	–	44	–	µA
	Max. load	–	970	990	µA
Line regulation	V_{in} from (V_o + 0.15V) to 1.5V, max load	–	–	5.5	mV/V
Load regulation	Load from 1 mA to 150 mA; $V_{in} \geq (V_o + 0.15V)$	–	0.025	0.045	mV/mA
Output noise	@30 kHz, 60-150 mA load C_o = 2.2 µF @100 kHz, 60-150 mA load C_o = 2.2 µF	–	–	60 35	nV/rt Hz nV/rt Hz
PSRR	@ 1kHz, Input > 1.35V, C_o= 2.2 µF, V_o = 1.2V	20	–	–	dB
LDO turn-on time	LDO turn-on time when rest of chip is up	–	–	180	µs
External output capacitor, C_o	Total ESR (trace/capacitor): 5 mΩ–240 mΩ	0.5[a]	2.2	4.7	µF
External input capacitor	Only use an external input capacitor at the VDD_LDO pin if it is not supplied from CBUCK output.	–	1	2.2	µF

a. Minimum capacitor value refers to the residual capacitor value after taking into account the part-to-part tolerance, DC-bias, temperature, and aging.

Section 12: System Power Consumption

Note:

- Values in this data sheet are design goals and are subject to change based on the results of device characterization.
- Unless otherwise stated, these values apply for the conditions specified in Table 10: “Recommended Operating Conditions and DC Characteristics,” on page 54.

WLAN Current Consumption

WLAN current consumption measurements are shown in Table 21 and Table 22 on page 71.

Table 21: 2.4 GHz WLAN Current Consumption

Parameter	*VDD33 = 3.3V*	*VDDIO = 3.3V*	*Unit*
Current PM1 DTIM1	20	23.6	mA
Current PM1 DTIM3	17.8	23.6	mA
Off current	0.13	0.02	mA
Sleep (interbeacon sleep)	16.2	23.6	mA
Listen Current	100	23.7	mA
Continuous RX Mode @ 54 Mbps	102	23.7	mA
Continuous RX Mode @ MCS7 HT20	102	23.8	mA
Continuous RX Mode @ MCS8 HT20	103	23.8	mA
Continuous RX Mode @ MCS15 HT20	109	23.8	mA
802.11b 1 Mbps @ 19.0 dBm	354	23.7	mA
802.11g 6 Mbps @ 22.5 dBm	464	23.7	mA
802.11g 54 Mbps, SISO, EVM = –25 dBc @ 18.5 dBm	348	23.7	mA
802.11g 54 Mbps, CDD, EVM = –25 dBc @ 18.5 dBm	677	23.7	mA
MCS7 HT20, SISO, EVM = –28 dBc @ +17.0 dBm	325	23.7	mA
MCS7 HT20, CDD, EVM = –28 dBc @ +17.0 dBm	615	23.7	mA
MCS7 HT40, SISO, EVM = –28 dBc @ +17.0 dBm	362	23.7	mA
MCS7 HT40, CDD, EVM = –28 dBc @ +17.0 dBm	670	23.7	mA
MCS15 HT20, EVM = –28 dBc @ +17.0 dBm/core	625	23.7	mA
MCS15 HT40, EVM = –28 dBc @ +17.0 dBm/core	674	23.7	mA

Table 22: 5 GHz WLAN Current Consumption

Parameter	*VDD33 = 3.3V*	*VDDIO = 3.3V*	*Unit*
Current PM1 DTIM1	20.1	23.6	mA
Current PM1 DTIM1	17.4	23.6	mA
Off current	0.13	0.02	mA
Sleep (interbeacon sleep)	16.1	23.6	mA
Continuous RX mode 6 Mbps	110	23.8	mA
Continuous RX mode 54 Mbps	109	23.8	mA
Continuous RX mode MCS7 HT20	110	23.8	mA
Continuous RX mode MCS7 HT40	152	23.8	mA
Continuous RX mode MCS8 HT20	123	23.8	mA
Continuous RX mode MCS8 HT40	154	23.8	mA
Continuous RX mode MCS15 HT20	116	23.8	mA
Continuous RX mode MCS15 HT40	171	23.8	mA
802.11a 6 Mbps, SISO @ +19.5 dBm	367	23.8	mA
802.11a 6 Mbps, CDD, @ +19.5 dBm	710	23.8	mA
802.11a 54 Mbps, SISO @ +16.5 dBm	326	23.8	mA
802.11a 54 Mbps, CDD @ +16.5 dBm	610	23.8	mA
MCS7 HT20 @ –28 dBc EVM, SISO @ +15.5 dBm	312	23.8	mA
MCS7 HT20 @ –28 dBc EVM, CDD,@ +15.5 dBm	580	23.8	mA
MCS7 HT40 @ –28 dBc EVM, SISO @ +15.5 dBm	346	23.8	mA
MCS7 HT40 @ –28 dBc EVM, CDD @ +15.5 dBm	632	23.8	mA
MCS15 HT20, –28 dBc EVM @ +15.5 dBm/core	585	23.8	mA
MCS15 HT40, –28 dBc EVM @ +15.5 dBm/core	630	23.8	mA

Section 13: Interface Timing and AC Characteristics

JTAG Timing

Table 23: JTAG Timing Characteristics

Signal Name	Period	Output Maximum	Output Minimum	Setup	Hold
TCK	125 ns	–	–	–	–
TDI	–	–	–	20 ns	0 ns
TMS	–	–	–	20 ns	0 ns
TDO	–	100 ns	0 ns	–	–
JTAG_TRST	250 ns	–	–	–	–

Section 14: Power-Up Sequence and Timing

Sequencing of Reset and Regulator Control Signals

The BCM43243 has signals that allow the host to control power consumption by enabling or disabling the WLAN and internal regulator blocks. These signals are described below. Additionally, diagrams are provided to indicate proper sequencing of the signals for various operational states (see Figure 17 and Figure 18). The timing values indicated are minimum required values; longer delays are also acceptable.

Note: The BCM43243 has an internal power-on reset (POR) circuit. The device will be held in reset for a maximum of 110 ms after VDDC and VDDIO have both passed the 0.6V threshold. Wait at least 150 ms after VDDC and VDDIO are available before initiating SDIO accesses.

Control Signal and Timing

The WL_REG_ON control signal is used by the PMU to power up the WLAN section. When this pin is high, the regulators are enabled and the WLAN section is out of reset. When this pin is low, the WLAN section is in reset. If WL_REG_ON is low, the regulators are disabled.

Figure 17: WLAN = ON

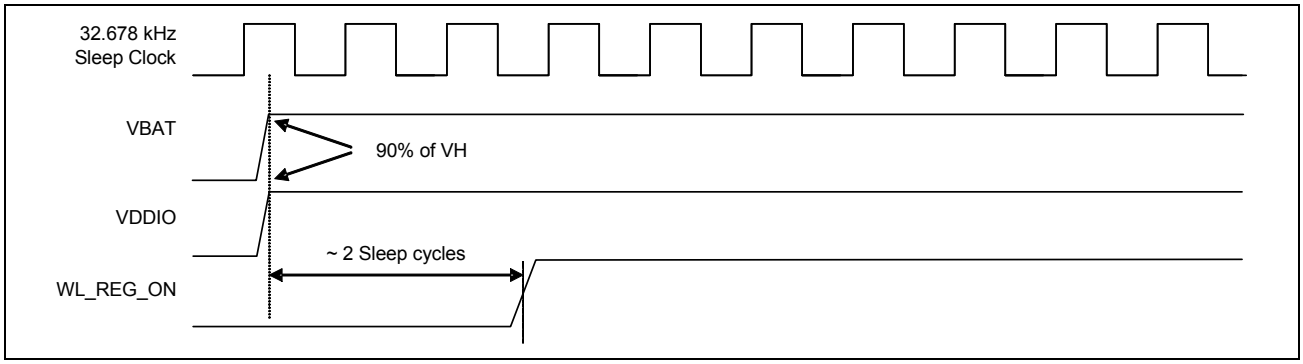
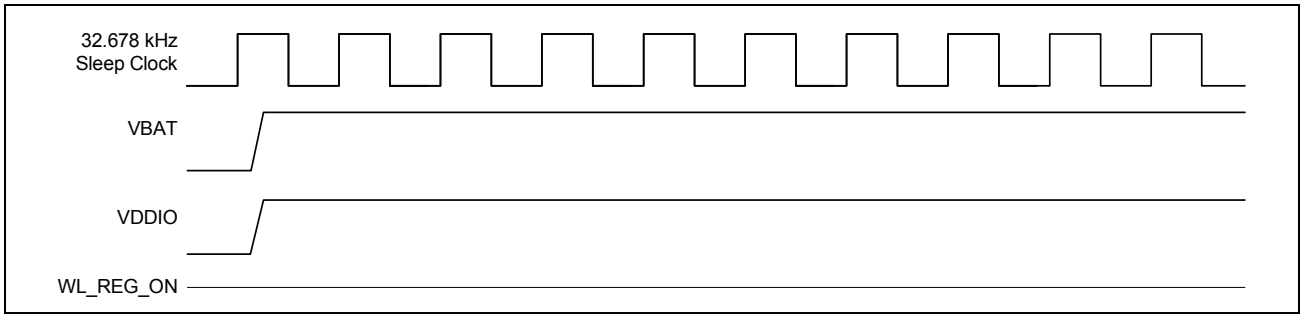


Figure 18: WLAN = OFF



Section 15: Package Information

Package Thermal Characteristics

Table 24: Package JEDEC Thermal Characteristics

Characteristic	*FCFBGA*
θ_{JA} (°C/W) (value in still air)	33.65
θ_{JB} (°C/W)	11.38
θ_{JC} (°C/W)	15.52
Ψ_{JT} (°C/W)	8.82
Ψ_{JB} (°C/W)	13.93
Maximum junction temperature T_j[a] (°C)	125
Maximum power dissipation (W)	2.1

a. Absolute junction temperature limits are maintained through active thermal monitoring and dynamic TX duty cycle limiting.

Junction Temperature Estimation and PSI_{JT} Versus $THETA_{JC}$

Package thermal characterization parameter PSI–J_T (Ψ_{JT}) yields a better estimation of actual junction temperature (T_J) versus using the junction-to-case thermal resistance parameter Theta–J_C (θ_{JC}). The reason for this is that θ_{JC} assumes that all the power is dissipated through the top surface of the package case. In actual applications, some of the power is dissipated through the bottom and sides of the package. Ψ_{JT} takes into account power dissipated through the top, bottom, and sides of the package. The equation for calculating the device junction temperature is:

$$T_J = T_T + P \times \Psi_{JT}$$

Where:

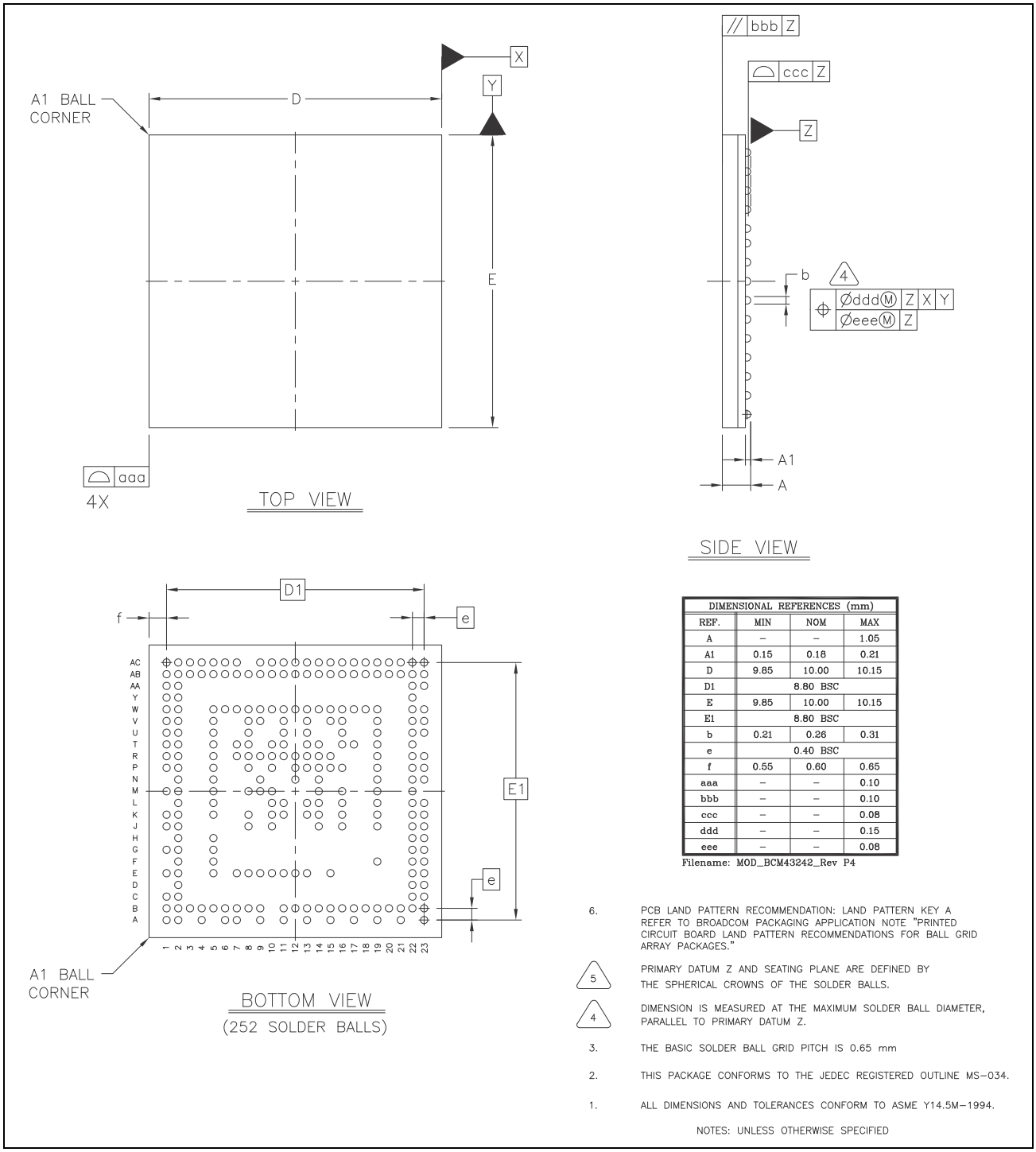
- T_J = Junction temperature at steady-state condition (°C)
- T_T = Package case top center temperature at steady-state condition (°C)
- P = Device power dissipation (Watts)
- Ψ_{JT} = Package thermal characteristics; no airflow (°C/W)

Environmental Characteristics

For environmental characteristics data, see Table 8: “Environmental Ratings,” on page 53.

Section 16: Mechanical Information

Figure 19: FCFBGA Package Mechanical Information



DIMENSIONAL REFERENCES (mm)			
REF.	MIN	NOM	MAX
A	–	–	1.05
A1	0.15	0.18	0.21
D	9.85	10.00	10.15
D1		8.80 BSC	
E	9.85	10.00	10.15
E1		8.80 BSC	
b	0.21	0.26	0.31
e		0.40 BSC	
f	0.55	0.60	0.65
aaa	–	–	0.10
bbb	–	–	0.10
ccc	–	–	0.08
ddd	–	–	0.15
eee	–	–	0.08

Filename: MOD_BCM43242_Rev P4

6. PCB LAND PATTERN RECOMMENDATION: LAND PATTERN KEY A REFER TO BROADCOM PACKAGING APPLICATION NOTE "PRINTED CIRCUIT BOARD LAND PATTERN RECOMMENDATIONS FOR BALL GRID ARRAY PACKAGES."

5 PRIMARY DATUM Z AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

4 DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM Z.

3. THE BASIC SOLDER BALL GRID PITCH IS 0.65 mm

2. THIS PACKAGE CONFORMS TO THE JEDEC REGISTERED OUTLINE MS–034.

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994.

NOTES: UNLESS OTHERWISE SPECIFIED

Section 17: Ordering Information

Part Number	*Package*	*Operating Ambient Temperature*
BCM43243KFFBG	FCFBGA (10.00 mm x 10.00 mm, 0.4 mm pitch)	–10°C to +70°C[a]

a. Absolute junction temperature limits are maintained through active thermal monitoring and dynamic TX duty cycle limiting.

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