65V, 1A, 2MHz Synchronous Step-Down Regulator with 20ns minimum on pulse

BD51180TL **Under Development**

General Description

BD51180TL is a current mode synchronous DC/DC converter integrating high voltage tolerant POWER MOSFETs. The wide range input up to 65V and the very short minimum on pulse down to 20ns enables direct conversion from 48 V battery to 3.3 V at 2.1 MHz operation.

Features

- AEC-Q100 Qualified
- Built-in N-Channel POWER MOSFETs
- Soft Start Function
- Current Mode Control
- Over Current Protection
- Thermal Shut Down Protection
- Input Under Voltage Lock Out Protection
- Input Over Voltage Protection
- Output Over Voltage Protection
- Short Circuit Protection
- Compact and High Power Surface-Mounted Package

Applications

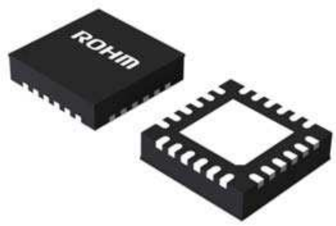
- Automotive Battery Powered Supplies
- Industrial Equipment
- Consumer Supplies

Key Specifications

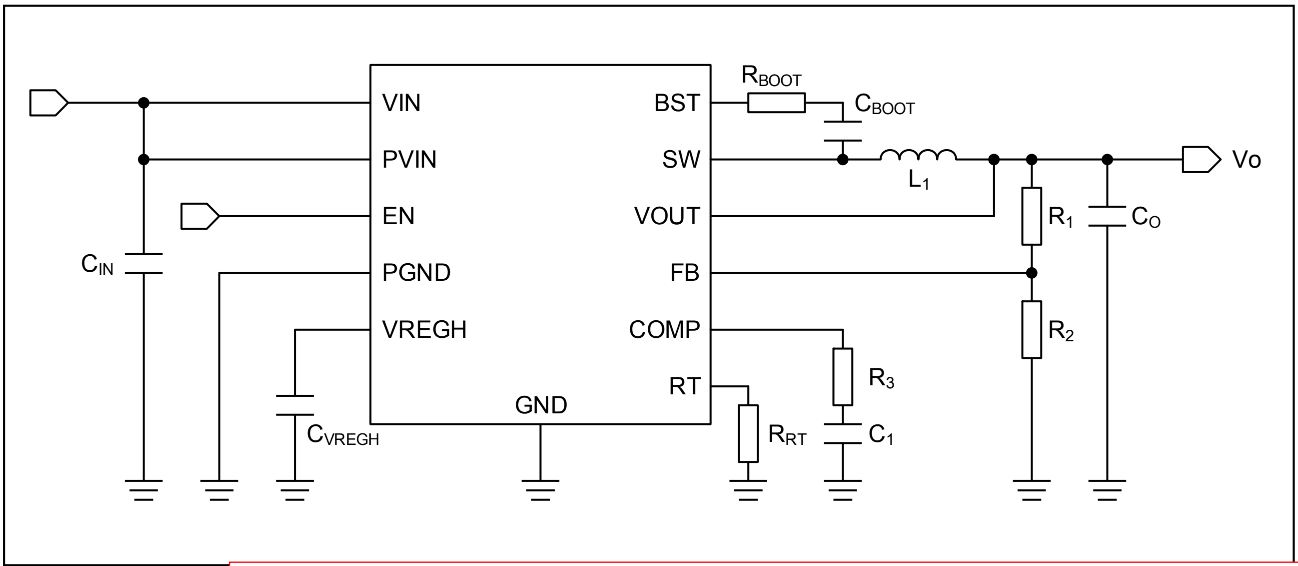
■Input Voltage Range:	12 V to 65 V
■Minimum ON pulse:	20 ns
■Output Voltage Range:	1 to 5 V
■Output Current:	1A (Max)
■Selectable Operating Frequency:	2.1 MHz (Typ)
■Reference Voltage Accuracy:	±2 %(-40 °C to +125 °C)
■Shutdown Circuit Current:	0 μA (Typ)
■Operating Temperature Range:	-40 °C to +125 °C

Package(s)

Package(s)	W(Typ) x D(Typ) x H(Max)
VQFN24SV4040	4.00mm x 4.00mm x 1.00mm



Typical Application Circuit



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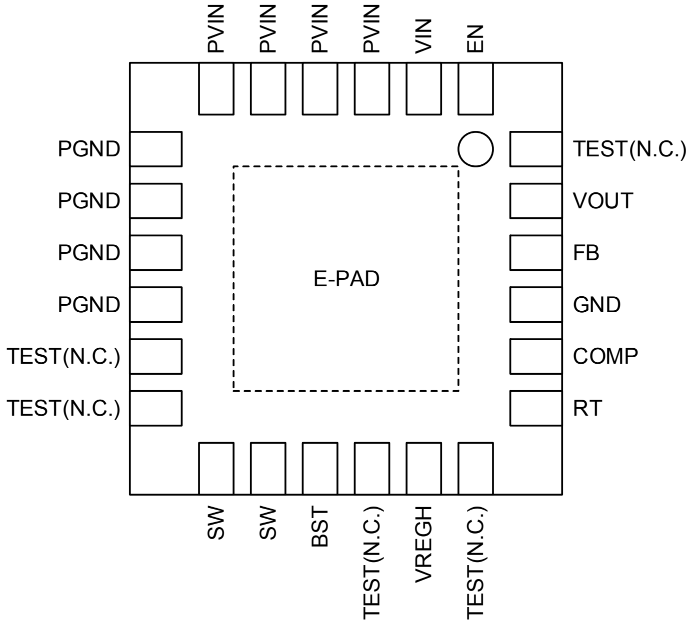
○Product structure : Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays

Pin Configuration



Pin Descriptions

Pin No.	Pin Name	Function
1	EN	Enable pin. Apply low-level (0.8 V or lower) to turn this device into shutdown mode. Apply high-level (2.5 V or higher) to enable this device.
2	VIN	Power supply input pin for internal circuits. Connect this pin to PVIN.
3 to 6	PVIN	Power supply input pin for the switching regulator. Connect VIN terminal of input capacitor(s). 10 μF and 0.1 μF ceramic capacitors are recommended.
7 to 10	PGND	Power GND input pin. Connect GND terminal of input capacitor(s).
11, 12, 16, 18, 24	TEST	No connection pins. Connect these pins to GND.
13, 14	SW	Switching node pin. This pin is connected to internal Power MOSFETs. Connect an power inductor to this pin.
15	BST	Connect a 0.1uF MLCC bootstrap capacitor between this pin and SW pin. This capacitor becomes the power supply of the high-side MOSFET gate driver.
17	VREGH	Internal power supply output terminal. A power supply is supplied to a circuit for the control.
19	RT	Switching frequency setting pin. Connect a frequency setting resistor between this pin and GND.
20	COMP	Output of the gm error amplifier, and the input of PWM comparator. Connect phase compensation components to this pin. See page TBD on how to calculate the resistance and capacitance for phase compensation.
21	GND	Ground
22	FB	Inverting input node for the gm error amplifier. Connect output voltage divider to this pin for setting the output voltage.
23	VOUT	Output voltage terminal.
-	E-PAD	Exposed pad. Connect this pad to the internal PCB ground plane using multiple vias to obtain excellent heat dissipation characteristics.

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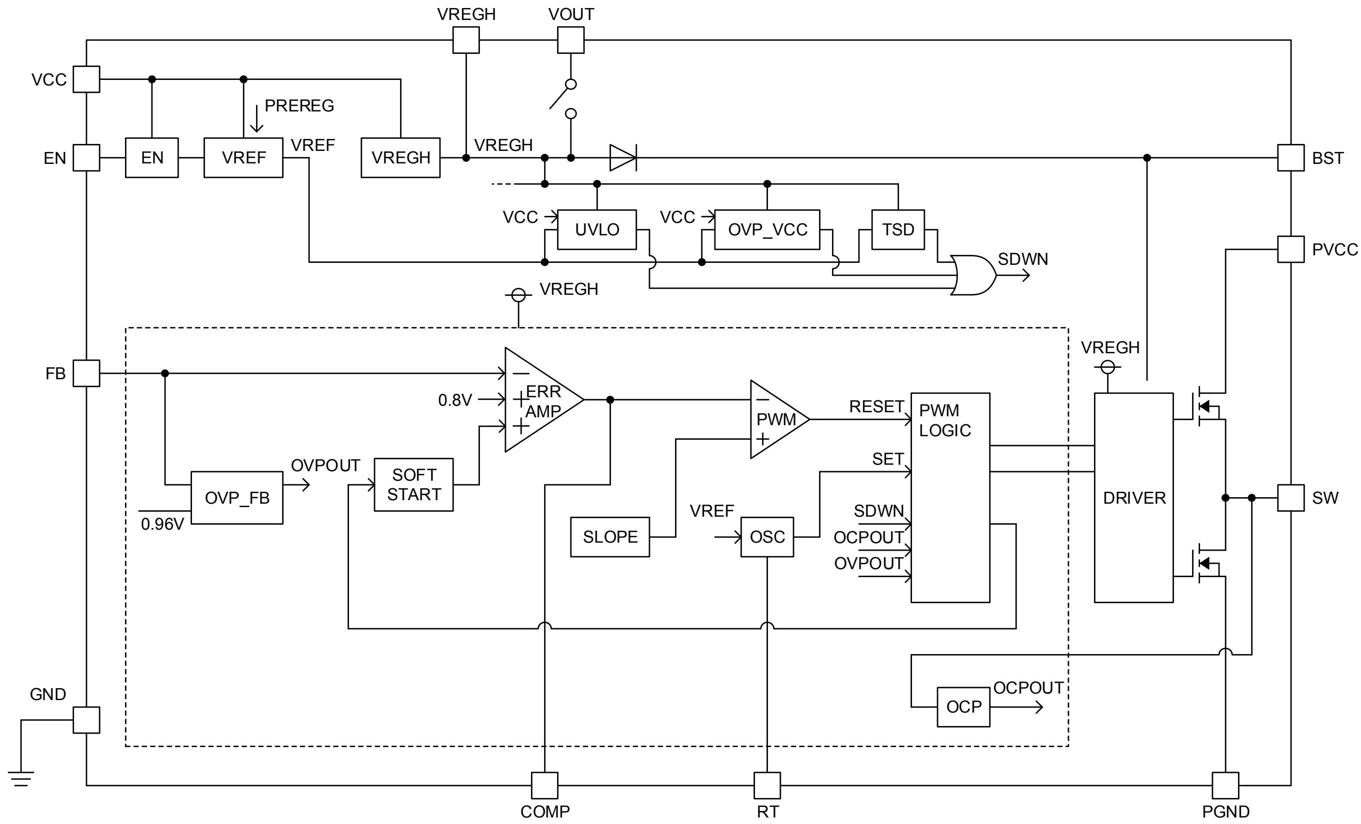
Block Diagram



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Description of Blocks

- ERROR AMP
  The ERROR-AMP block is an error amplifier and its inputs are the reference voltage 0.8 V (Typ) and the “FB” pin voltage. The output “COMP” pin controls the switching duty and output voltage Vo. Insert a capacitor and a resistor between this pin and GND for the loop phase compensation.

- SOFT START
  The SOFT START block prevents the overshoot of the output voltage V_O by gradually increasing the input of the error amplifier when the power supply turns ON to gradually increase the switching duty cycle. The soft start time is set to 1.1 ms (Typ). The soft start time can be changed by setting of the oscillating frequency.

- EN
  The IC is in normal operation when the voltage at “EN” terminal is more than 2.5 V. The IC will shut down when the voltage at “EN” terminal becomes less than 0.8 V.

- OSC (Oscillator)
  This circuit generates a clock signal which determines converter switching frequency. The frequency of the clock can be set by a resistor connected between the RT pin and GND, and the typical switching frequency is 2.1 MHz.
  This clock is also used to set the ramp rate of the Soft Start block.

- SLOPE
  This block generates saw tooth signal used for ramp compensation to prevent sub-harmonic oscillation. Inductor current information is added to the saw tooth signal.

- PWM
  This block modulates duty cycle by comparing the COMP pin voltage and the saw tooth signal from the SLOPE block.

- PWM LOGIC
  The PWM LOGIC block controls the power MOSFET on and off timings. The clock signal from OSC block determines the side MOSFET on timing, and the PWM block output determines the off timing in normal operation. In addition, each protection output signal is passed to the PWM LOGIC and it controls proper protection functions.

- TSD (Thermal Shut Down)
  This is a thermal shutdown circuit. The switching regulator operation is disabled to prevent thermal damage or a thermo-runaway of the IC when the chip temperature reaches to approximately 175 °C s (Typ), and the operation comes back when the chip temperature comes down. Note that the thermal shutdown circuit is intended to prevent catastrophic failure of the IC itself. Therefore it is highly recommended to keep the IC temperature always within the operating temperature range. Operation above operating temperature range will reduce lifetime.

- OCP (Over Current Protection)
  While the low-side N-Channel POWER MOSFET is ON, if the voltage between the drain and source exceeds the reference voltage which is internally set within the IC, the OCP will be activated. This protection is a self-return (foldback) type. However, this protection circuit is only effective in preventing destruction from sudden accident. It does not support the continuous operation of the protection circuit (e.g. when a load is connected, which significantly exceeds the output current capability).

- OVP_FB (Over Voltage Protection)
  Output over voltage protection circuit. When the output becomes than 120 % (Typ) of the target voltage, both of the output MOSFETs are turned off and the regulator operation is stopped. When the output voltage comes down to 110 % (Typ) of the target voltage, it returns to normal operation.

- UVLO (Under Voltage Lock-Out)
  UVLO is a protection circuit that prevents low voltage malfunction, especially during power up. It monitors the V_{IN} power supply voltage. If V_{IN} is less than the falling threshold voltage, 11 V (Max), the regulator is disabled. When the input voltage becomes higher than the rising threshold, the regulator restarts the operation with soft-start.

- DRIVER
  This circuit drives the gate of the N-Channel POWER MOSFETs.

- OVP_VCC
  Input over voltage protection circuit. When input voltage becomes higher than 65 V (Min), the regulator is disabled. When the input voltage becomes lower than the falling threshold, the regulator restarts the operation with soft-start. This hysteresis is typically 5 V.

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Absolute Maximum Ratings (Ta = 25°C)

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{IN}	-0.3 to +80	V
EN Input Voltage	$V_{EN/SYNC}$	-0.3 to V_{IN}	V
SW Input Voltage	V_{SW}	-1.0 to V_{IN}	V
BST Input Voltage	V_{BST}	-0.3 to V_{SW}+7	V
Voltage from SW to BST	$V_{BST\text{-}SW}$	-0.3 to +7	V
FB Input Voltage	V_{FB}	-0.3 to +7	V
REG Input Voltage	V_{REG}	-0.3 to +7	V
Storage Temperature Range	T_{stg}	-55 to +150	˚C
Maximum Junction Temperature	T_{jmax}	150	˚C

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Thermal Resistance *(Note 1)*

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s*(Note 3)*	2s2p*(Note 4)*	
VQFN24SV4040				
Junction to Ambient	θ_{JA}	150.6	37.9	°C/W
Junction to Top Characterization Parameter*(Note 2)*	Ψ_{JT}	20	9	°C/W

*(Note 1)*Based on JESD51-2A (Still-Air)

*(Note 2)*The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.

*(Note 3)*Using a PCB board based on JESD51-3.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3mm x 76.2mm x 1.57mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70μm

*(Note 4)*Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size	Thermal Via*(NOTE 5)*	
			Pitch	Diameter
4 Layers	FR-4	114.3mm x 76.2mm x 1.6mmt	1.20mm	Φ0.30mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70μm	74.2mm^2 (Square)	35μm	74.2mm^2(Square)	70μm

(Note 5) This thermal via connects with the copper pattern of all layers.

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Recommended Operating Conditions (Ta= -40 °C to +125 °C)

Parameter	Symbol	Min	Typ	Max	Unit
Operating Power Supply Voltage	V_{IN}	12	-	65	V
Operating Temperature Range	T_{opr}	-40	-	125	˚C
Output Voltage	V_{OUT}	0.8	-	5	V
SW minimum ON time	T_{ONMIN}	-	20	-	ns
Output Current (Note 1)	I_{OUT}	0	-	1	A

(Note 1) Overcurrent protection SW current should not be exceeded.

Electrical Characteristics (Unless otherwise specified Ta = -40 ˚C to +125 ˚C, V_{IN} = 48 V, $V_{EN/SYNC}$ = 5 V)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Shutdown Circuit Current	I_{SDN}	-	0	5	µA	$V_{EN/SYNC}$ = 0 V, Ta = 25 ˚C
Circuit Current	I_{CC}	-	3.5	TBD	mA	V_{FB} = 2.0 V
Reference Voltage	V_{FB}	0.784	0.800	0.816	V	V_{FB} = V_{COMP}
FB pin Input Current	I_{FB}	-	0	1	µA	V_{FB} = 2.0 V
COMP pin Sink Current	I_{CPSINK}	-	50	-	µA	V_{COMP} = 1.2 V, V_{FB} = 2 V
COMP pin Source Current	$I_{CPSOURCE}$	-	-50	-	µA	V_{COMP} = 1.2 V, V_{FB} = 0 V
Soft Start Time	T_{SS}	-	1.1	-	ms	f_{SW} = 2.1 MHz
POWER MOS Over ON Resistance	R_{ONH}	-	450	900	mΩ	I_O = 50 mA
POWER MOS Under ON Resistance	R_{ONH}	-	300	600	mΩ	I_O = 50 mA
Output Leak Current	I_{OLEAKH}	-	0	5	µA	V_{IN} = 80 V, $V_{EN/SYNC}$ = 0 V Ta = 25 ˚C, V_{SW} = 0 V
Operating Output Switch Current Of Overcurrent Protection	I_{SW}	TBD	TBD	TBD	A	
Oscillating Frequency	f_{SW}	1.9	2.1	2.3	MHz	
EN Threshold Voltage H	V_{ENH}	2.5	-	V_{IN}	V	
EN Threshold Voltage L	V_{ENL}	0	-	0.8	V	
EN pin Input Current	I_{EN}	-	25	50	µA	$V_{EN/SYNC}$ = 3 V
VIN Under Voltage Protection Detection Voltage	V_{UV_ON}	-	-	11.0	V	
VIN Under Voltage Protection Return Voltage	V_{UV_OFF}	-	-	12.0	V	
VIN Over Voltage Protection Detection Voltage	V_{OV_ON}	65	-	-	V	
VIN Over Voltage Protection Return Voltage	V_{OV_OFF}	60	-	-	V	

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Operational Notes

1. **Reverse Connection of Power Supply**
Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.
Except for pins the output and the input of which were designed to go below ground, ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the maximum junction temperature rating.

6. **Recommended Operating Conditions**
These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11. **Unused Input Pins**
Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

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12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

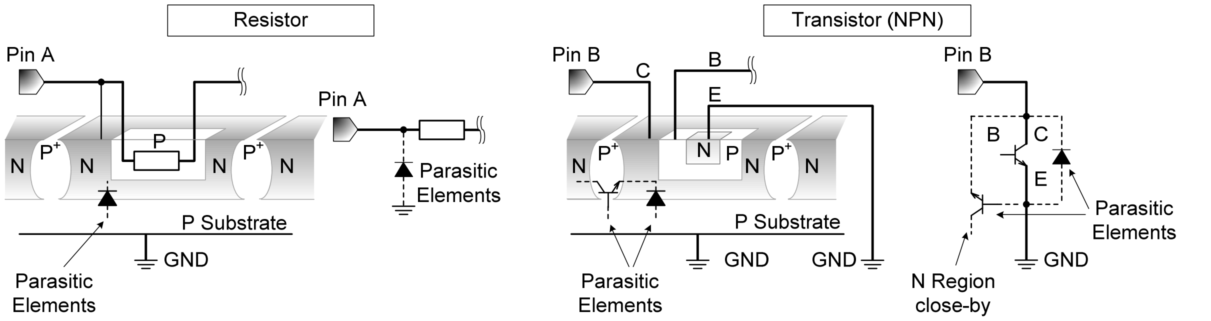

Figure 1. Example of monolithic IC structure

13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

14. Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and the maximum junction temperature rating are all within the Area of Safe Operation (ASO).

15. Thermal Shutdown Circuit(TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

16. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

17. Disturbance light

In a device where a portion of silicon is exposed to light such as in a WL-CSP, IC characteristics may be affected due to photoelectric effect. For this reason, it is recommended to come up with countermeasures that will prevent the chip from being exposed to light.

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(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
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   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

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7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

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1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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