CML Microcircuits

COMMUNICATION SEMICONDUCTORS

CMX148

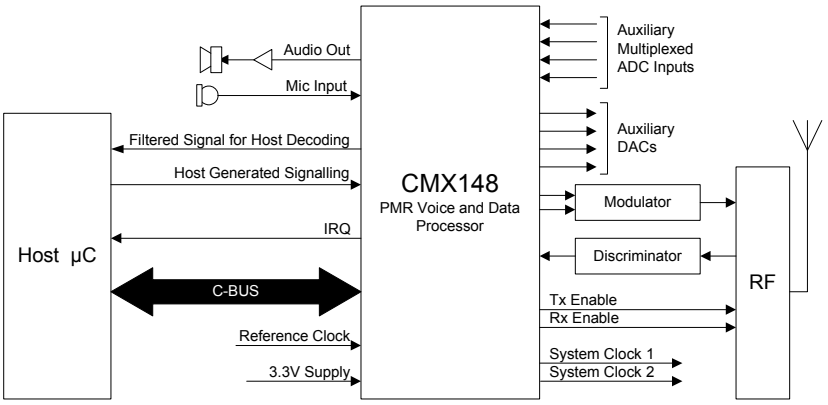
PMR Audio and Data Processor

D/148/6 November 2010

Audio Processing, DTMF and FFSK/MSK Data Modem with Auxiliary Functions for use in Analogue PMR Systems

Features

- Concurrent Audio/Signalling/Data Operations
- Complete Audio-band Processing:
  - Selectable Audio Processing Order
  - Pre and De-emphasis
  - Selectable 2.55/3.0 kHz Filtering
  - Selectable Audio HPF Cut-off
  - Compandor
  - Limiter
- Programmable Voice Scrambler
- MSK/FFSK Data Modem with Packet or Free-format Modes with FEC, CRC, Interleaving and Scrambling
- DTMF and Audio Tone Encoder/Decoder
- Routing to Support Host µController Signalling
- Sub-Audio Signalling Filters for CTCSS and DCS
- Dual Auxiliary ADC, 4 Multiplexed Inputs
- 4 x Auxiliary DACs
- Dual Programmable System Clock Outputs
- Tx Outputs for Single, Two-Point or I/Q Modulation
- Microphone and Discriminator Analogue Inputs
- Digital Gain Adjustment
- Default 3.6864MHz Xtal/Clock
- C-BUS Serial Interface to Host µController
- Flexible Powersave Modes
- Low-power 3.3V Operation
- Small VQFN and LQFP Packages



1. Brief Description

The CMX148 is a half-duplex, audio, signalling and data processing IC for use in PMR systems that utilise the host µC to perform signalling, including CTCSS/DCS encoding/decoding. The device is intended for use in general leisure and professional PMR terminals.

Comprehensive audio processing facilities include complete audio processing, filtering, companding, pre- or de-emphasis and frequency inversion scrambling. The CMX148 features an FFSK/MSK data modem for packetised or free-format data operations. Signal routing and filtering is included to assist host µC based signal encoding/decoding applications.

A DTMF encoder/decoder, a full complement of auxiliary ADCs and DACs and dual synthesised clock outputs are included in this low power PMR processor. The device also has flexible powersaving modes and is available in 48-pin VQFN and LQFP packages.

CONTENTS

Table Page

Figure Page

It is always recommended that you check for the latest product datasheet version from the CML website: [www.cmlmicro.com].

1.1. History

Version	Changes	Date
	•	
6	• Removal of spurious notes 32 and 33, section 9.1.3 • Enhanced description of C-BUS latency time, just before Fig 4. • Correction to Audio Tone ($CD) register, code 1100_b, section 8.1.29. • Correction to Program Block 4, registers P4.7, P4.10, P4.11, section 8.2.5.	25 Nov 10
5	• First documentation release	09 Jul 09
2-4	• Internal documentation updates	11 Mar 09
1	• Initial document created – based on 7031/7041FI-1.3 documentation	02 Jul 08

2. Block Diagram

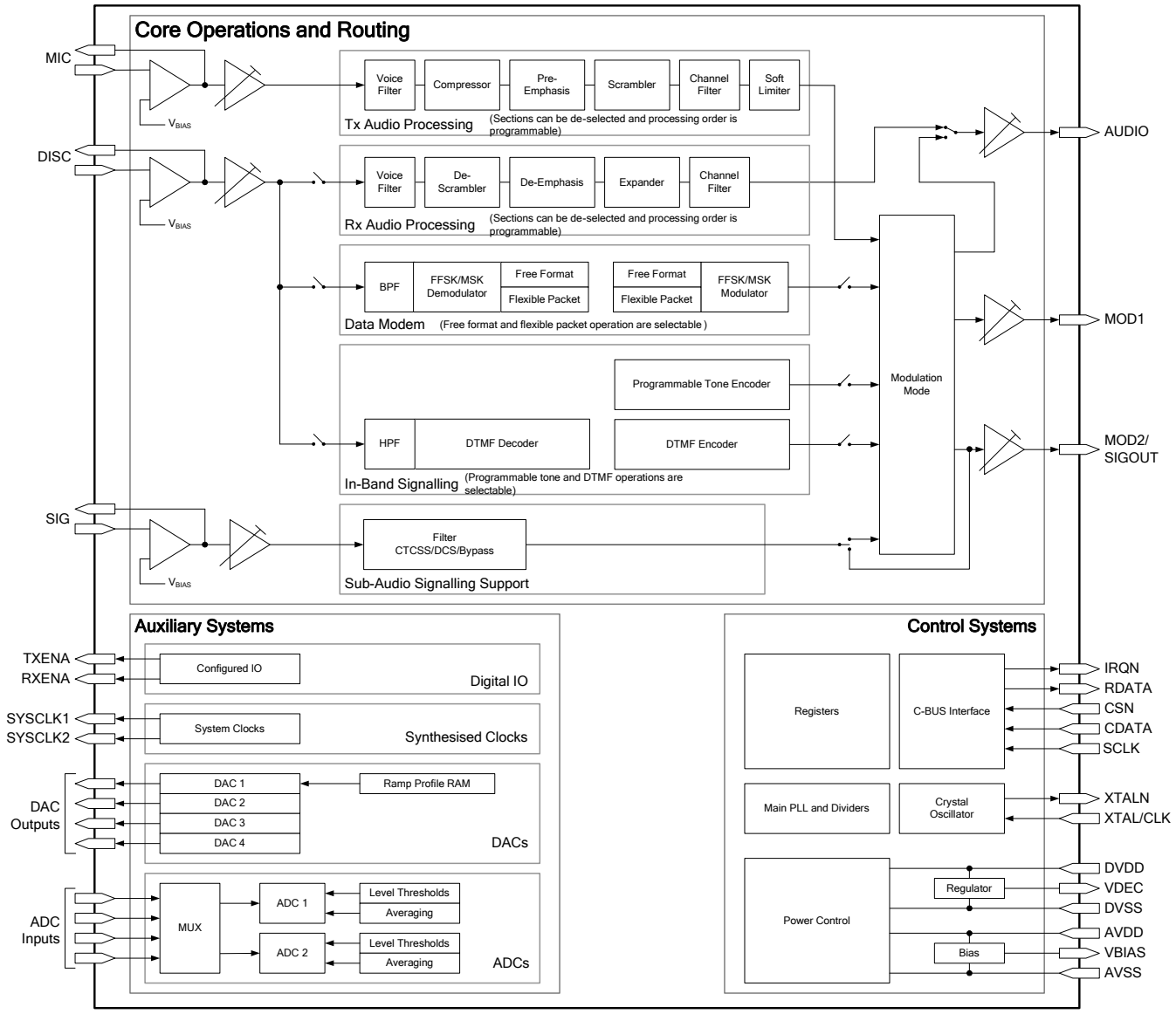


Figure 1 Block Diagram

3. Signal List

48-pin Q3/L4	Signal Name	Type	CMX148 Description
1	DVSS	PWR	Digital Ground
2	VDEC	PWR	Internally generated 2.5V supply voltage. Must be decoupled to DV_{SS} by capacitors mounted close to the device pins. No other connections allowed., except for the optional connection to RFV_{DD}.
3	XTAL/CLK	IP	Input to the oscillator inverter from the Xtal circuit or external clock source
4	XTALN	OP	The output of the on-chip Xtal oscillator inverter
5	DVDD	PWR	The 3.3V positive supply rail for the digital on-chip circuits. This pin should be decoupled to DVss by capacitors mounted close to the device pins.
6	CDATA	IP	C-BUS 'Command Data': Serial data input from the µC
7	RDATA	TS OP	C-BUS 'Reply Data': A 3-state C-BUS serial data output to the µC. This output is high impedance when not sending data to the µC
8	-	NC	Reserved – do not connect this pin
9	DVSS	PWR	Digital Ground
10	SCLK	IP	C-BUS 'Serial Clock' input from the µC
11	SYSCLK2	OP	Synthesised Digital System Clock Output 2
12	CSN	IP	C-BUS: The C-BUS chip select input from the µC - there is no internal pull-up on this input
13	-	NC	Reserved – leave unconnected
14	-	NC	Reserved – leave unconnected
15	-	NC	Reserved – leave unconnected
16	-	NC	Reserved – leave unconnected
17	-	NC	Reserved – leave unconnected
18	-	NC	Reserved – leave unconnected
19	DVSS	PWR	Digital Ground
20	IRQN	OP	C-BUS: A 'wire-ORable' output for connection to the Interrupt Request input of the host. Pulled down to DV_{SS} when active and is high impedance when inactive. An external pull-up resistor (R1) is required.
21	VDEC	PWR	Internally generated 2.5V digital supply voltage. Must be decoupled to DV_{SS} by capacitors mounted close to the device pins. No other connections allowed, except for optional connection to RFV_{DD}.
22	RXENA	OP	Rx Enable – active low when in Rx mode ($C1:b0 = 1)
23	-	NC	Reserved – leave unconnected
24	-	NC	Reserved – leave unconnected
25	SYSCLK1	OP	Synthesised Digital System Clock Output 1

48-pin Q3/L4	Signal Name	Type	CMX148 Description	
26	DVSS	PWR	Digital Ground	
27	TXENA	OP	Tx Enable – active low when in Tx mode ($C1:b1 = 1)	
28	DISC	IP	Discriminator amplifier inverting input	
29	DISCFB	OP	Discriminator amplifier feedback	
30	SIG	IP	Signal input amplifier inverting input	
31	SIGFB	OP	Signal input amplifier feedback	
32	MICFB	OP	Microphone amplifier feedback	
33	MIC	IP	Microphone amplifier inverting input	
34	AVSS	PWR	Analogue Ground	
35	MOD1	OP	Modulator 1 output	
36	MOD2/SIGOUT	OP	Modulator 2 output (Tx) or External Sub-Audio output (Rx)	
37	VBIAS	OP	Internally generated bias voltage of about $AV_{DD}/2$, except when the device is in 'Powersave' mode when V_{BIAS} will discharge to AV_{SS}. Must be decoupled to AV_{SS} by a capacitor mounted close to the device pins. No other connections allowed.	
38	AUDIO	OP	Audio output	
39	ADC1	IP	Auxiliary ADC input (1)	Each of the two ADC blocks can select its input signal from any one of these input pins, or from the MIC, SIG or DISC input pins. See section 8.1.5 for details.
40	ADC2	IP	Auxiliary ADC input (2)	
41	ADC3	IP	Auxiliary ADC input (3)	
42	ADC4	IP	Auxiliary ADC input (4)	
43	AVDD	PWR	Positive 3.3V supply rail for the analogue on-chip circuits. Levels and thresholds within the device are proportional to this voltage. This pin should be decoupled to AV_{SS} by capacitors mounted close to the device pins.	
44	DAC1	OP	Auxiliary DAC output 1/RAMDAC	
45	DAC2	OP	Auxiliary DAC output 2	
46	AVSS	PWR	Analogue Ground	
47	DAC3	OP	Auxiliary DAC output 3	
48	DAC4	OP	Auxiliary DAC output 4	
EXPOSED METAL PAD	SUBSTRATE	~	On this device, the central metal pad (which is exposed on Q3 packages only) may be electrically unconnected or, alternatively, may be connected to Analogue Ground (AVss). **No other electrical connections are permitted.**	

Notes:
IP = Input (+ PU/PD = internal pull-up/pull-down resistor)
OP = Output
BI = Bidirectional
TS OP = 3-state Output
PWR = Power Connection
NC = No Connection - should NOT be connected to any signal

4. External Components

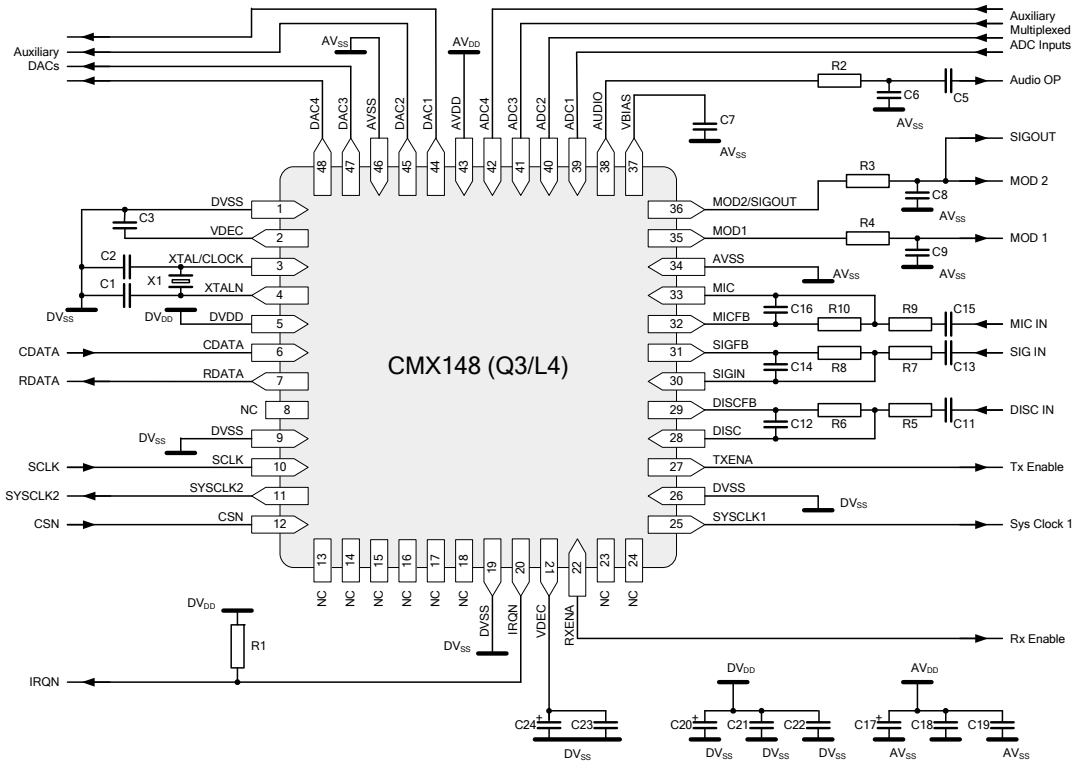


Figure 2 Recommended External Components

R1	100kΩ	C1	18pF	C11	See note 5	C21	10nF
R2	100kΩ	C2	18pF	C12	180pF	C22	10nF
R3	100kΩ	C3	10nF	C13	See note 5	C23	10nF
R4	100kΩ	C4	*not used*	C14	180pF	C24	10µF
R5	See note 2	C5	1nF	C15	See note 5		
R6	100kΩ	C6	100pF	C16	180pF		
R7	See note 3	C7	100nF	C17	10µF		
R8	100kΩ	C8	100pF	C18	10nF	X1	3.6864MHz
R9	See note 4	C9	100pF	C19	10nF		See note 1
R10	100kΩ	C10	*not used*	C20	10µF		

Resistors ±5%, capacitors and inductors ±20% unless otherwise stated.

Notes:

1. X1 can be a crystal or an external clock generator; this will depend on the application. The tracks between the crystal and the device pins should be as short as possible to achieve maximum stability and best start up performance. By default, a 3.6864MHz clock is selected, other values could be used if the various internal clock dividers are set to appropriate values.

2. R5 should be selected to provide the desired dc gain (assuming C11 is not present) of the DISC input, as follows:

$$|GAIN_{DISC}| = 100k\Omega / R5$$

The gain should be such that the resultant output at the DISCFB pin is within the input signal range specified in 7.14.2.

3. R7 should be selected to provide the desired dc gain (assuming C13 is not present) of the SIG input as follows:

$$|GAIN_{SIG}| = 100k\Omega / R7$$

The gain should be such that the resultant output at the SIGFB pin is within the input signal range specified in 7.14.

4. R9 should be selected to provide the desired dc gain (assuming C15 is not present) of the MIC input as follows:

$$|GAIN_{MIC}| = 100k\Omega / R9$$

The gain should be such that the resultant output at the MICFB pin is within the input signal range specified in 7.14.1. For optimum performance with low signal microphones, an additional external gain stage may be required.

5. C11, C13 and C15 should be selected to maintain the lower frequency roll-off of the MIC, SIG and DISC inputs as follows:

$$C11 \geq 1.0\mu F \times |GAIN_{DISC}|$$
$$C13 \geq 1.0\mu F \times |GAIN_{SIG}|$$
$$C15 \geq 30nF \times |GAIN_{MIC}|$$

6. SIG and SIGFB connections allow the user to have an additional signal input (usually assigned to the External Signalling). Component connections and values are as for the respective DISC and MIC networks. If this input is not required, the SIG pin should be connected to AVss.

7. C5 (AUDIO output) should be increased to 1.0µF if frequencies below 300Hz need to be used on this pin.

8. A single 10µF electrolytic capacitor (C24, fitted as shown) may be used for smoothing the power supply to both VDEC pins, providing they are connected together on the pcb with an adequate width power supply trace. Alternatively, separate smoothing capacitors should be connected to each VDEC pin. High frequency decoupling capacitors (C3 and C23) must always be fitted as close as possible to both VDEC pins.

5. PCB Layout Guidelines and Power Supply Decoupling

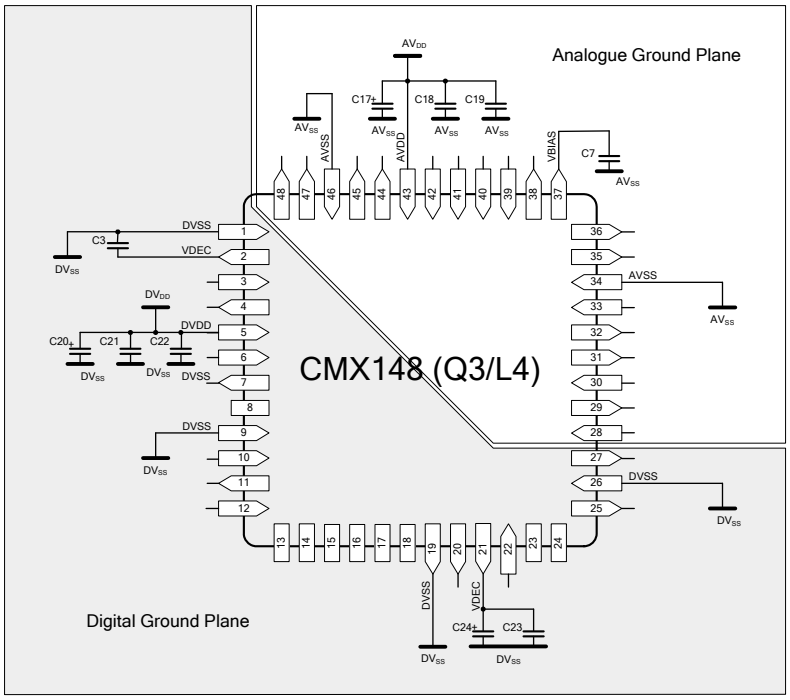


Figure 3 Power Supply and Decoupling

Component Values as per Figure 2.

Notes:

It is important to protect the analogue pins from extraneous inband noise and to minimise the impedance between the device and the supply and bias decoupling capacitors. The decoupling capacitors C3, C7, C18, C19, C21, C22, C24 and C25 should be as close as possible to the device. It is therefore recommended that the printed circuit board is laid out with separate ground planes for the AV_{SS} and DV_{SS} supplies in the area of the CMX148, with provision to make links between them, close to the device. Use of a multi-layer printed circuit board will facilitate the provision of ground planes on separate layers.

V_{BIAS} is used as an internal reference for detecting and generating the various analogue signals. It must be carefully decoupled, to ensure its integrity, so apart from the decoupling capacitor shown, no other loads should be connected. If V_{BIAS} needs to be used to set the discriminator mid-point reference, it must be buffered with a high input impedance buffer.

The single ended microphone input and audio output must be ac coupled (as shown), so that their return paths can be connected to AV_{SS} without introducing dc offsets. Further buffering of the audio output is advised.

The crystal X1 may be replaced with an external clock source.

6. General Description

The CMX148 is intended for use in half-duplex analogue two way mobile radio or family radio equipment and is particularly suited to both the PMR markets and enhanced MURS/GMRS/FRS with GPS terminal designs. The CMX148 provides radio signal filtering, encoder and decoder functions for: audio, inband tones, DTMF, and MSK/FFSK data, permitting simple to sophisticated levels of tone control and data transfer. A flexible power control facility allows the device to be placed in its optimum powersave mode when not actively processing signals.

The CMX148 includes a crystal clock generator, with a buffered output, to provide a common system clock if required. A block diagram of the CMX148 is shown in Figure 1.

The signal processing blocks can be individually assigned to either of two signal processing paths, which in turn, can be routed from any of the three audio/discriminator input pins. This allows for a very flexible routing architecture and allows the facility for different processing blocks to act on different analogue inputs.

Additional filtering is included to support host-generation or detection of sub-audible CTCSS/DCS tones.

Tx Functions:

- Single/dual microphone or external signalling inputs with input amplifier and programmable gain adjustment
- Filtering selectable for 12.5kHz and 25kHz channels
- Selectable pre-emphasis
- Selectable compression
- Selectable frequency inversion voice scrambling
- Selectable audio processing order
- 2-point modulation outputs with programmable level adjustment
- Filtering for external CTCSS or DCS signals
- Programmable audio tone generator (for custom audio tones)
- Programmable DTMF generator
- 1200/2400 baud MSK/FFSK modem and data packet encoder (suitable for text messaging/paging, caller identification, caller location, digital poll of remote radio location, GPS information in NMEA 0183 format, data transfer, MPT1327 etc.) incorporating interleaving, FEC, CRC and data scrambling
- Tx Enable output

Rx Functions:

- Single/dual demodulator inputs with input amplifier and programmable gain adjustment
- Audio-band and sub-audio rejection filtering
- Selectable de-emphasis
- Selectable expansion
- Selectable frequency inversion voice de-scrambling
- Selectable Audio Processing order
- Software volume control
- Filtering for external CTCSS or DCS signals
- DTMF decoder
- 1200/2400 baud MSK/FFSK data packet decoder with automatic bit rate recognition, 16-bit frame sync detection, error correction, data de-scrambler and packet disassembly
- Rx Enable output

Auxiliary Functions:

- 2 programmable system clock outputs
- 2 auxiliary ADCs with selectable input paths
- 4 auxiliary DACs, one with built-in programmable RAMDAC

Interface:

- C-BUS, 4-wire high-speed synchronous serial command/data bus
- Open drain IRQ to host

7. Detailed Descriptions

7.1. Device Identification Code

Following a Power-on or Reset (see 8.1.1), the device will report the Device Identification Code in the Tone Status register ($CC) to indicate that it is operational.

7.2. Xtal Frequency

The CMX148 is designed to work with a Xtal of 3.6864MHz. If this default configuration is not used, then Program Block 3 (see 8.2.4) should be loaded with the correct values to ensure that the device will work to specification with the user specified clock frequency. A table of common values can be found in Table 1. Note the maximum Xtal frequency is 12.288MHz, although an external clock source of up to 24.576MHz can be used.

The register values in Table 1 are shown in hex (however not all bits are relevant, see Program Block 3 for details), the default settings are shown in bold, and the settings which do not give an exact setting (but are within acceptable limits) are in italics. The new P3.2-3 settings take effect following the write to P3.3 (the settings in P3.4-7 are implemented on a change to Rx or Tx mode).

Table 1 Xtal/clock Frequency Settings for Program Block 3

Program Block entry			External Frequency Source (MHz)							
			3.6864	6.144	9.216	12.0	12.8	16.368	16.8	19.2
P3.2	Idle	GP Timer	**$01C**	$018	$018	$019	$019	*$018*	$019	$018
P3.3		VCO output and AUX clk divide	**$084**	$088	$08C	*$10F*	*$110*	*$095*	*$115*	$099
P3.4	Rx or Tx	Ref clk divide	**$030**	$040	$060	$07D	$0C8	$155	$15E	$0C8
P3.5		PLL clk divide	**$280**	$200	$200	$200	$300	$400	$400	$200
P3.6		VCO output and AUX clk divide	**$13C**	$140	$140	$140	$140	$140	$140	$140
P3.7		Internal ADC/DAC clk divide	**$008**	$008	$008	$008	$008	$008	$008	$008

7.3. Host Interface

A serial data interface (C-BUS) is used for command, status and data transfers between the CMX148 and the host µC; this interface is compatible with Microwire and SPI. Interrupt signals notify the host µC when a change in status has occurred and the µC should read the Status register across the C-BUS and respond accordingly. Interrupts only occur if the appropriate mask bit has been set. See section 8.1.3.

The CMX148 will monitor the state of the C-BUS registers that the host has written to every 250µs (the C-BUS latency period) hence it is not advisable for the host to make successive writes to the same C-BUS register within this period.

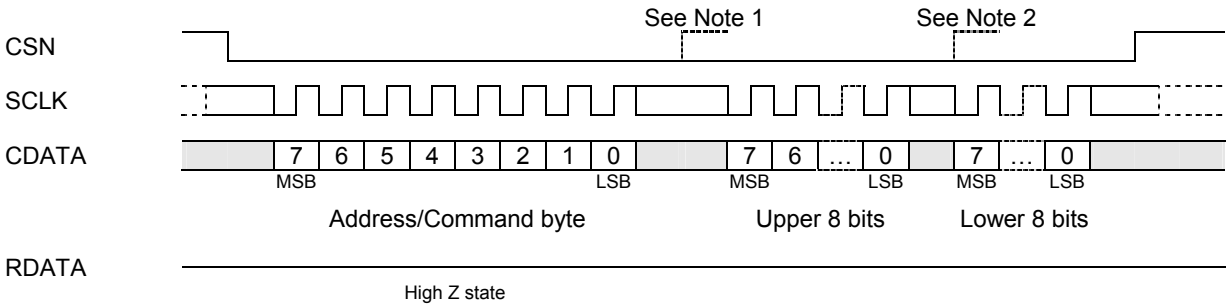
To minimise activity on the C-BUS interface, optimise response times and ensure reliable data transfers, it is advised that the IRQ facility be utilised (using the IRQ mask register, $CE). It is permissible for the host to poll the IRQ pin if the host µC does not support a fully interrupt-driven architecture. This removes the need to continually poll the C-BUS status register ($C6) for status changes.

The C-BUS block provides for the transfer of data and control or status information between the CMX148's internal registers and the host µC over the C-BUS serial interface. Each transaction consists of a single Address byte sent from the µC which may be followed by one or more Data byte(s) sent from the µC to be written into one of the CMX148's Write Only Registers, or one or more data byte(s) read out from one of the CMX148's Read Only Registers, as illustrated in Figure 4.

Data sent from the µC on the CDATA line is clocked into the CMX148 on the rising edge of the SCLK input. RDATA sent from the CMX148 to the µC is valid when SCLK is high. The CSN line must be held low during a data transfer and kept high between transfers. The C-BUS interface is compatible with most common µC serial interfaces and may also be easily implemented with general purpose µC I/O pins controlled by a simple software routine.

The number of data bytes following an Address byte is dependent on the value of the Address byte. The most significant bit of the address or data are sent first. For detailed timings see section 9.2. Note that, due to internal timing constraints, there may be a delay of up to 250µs between the end of a C-BUS write operation and the device reading the data from its internal register. Ensure that this C-BUS latency time (up to 250µs) is observed when writing multiple commands to the same C-BUS register.

C-BUS Write:



C-BUS Read:

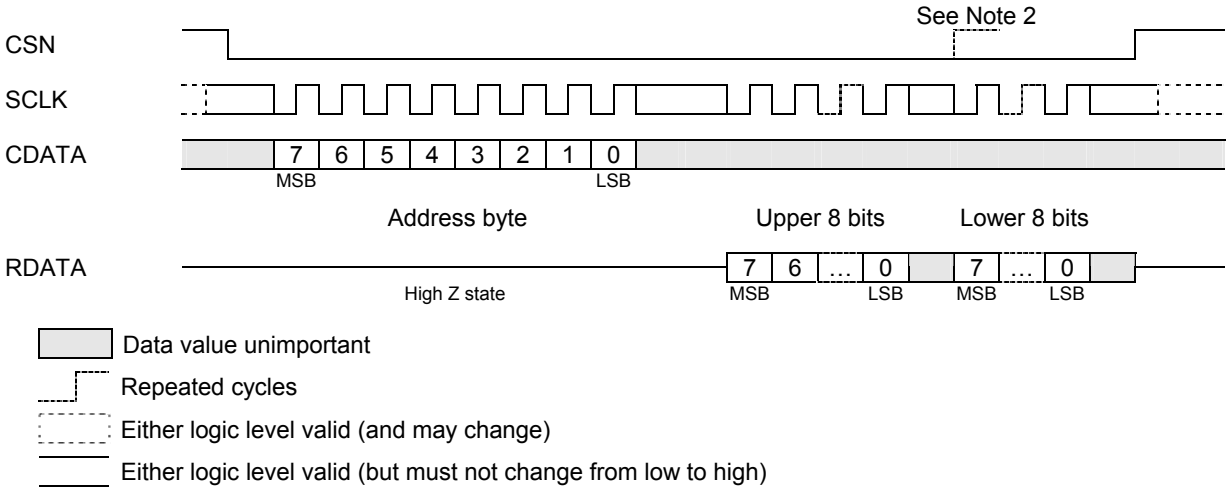


Figure 4 C-BUS Transactions

Notes:

1. For Command byte transfers only the first 8 bits are transferred ($01 = Reset).
2. For single byte data transfers only the first 8 bits of the data are transferred.
3. The CDATA and RDATA lines are never active at the same time. The Address byte determines the data direction for each C-BUS transfer.
4. The SCLK input can be high or low at the start and end of each C-BUS transaction.
5. The gaps shown between each byte on the CDATA and RDATA lines in the above diagram are optional, the host may insert gaps or concatenate the data as required.

7.4. Device Control

The CMX148 can be set into many modes to suit the environment in which it is to be used. These modes are described in the following sections and are programmed over the C-BUS: either directly to operational registers or, for parameters that are not likely to change during operation, via the Programming register ($C8).

For basic operation:

1. enable the relevant hardware sections via the Power Down Control register
2. set the appropriate mode registers to the desired state (Audio, Inband, Sub-audio, Data, etc.)
3. select the required Signal Routing and Gain
4. use the Mode Control register to place the device into Rx or Tx mode

To conserve power when the device is not actively processing an analogue signal, place the device into Idle mode. Additional powersaving can be achieved by disabling the unused hardware blocks, however, care must be taken not to disturb any sections that are automatically controlled.

See:
- Powerdown Control - $C0 write
- Mode Control – $C1 write

7.4.1. Signal Routing

The CMX148 offers a very flexible routing architecture, with three signal inputs, two separate signal processing paths and a selection of two modulator outputs (to suit 2-point as well as I/Q modulation schemes) and a single audio output. Each of the signalling processing blocks can be independently routed from either of the two input blocks (Input1 or Input2), which can be routed from any of the three input signal amplifiers. The audio/voice processing blocks are always routed from Input1. The outputs from signal processing blocks are determined by the settings of the AuxADC and TX MOD mode register in Tx mode.

In Tx mode, an externally generated sub-audio or in-band signal may be routed via Input2. The signal can be appropriately filtered and mixed with the in-band signalling and presented at the MOD1 and/or MOD2 outputs. In Rx mode, sub-audio signalling or in-band signalling can be recovered from the input signal, routed via Input1 or Input2, and presented on the MOD2 output..

See:
- Input Gain and Output Signal Routing - $B1 write
- AuxADC and Tx MOD Mode - $A7 write
- Mode Control – $C1 write

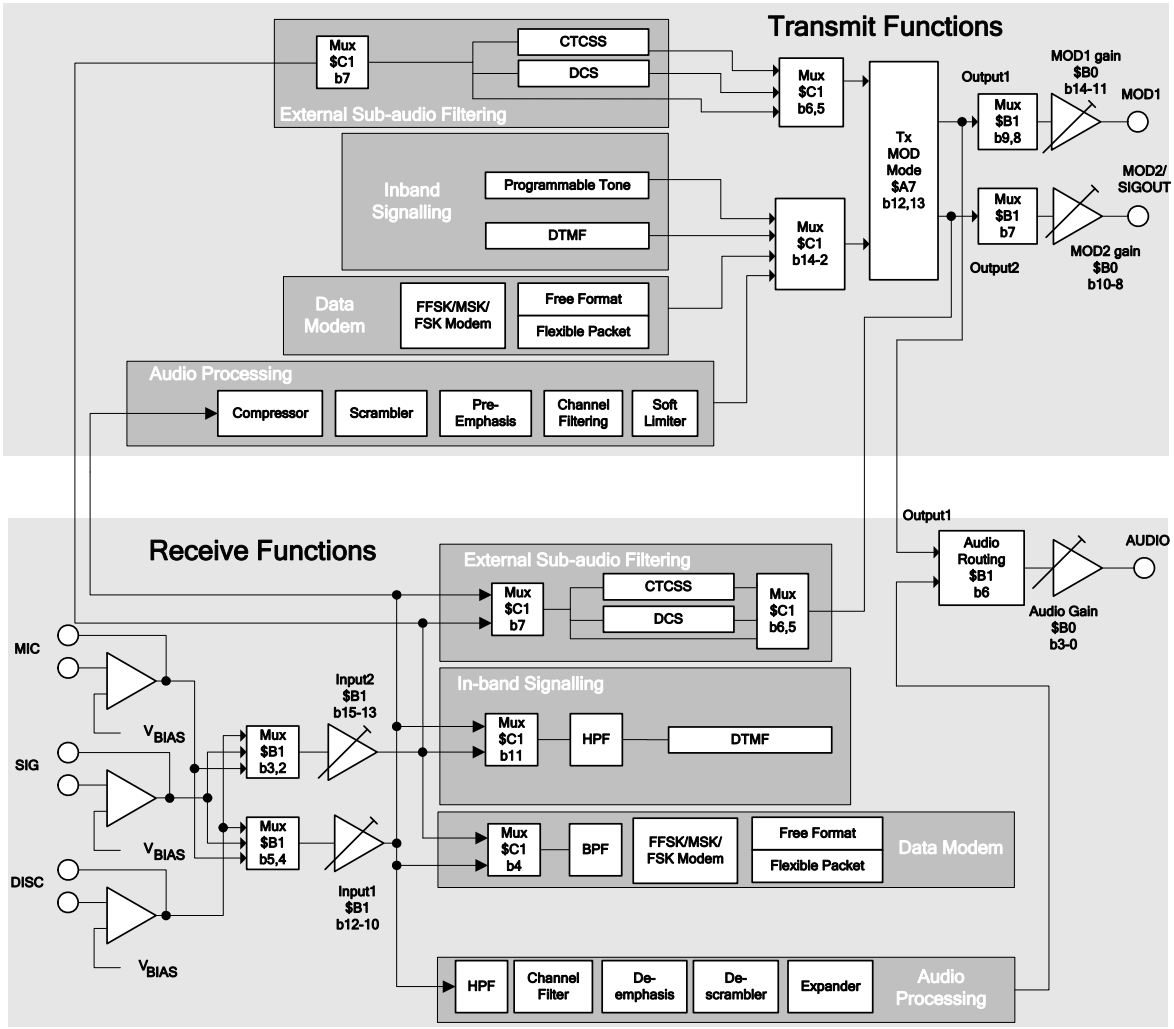


Figure 5 Signal Routing

The analogue gain/attenuation of each input and output can be set individually, with additional fine gain control available via the Programming register.

See:

- Analogue Output Gain - $B0 write
- Input Gain and Output Signal Routing - $B1 write

7.4.2. Mode Control

The CMX148 operates in one of three modes:

- IDLE
- Rx
- Tx

At power-on or following a Reset or General Reset, the device will automatically enter IDLE mode, which allows for the maximum powersaving whilst still retaining the capability of monitoring the four ADC inputs (if enabled). It is only possible to write to the Programming register whilst in IDLE mode.

See:

- Mode Control – $C1 write

7.5. Audio Functions

The audio signal can be processed in several ways, depending on the implementation required, by selecting the relevant bits in the Audio Control – $C2 write register. In both Rx and Tx modes, a selectable channel filter to suit either the 12.5kHz or 25kHz TIA/ETSI channel mask can be selected. This filter also incorporates a soft limiter to reduce the effects of over-modulation. Other features include 300Hz HPF, pre- and de-emphasis, companding and frequency inversion scrambling, all of which may be individually enabled[1]. The order in which these features are executed is selectable to ensure compatibility with existing implementations and provide optimal performance (see section 8.2.5). The alternate settings shown in section 8.2.5 may provide better performance than the default configuration

7.5.1. Audio Receive Mode

The CMX148 operates in half-duplex, so whilst in receive mode the transmit path (MIC input and MOD1/2 amplifiers) can be disabled and powered down if required. The AUDIO output signal level is equalised (to V_{BIAS}) before switching between the audio port and the modulator ports, to minimise unwanted audible transients. The Off/Powersave level at MOD1/2 outputs is the same as the V_{BIAS} pin, so the audio output level must also be at this level before switching.

See:

- Audio Control – $C2 write

Receiving Audio Band Signals

When a voice-based signal is being received, it is up to the host µC, in response to signal status information provided by the CMX148, to control muting/enabling of the audio signal to the AUDIO output.

The discriminator path through the device has a programmable gain stage. Whilst in receive mode this should normally be set to 0dB (the default) gain.

Receive Filtering

The incoming signal is filtered, as shown in Figure 7 (with the 300Hz HPF also active), to remove sub-audio components and to minimise high frequency noise. When appropriate, the audio signal can then be routed to the AUDIO output. Separate selectable filters are available for:

- 300Hz High Pass (to reject sub-audible signalling)
- 2.55kHz Low Pass (for 12.5kHz channel operation)
- 3.0kHz Low Pass (for 25kHz channel operation)

Note that with no filters selected, the low frequency response extends to below 5Hz at the low end but still rolls off above 3.3kHz at the top end.

The cut-off point of the 300Hz HPF can be set to either 280Hz, 300Hz or 320Hz by setting the relevant bits of Program Block P2.5, as shown in Figure 6.

[1] The typical responses shown in Figure 7, Figure 10, Figure 11 were recorded using the EV1480 Evkit, DISC to AUDIO and MOD1.

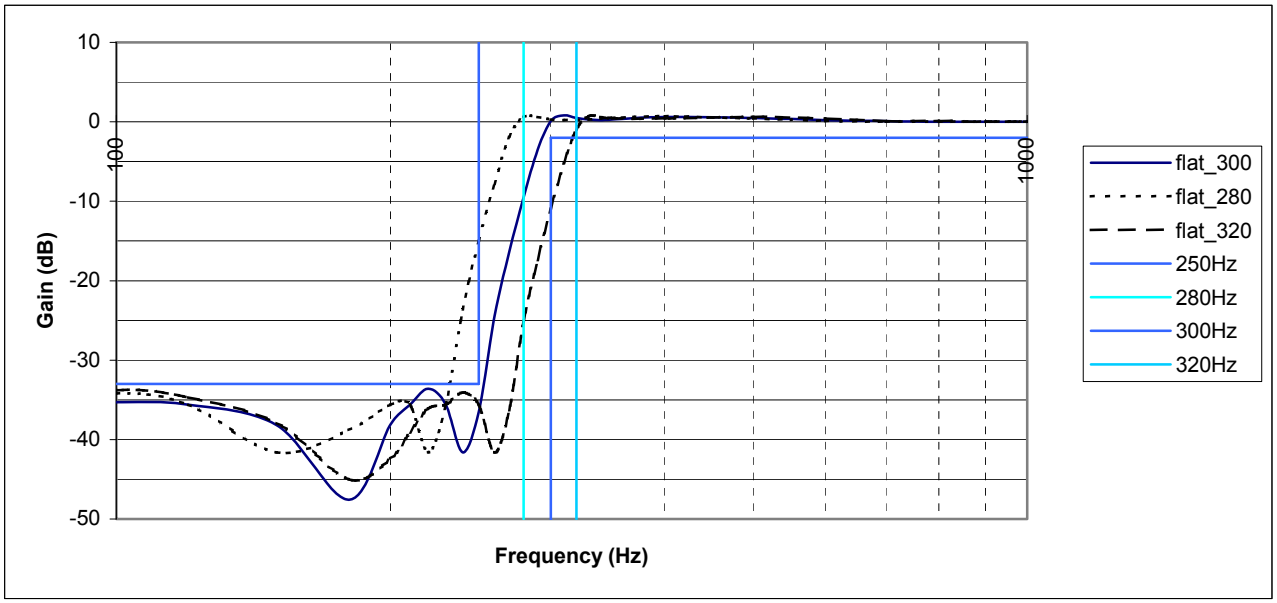


Figure 6 Adjustable HPF Response

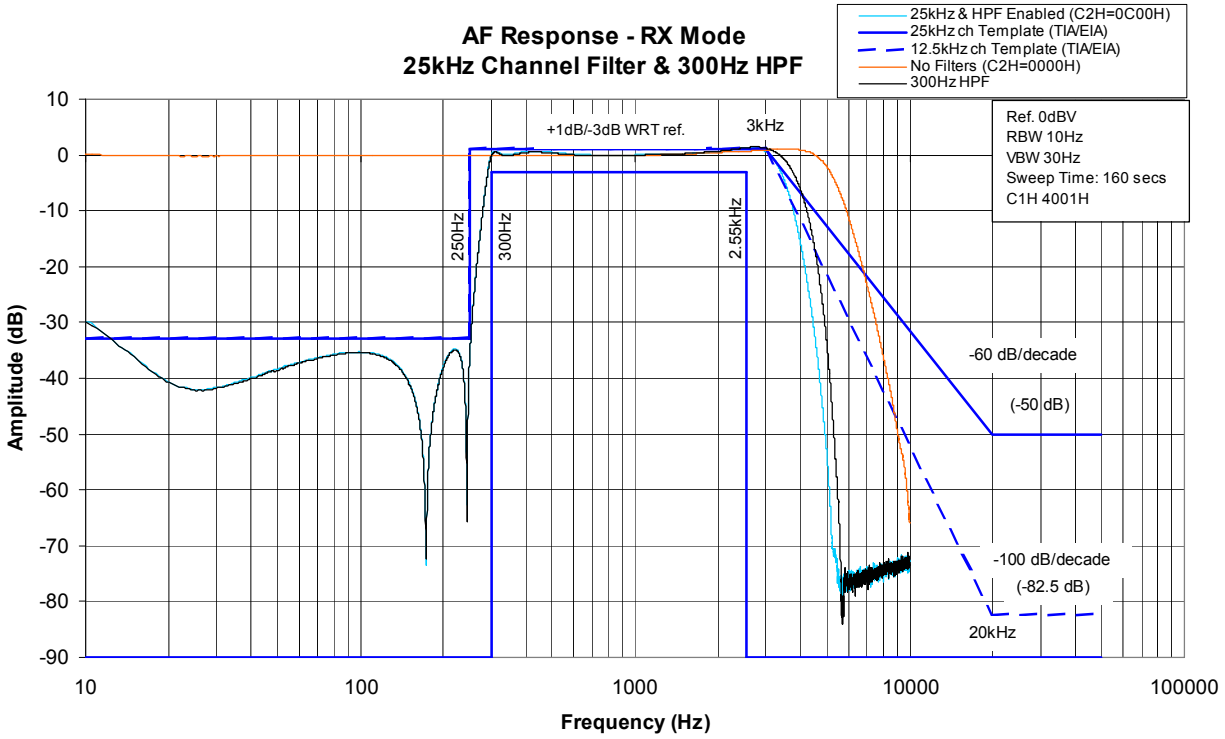


Figure 7 Rx 25kHz Channel Audio Filter Frequency Response

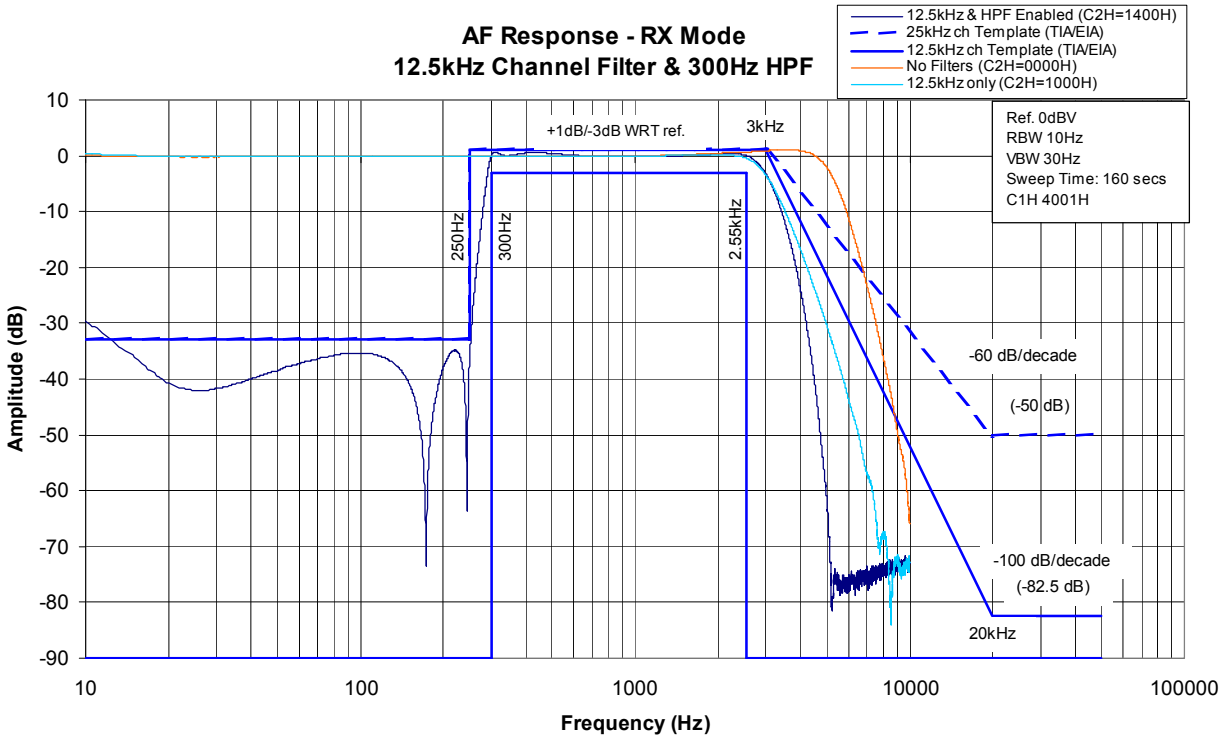


Figure 8 Rx 12.5kHz Channel Audio Filter Frequency Response

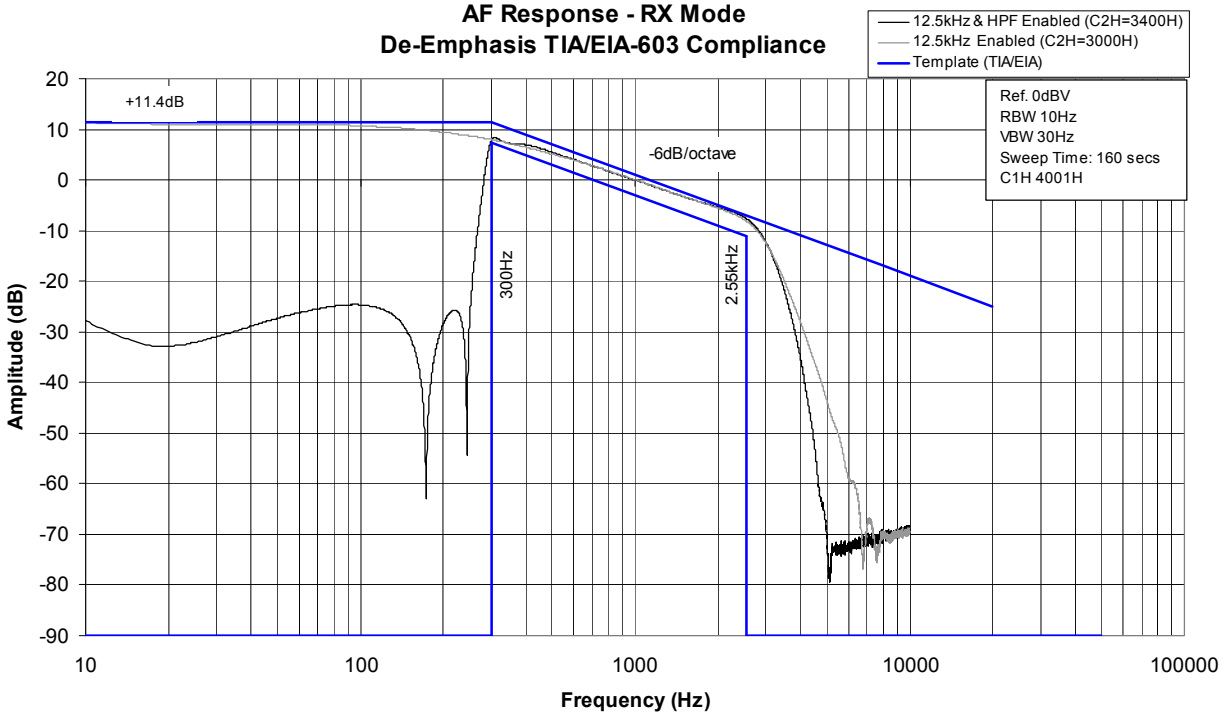


Figure 9 De-Emphasis 12.5kHz

De-emphasis
Optional de-emphasis at -6dB per octave from 300Hz to 3000Hz (shown in Figure 9) can be selected, to facilitate compliance with TIA/EIA-603, EN 300 086, EN 301 025 etc. The template shows the +1 and -3dB limits.

Rx Companding (Expanding)

The CMX148 incorporates an optional syllabic compandor in both transmit and receive modes. This expands received audio band signals that have been similarly compressed in the transmitter to enhance dynamic range. See the next section and:

- Audio Control – $C2 write

Audio De-scrambling
The CMX148 incorporates an optional frequency inversion de-scrambler in receive mode. This de-scrambles received audio band signals that have been scrambled in the transmitter. The inversion frequency defaults to 3300Hz, but maybe modified by writing to P4.8.

See:
- Audio Control – $C2 write

7.5.2. Audio Transmit Mode
The device operates in half-duplex, so when the device is in transmit mode the receive path (discriminator and audio output amplifiers) should be disabled, and can be powered down, by the host µC.

Two modulator outputs with independently programmable gains are provided to facilitate single or two-point modulation, separate sub-audio and audio band outputs. If one of the modulator outputs is not used it can be disabled to conserve power.

To avoid spurious transmissions when changing from Rx to Tx, the MOD1 and MOD2 outputs are ramped to the quiescent modulator output level, V_{BIAS} before switching (if enabled by b7 of the Analogue Gain register, $B0). Similarly, when starting a transmission, the transmitted signal is ramped up from the quiescent V_{BIAS} level and when ending a transmission the transmitted signal is ramped down to the quiescent V_{BIAS} level. The ramp rates are set in the Program Block P4.6. When the modulator outputs are disabled, their outputs will be set to V_{BIAS}. When the modulator output drivers are powered down, their outputs will be floating (high impedance), so the RF modulator will need to be turned off.

For all transmissions, the host µC must only enable signals after the appropriate data and settings for those signals are loaded into the C-BUS registers. As soon as any signalling is enabled the CMX148 will use the settings to control the way information is transmitted.

A programmable gain stage in the microphone input path facilitates a host controlled VOGAD capability, or an internal AGC function may be used.

See:
- Audio Control – $C2 write
- AuxADC and Tx MOD Mode - $A7 write
- Input Gain and Output Signal Routing - $B1 write

Processing Audio Signals for Transmission over Analogue Channels
The microphone input(s), with programmable gain, can be selected as the audio input source. Pre-emphasis is selectable with either of the two analogue Tx audio filters (for 12.5kHz and 25kHz channel spacing). These are designed for use in EN 300 086, TIA/EIA-603 or EN 301 025 compliant applications. When the 300Hz HPF is enabled, it will attenuate sub-audio frequencies below 250Hz by more than 33dB with respect to the signal level at 1kHz.

These filters, together with a built in limiter, help ensure compliance with EN 300 086 and EN 301 025 (25kHz and 12.5kHz channel spacing) when levels and gain settings are set up correctly in the target system.

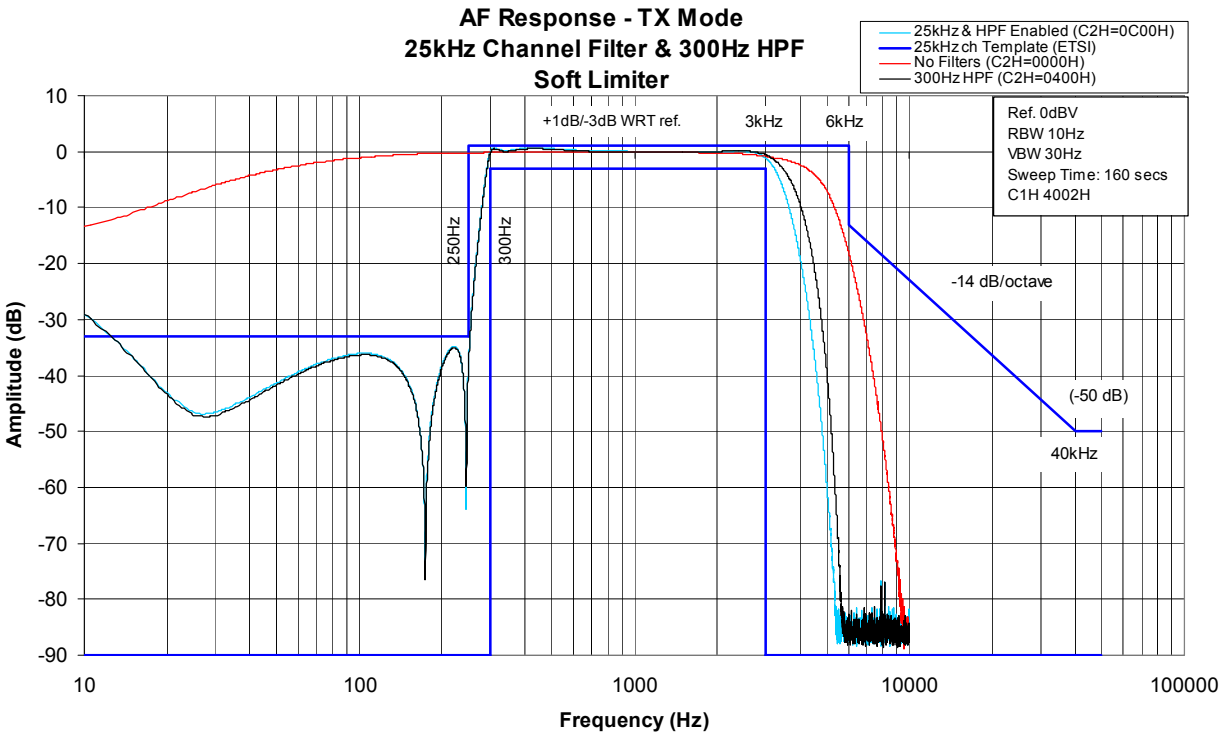


Figure 10 Tx Channel Audio Filter Response and Template (ETSI)

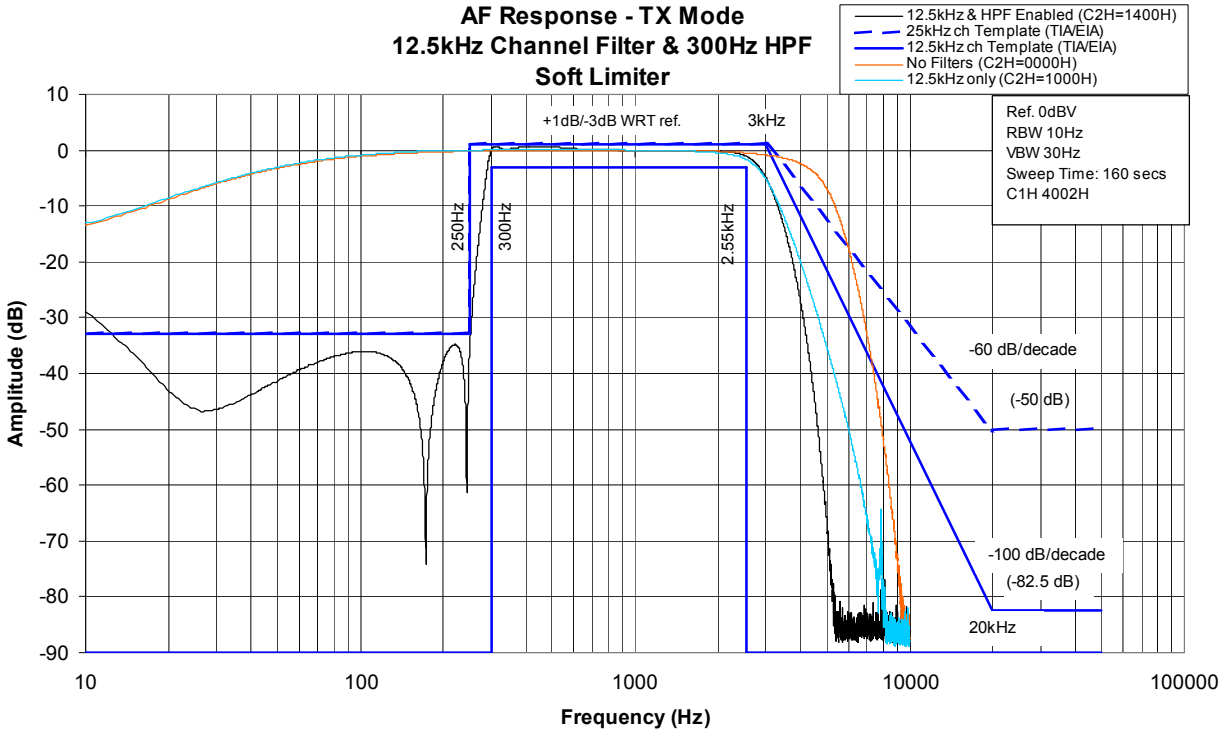


Figure 11 Tx Channel Audio Filter Response and Template (TIA)

The characteristics of the 12.5kHz channel filter fit the template shown in Figure 10 and Figure 11. This filter also facilitates implementation of systems compliant with TIA/EIA-603 ‘A’ , ‘B’ and ‘C’ bands .

The CMX148 provides selectable pre-emphasis filtering of +6dB per octave from 300Hz to 3000Hz, matching the template shown

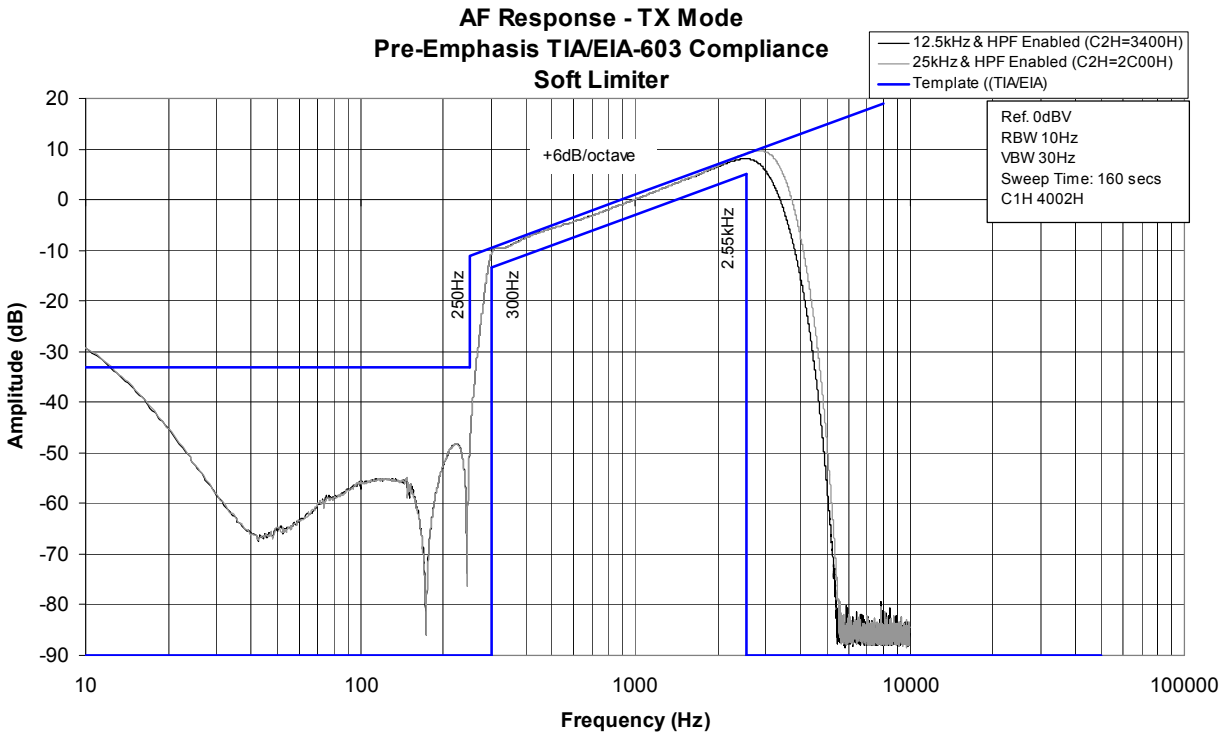


Figure 12 Audio Frequency Pre-emphasis

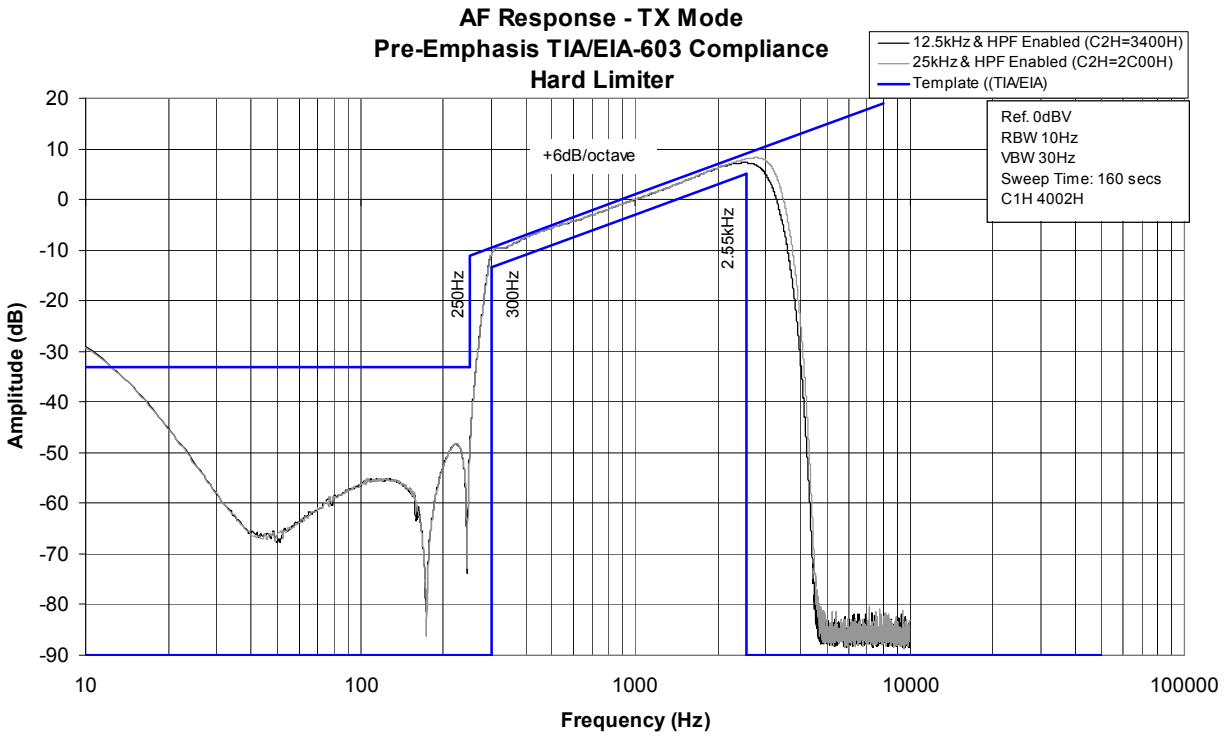


Figure 13 Audio Frequency Pre-emphasis

Modulator Output Routing

The sub-audio component can be combined with the audio band signal and this composite signal routed to both MOD1 and MOD2 outputs, or the sub-audio and audio band signal can be output separately (sub-audio to MOD2 and audio band to MOD1), in accordance with the settings of:

- AuxADC and Tx MOD Mode - $A7 write
- Input Gain and Output Signal Routing - $B1 write

Alternatively, the combined sub-audio and audio band composite signal can be output on MOD1 and MOD2 in a phase/quadrature (I/Q) format suitable for direct upconversion to the final RF signal.
Due to the nature of the I/Q modulation, this mode is only feasible in RF channels/systems which have a maximum frequency deviation of 3kHz or less. Additional test modes are provided for calibrating external circuits. Tx I/Q mode is particularly suitable for data transmission.

InputAGC

An Automatic Gain Control system can be enabled by setting the relevant bits of the Program Block P4.9. The setting of the Input1 Gain stage is recorded when the device enters Tx mode and if the signal exceeds the pre-set threshold, the Input1 Gain is automatically reduced in 3.2dB steps until it falls within the operational levels or the range of the gain stage is exhausted. When the signal level drops, the gain will be automatically increased in 3.2dB steps at the rate set in P4.9 until the initial values has been reached. For maximum effect the system should be designed such that the +22.4dB setting of the Input1 Gain stage achieves the nominal levels. To ensure consistent operation, it is recommended that the Input1 Gain stage value be re-initialised before entering Tx mode. The signal that is used as an input to this process can be selected to be either the:

- Output of Input1 Gain Stage
- Output of the Pre-emphasis Filter

by selecting the relevant bit in P4.9. The Pre-emphasis option should only be chosen if this block is actually in use.

- Input Gain and Output Signal Routing - $B1 write
- Program Block 4 – Gain and Offset Setup

Tx Companding (Compressing)
The CMX148 incorporates an optional syllabic compandor in both transmit and receive mode. This compresses audio band signals before transmission to enhance dynamic range. See section 7.5.1 and:

- Audio Control – $C2 write

Audio Scrambling
The CMX148 incorporates an optional frequency inversion scrambler in transmit mode. This scrambles audio band signals, to be de-scrambled in the receiver. The inversion frequency defaults to 3300Hz, but may be modified by writing to P4.8.

See:
- Audio Control – $C2 write

Audio Compandor
The compandor is comprised of a compressor and an expandor. The compressor's function is to reduce the dynamic range of a given signal by attenuating larger amplitudes while amplifying smaller amplitudes. The expandor's function is to expand the dynamic range of a given signal by attenuating small amplitude signals (e.g. noise) while amplifying large amplitude signals. The compressor is used prior to transmission and the expandor is used in the receiver. Hence, using a compandor will enhance performance in a communication system by transmitting a compressed signal, which is less likely to be corrupted by noise, and then at the receiver expanding the compressed signal, which will push the noise picked up during transmission down further.

The CMX148 uses a "syllabic compandor." This type of compandor, as opposed to the instantaneous compandor (e.g. μ/A-law PCM), responds to changes in the average envelope of the signal amplitude according to a syllabic time constant τ. Typically the steady state output for the compressor is proportional to the square root of the input signal. Ie:, for a 2 dB change in input signal, the output change will be 1 dB. Generally for voice communication systems a compressor is expected to have an input dynamic range of 60 dB, providing an output dynamic range of 30 dB. The expandor does the inverse.

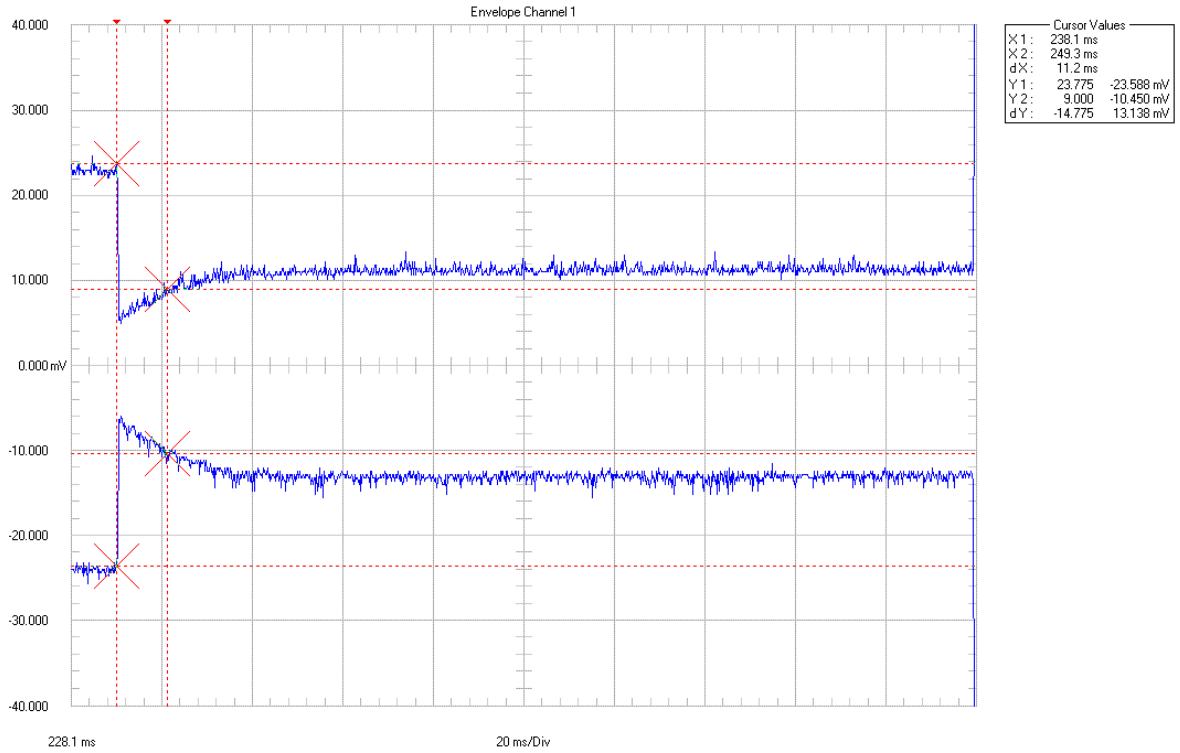


Figure 14 Expandor Transient Response

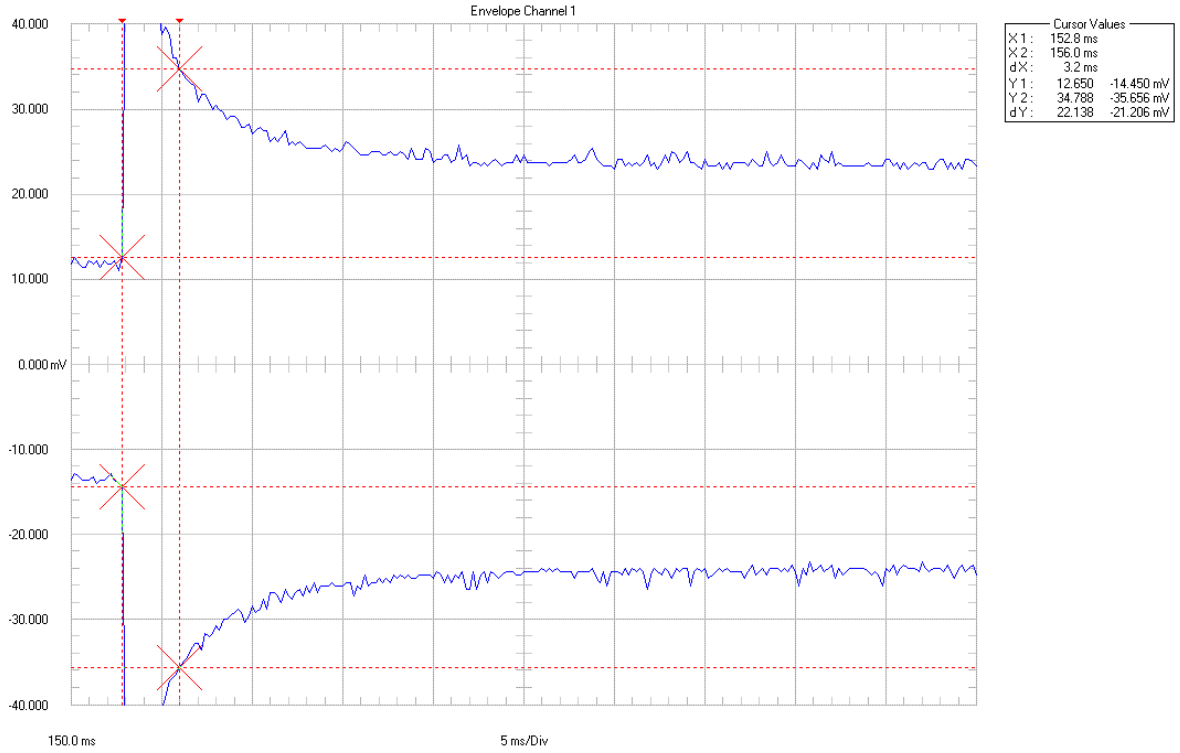


Figure 15 Compressor Transient Response

7.6. External Sub-Audio Signalling

Filtering for sub-audio signalling is available in the audio band below 260Hz. When sub-audio signalling is enabled, the 300Hz HPF in the audio section should also be enabled to remove the sub-audio signalling from the audio signal (in both Tx and Rx).

In Tx mode, the external sub-audio signal should be routed to Input2 (by convention, from the SIG input), and the filter selected using b6-5 of the Mode register, $C1. This signal will then be summed with the current In-band signal according to the settings in the ADC register, $A7. The level of this signal may be adjusted by using the Input2 Coarse and Fine gain settings ($B0 and P4.2) or the Tx Sub-Audio level control (P2.0). This signal path is dc–coupled.

In Rx mode, the input signal can be routed from either Input1 or Input2 depending on the setting of the Mode register, $C1, bit 7 and is then filtered according to the settings of b6-5 of the Mode register and presented at the MOD2 output. Suitable external switching is required if this output is also used in Tx mode.

To assist in compensating for the different levels expected for the sub-audio signalling compared with the in-band signals, the CTCSS and DCS filters exhibit 6dB of attenuation in Tx and 12dB of gain in Rx.

The DCS filter is a 4-pole Bessel filter with a –3dB point at 134Hz.

The CTCSS filter is a 6-pole Cauer filter with a –3dB point at 260Hz.

Setting both b6-5 to 1 enables a straight-through path which exhibits a roll off at 2700Hz.

See:

- Analogue Output Gain - $B0 write
- Mode Control – $C1 write

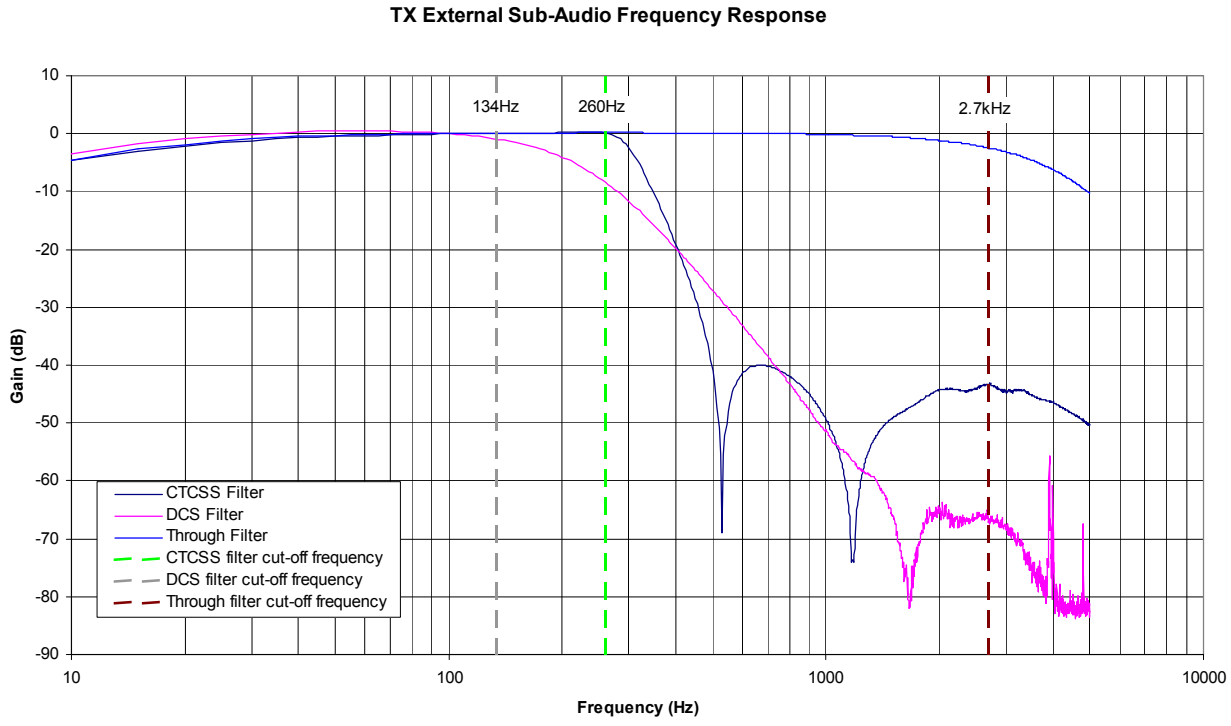


Figure 16 External Signalling Filter Response

7.7. Inband Signalling

The CMX148 supports DTMF signalling and generation of a user-programmable audio tone between 288Hz and 3000Hz. Note that if tones below 400Hz are used, sub-audio signalling should be disabled and the 300Hz HPF disabled.

Selection of the Inband signalling mode is performed by bits 11-8 of the Mode register ($C1). Detection of the selected Inband signalling mode can be performed in parallel with voice or data reception.

See:
- Mode Control – $C1 write
- Tx Inband Tones - $C3 write
- Tone Status - $CC read
- Audio Tone - $CD: write

7.7.1. Receiving DTMF Tones

DTMF Tone detection may be enabled in the Mode register ($C1) in parallel with other inband tone modes (however, this is not recommended due to the increased likelihood of false detects). When a DTMF tone has been detected, b10 of the Tone Status register ($CC) and b12 of the IRQ Status register, $C6, will be set. This value will over-write any existing inband tone value that may be present. The DTMF detector returns the values shown below in Table 2.

7.7.2. Transmitting DTMF Tones

The DTMF signals to be generated are defined in the TxTONE register ($C3). Single tones and twist (lower frequency tone reduced by 2dB) can be enabled by setting the appropriate bit in the $C3 register to 1. The DTMF level is set in Program Block P1.0. The DTMF tones must be transmitted on their own, the host µC must disable audio band signals prior to initiating transmission of the DTMF tones and (if required) restore the audio band signals after the DTMF transmission is complete. Table 2 shows the DTMF tone pairs, together with the values for programming the 'Tone Pair' field of the TxTONE register.

Table 2 DTMF Tone Pairs

Tone Code (Hex)	Key Pad Position	Low Tone (Hz)	High Tone (Hz)
1	1	697	1209
2	2	697	1336
3	3	697	1477
4	4	770	1209
5	5	770	1336
6	6	770	1477
7	7	852	1209
8	8	852	1336
9	9	852	1477
A	0	941	1336
B	*	941	1209
C	#	941	1477
D	A	697	1633
E	B	770	1633
F	C	852	1633
0	D	941	1633

Note: Only the underlined tone is generated when the 'Single Tone' bit is enabled.

7.7.3. Transmitting Audio Tones

See section 8.1.29 Audio Tone - $CD: write

7.8. MSK/FFSK Data Modem

The CMX148 supports both 1200 and 2400 baud MSK/FFSK data modes. In Rx mode, the device can be set to look for either of the MSK or FFSK modes, however, once a valid mode has been found, it will stay in that mode until the host resets it.

See:
- Mode Control – $C1 write
- Modem Control - $C7 write
- Rx Data 1 and 2 - $C5 and $C9 read
- Tx Data 1 and 2 - $CA and $CB write

7.8.1. Receiving MSK/FFSK Signals

The CMX148 can decode incoming MSK/FFSK signals at either 1200 or 2400 baud data rates, automatically detecting the rate from the received signal. Alternatively, a control word may set the baud rate, in which case the device only responds to signals operating at that rate. The form of MSK/FFSK signals for these baud rates is shown in Figure 17.

The received signal is filtered and data is extracted with the aid of a PLL to recover the clock from the serial data stream. The recovered data is stored in a 2- or 4-byte buffer (grouped into 16-bit words) and an interrupt issued to indicate received data is ready. Data is transferred over the C-BUS under host µC control. If this data is not read before the next data is decoded it will be overwritten and it is up to the user to ensure that the data is transferred at an adequate rate following data ready being flagged, see Table 5. The MSK/FFSK bit clock is not output externally.

The extracted data is compared with the 16-bit programmed Frame Sync pattern (preset to $CB23 following a RESET command). An interrupt will be flagged when the programmed Frame Sync pattern is detected or when the following Frame Head is decoded, see section 7.9.3. The host µC may stop the frame sync search by disabling the MSK/FFSK demodulator. Once a valid Frame Sync pattern has been detected, the frame sync search algorithm is disabled; it may be re-started by the host disabling the Modem Control bits of the Mode register ($C1:b2,3) and then re-enabling them (taking note of the C-BUS latency time).

If the CMX148 has been set to decode a Frame Head before interrupting, it will check the CRC portion of the Frame Head Control Field. If this indicates a corrupt Frame Head then a search for a new frame sync pattern will be automatically restarted.

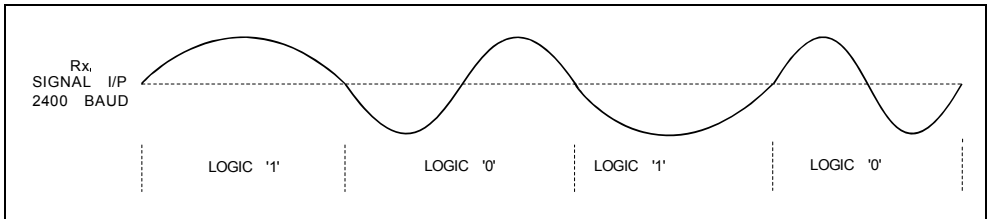
FFSK may be transmitted in conjunction with a CTCSS or DCS sub-audio component. The device will handle the sub-audio signals as previously described. If a sub-audio signal turns off during reception of FFSK, it is up to the host µC to turn off the decoding as the device will continue receiving and processing the incoming signal until commanded otherwise by the host µC.

The host µC must keep track of the message length or otherwise determine the end of reception (e.g. by using sub-audio information to check for signal presence) and disable the demodulator at the appropriate time. Note that when using packets with embedded size information, the CMX148 will indicate when the last data block has been received.

7.8.2. Transmitting MSK/FFSK Signals

The MSK/FFSK encoding operates in accordance with the bit settings in the Modem Control register ($C7). When enabled the modulator will begin transmitting data using the settings and values in Program Block 0 (bit sync and frame sync patterns), the Modem Control register and the Tx Data registers. Therefore, these registers should be programmed to the required values before transmission is enabled.

The CMX148 generates its own internal data clock and converts the binary data into the appropriately phased frequencies, as shown in Figure 17 and Table 3. The binary data is taken from Tx DATA 1 and 2 registers ($CA and $CB), most significant bit first. The following data words must be provided over the C-BUS within certain time limits to ensure the selected baud rate is maintained. The time limits will be dependent on the data coding being used, see Table 5.



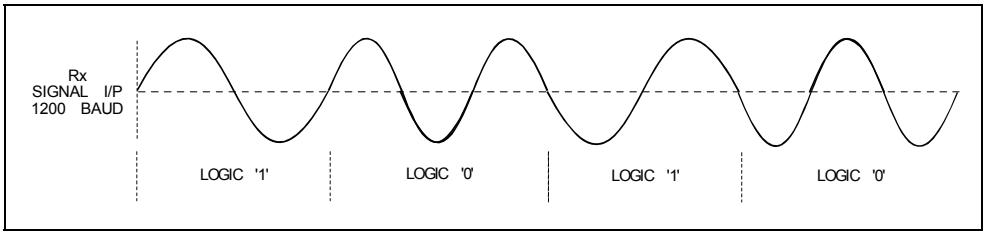


Figure 17 Modulating Waveforms for 1200 and 2400 Baud MSK/FFSK Signals

The table below shows the combinations of frequencies and number of cycles to represent each bit of data, for both baud rates.

Table 3 Data Frequencies for each Baud Rate

Baud Rate	Data	Frequency	Number of Cycles
1200baud	1	1200Hz	one
	0	1800Hz	one and a half
2400baud	1	1200Hz	half
	0	2400Hz	one

Note: FFSK may be transmitted in conjunction with a CTCSS or DCS sub-audio component.

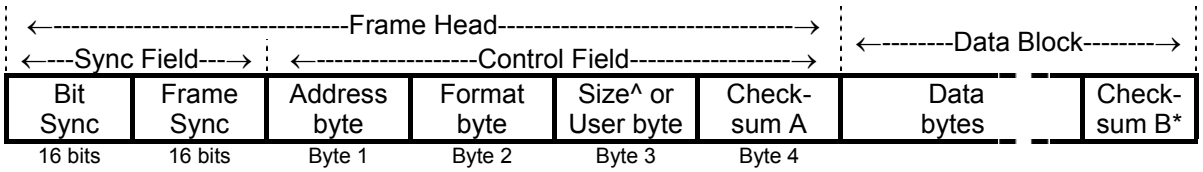
7.9. MSK/FFSK Data Packetising

The CMX148 has extensive data packetising features that can be controlled by the Modem Control register ($C7). The CMX148 can packetise data in a variety of formats so the user can have the optimum data throughput for various signal-to-noise ratios. Data is transferred in packets or frames, each frame is made up of a Frame Head followed by any associated user data. The Frame Head is composed of a 16-bit Bit Sync and 16-bit Frame Sync pattern immediately followed by a 4-byte control field. The 4 bytes start with an 8-bit address followed by 1 byte carrying information about the format of the following Data Block. The next byte indicates the size of the packet or can be used freely, depending on the format selected. The last byte is a checksum to detect if any of the 4 Frame Head bytes has been corrupted.

7.9.1. Tx Hang Bit

When transmitting MSK/FFSK data of types 0, 2 or 3, the user should ensure that the data is terminated with a hang bit. To do this, the host must set the 'Last Data' bit in the Modem Control register ($C7) after the last data word has been loaded into the Tx Data 1 register ($CA), as described in section 8.1.27. This will append a hang bit onto the end of the current word and will stop modulating after the hang bit has been transmitted. It will also generate an interrupt (if enabled) when the hang bit has left the modulator.

7.9.2. Frame Format



* Checksum B not applied to all Data Block types
^ Byte 3 is only reserved on sized data blocks.

The Data Block is made up from the user data. This consists of a variable number of data bytes optionally encoded to ensure secure delivery over a radio channel to the receiver. Checksum B is only applied at the end of sized Data Blocks, the receiver can then detect if any of the user data has been corrupted. Checksum B is composed of 16 bits for messages ≤16 bytes and 32 bits for longer messages.

7.9.3. Frame Head

In Frame Formats 3, 4 and 5, the Frame Head allows the receiver to detect and lock on to MSK/FFSK signals, provides basic addressing to screen out unwanted messages and indicates the format, coding and length of any following data.

The four Control Field bytes have Forward Error Correction (FEC) applied to them in the transmitter, this adds 4 bits to every byte and the receiver can correct errors in the received bytes. The 4 received bytes are then checked for a correct CRC, so that corrupted Frame Heads can be rejected. If checksum A indicates that the Control Field bytes are correct, the Address (byte 1) is compared with that stored in the MSK Header Address bits of Modem Address register, $B6 (b15:8). If a match occurs, or if the received address is '40', then an interrupt is raised indicating a valid Frame Head has been received. The Frame Head is 80 bits long (16 + 16 + {4x12}). The contents of a received Frame Head can be read from Rx Data registers $C5 and $C9.

7.9.4. Data Block Coding

The Data Block follows the Frame Head and can be coded with different levels of error correction and detection. The Data Block format is controlled by the Frame Format selected in Frame Head byte 2, see also section 8.1.24. Messages can take the following formats:

Format: Description:

0 **Un-Formatted Data**. This mode should be used with the En_RAW bit (b10 of the Modem Control Register) set to 1. The Interleave and Scrambler settings are ignored. This mode can be useful when interfacing to a system using a different format to those available in the CMX148.

In transmit, the device will transmit only the data loaded into the TxData 1 register. The host should provide bit sync, frame sync and any required formatting data as well as the Data Block through this register.

In receive, the device will search for the programmed 16-bit Frame Sync pattern and then output all following data 16 bits at a time. The host will have to perform all other data formatting.

1 **Frame Head only**. No Data Block will be added. This format can be useful for indicating channel or user status by using byte 3 and the User Bit of the Frame Head (see section 8.1.24).

2 **Frame Head followed by raw data**. User data is appended to the Frame Head in 2-byte units with no formatting or CRC added by the CMX148. No size information is set in the Frame Head and the Data Block may contain any even number of bytes per frame.

3 **Frame Head followed by FEC coded data only**. Each byte of the user data has 4 bits of FEC coding added. No size information is set in the Frame Head and Data Block may contain any even number of bytes per frame. No CRC is added to the data.

4 **Frame Head followed by FEC coded data with an automatic CRC** at the end of the Data Block. The number of user data bytes in the Frame must be set in Frame Head byte 3. The CRC is automatically checked in the receiver and the result indicated to the host µC. Up to 255 bytes of user data can be sent in each frame using this format.

5 **As '4 above', with the addition of all Data Block bytes being interleaved**. This spreads the transmitted information over time and helps reduce the effect of errors caused by fading. Interleaving is performed on blocks of 4 bytes, the CMX148 automatically adds and strips out pad bytes to ensure multiples of 4 bytes are sent over the radio channel.

Notes:

- Format 0, 1, 2 and 3 have no size information requirement and do not reserve Frame Head byte 3. This byte may be freely used by the host µC to convey information. In Format 4 and 5 this byte must be set to the number of user bytes in the message attached to that Frame Head (≤255) to allow the receiver to correctly decode and calculate the CRC.
- Format 0 data transfers do not use frame heads. In Tx the host µC must transfer the bit and frame sync data before sending the message data. In Rx the host µC must decode all data after the frame sync.

Table 4 Data Block Formats

Data Block Format:	Total over-air bits for an 80-byte message	Air time for MSK/FFSK message (ms) at 1200baud	Air time for MSK/FFSK message (ms) at 2400baud	Over air efficiency	Burst length protection at 1200baud *[for 2400baud divide both times by 2]*	Probability of detecting errors
2	720	600	300	89%	None	Zero
3	1040	867	433	62%	<0.83ms in any 10ms	Poor
4	1088	907	453	59%	<0.83ms in any 10ms	Excellent
5	1088	907	453	59%	<3.33ms in any 40ms	Excellent

Higher levels of error protection have the penalty of adding extra bits to the over air signal and this reduces the effective bit rate. Less error protection increases the effective bit rate, however in typical radio conditions the penalty is a greater risk of errors leading to repeated messages and a net reduction in effective bit rate compared to using error correction and detection.

7.9.5. CRC and FEC Encoding Information

For messages with FEC coding the following matrix is used to calculate and decode bytes:

Data bits								FEC bits			
7	6	5	4	3	2	1	0	3	2	1	0
1	1	1	0	1	1	0	0	1	0	0	0
1	1	0	1	0	0	1	1	0	1	0	0
1	0	1	1	1	0	1	0	0	0	1	0
0	1	1	1	0	1	0	1	0	0	0	1

An 8-bit CRC is used in all frame heads with the following generator polynomial (GP):

$x^8 + x^7 + x^4 + x^3 + x^1 + x^0$

A 16-bit CRC is used at the end of sized data messages of up to 16 bytes with the following GP:

$x^{16} + x^{12} + x^5 + x^0$

A 32-bit CRC is used at the end of sized data messages of over 16 bytes with the following GP:

$x^{32} + x^{31} + x^{30} + x^{28} + x^{27} + x^{25} + x^{24} + x^{22} + x^{21} + x^{20} + x^{16} + x^{10} + x^9 + x^6 + x^0$

7.9.6. Data Interleaving

The built in MSK/FFSK packetising includes the option of interleaving the data in each block (Type 5). This, together with Forward Error Correction (FEC), reduces the effects of burst errors. Interleaving does not add any bits to the message, the packet is assembled in 'rows' and then transmitting in 'columns'.

Data (8 bits)								FEC (4 bits)			
0	1	2	3	4	5	6	7	8	9	10	11
12	13	14	15	16	17	18	19	20	21	22	23
24	25	26	27	28	29	30	31	32	33	34	35
36	37	38	39	40	41	42	43	44	45	46	47

In the above example the packet is assembled as 4 rows with 12 bits of information per row. When this packet is transmitted, interleaved bits are sent over the communication channel in the following order:

0, 12, 24, 36, 1, 13, 25, 37, 2, 14, ... , 33, 45, 10, 22, 34, 46, 11, 23, 35, 47.

In the receiving modem the packet is re-assembled (de-interleaved) before error correction. The CMX148 has a built in packet receive modem which is able to recognise (by using the frame head bytes) when the data has been interleaved by the transmitter and will decode the data using the correct method.

7.9.7. Data Scrambling/Privacy Coding

It is preferable for MSK/FFSK over-air data to be reasonably random in nature to ensure the receiver can track timing using the bit changes and to smooth the frequency spectrum. To reduce the possibility of

user data causing long strings of 1's or 0's to be transmitted, a 16-bit data scrambler is provided and operates on all bits after the Frame Head.

The default (standard) setting for this scrambler is with a start code (seed) of $FFFF and any receivers with the same seed may decode this data. However, if the transmitter and receiver pre-arrange a different seed then the scrambler will start its sequence in another place and any simple receiver that does not know the transmitted seed will not be able to successfully decode the data. This method gives over 65,000 different starting points and the chance of others decoding data successfully is reduced.

The CMX148 provides the option of two custom 16-bit words that are programmable by the user in Program Block P0.4 to P0.7. Bits 0 and 1 in the Frame Head Format byte indicate which setting (standard, Seed1, Seed2 or none) the following Data Block has been scrambled with, see section 8.1.24. Note that a seed of $0000 will effectively turn off the Scrambler and provide no protection against long sequences of 1's or 0's. Reception of scrambled data will only be successful when the receiving device has been programmed with the correct (identical) seed to that used by the transmitter.

By using this method the CMX148 provides a privacy code that will protect against casual monitoring, however the data is not encrypted and a sophisticated receiver can decode the data by using moderately simple decoding techniques. If data encryption is required it must be performed by the host µC. The scrambler function is controlled by bits 0,1 of the Modem Control register, $C7.

7.9.8. Data Buffer Timing

Data must be transferred at the rate appropriate to the signal type and data format. The CMX148 buffers data in two 16-bit registers. The CMX148 will issue interrupts to indicate when data is available or required. The host must respond to these interrupts within the maximum allowable latency for the signal type. Table 5 shows the maximum latencies for transferring signal data to maintain appropriate data throughput.

Table 5 Maximum Data Transfer Latency

Data encoding type	Max. time to read from or write to data buffer		Data buffer size
	1200 baud	2400 baud	
0	13.3ms	6.6ms	2 bytes
1	N/A*	N/A*	4 bytes
2	13.3ms	6.6ms	2 bytes
3	20ms	10ms	2 bytes
4	40ms	20ms	4 bytes
5	40ms	20ms	4 bytes

* Type 1 message is an isolated Frame Head, there is no subsequent data to load (Tx) or read (Rx).

7.10. Auxiliary ADC Operation

The input to the Auxiliary ADCs can be independently routed to any of the signal input pins under control of the AuxADC and Tx MOD mode register, $A7. Conversions will be performed as long as a valid input source is selected, to stop the ADC, the input source should be set to "none". Register $C0, b6, BIAS, must be enabled for Auxiliary ADC operation.

Averaging can be applied to the ADC readings by selecting the relevant bits in the AuxADC and Tx MOD mode register, $A7, the length of the averaging is determined by the value in the Program Block (P3.0 and P3.1), and defaults to a value of 0. This is a rolling average system such that a proportion of the current data will be added to the last value. The proportion is determined by the value of the average counter in P3.0 and P3.1. For an average value of 0; 50% of the current value will be applied, for a value of 1 = 25%, 2 = 12.5% etc. The maximum useful value of this field is 8. Averaging will begin with the current value of the AuxADC, therefore it is recommended that the AuxADC be enabled for at least one sample (250µs) before starting the average process to ensure that its initial value is as expected, otherwise the initial value will default to zero.

High and Low thresholds may be independently applied to both ADC channels (the comparison is applied after averaging, if this is enabled) and an IRQ generated when either the High threshold is crossed by a rising edge signal or the Low threshold is passed by a falling edge signal, which allows the user to implement a selectable degree of hysterisis. The thresholds are programmed via the AuxADC Threshold register, $B5.

Auxiliary ADC data is read back in the AuxADC Data register ($A9) and includes the threshold status as well as the actual conversion data (subject to averaging, if enabled).

See:
- AuxADC and Tx MOD Mode - $A7 write
- AuxADC1 Data - $A9 read
- AuxADC2 Data - $AA read
- AuxADC Threshold Data - $B5 write

7.11. Auxiliary DAC/RAMDAC Operation

The four Auxiliary DAC channels are programmed via the AuxDAC Control register, $A8. AuxDAC channel 1 may also be programmed to operate as a RAMDAC which will automatically output a pre-programmed profile at a programmed rate. The AuxDAC Control register, $A8, with b12 set, controls this mode of operation. The default profile is a raised cosine (see Table 9), but this may be over-written with a user defined profile by writing to Program Block P3.11. The RAMDAC operation is only available in Tx mode and, to avoid glitches in the ramp profile, it is important not to change to IDLE or Rx mode whilst the RAMDAC is still ramping. The AuxDAC outputs (available on their respective DAC pins) hold the user-programmed level during a powersave operation if left enabled, otherwise they will return to zero. Note that access to all four AuxDACs is controlled by the AuxDAC Control register, $A8, and therefore to update all AuxDACs requires four writes to this register. It is not possible to simultaneously update all four AuxDACs.

See:
- AuxDAC Control/Data - $A8 write

7.12. Digital System Clock Generator

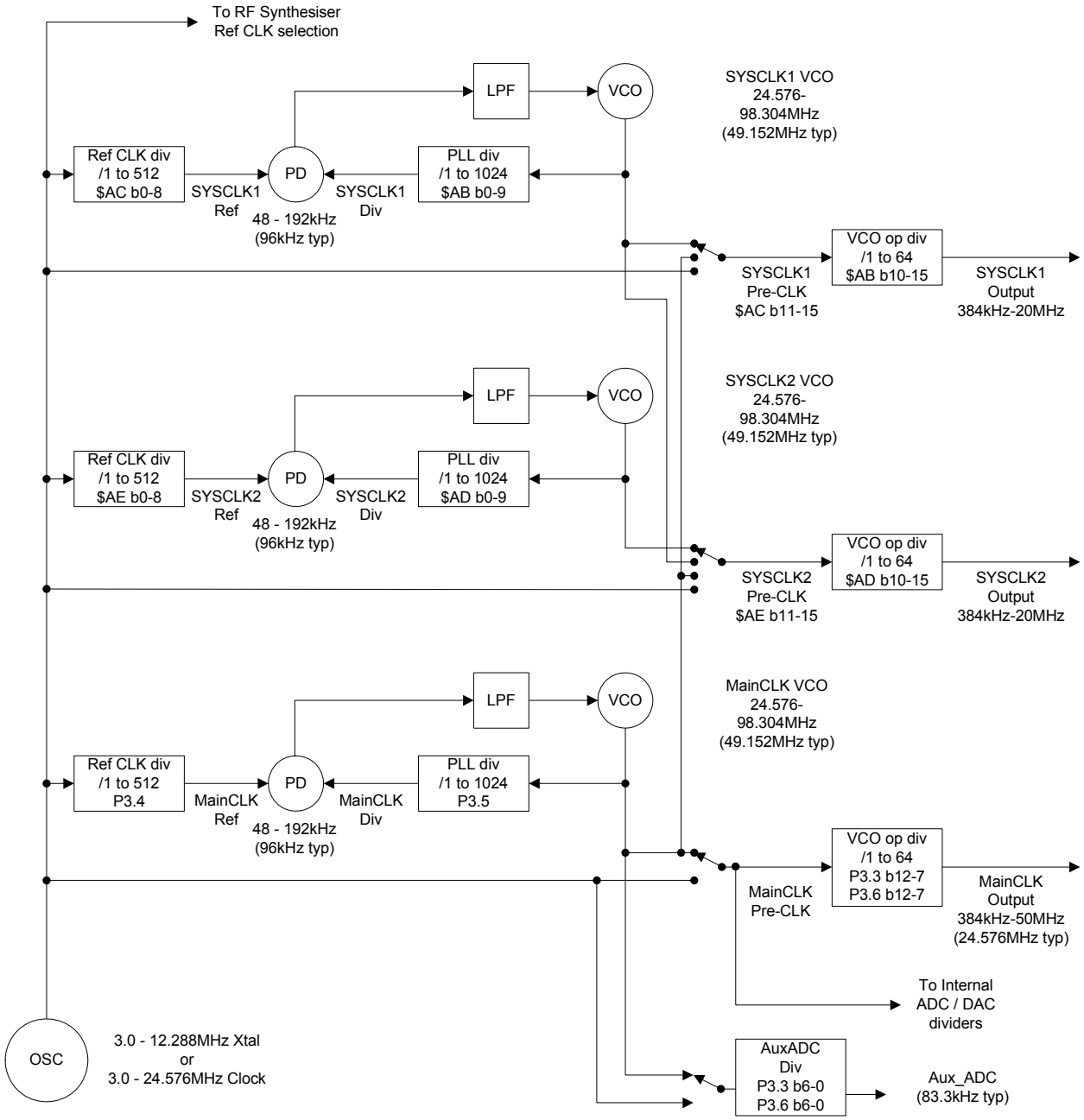


Figure 18 Digital Clock Generation Schemes

The CMX148 includes a 2-pin crystal oscillator circuit. This can either be configured as an oscillator, as shown in section 5, or the XTAL input can be driven by an externally generated clock. The crystal (Xtal) source frequency can go up to 12.288MHz (clock source frequency up to 24.576MHz), but by default, a 3.6864MHz Xtal is assumed for the functionality provided in the CMX148.

7.12.1. Main Clock Operation

A PLL is used to create the main clock (MainCLK - nominally 24.576MHz) for the internal sections of the CMX148. At the same time, other internal clocks are generated by division of either the Xtal Reference Clock or the Main Clock. These internal clocks are used for determining the sample rates and conversion times of A-to-D and D-to-A converters, running a General Purpose Timer, the signal processing block. In particular, it should be noted that in IDLE mode the setting of the GP Timer divider directly affects the C-BUS latency (with the default values this is nominally 250µs).

The CMX148 defaults to the settings appropriate for a 3.6864MHz Xtal, however if other frequencies are to be used (to facilitate commonality of Xtals between external RF synthesizers and the CMX148 for instance) then the Program Block P3.2 to P3.7 will need to be programmed appropriately at power-on. A table of common values is provided in Table 1.

See:

- Program Block 3 – AuxDAC, RAMDAC and Clock Control

7.12.2. System Clock Operation

Two System Clock outputs, SYSCLK1 and SYSCLK2, are available to drive additional circuits, as required. These are phase locked loop (PLL) clocks that can be programmed via the System Clock registers with suitable values chosen by the user. The System Clock PLL Configure registers ($AB and $AD) control the values of the VCO Output divider and Main Divide registers, while the System Clock Ref. Configure registers ($AC and $AE) control the values of the Reference Divider and signal routing configurations. The PLLs are designed for a reference frequency of 96kHz. If not required, these clocks can be independently powersaved. The clock generation scheme is shown in the block diagram of Figure 18. Note that at power-on, these outputs are disabled.

See:

- SYSCLK1 and SYSCLK2 PLL Data - $AB, $AD write
- SYSCLK1 and SYSCLK2 REF - $AC and $AE write

7.13. GPIO

Two pins are provided for control of external hardware. RXENA and TXENA are driven by the device to follow the state of the Rx and Tx Mode bits in the Mode register, $C1:

$C1 Mode:	b1	b0	TXENA	RXENA
IDLE	0	0	1	1
Rx	0	1	1	0
Tx	1	0	0	1
reserved	1	1	1	1

7.14. Signal Level Optimisation

The internal signal processing of the CMX148 will operate with wide dynamic range and low distortion only if the signal level at all stages in the signal processing chain is kept within the recommended limits. For a device working from a 3.3V ±10% supply, the maximum signal level which can be accommodated without distortion is [(3.3 x 90%) – (2 x 0.3V)] Volts p-p = 838mVrms, assuming a sine wave signal. Compared to the reference level of 308mVrms, this is a signal of +8.69dB. This level should not be exceeded at any stage.

7.14.1. Transmit Path Levels

For the maximum signal out of the MOD1 and MOD2 gain stages, the signal level at the output of the Analogue Routing block should not exceed +8.69dB, assuming both fine and coarse output gain stages are set to a gain of 0dB. The sub-audio level is normally set to 31mVrms ±1.0dB, which means that the output from the soft limiter must not exceed 803mVrms. If pre-emphasis is used, an output signal at 3000Hz will have three times the amplitude of a signal at 1000Hz, so the signal level before pre-emphasis should not exceed 268mVrms. If the compressor is also used, its 'knee' is at 100mVrms, which would allow a signal into the compressor of 718mVrms, which is less than the maximum signal level. The Fine

Input Gain adjustment has a maximum attenuation of 3.5dB and no gain, whereas the Coarse Input Gain adjustment has a variable gain of up to +22.4dB and no attenuation. If the highest gain setting were used, then the maximum allowable input signal level at the MICFB pin would be 54mVrms. With the lowest gain setting (0dB), the maximum allowable input signal level at the MICFB pin would be 718mVrms.

7.14.2. Receive Path Levels

For the maximum signal out of the AUDIO pin, the signal level at the output of the Analogue Routing block should not exceed +8.69dB, assuming both fine and coarse output gain stages are set to a gain of 0dB. In this case, there is no sub-audio signal to be added, so the maximum signal level remains at 838mVrms. If de-emphasis is used, an output signal at 300Hz will have three and a third times the amplitude of a signal at 1000Hz, so the signal level before de-emphasis should not exceed 251mVrms. If the expander is also used, its 'knee' is at 100mVrms, which would allow a signal into the expander of 158mVrms. The Fine Input Gain adjustment has a maximum attenuation of 3.5dB and no gain, whereas the Coarse Input Gain adjustment has a variable gain of up to +22.4dB and no attenuation. If the highest gain setting were used, then the maximum allowable input signal level at the DISCFB pin would be 12.0mV rms. With the lowest gain setting (0dB), the maximum allowable input signal level at the DISCFB pin would be 158mVrms. The signal level of +8.69dB (838mVrms) is an absolute maximum, which should not be exceeded anywhere in the signal processing chain if severe distortion is to be avoided.

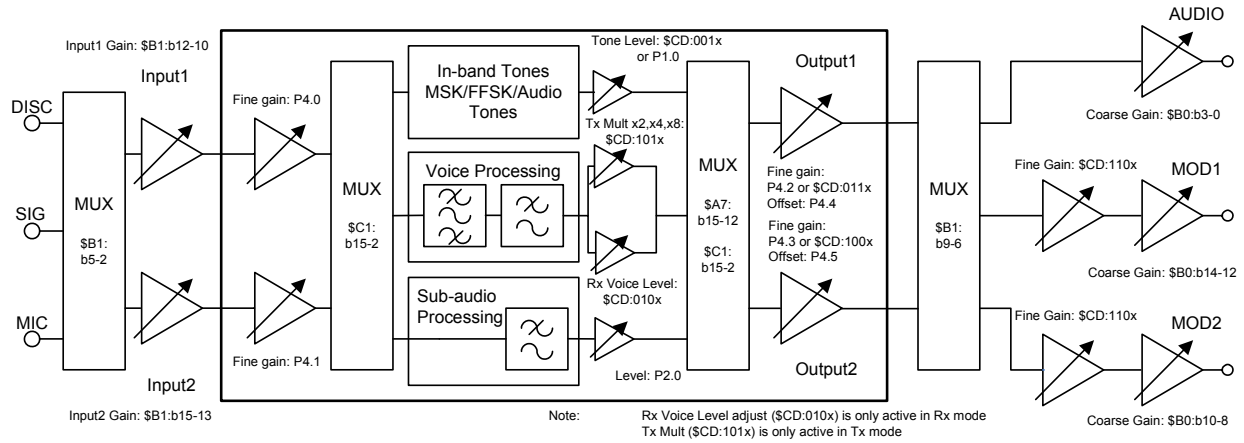


Figure 19 Level Adjustments

8. Configuration Guide

8.1. C-BUS Register Details

Addr. (hex)		Register	Word Size (bits)
$01	W	C-BUS RESET	0
$A7	W	AuxADC and TX MOD Mode	16
$A8	W	AuxDAC Control/Data	16
$A9	R	AuxADC1 Data	16
$AA	R	AuxADC2 Data	16
$AB	W	SYSCLK1 PLL Data	16
$AC	W	SYSCLK1 ref	16
$AD	W	SYSCLK2 PLL Data	16
$AE	W	SYSCLK2 ref	16
$AF		*reserved*	
$B0	W	Analogue Output Gain	16
$B1	W	Input Gain and Output Signal Routing	16
$B2		*reserved*	
$B3		*reserved*	
$B4		*reserved*	
$B5	W	AuxADC Threshold Data	16
$B6	W	Modem Address	16
$B8		*reserved*	
$B9		*reserved*	
$BB		*reserved*	
$BC		*reserved*	
$BD		*reserved*	
$BE		*reserved*	
$BF		*reserved*	
$C0	W	Power-Down Control	16
$C1	W	Mode Control	16
$C2	W	Audio Control	16
$C3	W	Tx Inband Tones	16
$C5	R	Rx Data 1	16
$C6	R	Status	16
$C7	W	Modem Control	16
$C8	W	Programming	16
$C9	R	Rx Data 2	16
$CA	W	Tx Data 1	16
$CB	W	Tx Data 2	16
$CC	R	Tone Status/Device Identification	16
$CD	W	Audio Tone	16
$CE	W	Interrupt Mask	16
$CF		*reserved*	

The detailed descriptions of the C-BUS registers are presented in numerical order and should be read in conjunction with the relevant functional descriptions.

All other C-BUS addresses (including those not listed above) are either reserved for future use or allocated for production testing and must not be accessed in normal operation.

8.1.1. Reset Operations

A power-on reset is automatically performed when power is applied to the CMX148. A reset can also be issued as a C-BUS command, either as a General Reset command ($01), or by setting the appropriate bit (b5) in the Powerdown Control register ($C0). In the latter case, an option exists to protect the values held in the Program Block (which is accessed via the Programming register, $C8). The action of each reset type is shown in the table below:

Table 6 Reset Operations

	Reset Type	Protect Bit ($C0 b4) state	Program Block State
1	Power-on	cleared by h/w	default
2	General Reset (C-BUS $01)	cleared by h/w	default
3	Reset (C-BUS $C0 b5)	0	default
4	Reset (C-BUS $C0 b5)	1	protected

8.1.2. General Reset - $01 write

The General Reset command has no data attached to it. It sets all operational C-BUS registers to $0000, (apart from the registers marked as *reserved*). Note that some transient data may appear in the following registers during the power-up process – this should be ignored:

Status	$C6	Tone Status	$CC
AuxADC1 Data	$A9	AuxADC2 Data	$AA
Rx Data 1	$C5	Rx Data 2	$C9

Once the PRG flag (Status register, $C6 bit 0) is set to 1, the device is available for use and the Device Identification Code ($1480) can be read from the Tone Status register ($CC).

A power-on reset performs the same action as a General Reset command.

8.1.3. Interrupt Operation

The CMX148 will issue an interrupt on the IRQN pin when the IRQ bit (bit 15) of the Status register and the IRQ Mask bit (bit 15) are both set to 1. The IRQ bit is set when the state of any of the interrupt flag bits in the Status register changes from 0 to 1 and the corresponding mask bit(s) in the Interrupt Mask register is(are) set. Enabling an interrupt by setting a mask bit (0→1) after the corresponding Status register bit has already been set to 1 will also cause the IRQ bit to be set to 1.

All interrupt flag bits in the Status register, except the Program flag (PRG, $C6 bit 0), are cleared and the interrupt request is cleared following the command/address phase of a C-BUS read of the Status register. The PRG flag is set to 1 only when it is permissible to write a new word to the Programming register. See:

- Status – $C6 read
- Interrupt Mask - $CE write

8.1.4. General Notes

In normal operation, the most significant registers are:

- Mode Control – $C1 write
- Status – $C6 read
- Analogue Output Gain - $B0 write
- Input Gain and Output Signal Routing - $B1 write
- Audio Control – $C2 write

Setting the Mode register to either Rx or Tx will automatically increase the internal clock speed to its operational rate, whilst setting the Mode register to IDLE will automatically return the internal clock to a

lower (powersaving) rate. To access the Program Blocks (through the Programming register, $C8) the device MUST be in IDLE mode.

Under normal circumstances the CMX148 manages the main clock control automatically, using the default values loaded in Program Block 3.

8.1.5. AuxADC and Tx MOD Mode - $A7 write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Tx Mod Mode				Aux ADC2 AV Mode		Aux ADC2 I/P Select			Aux ADC1 AV Mode		Aux ADC1 I/P Select			0	0

				Tx MOD Mode	
b15	**b14**	**b13**	**b12**	**Output1**	**Output2**
1	1	1	1	*reserved*	
1	1	1	0	*reserved*	
1	1	0	1	*reserved*	
1	1	0	0	*reserved*	
1	0	1	1	Inband	Inband + Sub-Audio
1	0	1	0	*reserved*	
1	0	0	1	*reserved*	
1	0	0	0	*reserved*	
0	1	1	1	*reserved*	
0	1	1	0	*reserved*	
0	1	0	1	*reserved*	
0	1	0	0	*reserved*	
0	0	1	1	Inband + Sub-Audio	Inband + Sub-Audio
0	0	1	0	Inband + Sub-Audio	Sub-Audio
0	0	0	1	Inband	Sub-Audio
0	0	0	0	Bias	Bias

To select the routing between the Output1, Output2 and MOD1, MOD2 and AUDIO, see section 8.1.12

		AuxADC Averaging Mode
b11	**b10**	**AuxADC2**
b6	**b5**	**AuxADC1**
1	1	*reserved*
1	0	*reserved*
0	1	rolling average, uses Program Block 3.0 value
0	0	No averaging

			AuxADC Input Select
b9	**b8**	**b7**	**AuxADC2**
b4	**b3**	**b2**	**AuxADC1**
1	1	1	ADC4
1	1	0	ADC3
1	0	1	ADC2
1	0	0	ADC1
0	1	1	MIC
0	1	0	SIG
0	0	1	DISC
0	0	0	off

8.1.6. AuxDAC Control/Data - $A8 write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ENA	0	0	RAM DAC	DAC Sel		AuxDAC Data/RAMDAC control									

b15 enable selected AuxDAC 0 = disable 1 = enable
b14 *reserved*
b13 *reserved*
b12 RAMDAC enable 0 = AuxDAC1 operates normally
1 = AuxDAC1 operates as a RAMDAC[2]. Data in b0-6 controls the RAMDAC functions.

b11-b10 select the AuxDAC that b9-b0 data will be written to
00 = AuxDAC1
01 = AuxDAC2
10 = AuxDAC3
11 = AuxDAC4
b9-b0 AuxDAC data (unsigned)

Note: the C-BUS latency period (250µs) should be observed between successive writes to this register.

Note: when $A8 b12 is set to 1, writing data to this register controls the RAMDAC settings. Writing to AuxDAC1 whilst the RAMDAC is still ramping may cause unintended operation. In this mode b10 and b11 are ignored and b9 to b0 perform the following functions:

b9 *reserved*, clear to 0
b8 *reserved*, clear to 0
b7 *reserved*, clear to 0
b6 RAMDAC RAM access, 0 resets the internal RAMDAC address pointer

			RAMDAC Scan Time	
b5	b4	b3	Divider	Time (ms)
0	0	0	1024	10.50
0	0	1	512	5.25
0	1	0	256	2.63
0	1	1	128	1.31
1	0	0	64	0.66
1	0	1	32	0.33
1	1	0	16	0.16
1	1	1	8	0.08

b2 Scan direction: 0 = ramp down 1 = ramp up
b1 Autocycle 0 = disable 1 = continuous ramp up/down
b0 RAMDAC start 0 = stop 1 = start RAMDAC ramping

To initiate a RAMDAC ramp up write: $9005
To initiate a RAMDAC ramp down, write: $9001

Note that initiating a RAMDAC scan will automatically bring AuxDAC1 out of powersave. To place AuxDAC1 back into powersave, it must be written to explicitly. Do NOT change IDLE/Rx/Tx mode whilst the RAMDAC is still ramping.

[2] Do NOT write to directly to AuxDAC 1 whilst the RAMDAC is in operation. RAMDAC is only available when in Tx mode.

8.1.7. AuxADC1 Data - $A9 read

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Threshold Status		x	x	x	x	Aux ADC 1 Data									

b15-14 Threshold Status

b15 = 1 signal is above the high threshold
= 0 signal is below the high threshold
b14 = 1 signal is below the low threshold
= 0 signal is above the low threshold

b13 *reserved*
b12 *reserved*
b11 *reserved*
b10 *reserved*
b9–0 AuxADC1 data or last reading (unsigned)

8.1.8. AuxADC2 Data - $AA read

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Threshold status		x	x	x	x	Aux ADC 2 Data									

b15-14 Threshold Status

b15 = 1 signal is above the high threshold
= 0 signal is below the high threshold
b14 = 1 signal is below the low threshold
= 0 signal is above the low threshold

b13 *reserved*
b12 *reserved*
b11 *reserved*
b10 *reserved*
b9-0 AuxADC2 data or last reading (unsigned)

8.1.9. SYSCLK1 and SYSCLK2 PLL Data - $AB, $AD write

C-BUS address: $AB – SYSCLK1 PLL
C-BUS address: $AD – SYSCLK2 PLL

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VCO Op Divide Ratio <5-0>						PLL Feedback Divide Ratio <9-0>									

b15-10 divide the selected output clock source by the value in these bits, to generate the System Clock output. Divide by 64 is selected by setting these bits to 0.

b9-0 divide System Clock PLL VCO clock by value set in these bits as feedback to the PLL phase detector (PD); when the PLL is stable, this will be the same frequency as the internal reference as set by b8-b0 of the System Clock Reference and Source Configuration register ($AC). Divide by 1024 is selected by setting these bits to 0.

8.1.10. SYSCLK1 and SYSCLK2 REF - $AC and $AE write

C-BUS address: $AC – SYSCLK1 Ref

C-BUS address: $AE – SYSCLK2 Ref

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Select and PS Clock Sources					O/P Slew		Ref Clock Divide Ratio <8-0>								

b15,12,11 Clock output divider source

SYSCLK1 Source	**b15**	**b12**	**b11**
Xtal	0	x	x
SYSCLK1 PLL	1	0	0
Main PLL	1	0	1
Test	1	1	x

SYSCLK2 Source	**b15**	**b12**	**b11**
Xtal	0	x	x
SYSCKL2 PLL	1	0	0
Main PLL	1	0	1
SYSCLK1 PLL	1	1	0
Test	1	1	1

b14 Powersave PLL 0 = powersave 1 = enabled

b13 Powersave Output Divider 0 = powersave/bypass 1 = enabled

b10-9 Output Slew Rate

b10	**b9**	**Output Slew Rate**
0	0	normal
0	1	slow
1	x	fast

b8-b0 Reference Clk divide value. Divide by 512 function is selected by setting these bits to 0.

Note that after a General Reset, there will be no signal present on the SYSCLK1 and SYSCLK2 pins.

8.1.11. Analogue Output Gain - $B0 write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Inv_1	MOD1 Attenuation			Inv_2	MOD2 Attenuation			Ramp Up/Dn	0	0	0	Audio Output Attenuation			

This register provides attenuation of the MOD1, MOD2 and AUDIO output signals, but no gain. Likewise, the fine gain adjustment (P4.2-3) only provides signal attenuation. If the signal output is too small, then the input gain stages (register $B1) will need to be adjusted.

b15 MOD1 output polarity 0 = true 1 = inverted
b11 MOD2 output polarity 0 = true 1 = inverted
Used when interfacing with RF circuitry or when generating an inverted turn-off code for CTCSS. Any change will take place immediately (within the C-BUS latency period) after these bits are changed.

b14	b13	b12	MOD1 Output Attenuation
b10	**b9**	**b8**	**MOD2 Output Attenuation**
0	0	0	>40dB (default)
0	0	1	12dB
0	1	0	10dB
0	1	1	8dB
1	0	0	6dB
1	0	1	4dB
1	1	0	2dB
1	1	1	0dB

b7 Ramp Up/Down enable 0 = off 1 = on
When bit 7 is set to 1 the MOD output signals are ramped to reduce transients in the transmitted signal. The ramp up/down time is set in the 'Ramp Rate Control' section of the Program Block (P4.6).

Bits 6 to 4 are reserved - set to 0.

b3	b2	b1	b0	Audio Output Attenuation
0	0	0	0	>60dB (default)
0	0	0	1	44.8dB
0	0	1	0	41.6dB
0	0	1	1	38.4dB
0	1	0	0	35.2dB
0	1	0	1	32.0dB
0	1	1	0	28.8dB
0	1	1	1	25.6dB
1	0	0	0	22.4dB
1	0	0	1	19.2dB
1	0	1	0	16.0dB
1	0	1	1	12.8dB
1	1	0	0	9.6dB
1	1	0	1	6.4dB
1	1	1	0	3.2dB
1	1	1	1	0dB

Note that fine control of Output1 and Output2 levels can be achieved with the FINE OUTPUT GAIN 1 and FINE OUTPUT GAIN 2 registers (P4.2-3). These affect the MOD1, MOD2 and AUDIO outputs according to the routing set in registers $A7 and $B1

8.1.12. Input Gain and Output Signal Routing - $B1 write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Input2 Gain			Input1 Gain			MOD1 Source		MOD2 Source	AUDIO Source	Input1 Routing		Input2 Routing		0	0

b12	b11	b10	Input1 Gain
b15	b14	b13	Input2 Gain
0	0	0	0dB (default)
0	0	1	3.2dB
0	1	0	6.4dB
0	1	1	9.6dB
1	0	0	12.8dB
1	0	1	16.0dB
1	1	0	19.2dB
1	1	1	22.4dB

b7	MOD2 Source
0	bias -> MOD2 (default)
1	Output2 -> MOD2

b6	AUDIO Source
0	bias -> AUDIO (default)
1	Output1 -> AUDIO

b9	b8	MOD1 Source
0	0	bias (default)
0	1	bias
1	0	Output1 -> MOD1
1	1	Output2 -> MOD1

b5	b4	Input1 Signal Routing
b3	b2	Input2 Signal Routing
0	0	bias (default)
0	1	DISC
1	0	SIG
1	1	MIC

Output1 and Output2 signal sources are also defined in section 8.1.5.

Bits 1, 0 are reserved – clear to 0.

In normal operation, all signal processing blocks would be set to work with Input1. There are a number of applications where it may be desirable to split the processing across both inputs. Such applications could be monitoring two RF receivers, or where an external voice encryption unit is required which does not pass Sub-Audio signalling in Rx (in which case, Input1 could be routed from the DISC input with voice and Inband processing set to Input2 from the SIG input).

Similarly, for the output routing, under normal operation, In Tx Mode, Output1 would be routed to MOD1 and Output2 to MOD2. The signals that appear on Output1 and Output2 are defined in the Tx MOD Mode register, $A7 bits14-12.

If the AUDIO output is selected in Tx mode (using b6) it will present the signal that has been routed to Output1. This can be used for “sidetone” when transmitting Inband signalling in 1 or 2-point modulation modes. In Rx mode, the Audio Process is automatically routed to Output1.

An audio output is only available when in Rx or Tx Mode.

8.1.13. Reserved - $B2 write

8.1.14. Reserved - $B3 write

8.1.15. Reserved - $B4 read

8.1.16. AuxADC Threshold Data - $B5 write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADC Sel	High /Low	0	0	0	0	Aux ADC Threshold Data									

b15 AuxADC select 0 = AuxADC1 1 = reserved
b14 high/low select 0 = low threshold 1 = high threshold
b13 *reserved* 0
b12 *reserved* 0
b11 *reserved* 0
b10 *reserved* 0
b9-0 Threshold Data

8.1.17. Modem Address - $B6 write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSK Header Address								0	0	0	0	0	0	0	0

b15 – 8 MSK Header Address
b7 – 0 reserved, clear to 0

8.1.18. Reserved - $BB read

8.1.19. Powerdown Control - $C0 write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SIG Amp	MIC Amp	DISC Amp	IP1 ENA	OP1 ENA	OP2 ENA	MOD1 ENA	MOD2 ENA	AUDIO ENA	BIAS	Reset	Protect	XTAL DIS	IP2 ENA	0	0

b15 SIG Amp Enable 0 = off 1 = enabled
b14 MIC Amp Enable 0 = off 1 = enabled
b13 DISC Amp Enable 0 = off 1 = enabled
b12 Input1 Enable 0 = off 1 = enabled
b11 Output1 Enable 0 = off 1 = enabled
b10 Output2 Enable 0 = off 1 = enabled
b9 MOD1 Enable 0 = off 1 = enabled
b8 MOD2 Enable 0 = off 1 = enabled
b7 AUDIO Enable 0 = off 1 = enabled
b6 BIAS Block Enable 0 = off 1 = enabled
b5 Reset 0 = normal 1 = reset/powersave
b4 Program Block Protect 0 = normal 1 = protected
If cleared, the Program Blocks will be initialised on Power on or Reset. If set, then the Program Blocks will retain their previous contents.
b3 XTAL Disable 0 = enabled 1 = disabled/powersave
Setting this bit effectively stops all signal processing within the device.
b2 Input2 Enable 0 = off 1 = enabled
b1 *reserved* 0 1 = DO NOT USE
b0 *reserved* 0 1 = DO NOT USE

Note: Care should be taken when writing to b5 and b3. These are automatically programmed to an operational state following a power-on (ie: all 0s). Writing a 1 to either b5 or b3 will effectively cause the device to cease all processing activity, including responding to other C-BUS commands (except General Reset, $01).

When b5 is set, the device will be held in reset and all signal processing will cease (including AuxADC operation.

When b3 is set the Xtal is disabled. When b3 is subsequently cleared, it may take some time for the clock signal to become stable, hence care should be taken in using this feature.

8.1.20. Mode Control – $C1 write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	Audio	0	0	Inband Modes				Sub-Audio Mode			Data Mode			IDLE/Rx/Tx	

b15	*reserved*	0	
b14	Audio Processing Enable	0 = off	1 = enabled (uses Input1 source)
b13	*reserved*	0	
b12	*reserved*	0	
b11	Inband Processing Source	0 = Input1	1 = Input2
b10	Audio Tones Enable	0 = off	1 = enabled
b9	*reserved*	0	
b8	DTMF Enable	0 = off	1 = enabled
b7	Sub-Audio Filtering Source	0 = Input1	1 = Input2
b6	CTCSS Enable	0 = off	1 = enabled
b5	DCS Enable	0 = off	1 = enabled
b4	Data Processing Source	0 = Input1	1 = Input2
b3	FFSK 2400 Enable	0 = off	1 = enabled
b2	MSK 1200 Enable	0 = off	1 = enabled
b1-0	Operational mode	00 IDLE 01 Rx 10 Tx 11 reserved	

Changes to the settings of the bits in this register are implemented as soon as they are received over the C-BUS (note that the C-BUS has a potential latency of up to 250µs).

In Tx mode, it is not permissible to set BOTH b3 and b2 at the same time.
In Tx mode, it is only permissible to select ONE of the following at any time:

Audio
Inband Signalling
MSK/FFSK data

Note that if the Audio Processing bit (b14) is set at the same time as an In-band signalling bit in Tx mode, the In-band signal will be subjected to a 6dB gain.

If both b5 and b6 are set, then a “straight-through” path for the External Sub-Audio signal is provided – this has an essentially flat response from approximately 10Hz to 2.7kHz. In Tx mode, Input2 should be selected.

It is essential that changes to the Program Blocks and the Audio Control register are completed before entering Rx or Tx mode.

The following other registers or bits can be changed as appropriate (Note: not all possible changes are appropriate), whilst the device is in Tx or Rx mode:

- Analogue Output Gain register ($B0)
- AuxADC and Tx MOD Mode register ($A7)
- Input Gain and Output Signal Routing register ($B1)
- Power Down Control register ($C0)
- Tx Inband Tones register ($C3)
- Modem Control register ($C7) bit 9 only, as described in section 8.1.24
- Tx Data registers ($CA and $CB)
- Audio Tone register ($CD)
- Interrupt Mask register ($CE)

In Rx mode, as certain FFSK bit patterns can mimic Inband tones, the Inband receiver is temporarily disabled when an FFSK frame sync is detected. If using sized packets (Formats 1, 4 and 5) the CMX148 will automatically restore Inband tone detection when the received message has ended. If using unsized packets (Formats 0, 2 and 3) the host must monitor the received data and restore Inband tones (by setting bits 15, 11, 10, 9 and 8, as required) when it has detected the end of data.

8.1.21. Audio Control – $C2 write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Scra-mble	Comp	Emph	12k5	25k	HPF	0	0	0	0	0	0	0	0	0	0

b15 Audio Scrambling Enable 0 = off 1 = enabled
b14 Audio Compandor Enable 0 = off 1 = enabled
b13 Audio Pre/De-emphasis 0 = off 1 = enabled[3]
b12 Audio 12.5kHz Filter Enable 0 = off 1 = enabled
b11 Audio 25kHz Filter Enable 0 = off 1 = enabled
b10 Audio 300Hz HPF Enable 0 = off 1 = enabled

b9-0 *reserved*

8.1.22. Tx Inband Tones - $C3 write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	twist	sgl	Tx DTMF tone			

b15-6 *reserved*, clear to 0.
b5 DTMF Twist 0 = normal 1 = -2dB of twist applied to the lower DTMF tone.
b4 DTMF Single Tone 0 = normal 1 = Single Tone, see Table 2 DTMF Tone Pairs
b3-0 DTMF tone value – see Table 2 DTMF Tone Pairs

See section 7.8.1 and 8.1.26.

[3] In order to pre-emphasise the MSK/FFSK data, Program Block P1.0 bit 11 should be set.

8.1.23. Status – $C6 read

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IRQ	res	res	DTMF	res	res	Aux ADC2	Aux ADC1	Data End	Data RDY	Data CRC	2k4	1k2	res	res	PRG

b15 IRQ

Changes in the Status register will cause this bit to be set to 1 if the corresponding interrupt mask bit is enabled. An interrupt request is issued on the IRQN pin when this bit is 1 and the IRQ MASK bit (b15 of Interrupt Mask register, $CE) is set to 1.

b14 *reserved*

b13 *reserved*

b12 DTMF event

A valid DTMF tone has been detected and can be read from the Tone Status register, $CC.

b11 *reserved*

b10 *reserved*

b9 AuxADC2 Threshold change

AUXADC2 signal has just gone above the high threshold or has just gone below the low threshold. The AuxADC2 data register $AA should be read to determine the exact cause.

b8 AuxADC1 Threshold change

AUXADC1 signal has just gone above the high threshold or has just gone below the low threshold The AuxADC1 data register $A9 should be read to determine the exact cause.

b7 Data End

Rx mode: this is only valid when bit 6 'Data Ready' is set. It is set when receiving the last part of a sized MSK/FFSK Frame or Frame Format 1 (frame head only) message, bit 5 (CRC) will also be updated at this time. When the host detects bit 7 is set it may power down the CMX148 or set the CMX148 to transmit or receive new information as appropriate.

Tx mode: this will be set when the last bit of MSK/FFSK data has been transmitted. Note; when using Formats 0, 2 or 3 (see section 7.9) this bit will only be set if bit 9 of the Modem Control register ($C7) is set at the appropriate time. After allowing a short time delay associated with the external components and radio circuitry, the host may power down the CMX148 and transmitter or set the CMX148 to transmit or receive new information as appropriate.

b6 Data Ready

Tx mode: indicates that new transmit data is required.

Rx mode: received data is ready to be read.

For continuous transmission or reception of information, a data transfer should be completed within the time appropriate for that data (see Table 5).

b5 Data CRC received

Bit 5 will be set after receiving an incorrect CRC portion of a sized Data Block (Frame Formats 4 and 5).

b4 2400 FSK data received

b3 1200 MSK data received

Bits 4 and 3 indicate the received data rate after a valid data sequence has been received. If Frame Format 0 is enabled these bits will be set on detection of a valid frame sync pattern (the Sync data is available in the RxData register). If Frame Format 0 is disabled then these bits will only be set when a Frame Head is detected with a correct CRC.

b2 *reserved*

b1 *reserved*

b0 PRG flag

When set to 1, this bit indicates that the Programming Register, $C8, is available for the host to write to it. Cleared by writing to the Programming Register, $C8.

Bits 2 to 15 of the Status register are cleared to 0 after the Status register is read.

The data in this register is not valid if bit 5 of the Power Down Control register, $C0 is set to 1.

8.1.24. Modem Control - $C7 write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SynC	SynD	SynT	0	0	En_ RAW	Last Tx Data	Inter- leave	MSK/FFSK Message Format			0	0	User Bit	Scramble Seed	

This register configures the way the CMX148 handles MSK data in Tx and Rx modes.

b15 SynC detect (MSK/FFSK) 0 = off 1 = enabled
b14 SynD detect (MSK/FFSK) 0 = off 1 = enabled
b13 SynT detect (MSK/FFSK) 0 = off 1 = enabled
note: SynC, SynD and SynT patterns are defined in Program Block P0.0-3
b12 *reserved* 0
b11 *reserved* 0
b10 En_RAW: 0 = data packetising on 1 = raw data mode
This selects the raw or formatted mode for type 0 MSK/FFSK or DSC data.
MSK/FFSK Receive mode:
b10 = 1: device will look for the programmed Frame Sync. pattern, raise an interrupt (if enabled) and decode the following data 16 bits at a time, making them available in Rx Data 1 register ($C5).
b10 = 0: device will look for a complete Frame Head before raising an interrupt (if enabled) and then decode the following data in accordance with the received message format. The Frame Head Control Field bytes, user data and any CRC will be presented in the appropriate Rx Data registers ($C5 and $C9).
MSK/FFSK Transmit mode:
b10 = 1: device will transmit data 16 bits at a time from Tx Data 1 register ($CA). Bit and frame sync pattern generation and all formatting of the data have to be performed by the host in this case.
b10 = 0: device will transmit the programmed bit and frame sync patterns followed by a Frame Head containing the information supplied in bits 7–0 of this register and the 2 bytes in Tx Data 1 register ($CA). Subsequently the host must supply data when requested to complete the transmission of the Frame Head and Data Block.
b9 Last Tx data:
This is only valid when transmitting data with Formats 0, 2 or 3 in MSK/FFSK modes and indicates to the CMX148 that it can cease modulation. The host must set this bit to 1 immediately after the interrupt for 'load more data' occurs ($C6 bit 6). In receive, or when transmitting other message formats, this bit must be cleared to 0.
b8 Interleave: 0 = off 1 = on
This bit selects if Frame Headers in MSK/FFSK modes will be interleaved or not.

b7-5 Data Format:

b7	b6	b5	Format	Message Format
0	0	0	0	Raw Data (En_RAW = 1)
0	0	1	1	Frame Head only, no payload
0	1	0	2	Frame Head + Unsized payload of raw 16 bit words
0	1	1	3	Frame Head + Unsized payload with FEC
1	0	0	4	Frame Head + Sized payload with FEC + CRC
1	0	1	5	Frame Head + Sized payload with FEC + CRC + interleaving
All other patterns			-	reserved

b4 *reserved*, clear to 0.
b3 *reserved*, clear to 0.
b2 User bit.
May be freely used by the host in MSK/FFSK modes. This bit has no effect on the message format or encoding and will be reported in the Rx Data 1 register for the receiving host to use as appropriate. This bit could be used to indicate a special message, e.g. one containing handset or channel set-up information.

b1-0 Scrambler Seed Select.

Used when transmitting user-data in MSK/FFSK modes. The receiving CMX148 will automatically de-scramble the received data block using the setting indicated in the received Frame Head. The receiving host can read the scrambler setting (0-3) used by the transmitter via Rx Data 1 register ($C5: bits 1,0) and may use this when returning messages. See also section 7.9.7.

b1	b0	**MSK Data Scrambling Setting**
0	0	Standard Scrambling (seed = $FFFF)
0	1	Scramble Seed1 (see P0.4-5)
1	0	Scramble Seed2 (see P0.6-7)
1	1	No Scrambling (seed = $0000)

8.1.25. Programming Register – $C8 write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Program Block Address				Program Block Data											

See section 8.2 for a definition of Program Block operation.

8.1.26. Rx Data 1 and 2 - $C5 and $C9 read

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
$C5	Rx Data Byte 0 (Frame Head: Address byte)								Rx Data Byte 1 (Frame Head: Format byte)							
$C9	Rx Data Byte 2* (Frame Head: Size/user byte)								Rx Data Byte 3* (Frame Head: CRC byte)							

*$C9 is used when receiving Format 4 or 5 and Frame Heads, the Rx buffer is effectively 4 bytes long in these cases.

These 2 words hold the most recent 2 bytes (Byte 0 and 1) or 4 bytes (Bytes 0, 1, 2 and 3) of MSK data decoded. Received data is continuous, if the data is not read before the next data is received the current data will be over-written.

After receiving a Frame Head the host can read the Address and Format bytes for the following packet from Rx Data 1 register ($C5) and the size/user byte and the Frame Head Checksum A byte from Rx Data 2 register ($C9). The Format byte corresponds to the settings of b0-7 of the Modem Control Register ($C7) used by the transmitting device. The CMX148 will read the size and message formatting information and if the message is of Format 3, 4 or 5 (see section 7.9) it will start the automatic decoding of the following data; descrambling, de-interleaving, decoding error correction bytes, stripping out pad bytes, calculating and checking Checksum B as required. The only task the host need perform during the reception of formatted frames is to read out data when it is ready.

8.1.27. Tx Data 1 and 2 - $CA and $CB write

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
$CA	Tx Data Byte 0 (Frame Head: Address byte)								Tx Data Byte 1 (Frame Head: Size/user byte)							
$CB	Tx Data Byte 2*								Tx Data Byte 3*							

*Register $CB is only used for Format 4 or 5, the Tx buffer is effectively 4 bytes long in these cases.

These 2 words hold next 2 bytes (Byte 0 and 1) or 4 bytes (Bytes 0, 1, 2 and 3) of MSK/FFSK data to be transmitted. Outgoing data is continuous, if new data is not provided before the current data has been transmitted the current data will be re-transmitted, until new data is provided. Transmission of current data will be completed before transmission of newly loaded data begins. See section 7.8.2.

When transmitting formatted MSK/FFSK data packets, the host must first load the correct Address and size/user bytes for the following packet into TxData 1 register ($CA). The CMX148 will automatically add the Control byte, based on the settings in Modem Control register ($C7), and calculate the Frame Head Checksum A byte. The CMX148 will read the Size and Message formatting information and automatically format all following data; adding error correction bytes, adding pad bytes, interleaving, scrambling and calculating and appending Checksum B as required. The only task the host need perform during the transmission of a frame is to download new data when it is required.

Note: These 2 words must be written separately, i.e. Two 16-bit C-BUS transactions.

8.1.28. Tone Status - $CC read

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Device Identification Code															
x	DTMF Tone Detected				DT	x	x	x	x	x	x	x	x	x	x

After power-on or General Reset, this register will contain the Device Identification code ($1480) related to this particular device. The host µC may use this to confirm that the device is in its correct operational mode before attempting to actively use the device.

In normal operation, this word holds the current status of the CMX148 Inband tone sections. This word should be read by the host after an interrupt caused by an Inband tone event. In Tx mode this register will be cleared to 0.

b15 *reserved* – ignore this bit.

b10 set if b14-11 represent DTMF tone.

b14-11 Detected Inband frequency; identifies the frequency by its position in Table 2 DTMF Tone Pairs. A change in the state of bits 14 to 10 will cause bit 12 of the Status register ($C6), to be set to 1.

b9-0 *reserved* – ignore these bits.

8.1.29. Audio Tone - $CD: write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	Audio Tone Frequency											
0	0	1	0	Audio Tone Level											
0	1	0	0	Rx Voice Level											
0	1	1	0	Output1 Fine Gain (also see P4.2)											
1	0	0	0	Output2 Fine Gain (also see P4.3)											
1	0	1	0	Tx Voice Level Multiplier											
1	0	1	1	*reserved*											
1	1	0	0	MOD1 and MOD2 Fine Attenuation											
1	1	0	1	Sub Audio Tx Level											
1	1	1	0	*reserved*											
1	1	1	1	*reserved*											
				All other values reserved											

Bits 15-12 determine how the remaining bit fields will be interpreted:

0000_2:

When the appropriate bits of the Mode Control register ($C1, b10) are set, an audio tone will be generated with the frequency set by bits (11-0) of this register in accordance with the formula below. If bits 11-0 are programmed with 0, no tone (i.e. V_{BIAS}) will be generated when the Audio Tone is enabled.

Frequency = Audio Tone (i.e. 1Hz per LSB)

The Audio Tone frequency should only be set to generate frequencies from 300Hz to 3000Hz.

The host should disable other audio band signalling and set the correct audio routing before generating an audio tone and re-enable signalling and audio routing on completion of the audio tone. The timing of intervals between these actions is controlled by the host µC.

This register may be written to whilst the audio tone is being generated, any change in frequency will take place after the end of the C-BUS write to this register. This allows complex sequences (e.g. ring or alert tunes) to be generated for the local speaker (Tx or Rx via the AUDIO pin) or transmitted signal (Tx via the MOD1/MOD2 pins).

0010_2:

The Audio Tone Level may be attenuated by the value written to b11-0. The value of $FFF is equivalent to x1 ie: 0dB (use with care as high values may result in signal “clipping”). Note that this adjustment will affect ALL signals generated by the In-Band signalling block (DTMF, MSK/FFSK, Audio Tone). This register operates in parallel with P1.0, so that the last register written ($CD with value $2xxx or $C8 P1.0 with value $Dxxx) will set the attenuation. With the Audio Tone ($CD) register, however, the level can be adjusted “on-the-fly”, thus avoiding the need to drop back into IDLE mode. Approximate values for 0.2dB attenuation steps are shown in .

0100_2:

In Rx mode, the Voice Level may be attenuated by the value written to b11-0. The value of $FFF is equivalent to x1. Note that this adjustment will only affect signals in the Voice processing path as enabled by the Mode Control register ($C1, b14). This allows the Voice level to be adjusted “on-the-fly”, without needing to drop back into IDLE mode, and offers a “fine gain” volume control when used in conjunction with the coarse gain control (b3-0) of the Audio Output Gain register ($B0). Approximate values for 0.2dB steps are shown in Table 7.

b11-0 value (hex)	Attenuation (dB)	b11-0 value (hex)	Attenuation (dB)
FFF	0	D50	1.6
F90	0.2	CF0	1.8
F40	0.4	CB0	2.0
EE0	0.6	C60	2.2
EA0	0.8	C20	2.4
E50	1.0	BF0	2.6
DE0	1.2	BA0	2.8
DA0	1.4	B60	3.0

Table 7 Audio Tone Register - Attenuation Steps

0110_2:

The Output1 level may be attenuated by the value written to b11-0. The value of $FFF is equivalent to x1. This register operates in parallel with P4.2 and allows the level to be adjusted “on-the-fly”, without needing to drop back into IDLE mode. Approximate values for 0.2dB attenuation steps are shown in Table 7.

1000_2:

The Output2 level may be attenuated by the value written to b11-0. The value of $FFF is equivalent to x1. This register operates in parallel with P4.3 and allows the level to be adjusted “on-the-fly”, without needing to drop back into IDLE mode. Approximate values for 0.2dB attenuation steps are shown in Table 7.

1010_2:

This sets the value of the Tx Voice Level Multiplier at the output of the Tx limiter stage. This can be useful in situations where it has been necessary to use a small limiting threshold and still maintain an acceptable level at the MOD outputs. The default state is x1. Bits 11 - 3 should be set to 0.

b2	b1	b0	Tx Voice Level Multiplier
0	0	0	x1
0	0	1	x2
0	1	0	x4
0	1	1	x8
1	0	0	x16
1	0	1	x32

1100_2:

MOD1 and MOD2 fine attenuation controls. These bits attenuate MOD1 and MOD2 signals in 0.2dB steps, as shown below, and may be changed whilst the device is in Tx or Rx mode. Bits 11 - 8 should be set to 0. These controls operate in conjunction with the coarse gain controls of the Analogue Output Gain register ($B0). Additional gain and offset control of Output1 and Output2 signals, which precedes the MOD1 and MOD2 fine gain controls, is provided by the settings in register $CD:0110 and $CD:1000. These additional gain and offset controls operate in parallel with the Program Block registers P4.2 – 4.5.

b3	b2	b1	b0	MOD1 Fine Output Attenuation
b7	b6	b5	b4	MOD2 Fine Output Attenuation
0	0	0	0	0dB
0	0	0	1	0.2dB
0	0	1	0	0.4dB
0	0	1	1	0.6dB
0	1	0	0	0.8dB
0	1	0	1	1.0dB
0	1	1	0	1.2dB
0	1	1	1	1.4dB

b3	b2	b1	b0	MOD1 Fine Output Attenuation
b7	**b6**	**b5**	**b4**	**MOD2 Fine Output Attenuation**
1	0	0	0	1.6dB
1	0	0	1	1.8dB

1101_2:

The Sub Audio Tx level may be attenuated by the value written to b11-0. The value of $FFF is equivalent to x1. This register operates in parallel with P2.0 and allows the level to be adjusted “on-the-fly”, without needing to drop back into IDLE mode. Approximate values for 0.2dB attenuation steps are shown in Table 7.

8.1.30. Interrupt Mask - $CE write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IRQ	0	0	DTMF	0	0	Aux ADC2	Aux ADC1	Data End	Data RDY	Data CRC	2k4	1k2	0	0	PRG

Bit	Value	Function
15	1	Enable selected interrupts
	0	Disable all interrupts (IRQN pin not activated)
14	0	*reserved*
13	0	*reserved*
12	1	Enable interrupt when a valid DTMF tone is detected
	0	Disabled
11	0	*reserved*
10	0	*reserved*
9	1	Enable interrupt when the Aux ADC 2 status bit changes
	0	Disabled
8	1	Enable interrupt when the Aux ADC 1 status bit changes
	0	Disabled
7	1	Enable interrupt when MSK/FFSK data transmission has ended
	0	Disabled
6	1	Enable interrupt when an MSK/FFSK data transfer is required
	0	Disabled
5	1	Enable interrupt when an incorrect CRC portion of a sized Data Block is received
	0	Disabled
4	1	Enable interrupt when valid 2400baud data is detected
	0	Disabled
3	1	Enable interrupt when valid 1200baud data is detected
	0	Disabled
2	1	*reserved*
1	1	*reserved*
0	1	Enable interrupt when PRG flag bit of the Status register changes from 0 to 1 (see Programming register $C8)
	0	Disabled

8.1.31. Reserved - $CF write

This C-BUS address is allocated for production testing and must not be accessed in normal operation.

8.2. Programming Register Operation

In order to support radio systems that may not comply with the default settings of the CMX148, a set of Program Blocks is available to customise the features of the device. It is envisaged that these blocks will only be written to following a power-on of the device and hence can only be accessed while the device is in IDLE mode. Access to these blocks is via the Programming register ($C8).

All other interrupt sources should be disabled and the AuxADCs switched off while loading the Program Blocks.

The Programming register should only be written to when the PRG flag ($C8 bit 0) of the Status register is set to 1, the Rx and Tx modes are disabled (bits 0 and 1 of the Mode Control register both 0) and the AuxADC is disabled.

The PRG flag is cleared when the Programming register is written to by the host. When the corresponding programming action has been completed (normally within 250µs) the CMX148 will set the flag back to 1 to indicate that it is now safe to write the next value. The Programming register must not be written to while the PRG flag bit is 0. Programming is performed by writing a sequence of 16-bit words to the Programming register in the order shown in the following tables. Writing data to the Programming register MUST be performed in the order shown for each of the Program Blocks, however the order in which the blocks are written is not critical. If later words in a block do not require updating, the user may stop programming that block when the last change has been performed. e.g. If only 'Fine Output Gain 1' needs to be changed the host will need to write to Program Block P4.0, P4.1 and P4.2 only.

The user must not exceed the defined word counts for each block.

The internal pointer for each Program Block write is initialised by setting b15 to 1. b14-12 are then used to select the particular Program Block in use as shown in Table 8. Subsequent writes to the Programming register (with b15 cleared to 0) will increment the pointer until the end of the Program Block is reached. Program Block 3 has an additional feature to facilitate RAMDAC programming, where the first eleven entries of the block may be skipped by setting both b15 and b10 to 1 to initialise the pointer directly to the start of the RAMDAC table.

Table 8 Program Block Selection

b15	b14	b13	b12		Bit field (max)
1	0	x	x	Select Block 4	14
1	1	0	0	Select Block 0	12
1	1	0	1	Select Block 1	12
1	1	1	0	Select Block 2	12
1	1	1	1	Select Block 3	12

Once the final write to the Programming register has been executed, a final check of the PRG flag should be performed before returning to normal operation.

8.2.1. Program Block 0 – Modem Configuration

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P0.0	1	1	0	0	Pre	0			MSK/FFSK Frame SynC LSB							
P0.1	0	1	0	0	0				MSK/FFSK Frame SynC MSB							
P0.2	0	1	0	0	0				MSK/FFSK Frame SynD LSB							
P0.3	0	1	0	0	0				MSK/FFSK Frame SynD MSB							
P0.4	0	1	0	0	0				Scramble Seed 1 LSB							
P0.5	0	1	0	0	0				Scramble Seed 1 MSB							
P0.6	0	1	0	0	0				Scramble Seed 2 LSB							
P0.7	0	1	0	0	0				Scramble Seed 2 MSB							
P0.8	0	1	0	0	0				MSK/FFSK Bit Sync LSB							
P0.9	0	1	0	0	0				MSK/FFSK Bit Sync MSB							

Default values:

P0.0	$C023	P0.5	$4000
P0.1	$40CB	P0.6	$4000
P0.2	$4033	P0.7	$4000
P0.3	$40B4	P0.8	$4055
P0.4	$4000	P0.9	$4055

This initiates the device with the MSK frame sync pattern of $CB23 and bit sync of alternate 1s and 0s.

$C8 (P0.0-3) MSK Frame Sync

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P0.0	1	1	0	0	Pre	0			MSK/FFSK Frame SynC LSB							
P0.1	0	1	0	0	0				MSK/FFSK Frame SynC MSB							
P0.2	0	1	0	0	0				MSK/FFSK Frame SynD LSB							
P0.3	0	1	0	0	0				MSK/FFSK Frame SynD MSB							

Bits 7 to 0 set the Frame Sync pattern used in Tx and Rx MSK data. Bit 7 of the MSB is compared to the earliest received data. Note that SynT is the inverse pattern of SynC.

Bit 11 of P0.0 enables pre-emphasis of the transmitted MSK/FFSK/FSK signal (default = 0, disabled).

$C8 (P0.4-7) Scramble Seed 1 and 2

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P0.4	0	1	0	0	0				Scramble Seed 1 LSB							
P0.5	0	1	0	0	0				Scramble Seed 1 MSB							
P0.6	0	1	0	0	0				Scramble Seed 2 LSB							
P0.7	0	1	0	0	0				Scramble Seed 2 MSB							

These bits set the scramble seed used on all data bits following a Frame Head. If $0000 is programmed as the seed then no scrambling will occur when selected. If either programmable scramble seeds are selected, both the transmit and receive devices must use the same seed pattern for data to be transferred correctly.

$C8 (P0.8-9) MSK Bit Sync

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P0.8	0	1	0	0	0				MSK/FFSK Bit Sync LSB							
P0.9	0	1	0	0	0				MSK/FFSK Bit Sync MSB							

This bit pattern is used when transmitting the bit sync portion of a Frame Head.

8.2.2. Program Block 1 – Inband Tone Setup

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P1.0	1	1	0	1	Audio Band Tones/Data Tx Level											Emph

Default value: P1.0: $D800

$C8 (P1.0) Audio Band Tones Tx Level

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P1.0	1	1	0	1	Audio Band Tones/Data Tx Level											Emph

Bits 11 (MSB) to 1 (LSB) set the transmitted Inband tone, Audio Tone and MSK/FFSK signal level (p-p) with a resolution of $AV_{DD}/2048$ per LSB (1.611mV per LSB at AV_{DD}=3.3V). Valid range for this value is 0 to 1536 – use with care as higher values may result in signal "clipping".

Bit 0 controls Inband tone de-emphasis. When Inband tones are enabled in the Mode Control register ($C1), de/pre-emphasis is enabled in the Audio Control register ($C2) and this bit (b0) is set to 1; signals going to the Inband tone detector are de-emphasised in accordance with Figure 9 of the datasheet. This combination of settings should only be used in Rx mode. If this bit is set, then in Tx mode, the user is advised to clear the de/pre-emphasis bit in the Audio Control register ($C2). This has no effect on DTMF signals.

8.2.3. Program Block 2 – CTCSS and DCS Setup

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P2.0	1	1	1	0	CTCSS and DCS Tx Level											
P2.1	0	1	1	0	*reserved* - 0											
P2.2	0	1	1	0	*reserved* - 0											
P2.3	0	1	1	0	*reserved* - 0											
P2.4	0	1	1	0	*reserved* - 0											
P2.5	0	1	1	0	0	0	0	0	0	0	0	0	0	0	HPF	
P2.6	0	1	1	0	*reserved* - 0											

Default values:

P2.0	$E800	P2.3	$6000
P2.1	$6000	P2.4	$6000
P2.2	$6000	P2.5	$6000
		P2.6	$6000

$C8 (P2.0) CTCSS and DCS Tx Level

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P2.0	1	1	1	0	CTCSS and DCS Level											

Bits 11 (MSB) to 0 (LSB) set the transmitted external CTCSS or DCS sub-audio signal level (p-p) with a resolution of AV_{DD}/16384 per LSB (0.201mV per LSB at AV_{DD}=3.3V, giving a range 0 to 824.8mV p-p)[4].

$C8 (P2.1 to 2.4) reserved

$C8 (P2.5) 300Hz High-Pass Filter Select

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P2.5	0	1	1	0	0	0	0	0	0	0	0	0	0	0	HPF Select	

The HPF select field determines the cut-off point of the 300Hz Audio High-pass filter:

00 = 300Hz (default)
01 = 280Hz
10 = 320Hz
11 = reserved

$C8 (P2.6) Reserved – do not access

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P2.6	0	1	1	0	reserved – set to $000											

[4] Assuming a 1648mV pk-pk input signal with Input and Output Gains set for 0dB.

8.2.4. Program Block 3 – AuxDAC, RAMDAC and Clock Control

This block is divided into two sections to facilitate loading the RAMDAC buffer. Set bit 15 to 1 and clear bit 10 to 0 to start the loading sequence from P3.0. Set both bits 15 and 10 to start the loading sequence from P3.11 (RAMDAC data).

The Internal clk dividers only require modification if a non-standard XTAL frequency is used (see Table 1)

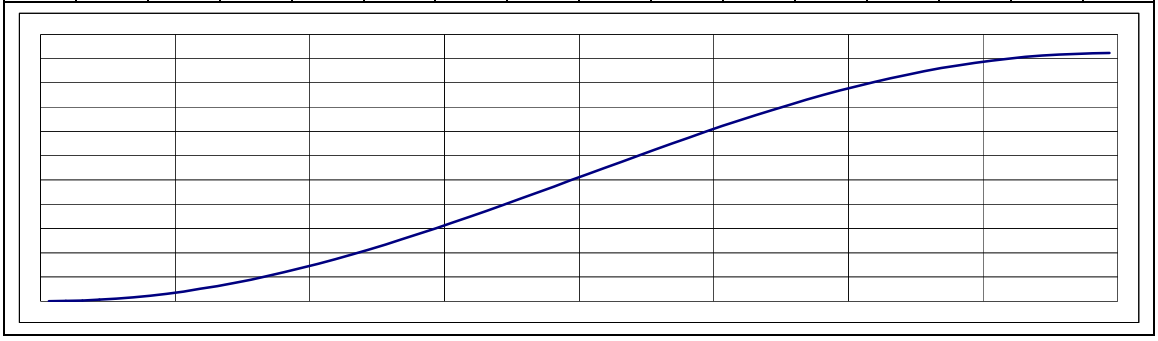
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P3.0	1	1	1	1	0	0	0	0	AuxADC1 Average Counter							
P3.1	0	1	1	1	0	0	0	0	reserved							
P3.2	0	1	1	1	GP Timer value in IDLE mode											
P3.3	0	1	1	1	VCO output and AUX clk divide in IDLE mode											
P3.4	0	1	1	1	Ref clk divide in Rx or Tx mode											
P3.5	0	1	1	1	PLL clk divide in Rx or Tx mode											
P3.6	0	1	1	1	VCO output and AUX clk divide in Rx or Tx mode											
P3.7	0	1	1	1	0	0	0	0	Internal ADC / DAC clk divide in Rx or Tx mode							
P3.8	0	1	1	1	0	0	0	0	ADC Internal Control 1							
P3.9	0	1	1	1	0	0	0	0	ADC Internal Control 2							
P3.10	0	1	1	1	0	0	0	0	0	0	0	0	ADC Internal Control 3			
P3.11	1	1	1	1	0	1	User Defined RAMDAC data 0									
P3.xx	0	1	1	1	0	1	User Defined RAMDAC data xx									
P3.74	0	1	1	1	0	1	User Defined RAMDAC data 63									

Default Values:

P3.0	$F000
P3.1	$7000
P3.2 - P3.7:	see Table 1
P3.8	$7000
P3.9	$7101
P3.10	$7002
P3.11 - P3.74:	see Table 9

Table 9 RAMDAC Values

Default RAMDAC Contents After Reset (hex)															
0 000	1 001	2 003	3 006	4 00A	5 010	6 017	7 01F	8 028	9 033	10 03E	11 04B	12 059	13 068	14 078	15 089
16 09A	17 0AD	18 0C1	19 0D5	20 0EA	21 100	22 116	23 12D	24 145	25 15D	26 175	27 18E	28 1A7	29 1C0	30 1D9	31 1F3
32 20C	33 226	34 23F	35 258	36 271	37 28A	38 2A2	39 2BA	40 2D2	41 2E9	42 2FF	43 315	44 32A	45 33E	46 352	47 365
48 376	49 387	50 397	51 3A6	52 3B4	53 3C1	54 3CC	55 3D7	56 3E0	57 3E8	58 3EF	59 3F5	60 3F9	61 3FC	62 3FE	63 3FF



8.2.5. Program Block 4 – Gain and Offset Setup

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P4.0	1	0	Fine Input Gain 1													
P4.1	0	0	Fine Input Gain 2													
P4.2	0	0	Fine Output Gain 1													
P4.3	0	0	Fine Output Gain 2													
P4.4	0	0	Output1 Offset Control													
P4.5	0	0	Output2 Offset Control													
P4.6	0	0	Ramp Rate Control													
P4.7	0	0	Limiter Setting													
P4.8	0	0	Scrambler Inversion Frequency													
P4.9	0	0	Audio Filter Sequence													
P4.10	0	0	*reserved*													
P4.11	0	0	InputAGC Threshold Level													

Default values:

P4.0	$8000	P4.6	$0000
P4.1	$0000	P4.7	$3FFF
P4.2	$0000	P4.8	$119A
P4.3	$0000	P4.9	$001B
P4.4	$0000	P4.10	$0608
P4.5	$0000	P4.11	$0FFF

$C8 (P4.0) Fine Input Gain 1 and Fine Input Gain 2

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P4.0	1	0	Fine Input Gain 1 (unsigned integer)													
P4.1	0	0	Fine Input Gain 2 (unsigned integer)													

Gain = 20 × log([32768-IG]/32768)dB. IG is the unsigned integer value in the 'Fine Input Gain' field.

Fine input gain adjustment should be kept within the range 0 to -3.5dB. This adjustment occurs after the coarse input gain adjustment (register $B1).

$C8 (P4.2-3) Fine Output Gain 1 and Fine Output Gain 2

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P4.2	0	0	Fine Output Gain 1 (unsigned integer)													
P4.3	0	0	Fine Output Gain 2 (unsigned integer)													

Gain = 20 × log([32768-OG]/32768)dB. OG is the unsigned integer value in the 'Fine Output Gain' field.

Fine output gain adjustment should be kept within the range 0dB to -3.5dB. This adjustment occurs before the coarse output gain adjustment (register $B0). Alteration of Fine Output Gain 1 will affect the gain of both MOD1 and AUDIO outputs.

$C8 (P4.4-5) Output1 Offset and Output2 Offset

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P4.4	0	0	2's complement Offset for MOD1, resolution = AV_{DD} / 65536 per LSB													
P4.5	0	0	2's complement Offset for MOD2, resolution = AV_{DD} / 65536 per LSB													

The programmed value is subtracted from the output signal. Can be used to compensate for inherent offsets in the output path via MOD1 (Output1 Offset) and MOD2 (Output2 Offset). It is recommended that the offset correction is kept within the range +/-50mV. This adjustment occurs before the coarse output gain adjustment (register $B0), therefore an alteration to the latter register will require a compensation to be made to the output offsets.

$C8 (P4.6) Ramp Rate Control

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P4.6	0	0	Ramp Rate Up Control (RRU)							Ramp Rate Down Control (RRD)						

The ramp-up and ramp-down rates can be independently programmed. The ramp rates apply to all the analogue output ports. They only affect those ports being turned on (ramp-up) or turned off (ramp down). The ramp rates should be programmed before ramping any outputs.

Time to ramp-up to full gain = (1 + RRU) × 1.333ms
Time to ramp down to zero gain = (1 + RRD) × 1.333ms

Ramp up starts from when the transmit mode starts (Mode Control Register bit 1 set = 1). Ramp down starts from when transmit mode is turned off (Mode Control Register bit 1 cleared = 0).

$C8 (P4.7) Transmit Limiter Control

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P4.7	0	0	Limiter Setting													

This unsigned number sets the clipping point (maximum deviation from the centre value) for the MOD1 and MOD2 pins. The maximum setting ($3FFF) is $V_{BIAS} \pm (AV_{DD}/2)$ i.e. output limited from 0 to AV_{DD}.

For an AV_{DD} of 3.3V, the resolution is approx. 0.3mV per LSB.

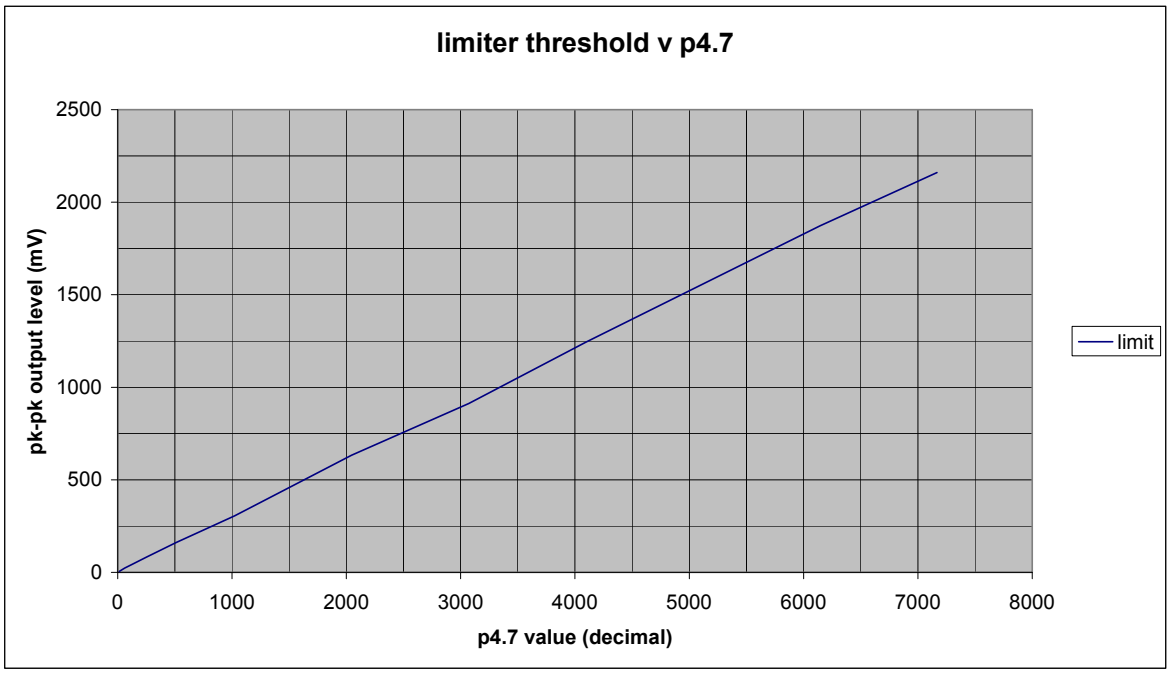


Figure 20 Limiter Values

The limiter is set to maximum following a C-BUS Reset or a Power-Up Reset. The levels of internally generated signals may need to be adjusted by setting appropriate transmit levels to avoid un-intentional limiting.

$C8 (P4.8) Scrambler Inversion Frequency

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P4.8	0	0	Scrambler Inversion Frequency = f / 0.7324													

This unsigned hex number sets the inversion frequency for the Voice Scrambler and de-Scrambler (Default is 3300Hz).

$C8 (P4.9) Audio Filter Sequence

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P4.9	0	0	Limit	src	InputAGC				Pre-emp		Comp		Scramble		300Hz	

b13 sets the position of the Limiter in the Audio Processing chain. The default is a soft limiter function; setting this bit provides a hard limiter function.

b12 sets the source of the reference signal when the InputAGC function is active.

0 = Audio input
1 = Pre-emphasis output

b11-8 control the hardware InputAGC function and its release timer for voice/audio signals on Input1 in 64ms steps:

0000	InputAGC off
0001	InputAGC on, release time = 64ms
0010	InputAGC on, release time = 128ms
0011	InputAGC on, release time = 196ms
0100	InputAGC on, release time = 256ms
0101	InputAGC on, release time = 320ms
- - - -	- -
1111	InputAGC on, release time = 960ms

b7-0 set the order of the Audio Filter processing. This feature can be used to optimise the signal to noise performance of particular radio hardware designs. Each filter/process block can be specified in any order. Each two-bit field specifies the order in which the process will be executed in Tx mode, therefore it is imperative that each set of bit fields be different. The reverse sequence is used in Rx mode. The Voice Filter and Soft Limiter will always be implemented as the final block in the Tx sequence.

The default settings are:

- Pre-emp: 00
- Compress: 01
- Scramble: 10
- 300Hz HPF: 11

which will implement the line-up as shown in Figure 21 and Figure 22.

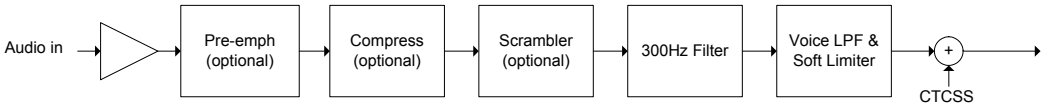


Figure 21 Default Tx Audio Filter Line-up

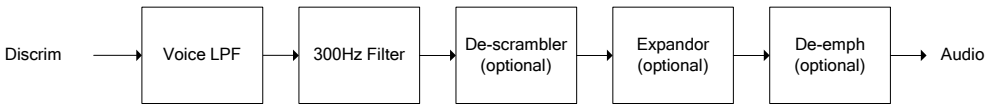


Figure 22 Default Rx Audio Filter Line-up

An alternative, preferred, line-up is shown in Figure 23 and Figure 24 for the following settings (P4.9 = $004B):

- Pre-emp: 01
- Compress: 00
- Scramble: 10
- 300Hz HPF: 11

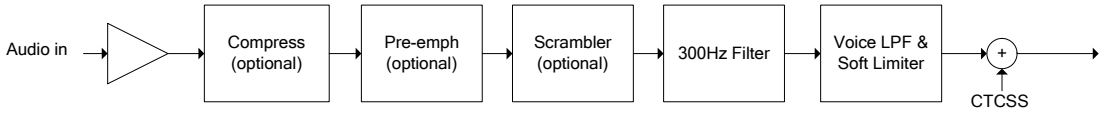


Figure 23 Preferred Tx Audio Filter Line-up

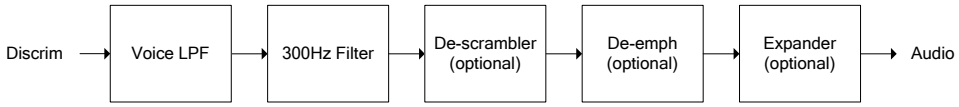


Figure 24 Preferred Rx Audio Filter Line-up

$C8 (P4.10) Reserved

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P4.10	0	0	*reserved* – set to $0608													

Reserved – set to $0608

$C8 (P4.11) InputAGC Threshold Level

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P4.11	0	0	Threshold Setting, resolution = AV_{DD}/16384 per LSB													

This unsigned number sets the threshold point (maximum deviation from the centre value) for the Input AGC function, where the input gain will be stepped to avoid exceeding the specification limits.

The threshold is set to half of full-scale ($0FFF = $V_{BIAS} \pm (AV_{DD}/4)$) following a C-BUS Reset or a Power-Up Reset.

8.2.6. Initialisation of the Program Blocks

Removal of the Signal Processing block from reset (Power-down register, $C0, b5 1→ 0), with b4 kept low (= 0), will cause all of the Program Blocks (P0 – P4) to be reset to their default values.

9. Performance Specification

9.1. Electrical Performance

9.1.1. Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

	Min.	Max.	Unit
Supply: DV_{DD}- DV_{SS}	−0.3	4.5	V
AV_{DD}- AV_{SS}	−0.3	4.5	V
Voltage on any pin to DV_{SS}	−0.3	DV_{DD} + 0.3	V
Voltage on any pin to AV_{SS}	−0.3	AV_{DD} + 0.3	V
Current into or out of any power supply pin (excluding V_{BIAS}) (i.e. V_{DEC}, AV_{DD}, AV_{SS}, DV_{DD}, DV_{SS})	−30	+30	mA
Current into or out of any other pin	−20	+20	mA
Voltage differential between power supplies:			
DV_{DD} and AV_{DD}	0	0.3	V
DV_{SS} and AV_{SS}	0	50	mV

Q3 Package (48-pin VQFN)	Min.	Max.	Unit
Total Allowable Power Dissipation at Tamb = 25°C	–	1750	mW
... Derating	–	17.5	mW/°C
Storage Temperature	−55	+125	°C
Operating Temperature	−40	+85	°C

L4 Package (48-pin LQFP)	Min.	Max.	Unit
Total Allowable Power Dissipation at Tamb = 25°C	–	1600	mW
... Derating	–	16	mW/°C
Storage Temperature	−55	+125	°C
Operating Temperature	−40	+85	°C

9.1.2. Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	Min.	Max.	Unit
Supply Voltage:				
DV_{DD} – DV_{SS}		3.0	3.6	V
AV_{DD} – AV_{SS}		3.0	3.6	V
V_{DEC} – DV_{SS}	12	2.25	2.75	V
Operating Temperature		−40	+85	°C
XTAL/CLK Frequency (using a Xtal)	11	3.0	12.288	MHz
XTAL/CLK Frequency (using an external clock)	11	3.0	24.576	MHz

Notes: 11 Nominal XTAL/CLK frequency is 3.6864MHz.
12 The V_{DEC} supply is automatically created from DV_{DD} by the on-chip voltage regulator.

9.1.3. Operating Characteristics

For the following conditions unless otherwise specified:

External components as recommended in Figure 2.
Maximum load on digital outputs = 30pF.
Xtal Frequency = 3.6864MHz ±0.01% (100ppm); Tamb = –40°C to +85°C.
AV_{DD} = DV_{DD} = 3.0V to 3.6V
Reference Signal Level = 308mV rms at 1kHz with AV_{DD} = 3.3V.
Signal levels track with supply voltage, so scale accordingly.
Signal to Noise Ratio (SNR) in bit rate bandwidth.
Input stage gain = 0dB. Output stage gain = 0dB.

DC Parameters	Notes	Min.	Typ.	Max.	Unit
Supply Current	21				
All Powersaved					
DI_{DD} (DV_{DD} = 3.3V, V_{DEC} = 2.5V)		–	8	100	µA
AI_{DD} (AV_{DD} = 3.3V)		–	4	20	µA
IDLE Mode	22				
DI_{DD} (DV_{DD} = 3.3V, V_{DEC} = 2.5V)		–	1.12	–	mA
AI_{DD} (AV_{DD} = 3.3V)		–	250	–	µA
Rx Mode	22				
DI_{DD} (DV_{DD} = 3.3V, V_{DEC} = 2.5V)		–	6.80	–	mA
AI_{DD} (AV_{DD} = 3.3V)		–	3.05	–	mA
Tx Mode	22				
DI_{DD} (DV_{DD} = 3.3V, V_{DEC} = 2.5V)		–	6.33	–	mA
AI_{DD} (AV_{DD} = 3.3V)		–	6.90	–	mA
Additional current for Auxiliary ADC					
DI_{DD} (DV_{DD} = 3.3V, V_{DEC} = 2.5V)		–	50	–	µA
Additional current for each Auxiliary DAC					
AI_{DD} (AV_{DD} = 3.3V)		–	200	–	µA

Notes: 21 Tamb = 25°C. Not including any current drawn from the device pins by external circuitry.

22 Auxiliary circuits, audio Scrambler, Compandor and Pre/De-emphasis disabled, but all other digital circuits (including the Main Clock PLL) enabled. A single analogue path is enabled through the device.

DC Parameters (continued)	Notes	Min.	Typ.	Max.	Unit
XTAL/CLK	25				
Input Logic 1		70%	–	–	DV_{DD}
Input Logic 0		–	–	30%	DV_{DD}
Input Current (Vin = DV_{DD})		–	–	40	µA
Input Current (Vin = DV_{SS})		−40	–	–	µA
C-BUS Interface and Logic Inputs					
Input Logic 1		70%	–	–	DV_{DD}
Input Logic 0		–	–	30%	DV_{DD}
Input Leakage Current (Logic 1 or 0)	21	−1.0	–	1.0	µA
Input Capacitance		–	–	7.5	pF
C-BUS Interface and Logic Outputs					
Output Logic 1 (I_{OH} = 120µA)		90%	–	–	DV_{DD}
(I_{OH} = 1mA)		80%	–	–	DV_{DD}
Output Logic 0 (I_{OL} = 360µA)		–	–	10%	DV_{DD}
(I_{OL} = -1.5mA)		–	–	15%	DV_{DD}
"Off" State Leakage Current	21	–	–	10	µA
IRQN (Vout = DV_{DD})		−1.0	–	+1.0	µA
RDATA (output HiZ)		−1.0	–	+1.0	µA
V_{BIAS}	26				
Output Voltage Offset wrt $AV_{DD}/2$ (I_{OL} < 1µA)		–	±2%	–	AV_{DD}
Output Impedance		–	22	–	kΩ

Notes:

25 Characteristics when driving the XTAL/CLK pin with an external clock source.

26 Applies when utilising V_{BIAS} to provide a reference voltage to other parts of the system. When using V_{BIAS} as a reference, V_{BIAS} must be buffered. V_{BIAS} must always be decoupled with a capacitor as shown in Figure 2.

AC Parameters		Notes	Min.	Typ.	Max.	Unit
XTAL/CLK Input						
'High' Pulse Width		31	15	–	–	ns
'Low' Pulse Width		31	15	–	–	ns
Input Impedance (measured at 6.144MHz)						
Powered-up	Resistance		–	150	–	kΩ
	Capacitance		–	20	–	pF
Powered-down	Resistance		–	300	–	kΩ
	Capacitance		–	20	–	pF
Xtal Start-up Time (from powersave)			–	400	–	ms
V_{BIAS}						
Start-up Time (from powersave)			–	30	–	ms
Microphone, Signal and Discriminator Inputs (MIC, SIG, DISC)						
Input Impedance		34	–	1	–	MΩ
Maximum Input Level (p-p)		35	–	–	80%	AV_{DD}
Load Resistance (feedback pins)			80	–	–	kΩ
Amplifier Open Loop Voltage Gain (I/P = 1mV rms at 100Hz)			–	60	–	dB
Unity Gain Bandwidth			–	1.0	–	MHz
Programmable Input Gain Stage		36				
Gain (at 0dB)		37	−0.5	0	+0.5	dB
Cumulative Gain Error (wrt gain at 0dB)		37	−1.0	0	+1.0	dB

Notes:

31 Timing for an external input to the XTAL/CLK pin.

34 With no external components connected.

35 Centred about $AV_{DD}/2$; after multiplying by the gain of input circuit (with external components connected).

36 Gain applied to signal at output of buffer amplifier: DISCFB, SIGFB OR MICFB

37 Design value for this block only in test mode. Overall gain input to output has a tolerance of 0dB ±1.0dB.

AC Parameters	Notes	Min.	Typ.	Max.	Unit
Modulator Outputs 1/2 and Audio Output (MOD1, MOD2, AUDIO)					
Power-up to Output Stable	41	–	50	100	µs
Modulator Attenuators					
Attenuation (at 0dB)	43	−1.0	0	+1.0	dB
Cumulative Attenuation Error (wrt attenuation at 0dB)		−0.6	0	+0.6	dB
Output Impedance Enabled	42	–	600	–	Ω
Output Impedance Disabled	42	–	500	–	kΩ
Output Current Range (AV_{DD} = 3.3V)		–	–	±125	µA
Output Voltage Range	44	0.5	–	AV_{DD} –0.5	V
Load Resistance		20	–	–	kΩ
Audio Attenuator					
Attenuation (at 0dB)	43	−1.0	0	+1.0	dB
Cumulative Attenuation Error (wrt attenuation at 0dB)		−1.0	0	+1.0	dB
Output Impedance Enabled	42	–	600	–	Ω
Output Impedance Disabled	42	–	500	–	kΩ
Output Current Range (AV_{DD} = 3.3V)		–	–	±125	µA
Output Voltage Range	44	0.5	–	AV_{DD} –0.5	V
Load Resistance		20	–	–	kΩ

Notes:

41 Power-up refers to issuing a C-BUS command to turn on an output. These limits apply only if V_{BIAS} is on and stable. At power supply switch-on, the default state is for all blocks, except the XTAL and C-BUS interface, to be placed in powersave mode.

42 Small signal impedance, at AV_{DD} = 3.3V and Tamb = 25°C.

43 With respect to the signal at the feedback pin of the selected input port.

44 Centred about $AV_{DD}/2$; with respect to the output driving a 20kΩ load to $AV_{DD}/2$.

AC Parameters (cont.)	Notes	Min.	Typ.	Max.	Unit
Auxiliary Signal Inputs (AUXADC1-4)					
Source Output Impedance	51	–	–	24	kΩ
Auxiliary 10-Bit ADCs					
Resolution		–	10	–	Bits
Maximum Input Level (p-p)	54	–	–	80%	AV_{DD}
Conversion Time	52	–	250	–	µs
Input Impedance					
Resistance		–	10	–	MΩ
Capacitance		–	5	–	pF
Zero Error (input offset to give ADC output = 0)		0	–	±10	mV
Integral Non-linearity		–	–	±3	LSBs
Differential Non-linearity	53	–	–	±1	LSBs
Auxiliary 10-Bit DACs					
Resolution		–	10	–	Bits
Maximum Output Level (p-p), no load	54	80%	–	–	AV_{DD}
Zero Error (output offset from a DAC input = 0)		0	–	±10	mV
Resistive Load		5	–	–	kΩ
Integral Non-linearity		–	–	±4	LSBs
Differential Non-linearity	53	–	–	±1	LSBs

Notes:

51 Denotes output impedance of the driver of the auxiliary input signal, to ensure < 1 bit additional error under nominal conditions.

52 With an auxiliary clock frequency of 3.6864MHz.

53 Guaranteed monotonic with no missing codes.

54 Level centred about $AV_{DD}/2$.

9.1.4. Parametric Performance

For the following conditions unless otherwise specified:
External components as recommended in Figure 2.
Maximum load on digital outputs = 30pF.
Xtal Frequency = 6.144MHz ±0.01% (100ppm)); Tamb = –40°C to +85°C.
AV_{DD} = DV_{DD} = 3.0V to 3.6V.
Reference Signal Level = 308mVrms at 1kHz with AV_{DD} = 3.3V.
Signal levels track with supply voltage, so scale accordingly.
Signal to Noise Ratio (SNR) in bit rate bandwidth.
Input stage gain = 0dB, Output stage gain = 0dB.

AC Parameters (cont.)	Notes	Min.	Typ.	Max.	Unit
Receiver Signal Type Identification					
Probability of correctly identifying signal type (SNR = 12dB)		–	>>99.9	–	%
MSK/FFSK Decoder					
Signal Input Dynamic Range	74	100	–	800	mVrms
Bit Error Rate (SNR = 20dB)	74	–	<1	–	10^{-8}
Receiver Synchronisation (SNR = 12dB) Probability of bit 16 being correct		–	>99.9	–	%

Notes:

74 AV_{DD} = 3.3V, for a “101010101 … 01” pattern measured at the input amplifier feedback pin. Signal level scales with AV_{DD}.

AC Parameters (cont.)	Notes	Min.	Typ.	Max.	Unit
DTMF Decoder					
Sensitivity		–	−22	+3	dB
Response Time		–	35	–	ms
De-response Time		–	–	45	ms
Falsing Rate (per 30min Voice input)		–	10	–	
Frequency Tolerance		–	±2.5	–	%
Twist		−10	–	+10	dB
Audio Compandor					
Attack Time		–	4.0	–	ms
Decay Time		–	13	–	ms
0dB Point	84	–	100	–	mVrms
Compression/Expansion Ratio		–	2:1	–	
DTMF Encoder					
Output Signal Level	84,85	–	775	–	mVrms
Output Level Variation					dB
Output Distortion		–	–	5	%
MSK/FFSK Encoder					
Output Signal Level	84	–	775	–	mVrms
Output Level Variation		−1.0	0	+1.0	dB
Output Distortion		–	–	5	%
3rd Harmonic Distortion		–	–	3	%
Logic 1 frequency 1200baud and 2400baud		1198	1200	1202	Hz
Logic 0 frequency 1200baud		1798	1800	1802	Hz
2400baud		2398	2400	2402	Hz
Isochronous Distortion (0 to 1 and 1 to 0)		–	–	40	µs

Notes: 84 AV_{DD} = 3.3V.
85 Measured in single tone mode, P1.0 set to $DAA0.

AC Parameters (cont.)	Notes	Min.	Typ.	Max.	Unit
Analogue Channel Audio Filtering					
Pass-band (nominal bandwidth):					
Received Audio	91	300	–	3300	Hz
12.5kHz Channel Transmitted Audio	92	300	–	2550	Hz
25kHz Channel Transmitted Audio	93	300	–	3000	Hz
Pass-band Gain (at 1.0kHz)		–	0	–	dB
Pass-band Ripple (wrt gain at 1.0kHz)		−2.0	0	+0.5	dB
Stop-band Attenuation		33.0	–	–	dB
Residual Hum and Noise Tx	96	–	−47	–	dBm
Residual Hum and Noise Rx	96	–	−74	–	dBm
Pre-emphasis	94	–	+6	–	dB/oct
De-emphasis	95	–	−6	–	dB/oct
Audio Scrambler					
Inversion Frequency	98	2632	3300	3496	Hz
Pass-band	99	300	–	3000	Hz
Audio Expandor					
Input Signal Range	97	–	–	0.55	Vrms

Notes:

91 The receiver audio filter complies with the characteristic shown in Figure 7. The high pass filtering removes sub-audio components from the audio signal.

92 The 12.5kHz channel filter complies with the characteristic shown in Figure 11.

93 The 25kHz channel filter complies with the characteristic shown in Figure 10.

94 The pre-emphasis filter complies with the characteristic shown in Figure 12.

95 The de-emphasis filter complies with the characteristic shown in Figure 12.

96 Psophometrically weighted. Pre/De-emphasis, Compandor and 25kHz channel filter selected.

97 AV_{DD} = 3.3V.

98 Use of a scrambler inversion frequency other than 3300Hz will shift the scrambled voice signal outside the audio band, so that some of the signal will be lost in the channel filter. The result is that the descrambled voice signal will have a restricted bandwidth. The limits quoted are subjective and relate to the onset of a loss of speech intelligibility.

99 -6dB points, assuming default inversion frequency in use.

9.2. C-BUS Timing

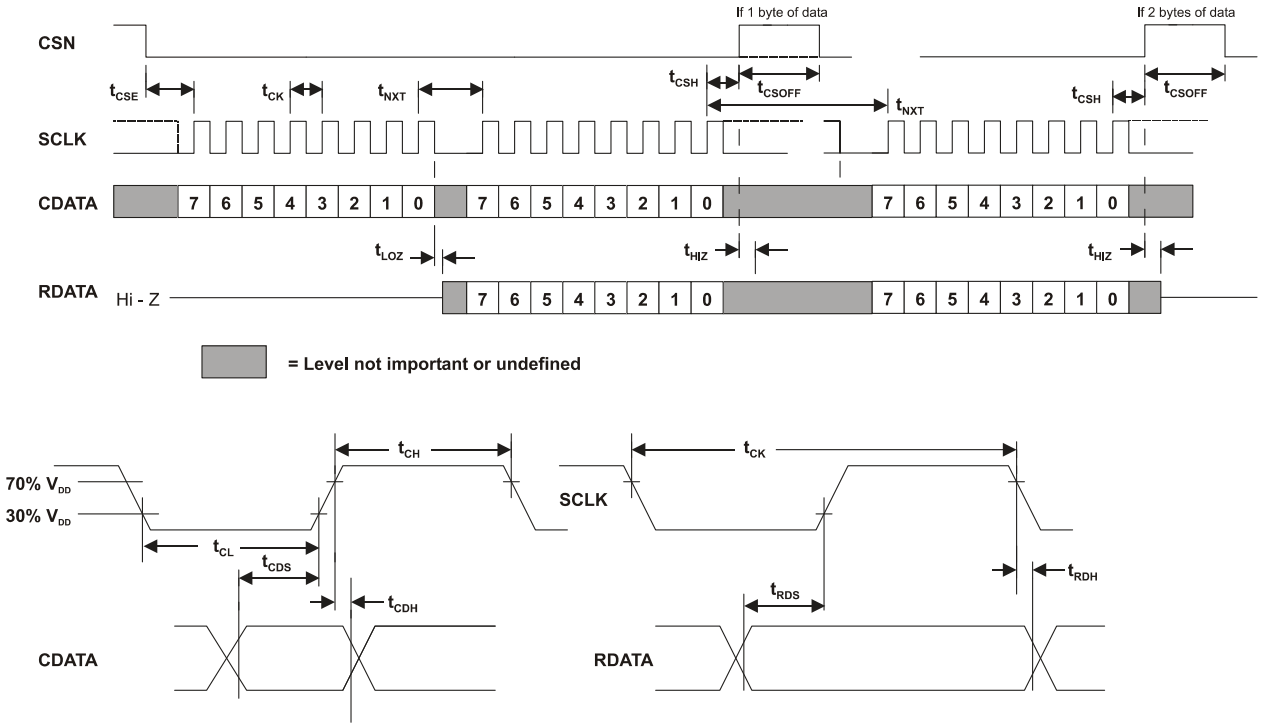


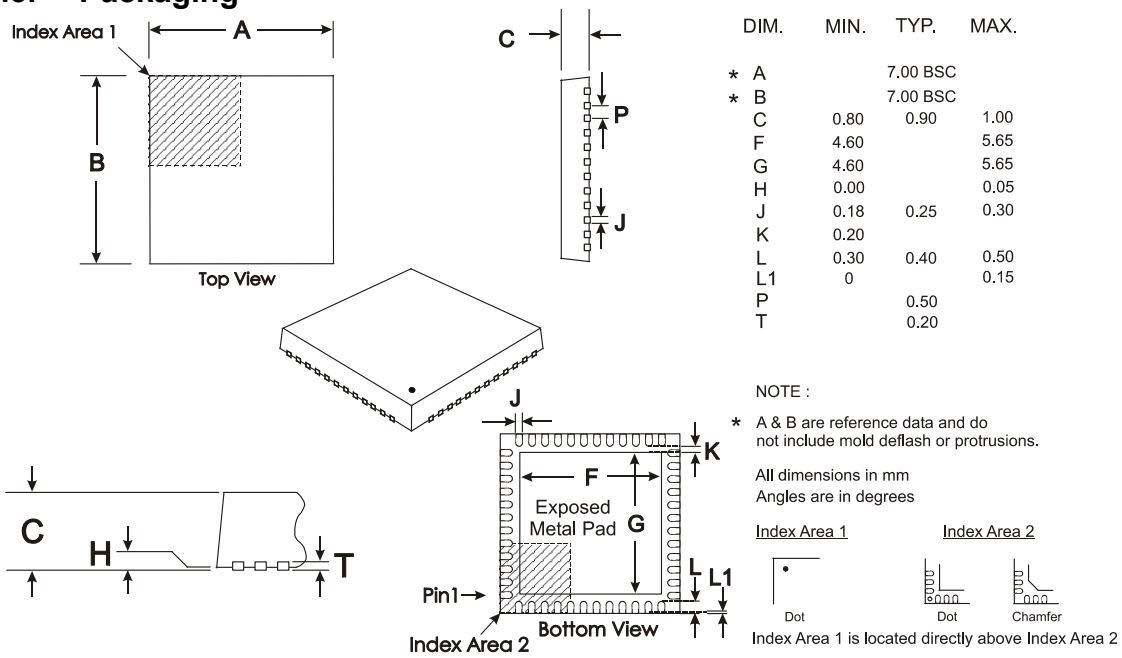
Figure 25 C-BUS Timing

C-BUS Timing		Notes	Min.	Typ.	Max.	Unit
t_{CSE}	CSN Enable to SCLK high time		100	–	–	ns
t_{CSH}	Last SCLK high to CSN high time		100	–	–	ns
t_{LOZ}	SCLK low to RDATA Output Enable time		0.0	–	–	ns
t_{HIZ}	CSN high to RDATA high impedance		–	–	1.0	µs
t_{CSOFF}	CSN high time between transactions		1.0	–	–	µs
t_{NXT}	Inter-byte time		200	–	–	ns
t_{CK}	SCLK cycle time		200	–	–	ns
t_{CH}	SCLK high time		100	–	–	ns
t_{CL}	SCLK low time		100	–	–	ns
t_{CDS}	CDATA setup time		75	–	–	ns
t_{CDH}	CDATA hold time		25	–	–	ns
t_{RDS}	RDATA setup time		50	–	–	ns
t_{RDH}	RDATA hold time		0	–	–	ns

Notes:
1. Depending on the command, 1 or 2 bytes of CDATA are transmitted to the peripheral MSB (Bit 7) first, LSB (Bit 0) last. RDATA is read from the peripheral MSB (Bit 7) first, LSB (Bit 0) last.
2. Data is clocked into the peripheral on the rising SCLK edge.
3. Commands are acted upon at the end of each command (rising edge of CSN).
4. To allow for differing µC serial interface formats C-BUS compatible ICs are able to work with SCLK pulses starting and ending at either polarity.
5. Maximum 30pF load on IRQN pin and each C-BUS interface line.

These timings are for the latest version of C-BUS and allow faster transfers than the original C-BUS timing specification. The CMX148 can be used in conjunction with devices that comply with the slower timings, subject to system throughput constraints.

9.3. Packaging



DIM.	MIN.	TYP.	MAX.
* A		7.00 BSC	
* B		7.00 BSC	
C	0.80	0.90	1.00
F	4.60		5.65
G	4.60		5.65
H	0.00		0.05
J	0.18	0.25	0.30
K	0.20		
L	0.30	0.40	0.50
L1	0		0.15
P		0.50	
T		0.20	

NOTE :

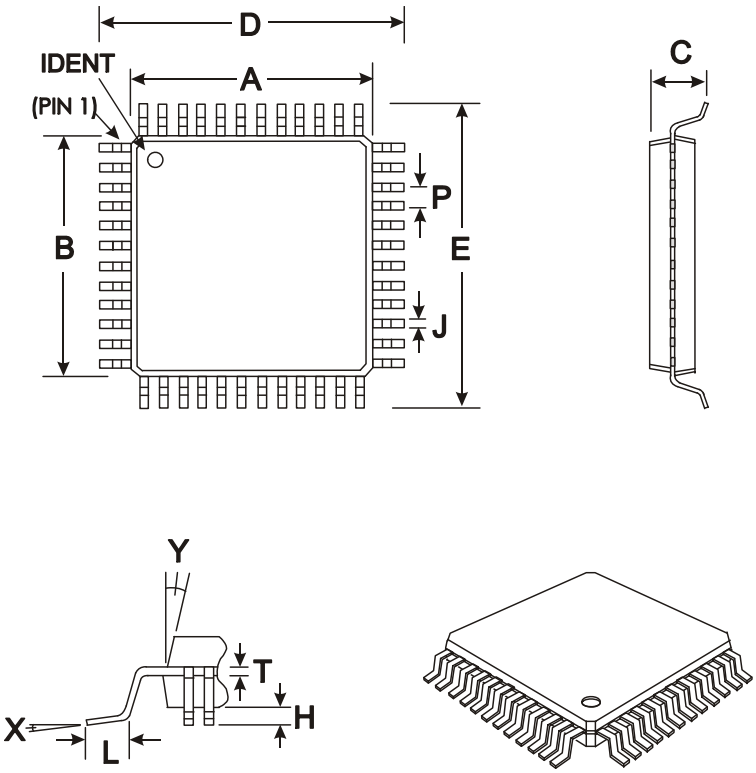
* A & B are reference data and do not include mold deflash or protrusions.

All dimensions in mm
Angles are in degrees

Depending on the method of lead termination at the edge of the package, pull back (L1) may be present.
L minus L1 to be equal to, or greater than 0.3mm
The underside of the package has an exposed metal pad which should ideally be soldered to the pcb to enhance the thermal conductivity and mechanical strength of the package fixing. Where advised, an electrical connection to this metal pad may also be required

Figure 26 Mechanical Outline of 48-pin VQFN (Q3)

Order as part no. CMX148Q3



	DIM.	MIN.	TYP.	MAX.
*	A	6.91		7.11
*	B	6.91		7.11
	C	1.40		1.60
	D	8.74		9.25
	E	8.74		9.25
	H	0.05		0.15
	J	0.10		0.28
	L	0.35		0.76
	P		0.50	
	T		0.13	
	X	0°		7°
	Y	11°		13°

NOTE :

* A & B are reference data and do not include mold deflash or protrusions.

All dimensions in mm
Angles are in degrees
Co-Planarity of leads within 0.1mm

Figure 27 Mechanical Outline of 48-pin LQFP (L4)

Order as part no. CMX148L4

As package dimensions may change after publication of this datasheet, it is recommended that you check for the latest Packaging Information from the Datasheet page of the CML website: [www.cmlmicro.com].

CML Microcircuits (UK) Ltd COMMUNICATION SEMICONDUCTORS	CML Microcircuits (USA) Inc. COMMUNICATION SEMICONDUCTORS	CML Microcircuits (Singapore) Pte Ltd COMMUNICATION SEMICONDUCTORS
Tel: +44 (0)1621 875500 **Fax:** +44 (0)1621 875600 **Sales:** sales@cmlmicro.com **Tech Support:** techsupport@cmlmicro.com	**Tel:** +1 336 744 5050 800 638 5577 **Fax:** +1 336 744 5054 **Sales:** us.sales@cmlmicro.com **Tech Support:** us.techsupport@cmlmicro.com	**Tel:** +65 67450426 **Fax:** +65 67452917 **Sales:** sg.sales@cmlmicro.com **Tech Support:** sg.techsupport@cmlmicro.com
- www.cmlmicro.com -		