Integrated
Circuit
Systems, Inc.

ICS9169C-41

Frequency Generator for PentiumPro™ Based Systems

General Description

The **ICS9169C-41** is a Clock Synthesize/Driver chip for Pentium, PentiumPro or Cyrix 68x86 based motherboards using SDRAM.

Features include four dual purpose I/O pins which provide extra CPU clocks and enable the part to be packaged in a low-cost 34-pin SSOP package. These four pins latch the select inputs at the internal Power-On Reset. Additionally, the device meets the Pentium and PentiumPro power-up stabilization, which requires that CPU and PCI clocks be stable within 2ms after power-up.

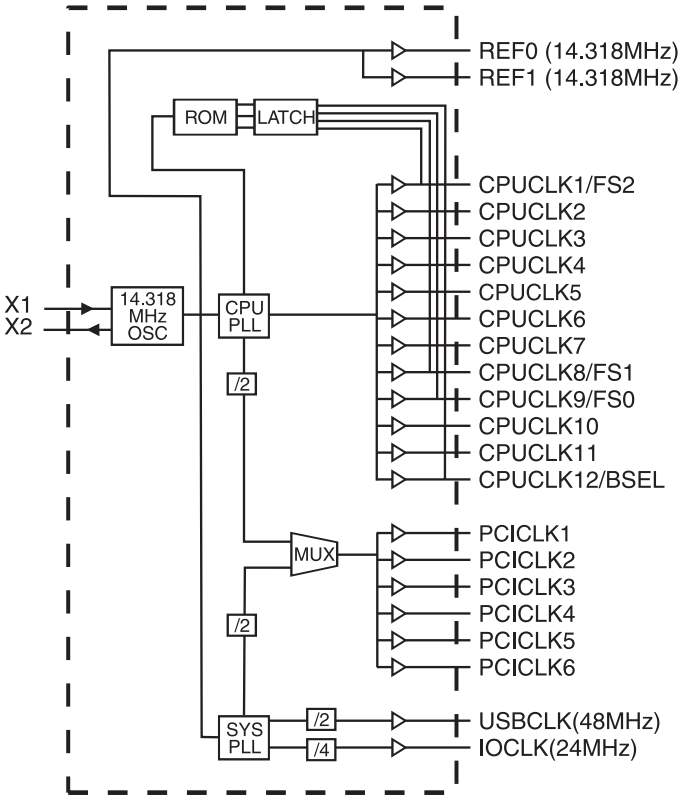
The **ICS9169C-41** clock outputs are designed for low EMI emissions. Controlled rise and fall times, unique output driver circuits and innovative circuit layout techniques enable the **ICS9169C-41** to have lower EMI than other clock devices.

The **ICS9169C-41** accepts a 14.318MHz reference crystal or clock as its input and runs from a 3.3V supply.

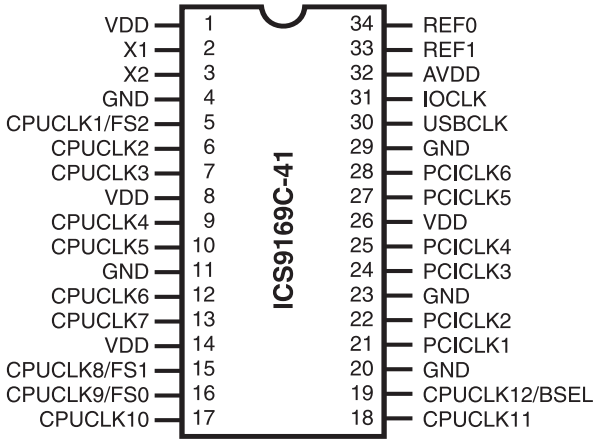
Features

- 12 selectable CPU/SDRAM/AGP clocks up to 75 MHz
- Six PCI clocks, synchronous or asynchronous mode, pin selectable by Bus Select input (pin 19)
- One USB clock at 48MHz, meets Intel jitter, accuracy, as well as rise and fall time requirements
- One I/O clock at 24MHz
- Two Ref. Clocks at 14.318MHz
- CPU clocks to PCI clock skew of 1-4ns (CPU early)
- Low CPU and PCI clock jitter <200ps
- Low skew outputs, skew window 250ps for CPU clocks and for PCI clocks
- Improved output drivers are designed for low EMI
- Test Mode
- 3.3V ±10% operation
- Space saving and low cost 34-pin SSOP package

Block Diagram



Pin Configuration



34-Pin SSOP

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Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1, 8, 14, 26	V_{DD}	PWR	Voltage Supply
2	X1	IN	Crystal input. Nominally 14.318MHz
3	X2	OUT	Crystal output. Nominally 14.318MHz
4, 11 20, 23, 29	GND	PWR	Ground
5	CPUCLK1	OUT	Processor clock output which are a multiple of the input reference clock as shown in the preceding table.
	FS2	IN	Frequency multiplier select pins. See shared pin programming description later in this data sheet for further explanation.
18, 17, 13, 12, 10, 9, 7, 6,	CPUCLK(11,10,7:2)	OUT	CPU clock output
15	CPUCLK8	OUT	Processor clock output which are a multiple of the input reference clock as shown in the preceding table.
	FS1	IN	Frequency multiplier select pin. See shared pin programming description later in this data sheet for further explanation.
16	CPUCLK9	OUT	Processor clock output which are a multiple of the input reference clock as shown in the preceding table.
	FS0	IN	Frequency multiplier select pins. See shared pin programming description later in this data sheet for further explanation.
19	CPUCLK12	OUT	Processor clock output which are a multiple of the input reference clock as shown in the preceding table.
	BSEL	IN	Selection for synchronous (High) or asynchronous (Low) bus clock operation. See shared pin programming description later in this data sheet for further explanation.
28, 27, 25, 24, 22, 21	PCICLK (6:1)	OUT	PCI Clock outputs. syncronous to CPU with 1-4ns delay.
30	USBCLK	OUT	USB clock output 48 MHz
31	IOCLK	OUT	I/O clock output 24 MHz
32	AVDD	PWR	Analog Voltage Supply
33	REF1	OUT	Reference clock output (14.318 MHz)
34	REF0	OUT	Reference clock output (14.318 MHz) for ISA slots (drives C_{LOAD} = 45pF)

Functionality

3.3V±10%, 0-70°C
Crystal (X1, X2) = 14.31818 MHz

FS2	FS1	FS0	XTALIN	CPUCLK	PCICLK(1-5) BSEL = 1	PCICLK(1-5) BSEL = 0	REF(0-1)	USBCLK	IOCLK
0	0	0	14.318MHz	33.33MHz	16.67MHz	32MHz	14.318MHz	48MHz	24MHz
0	0	1	14.318MHz	75.0MHz	37.5MHz	32MHz	14.318MHz	48MHz	24MHz
0	1	0	14.318MHz	55.0MHz	27.5MHz	32MHz	14.318MHz	48MHz	24MHz
0	1	1	14.318MHz	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z
1	0	0	14.318MHz	50.0MHz	25.0MHz	32MHz	14.318MHz	48MHz	24MHz
1	0	1	14.318MHz	66.67MHz	33.33MHz	32MHz	14.318MHz	48MHz	24MHz
1	1	0	14.318MHz	60.0MHz	30.0MHz	32MHz	14.318MHz	48MHz	24MHz
1	1	1	TCLK[1]	TCLK/2[2]	TCLK/4	TCLK/3	TCLK	TCLK/2	TCLK/4

Notes

1. TCLK is supplied on XTALIN pin
2. Bidirectional CPUCLK I/O pins are high in test mode.

Absolute Maximum Ratings

Supply Voltage . . . . . 7.0 V

Logic Inputs . . . . . GND –0.5 V to V_{DD} +0.5 V

Ambient Operating Temperature . . . . . 0°C to +70°C

Storage Temperature . . . . . –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics at 3.3V

V_{DD} = 3.0 – 3.7 V, T_A = 0 – 70° C unless otherwise stated

DC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}		-	-	$0.2V_{DD}$	V
Input High Voltage	V_{IH}		$0.7V_{DD}$	-	-	V
Input Low Current	I_{IL}	VIN=0V	-28.0	-10.5	-	µA
Input High Current	I_{IH}	VIN=V_{DD}	-5.0	-	5.0	µA
Output Low Current[1]	I_{OL}	VOL=0.8V; for CPU, PCI, REF CLKS	16.0	25.0	-	mA
Output High Current[1]	I_{OH}	VOL=2.0V; for CPU, PCI, REF CLKS	-	-30.0	-14.0	mA
Output Low Current[1]	I_{OL}	VOL=0.8V; for Fixed CLK	19.0	30.0	-	mA
Output High Current[1]	I_{OH}	VOL=2.0V; for Fixed CLK	-	-38.0	-16.0	mA
Output Low Voltage[1]	V_{OL}	IOL=8mA; for CPU, PCI, REF	-	0.3	0.4	V
Output High Voltage[1]	V_{OH}	IOH=-8mA; for CPU, PCI, REF	2.4	2.8	-	V
Output Low Voltage[1]	V_{OL}	IOL=18mA; Fixed CLK's	-	0.3	0.4	V
Output High Voltage[1]	V_{OH}	IOH=-18mA; Fixed CLK's	2.4	2.8	-	V
Supply Current	I_{DD}	@66.6 MHz; all outputs unloaded	-	75	95	mA

Note 1: Parameter is guaranteed by design and characterization. Not 100% tested in production.

Electrical Characteristics at 3.3V

V_{DD} = 3.0 – 3.7 V, T_A = 0 – 70° C unless otherwise stated

AC Characteristics						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
Rise Time[1]	Tr1	20pF load, 0.8 to 2.0V; All Except Ref	-	0.9	1.2	ns
Fall Time[1]	Tf1	20pF load, 2.0 to 0.8V; All Except Ref	-	0.8	1.2	ns
Rise Time[1]	Tr2	30pF load, 0.8 - 2.0V All Except Ref	-	1.3	1.6	ns
Fall Time[1]	Tf2	30pF load, 2.0 - 0.8V All Except Ref	-	1.3	1.6	ns
Rise Time	Tr3	45pF; 0.8 - 2.0V; Ref only	-	1.7	2.0	ns
Fall Time	Tf3	45pF; 2.0 - 0.8V; Ref only	-	1.0	2.0	ns
Duty Cycle[1]	Dt	20, 30, 45pF load @ VOUT=1.5V	45	50	55	%
Jitter, One Sigma[1]	Tj1s1	CPU & PCI Clocks	-	50	150	ps
Jitter, Absolute[1]	Tjab1	CPU & PCI Clocks (@ 60 & 66MHz)	-250	-	250	ps
Jitter, One Sigma[1]	Tj1s2	Ref & Fixed CLKs	-	1	3	%
Jitter, Absolute[1]	Tjab2	Ref & Fixed CLKs	-	1.0	2.5	%
Jitter - Cycle to Cycle	Tcc	CPU Outputs	-	290	350	ps
		Fixed Clocks & REF0	-	4.5	6	%
Input Frequency[1]	Fi		12.0	14.318	16.0	MHz
Logic Input Capacitance[1]	CIN	Logic input pins	-	5	-	pF
Crystal Oscillator Capacitance[1]	CINX	X1, X2 pins	-	18	-	pF
Power-on Time[1]	ton	From VDD=1.6V to 1st crossing of 66.6 MHz VDD supply ramp < 40ms	-	1.9	2.0	ms
Frequency Settling Time[1]	ts	From 1st crossing of acquisition to <1% settling	-	2.0	4.0	ms
Clock Skew[1] (window)	Tsk1	CPU to CPU & PCI - PCI; Same Load; @1.5V	-	188	300	ps
Clock Skew[1] (window)	Tsk2	CPU(20pF) - PCI (30pF); @1.5V (CPU is Early)	1.0	1.2	4.0	ns

Note 1: Parameter is guaranteed by design and characterization. Not 100% tested in production.

Technical Pin Function Descriptions

VDD
This is the power supply to the internal logic of the device as well as the following clock output buffers:

This pin may be operated at any voltage between 3.0 and 3.7 volts. Clocks from the listed buffers that it supplies will have a voltage swing from ground to this level. For the actual guaranteed high and low voltage levels of these clocks, please consult the AC parameter table in this data sheet.

GND
This is the power supply ground return pin.

X1
This pin serves one of two functions. When the device is used with a crystal, X1 acts as the input pin for the reference signal that comes from the discrete crystal. When the device is driven by an external clock signal, X1 is the device input pin for that reference clock. This pin also implements an internal crystal loading capacitor that is connected to ground. See the data tables for the value of the capacitor.

X2
This pin is used only when the device uses a Crystal as the reference frequency source. In this mode of operation, X2 is an output signal that drives (or excites) the discrete crystal. This pin also implements an internal crystal loading capacitor that is connected to ground. See the data tables for the value of the capacitor.

CPU (1:12)
These pins are the clock output that drive the processor and other CPU related circuitry that require clocks which are in tight skew tolerance with the CPU clock. See the Functionality table at the beginning of this data sheet for a list of the specific frequencies that these clocks operate at and the selection codes that are necessary to produce these frequencies. Some of these pin serve dual functions.

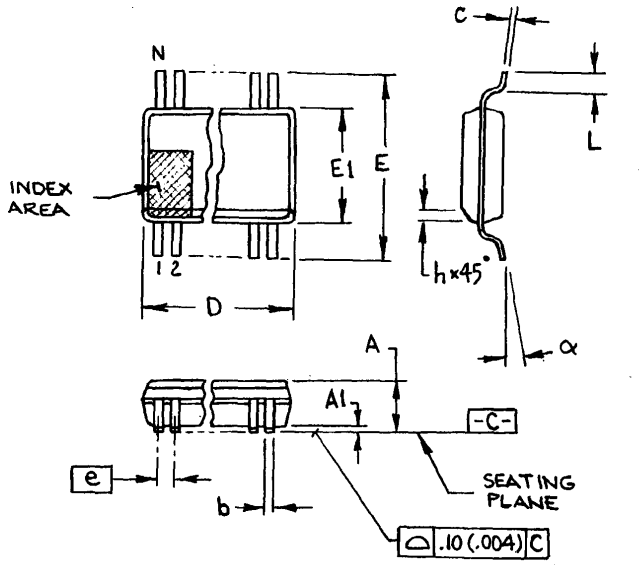
PCICLK
Clock output driver for the PCI Bus.

FS0, FS1, FS2
These pins control the frequency of the clocks at the CPU, BUS and SDRAM pins. See the Funtionality table at the beginning of this data sheet for a list of the specific frequencies that these clock operate at and the selection codes that are necessary to produce these frequencies. The device reads these pins at power-up and stores the programmed selection code in an internal data latch. If a "1" value is desired for a specific frequency selection bit,a 10K ohm resistor must be connected from the appropriate FS pin to the VDD supply. If a "O" value is desired, then the 10K resistor must be connected to ground. After the internal power On reset latches the input data, these pins become output clocks and no further frequency selection is possible.

48MHz
This is a fixed frequency clock that is typically used to drive USB peripheral device needs.

24MHz
This is a fixed frequency clock that is typically used to drive super I/O peripheral device needs.

REF (0:1)
This is a fixed frequency clock that runs at the same frequency as the input freerence clock (typically 14.31818 MHz) is and typically used to drive Video and ISA BUS requirements.



300 mil SSOP

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	2.40	2.80	.095	.110
A1	0.20	0.40	.008	.016
b	0.20	0.34	.008	.0135
c	0.13	0.25	.005	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	10.00	10.70	.395	.420
E1	7.40	7.60	.291	.299
e	0.065 BASIC		0.025 BASIC	
h	0.40	0.65	.015	.025
L	0.50	1.00	.020	.040
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
28	9.40	9.65	.370	.380
34	11.30	11.55	.445	.455
48	15.75	16.00	.620	.630
56	18.30	18.55	.720	.730
64	20.80	21.05	.820	.830

Ordering Information

ICS9169CF-41

Example:

ICS XXXX F - PPP

- **Pattern Number (2 or 3 digit number for parts with ROM code patterns)**
- **Package Type**
  F=SSOP
- **Device Type (consists of 3 or 4 digit numbers)**
- **Prefix**
  ICS, AV = Standard Device