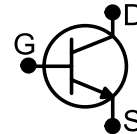
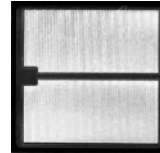


## Normally – OFF Silicon Carbide Junction Transistor

$V_{DS}$	=	600 V
$R_{DS(ON)}$	=	25 mΩ
$I_D @ 25\text{ }^\circ\text{C}$	=	100 A
$h_{FE}$	=	105

### Features

- 210°C maximum operating temperature
- Gate Oxide Free SiC switch
- Exceptional Safe Operating Area
- Excellent Gain Linearity
- Temperature Independent Switching Performance
- Low Output Capacitance
- Positive Temperature Co-efficient of  $R_{DS(ON)}$
- Suitable for connecting an anti-parallel diode



Die Size = 4.35 mm x 4.35 mm

### Advantages

- Compatible with Si MOSFET/IGBT gate-drivers
- > 20 μs Short-Withstand Capability
- Lowest-in-class Conduction Losses
- High Circuit Efficiency
- Minimal Input Signal Distortion
- High Amplifier Bandwidth

### Applications

- Down Hole Oil Drilling, Geothermal Instrumentation
- Hybrid Electric Vehicles (HEV)
- Solar Inverters
- Switched-Mode Power Supply (SMPS)
- Power Factor Correction (PFC)
- Induction Heating
- Uninterruptible Power Supply (UPS)
- Motor Drives

### Absolute Maximum Ratings ( $T_C = 25\text{ }^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Drain – Source Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}$		600		V
Continuous Drain Current	$I_D$	$T_C = 25\text{ }^\circ\text{C}$		100		A
Continuous Drain Current	$I_D$	$T_C > 125\text{ }^\circ\text{C}$ , assumes $R_{thJC} < 0.26\text{ }^\circ\text{C/W}$		50		A
Gate Peak Current	$I_{GM}$			3.5		A
Turn-Off Safe Operating Area	RBSOA	$T_{VJ} = 210\text{ }^\circ\text{C}$ , Clamped Inductive Load		$I_{D,max} = 50$ @ $V_{DS} \leq V_{DSmax}$		A
Short Circuit Safe Operating Area	SCSOA	$T_{VJ} = 210\text{ }^\circ\text{C}$ , $I_G = 1\text{ A}$ , $V_{DS} = 400\text{ V}$ , Non Repetitive		20		μs
Reverse Gate – Source Voltage	$V_{GS}$			30		V
Reverse Drain – Source Voltage	$V_{DS}$			25		V
Operating Junction and Storage Temperature	$T_j, T_{stg}$			-55 to 210		°C
Maximum Processing Temperature	$T_{Proc}$	10 min. maximum		325		°C

### Electrical Characteristics

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
<b>On Characteristics</b>						
Drain – Source On Resistance	$R_{DS(ON)}$	$I_D = 50\text{ A}$ , $I_G = 1000\text{ mA}$ , $T_j = 25\text{ }^\circ\text{C}$ $I_D = 50\text{ A}$ , $I_G = 1000\text{ mA}$ , $T_j = 125\text{ }^\circ\text{C}$ $I_D = 50\text{ A}$ , $I_G = 2000\text{ mA}$ , $T_j = 175\text{ }^\circ\text{C}$ $I_D = 50\text{ A}$ , $I_G = 2000\text{ mA}$ , $T_j = 210\text{ }^\circ\text{C}$		25		mΩ
				39		
				43		
				62		
Gate – Source Saturation Voltage	$V_{GS,SAT}$	$I_D = 50\text{ A}$ , $I_D/I_G = 40$ , $T_j = 25\text{ }^\circ\text{C}$ $I_D = 50\text{ A}$ , $I_D/I_G = 30$ , $T_j = 175\text{ }^\circ\text{C}$		3.42		V
				3.23		
DC Current Gain	$\beta$	$V_{DS} = 5\text{ V}$ , $I_D = 50\text{ A}$ , $T_j = 25\text{ }^\circ\text{C}$ $V_{DS} = 5\text{ V}$ , $I_D = 50\text{ A}$ , $T_j = 125\text{ }^\circ\text{C}$ $V_{DS} = 5\text{ V}$ , $I_D = 50\text{ A}$ , $T_j = 175\text{ }^\circ\text{C}$ $V_{DS} = 5\text{ V}$ , $I_D = 50\text{ A}$ , $T_j = 210\text{ }^\circ\text{C}$		105		
				77		
				71		
				69		
<b>Off Characteristics</b>						
Drain Leakage Current	$I_{DSS}$	$V_R = 600\text{ V}$ , $V_{GS} = 0\text{ V}$ , $T_j = 25\text{ }^\circ\text{C}$ $V_R = 600\text{ V}$ , $V_{GS} = 0\text{ V}$ , $T_j = 210\text{ }^\circ\text{C}$		10		μA
				100		
Gate – Source Leakage Current	$I_{GSS}$	$V_{GS} = -20\text{ V}$ , $T_j = 25\text{ }^\circ\text{C}$		20		nA

Electrical Characteristics

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
<b>Capacitance Characteristics</b>						
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}, V_D = 100\text{ V}, f = 1\text{ MHz}$		6440		pF
Reverse Transfer/Output Capacitance	$C_{rss}/C_{oss}$	$V_D = 100\text{ V}, f = 1\text{ MHz}$		420		pF

Figures

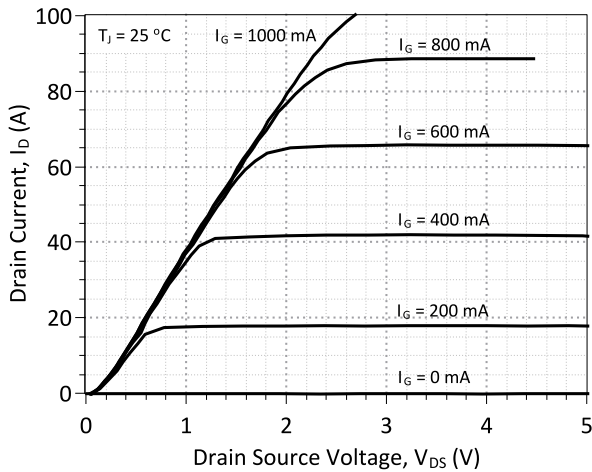


Figure 1: Typical Output Characteristics at 25 °C

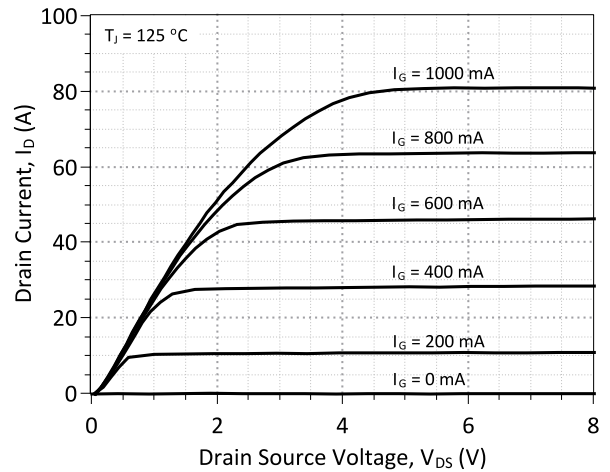


Figure 2: Typical Output Characteristics at 125 °C

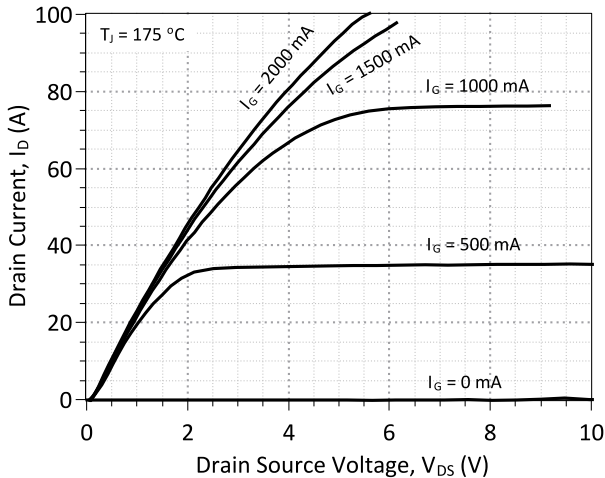


Figure 3: Typical Output Characteristics at 175 °C

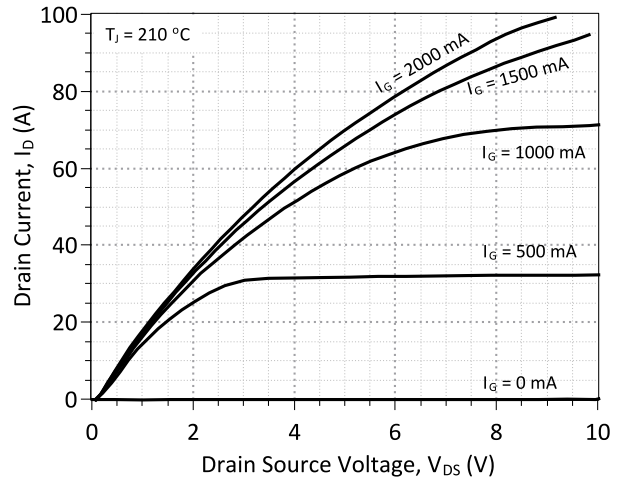


Figure 4: Typical Output Characteristics at 210 °C

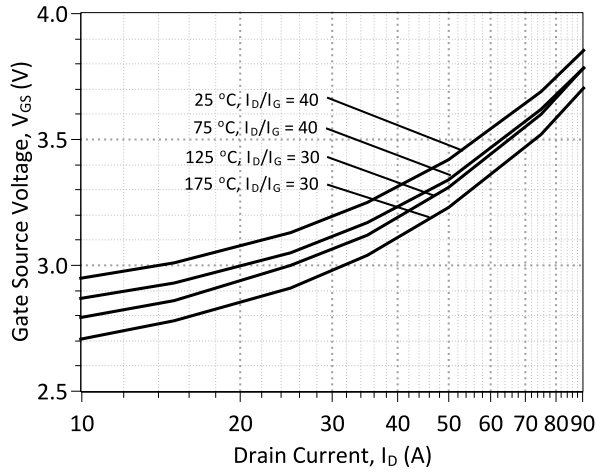


Figure 5: Typical Gate – Source Saturation Voltage

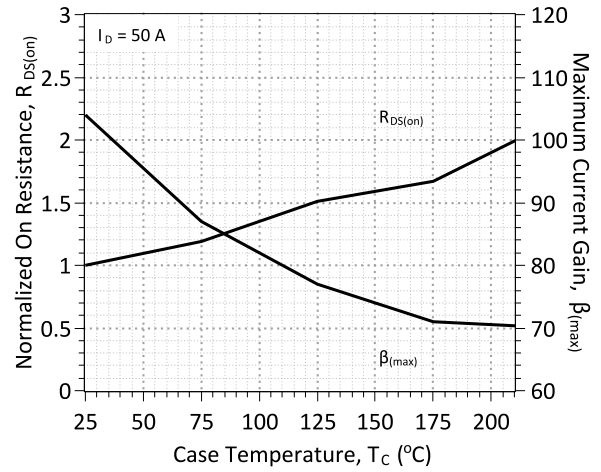


Figure 6: Normalized On-Resistance and Current Gain vs. Temperature

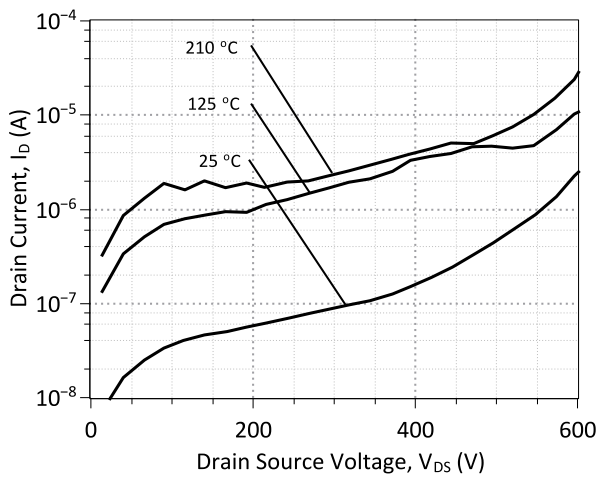


Figure 7: Typical Blocking Characteristics

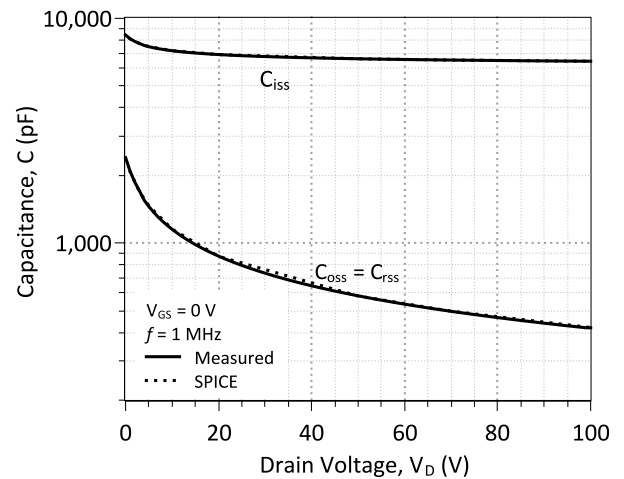


Figure 8: Capacitance Characteristics

Driving the GA50JT06-CAL

Drive Topology	Gate Drive Power Consumption	Switching Frequency	Application Emphasis	Availability
TTL Logic	High	Low	Wide Temperature Range	Coming Soon
Constant Current	Medium	Medium	Wide Temperature Range	Coming Soon
High Speed – Boost Capacitor	Medium	High	Fast Switching	Production
High Speed – Boost Inductor	Low	High	Ultra Fast Switching	Coming Soon
Proportional	Lowest	High	Wide Drain Current Range	Coming Soon
Pulsed Power	Medium	N/A	Pulse Power	Coming Soon

**A: Static TTL Logic Driving**

The GA50JT06-CAL may be driven using direct (5 V) TTL logic after current amplification. The (amplified) current level of the supply must meet or exceed the steady state gate current ( $I_{G,steady}$ ) required to operate the GA50JT06-CAL. The power level of the supply can be estimated from the target duty cycle of the particular application.  $I_{G,steady}$  is dependent on the anticipated drain current  $I_D$  through the SJT and the DC current gain  $h_{FE}$ , it may be calculated from the following equation. An accurate value of the  $h_{FE}$  may be read from Figure 6.

$$I_{G,steady} \approx \frac{I_D}{h_{FE}(T, I_D)} * 1.5$$

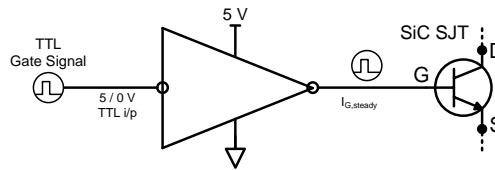


Figure 9: TTL Gate Drive Schematic

**B: High Speed Driving**

The SJT is a current controlled transistor which requires a positive gate current for turn-on as well as to remain in on-state. An ideal gate current waveform for ultra-fast switching of the SJT, while maintaining low gate drive losses, is shown in Figure 10 which features a positive current peak during turn-on, a negative current peak during turn-off, and continuous gate current to remain on.

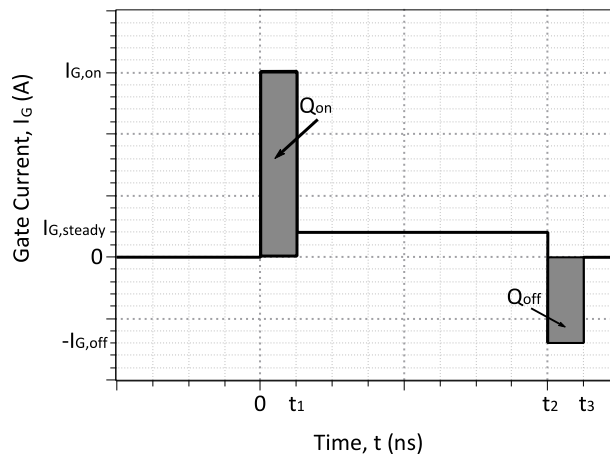


Figure 10: An idealized gate current waveform for fast switching of an SJT.

An SJT is rapidly switched from its blocking state to on-state, when the necessary gate charge,  $Q_G$ , for turn-on is supplied by a burst of high gate current,  $I_{G,on}$ , until the gate-source capacitance,  $C_{GS}$ , and gate-drain capacitance,  $C_{GD}$ , are fully charged.

$$Q_{on} = I_{G,on} * t_1$$

$$Q_{on} \geq Q_{gs} + Q_{gd}$$

Ideally,  $I_{G,on}$  should terminate when the drain voltage falls to its on-state value in order to avoid unnecessary drive losses during the steady on-state. In practice, the rise time of the  $I_{G,on}$  pulse is affected by the parasitic inductances,  $L_{par}$  in the device package and drive circuit. A voltage developed across the parasitic inductance in the source path,  $L_s$ , can de-bias the gate-source junction, when high drain currents begin to flow through the device. The voltage applied to the gate pin should be maintained high enough, above the  $V_{GS,sat}$  (see Figure 5) level to counter these effects.

A high negative peak current,  $-I_{G,off}$  is recommended at the start of the turn-off transition, in order to rapidly sweep out the injected carriers from the gate, and achieve rapid turn-off. While satisfactory turn off can be achieved with  $V_{GS} = 0$  V, a negative gate voltage  $V_{GS}$  may be used in order to speed up the turn-off transition.

Two high-speed drive topologies for the SiC SJTs are presented below.

**B:1: High Speed, Low Loss Drive with Boost Capacitor, GA15IDDJT22-FR4**

The GA50JT17-CAL may be driven using a High Speed, Low Loss Drive with Boost Capacitor topology in which multiple voltage levels, a gate resistor, and a gate capacitor are used to provide fast switching current peaks at turn-on and turn-off and a continuous gate current while in on-state. An evaluation gate drive board (GA15IDDJT22-FR4) utilizing this topology is commercially available for low-side driving, its datasheet provides additional details.

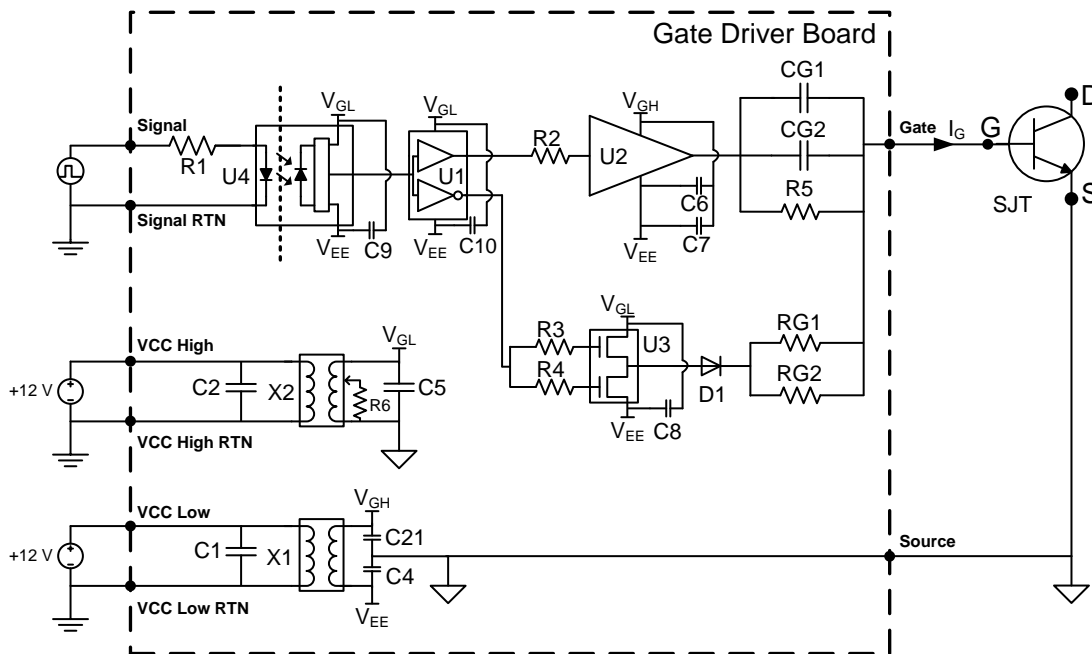


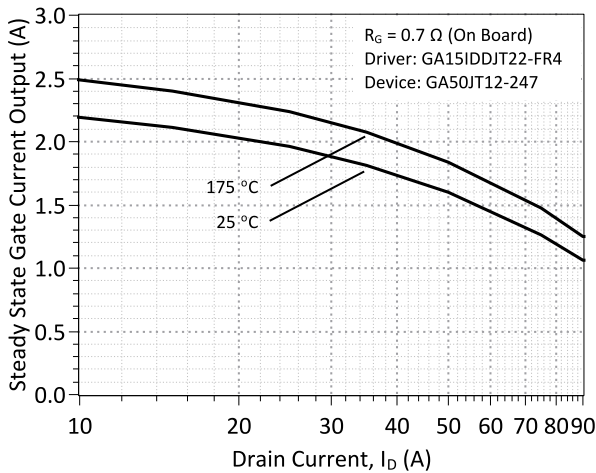
Figure 1: Topology of the GA15IDDJT22-FR4 Two Voltage Source gate driver.

The GA15IDDJT22-FR4 evaluation board comes equipped with two on board gate drive resistors (RG1, RG2) pre-installed for an effective gate resistance<sup>3</sup> of  $R_G = 0.7 \Omega$ . It may be necessary for the user to reduce RG1 and RG2 under high drain current conditions for safe operation of the GA50JT17-CAL. The steady state current supplied to the gate pin of the GA50JT17-CAL with on-board  $R_G = 0.7 \Omega$ , is shown in Figure 25. The maximum allowable safe value of  $R_G$  for the user's required drain current can be read from Figure 26.

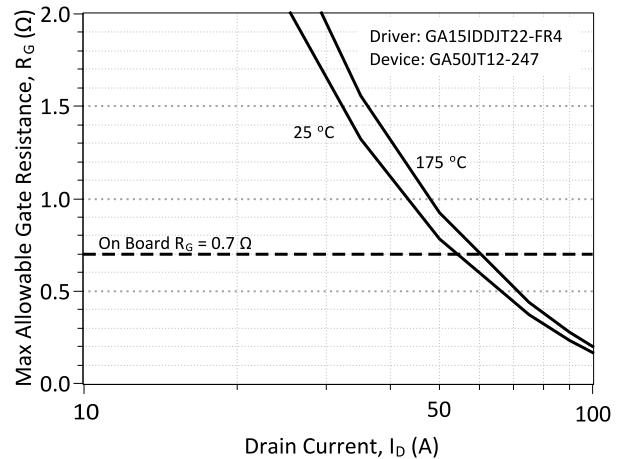
**For the GA50JT17-CAL,  $R_G$  must be reduced for  $I_D \geq \sim 60$  A for safe operation with the GA15IDDJT22-FR4.**

For operation at  $I_D \geq \sim 60$  A,  $R_G$  may be calculated from the following equation, which contains the DC current gain  $h_{FE}$  (Figure 4) and the gate-source saturation voltage  $V_{GS,sat}$  (Figure 7).

$$R_{G,max} = \frac{(4.7V - V_{GS,sat}) * h_{FE}(T, I_D)}{I_D * 1.5} - 0.1\Omega$$



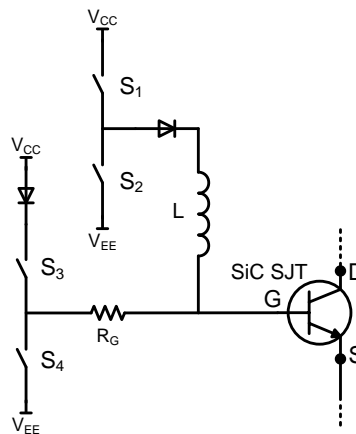
**Figure 2: Typical steady state gate current supplied by the GA15IDDJT22-FR4 board for the GA50JT17-CAL with the on board resistance of 0.7 Ω**



**Figure 3: Maximum gate resistance for safe operation of the GA50JT17-CAL at different drain currents using the GA15IDDJT22-FR4 board.**

**B:2: High Speed, Low Loss Drive with Boost Inductor**

A High Speed, Low-Loss Driver with Boost Inductor is also capable of driving the GA50JT06-CAL at high-speed. It utilizes a gate drive inductor instead of a capacitor to provide the high-current gate current pulses  $I_{G,on}$  and  $I_{G,off}$ . During operation, inductor L is charged to a specified  $I_{G,on}$  current value then made to discharge  $I_L$  into the SiC SJT gate pin using logic control of  $S_1$ ,  $S_2$ ,  $S_3$ , and  $S_4$ , as shown in Figure 14. After turn on, while the device remains on the necessary steady state gate current  $I_{G,steady}$  is supplied from source  $V_{CC}$  through  $R_G$ . Please refer to the article “A current-source concept for fast and efficient driving of silicon carbide transistors” by Dr. Jacek Rąbkowski for additional information on this driving topology.<sup>4</sup>



**Figure 14: Simplified Inductive Pulsed Drive Topology**

<sup>3</sup> –  $R_G = (1/RG1 + 1/RG2)^{-1}$ . Driver is pre-installed with  $RG1 = RG2 = 7.5 \Omega$

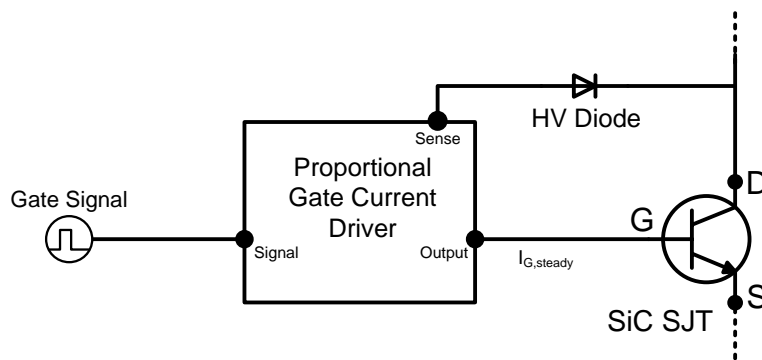
<sup>4</sup> – Archives of Electrical Engineering. Volume 62, Issue 2, Pages 333–343, ISSN (Print) 0004-0746, DOI: 10.2478/ae-2013-0026, June 2013

**C: Proportional Gate Current Driving**

For applications in which the GA50JT06-CAL will operate over a wide range of drain current conditions, it may be beneficial to drive the device using a proportional gate drive topology to optimize gate drive power consumption. A proportional gate driver relies on instantaneous drain current  $I_D$  feedback to vary the steady state gate current  $I_{G,steady}$  supplied to the GA50JT06-CAL.

**C:1: Voltage Controlled Proportional Driver**

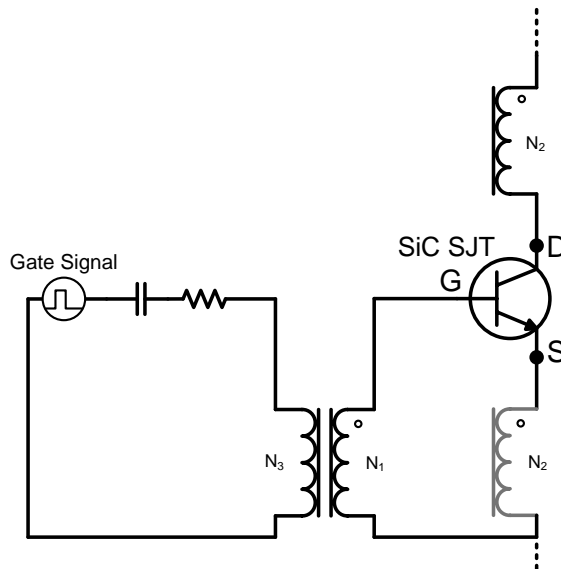
The voltage controlled proportional driver relies on a gate drive IC to detect the GA50JT06-CAL drain-source voltage  $V_{DS}$  during on-state to sense  $I_D$ . The gate drive IC will then increase or decrease  $I_{G,steady}$  in response to  $I_D$ . This allows  $I_{G,steady}$ , and thus the gate drive power consumption, to be reduced while  $I_D$  is relatively low or for  $I_{G,steady}$  to increase when is  $I_D$  higher. A high voltage diode connected between the drain and sense protects the IC from high-voltage when the driver and GA50JT06-CAL are in off-state. A simplified version of this topology is shown in Figure 15, additional information will be available in the future at <http://www.genesicsemi.com/commercial-sic/sic-junction-transistors/>



**Figure 15: Simplified Voltage Controlled Proportional Driver**

**C:2: Current Controlled Proportional Driver**

The current controlled proportional driver relies on a low-loss transformer in the drain or source path to provide feedback  $I_D$  of the GA50JT06-CAL during on-state to supply  $I_{G,steady}$  into the device gate.  $I_{G,steady}$  will then increase or decrease in response to  $I_D$  at a fixed forced current gain which is set by the turns ratio of the transformer,  $h_{force} = I_D / I_G = N_2 / N_1$ . GA50JT06-CAL is initially tuned-on using a gate current pulse supplied into an RC drive circuit to allow  $I_D$  current to begin flowing. This topology allows  $I_{G,steady}$ , and thus the gate drive power consumption, to be reduced while  $I_D$  is relatively low or for  $I_{G,steady}$  to increase when is  $I_D$  higher. A simplified version of this topology is shown in Figure 16, additional information will be available in the future at <http://www.genesicsemi.com/commercial-sic/sic-junction-transistors/>.

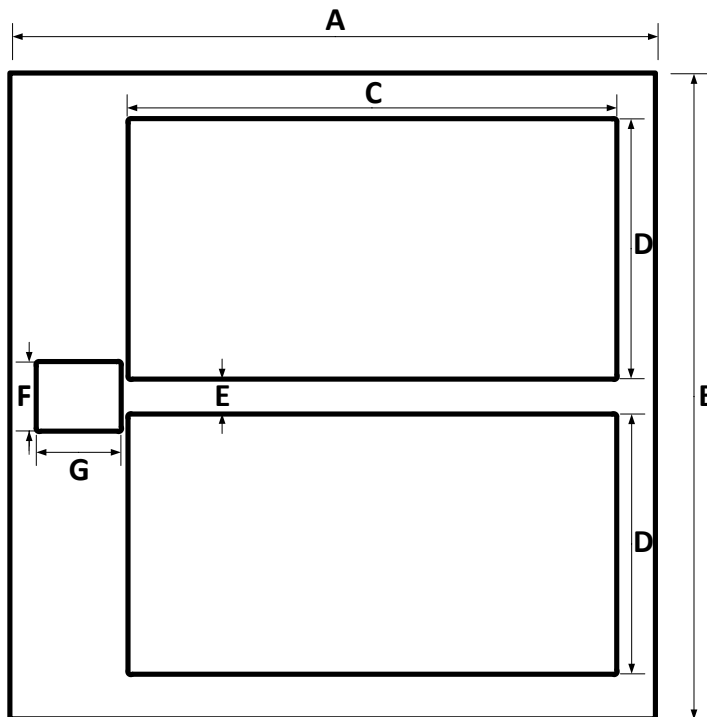


**Figure 16: Simplified Current Controlled Proportional Driver**

**Mechanical Parameters**

Die Dimensions	4.35 x 4.35	mm <sup>2</sup>	171 x 171	mil <sup>2</sup>
Die Area total / active	18.92/16.56	mm <sup>2</sup>	29330/25677	mil <sup>2</sup>
Die Thickness	360	μm	14	mil
Wafer Size	100	mm	3937	mil
Flat Position	0	deg	0	deg
Die Frontside Passivation	Polyimide			
Gate/Source Pad Metallization	4000 nm Al			
Bottom Drain Pad Metallization	400 nm Ni + 200 nm Au			
Die Attach	Electrically conductive glue or solder			
Wire Bond	Al ≤ 12 mil (Source) Al ≤ 5 mil (Gate)			
Reject ink dot size	Φ ≥ 0.3 mm			
Recommended storage environment	Store in original container, in dry nitrogen, < 6 months at an ambient temperature of 23 °C			

**Chip Dimensions:**



		mm	mil
DIE	A	4.35	171
	B	4.35	171
SOURCE WIREBONDABLE	C	3.30	130
	D	1.75	69
	E	0.24	9
GATE WIREBONDABLE	F	0.46	18
	G	0.57	22



**Revision History**

Date	Revision	Comments	Supersedes
2015/02/09	3	Updated Electrical Characteristics	
2014/08/26	2	Updated Electrical Characteristics	
2014/03/03	1	Updated Electrical Characteristics	
2013/12/04	0	Initial release	

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## SPICE Model Parameters

This is a secure document. Please copy this code from the SPICE model PDF file on our website [http://www.genesicsemi.com/images/hit\\_sic/baredie/sjt/GA50JT06-CAL\\_SPICE.pdf](http://www.genesicsemi.com/images/hit_sic/baredie/sjt/GA50JT06-CAL_SPICE.pdf) into LTSPICE (version 4) software for simulation of the GA50JT06-CAL.

```
*      MODEL OF GeneSiC Semiconductor Inc.
*
*      $Revision:   1.1           $
*      $Date:      03-Mar-2014   $
*
*      GeneSiC Semiconductor Inc.
*      43670 Trade Center Place Ste. 155
*      Dulles, VA 20166
*
*      COPYRIGHT (C) 2013 GeneSiC Semiconductor Inc.
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* These models are provided "AS IS, WHERE IS, AND WITH NO WARRANTY
* OF ANY KIND EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED
* TO ANY IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A
* PARTICULAR PURPOSE."
* Models accurate up to 2 times rated drain current.
*
.model GA50JT06 NPN
+ IS      5.00E-47
+ ISE     1.26E-28
+ EG      3.23
+ BF      106
+ BR      0.55
+ IKF     9000
+ NF      1
+ NE      2
+ RB      0.26
+ RE      0.01
+ RC      0.013
+ CJC     2.3989E-9
+ VJC     2.8346223
+ MJC     0.4846
+ CJE     6.026E-09
+ VJE     3.17915435
+ MJE     0.52951635
+ XTI     3
+ XTB     -1.2
+ TRC1    7.00E-3
+ VCEO    600
+ ICRATING 50
+ MFG     GeneSiC_Semiconductor

* End of GA50JT06-CAL SPICE Model
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