## MB90895 Series

## (Continued)

- Instruction system best suited to controller
- Wide choice of data types (bit, byte, word, and long word)
- Wide choice of addressing modes (23 types)
- Enhanced multiply-divide instructions and RETI instructions
- Enhanced high-precision computing with 32-bit accumulator
- Instruction system compatible with high-level language (C language) and multitask
- Employing system stack pointer
- Enhanced various pointer indirect instructions
- Barrel shift instructions
- Increased processing speed
- 4-byte instruction queue
- Powerful interrupt function with 8 levels and 34 factors
- Automatic data transfer function independent of CPU
- Extended intelligent l/O service function ( $\mathrm{El}^{2} \mathrm{OS}$ ): Maximum of 16 channels


## - Low power consumption (standby) mode

- Sleep mode (a mode that halts CPU operating clock)
- Time-base timer mode (a mode that operates oscillation clock, sub clock, time-base timer and watch timer only)
- Watch mode (a mode that operates sub clock and watch timer only)
- Stop mode (a mode that stops oscillation clock and sub clock)
- CPU intermittent operation mode


## - Process

- CMOS technology
- I/O port
- General-purpose input/output port (CMOS output) :

| MB90F897/Y | $: 34$ ports (including 4 high-current output ports) |
| :--- | :--- |
| MB90F897S/YS $: 36$ ports (including 4 high-current output ports) |  |

- Timer
- Time-base timer, watch timer, watchdog timer: 1 channel
- 8/16-bit PPG timer: 8-bit x 4 channels, or 16 -bit x 2 channels
- 16-bit reload timer: 2 channels
- 16-bit input/output timer
- 16-bit free run timer: 1 channel
- 16-bit input capture: (ICU): 4 channels

Interrupt request is issued upon latching a count value of 16-bit free run timer by detection of an edge on pin input.

- CAN controller: 1 channel
- Complied with Ver 2.0A and Ver 2.0B CAN specifications
- 8 built-in message buffers
- Transmission rate of 10 kbps to 1 Mbps (by 16 MHz machine clock)
- CAN wake-up
- UART0 (SCI), UART1(SCI): 2 channels
- Equipped with full-duplex double buffer
- Clock-asynchronous or clock-synchronous serial transmission is available.
- DTP/External interrupt: 4 channels, CAN wake-up: 1channel
- Module for activation of extended intelligent I/O service (EI²OS), and generation of external interrupt.


## - Delay interrupt generator module

- Generates interrupt request for task switching.
- 8/10-bit A/D converter: 8 channels
- Resolution is selectable between 8-bit and 10-bit.
- Activation by external trigger input is allowed.
- Conversion time: $6.125 \mu \mathrm{~s}$ (at $16-\mathrm{MHz}$ machine clock, including sampling time)


## - Program patch function

- Address matching detection for 2 address pointers.


## MB90895 Series

## (Continued)

|  | MB90F897  <br> MB90F897S MB90V495G <br> MB90F897Y (Under development)  <br> MB90F897YS (Under development)  |
| :---: | :---: |
| DTP/External interrupt | Number of inputs: 4 <br> Activated by rising edge, falling edge, " H " level or " L " level input. <br> External interrupt or extended intelligent I/O service (EI ${ }^{2} O S$ ) is available. |
| 8/10-bit A/D converter | Number of channels: 8 <br> Resolution: Selectable 10-bit or 8-bit. <br> Conversion time: $6.125 \mu \mathrm{~s}$ (at 16-MHz machine clock, including sampling time) <br> Sequential conversion of two or more successive channels is allowed. (Setting <br> a maximum of 8 channels is allowed.) <br> Single conversion mode : Selected channel is converted only once. <br> Sequential conversion mode: Selected channel is converted repetitively. <br> Halt conversion mode : Conversion of selected channel is stopped and activated alternately. |
| UART0 (SCI) | Number of channels: 1 <br> Clock-synchronous transfer: 62.5 kbps to 2 Mbps <br> Clock-asynchronous transfer: 1,202 bps to 62,500 bps <br> Communication is allowed by bi-directional serial communication function and master/slave type connection. |
| UART1 (SCI) | Number of channels: 1 <br> Clock-synchronous transfer: 62.5 kbps to 2 Mbps <br> Clock-asynchronous transfer: 9,615 bps to 500 kbps <br> Communication is allowed by bi-directional serial communication function and master/slave type connection. |
| CAN | Complied with Ver 2.0A and Ver 2.0B CAN specifications. 8 built-in message buffers. <br> Transmission rate of 10 kbps to 1 Mbps (by 16 MHz machine clock) CAN wake-up |

*1 : Settings of DIP switch S2 for using emulation pod MB2145-507. For details, see MB2145-507 Hardware Manual (2.7 Power Pin solely for Emulator).
*2 : MB90F897S/YS

## PACKAGES AND PRODUCT MODELS

| Package | MB90F897/S/Y/YS |
| :---: | :---: |
| FPT-48P-M26 | $\bigcirc$ |

: Yes, $\times$ : No
Note : Refer to "■ PACKAGE DIMENSION" for details of the package.

## MB90895 Series

## PRODUCT COMPARISON

## Memory space

When testing with test product for evaluation, check the differences between the product and a product to be used actually. Pay attention to the following points:

- The MB90V495G has no built-in ROM. However, a special-purpose development tool allows the operations as those of one with built-in ROM. ROM capacity depends on settings on a development tool.
- On MB90V495G, an image from FF4000н to FFFFFFF is viewed on 00 bank and an image of FE0000н to FF3FFFH is viewed only on FE bank and FF bank. (Modified on settings of a development tool.)
- On MB90F897/S/Y/YS, an image from FF4000н to FFFFFFн is viewed on 00 bank and an image of FF0000н to FF3FFFH is viewed only on FF bank.


## MB90895 Series

## PIN ASSIGNMENT

## (TOP VIEW)


(FPT-48P-M26)
*: MB90F897/Y : X1A, X0A
MB90F897S/YS : P36, P35

## MB90895 Series

## PIN DESCRIPTION

| Pin No. | Pin name | Circuit type | Function |
| :---: | :---: | :---: | :---: |
| 1 | AVcc | - | Vcc power input pin for A/D converter. |
| 2 | AVR | - | Power (Vreft) input pin for A/D converter. Use as input for Vcc or lower. |
| 3 to 10 | P50 to P57 | E | General-purpose input/output ports. |
|  | AN0 to AN7 |  | Functions as analog input pin for A/D converter. Valid when analog input setting is "enabled." |
| 11 | P37 | D | General-purpose input/output ports. |
|  | ADTG |  | Function as an external trigger input pin for A/D converter. Use the pin by setting as input port. |
| 12 | P20 | D | General-purpose input/output ports. |
|  | TIN0 |  | Function as an event input pin for reload timer 0 . Use the pin by setting as input port. |
| 13 | P21 | D | General-purpose input/output ports. |
|  | TOT0 |  | Function as an event output pin for reload timer 0 . Valid only when output setting is "enabled." |
| 14 | P22 | D | General-purpose input/output ports. |
|  | TIN1 |  | Function as an event input pin for reload timer 1. Use the pin by setting as input port. |
| 15 | P23 | D | General-purpose input/output ports. |
|  | TOT1 |  | Function as an event output pin for reload timer 1. Valid only when output setting is "enabled." |
| 16 to 19 | P24 to P27 | D | General-purpose input/output ports. |
|  | INT4 to INT7 |  | Functions as external interrupt input pin. Use the pin by setting as input port. |
| 20 | MD2 | F | Input pin for specifying operation mode. Connect directly to Vss. |
| 21 | MD1 | C | Input pin for specifying operation mode. Connect directly to Vcc. |
| 22 | MD0 | C | Input pin for specifying operation mode. Connect directly to Vcc. |
| 23 | $\overline{\mathrm{RST}}$ | B | External reset input pin. |
| 24 | Vcc | - | Power supply (5 V) input pin. |
| 25 | Vss | - | Power supply (0 V) input pin. |
| 26 | C | - | Capacitor pin for stabilizing power supply. Connect a ceramic capacitor of approximately $0.1 \mu \mathrm{~F}$. |
| 27 | X0 | A | Pin for high-rate oscillation. |
| 28 | X1 | A | Pin for high-rate oscillation. |
| 29 to 32 | P10 to P13 | D | General-purpose input/output ports. |
|  | IN0 to IN3 |  | Functions as trigger input pins of input capture channels 0 to 3 . Use the pins by setting as input ports. |

(Continued)

## MB90895 Series

(Continued)

| Pin No. | Pin name | $\begin{gathered} \hline \text { Circuit } \\ \text { type } \end{gathered}$ | Function |
| :---: | :---: | :---: | :---: |
| 33 to 36 | P14 to P17 | G | General-purpose input/output ports. High-current output ports. |
|  | PPG0 to PPG3 |  | Functions as output pin of PPG timers 01 and 23. Valid when output setting is "enabled." |
| 37 | P40 | D | General-purpose input/output port. |
|  | SIN1 |  | Serial data input pin for UART1. Use the pin by setting as input port. |
| 38 | P41 | D | General-purpose input/output port. |
|  | SCK1 |  | Serial clock input/output pin for UART1. Valid only when serial clock input/ output setting on UART1 is "enabled." |
| 39 | P42 | D | General-purpose input/output port. |
|  | SOT1 |  | Serial data output pin for UART1. Valid only when serial data output setting on UART1 is "enabled." |
| 40 | P43 | D | General-purpose input/output port. |
|  | TX |  | Transmission output pin for CAN. Valid only when output setting is "enabled." |
| 41 | P44 | D | General-purpose input/output port. |
|  | RX |  | Receive input pin for CAN. Use the pin by setting as input port. |
| 42 | P30 | D | General-purpose input/output port. |
|  | SOT0 |  | Serial data output pin for UARTO. Valid only when serial data output setting on UARTO is "enabled." |
| 43 | P31 | D | General-purpose input/output port. |
|  | SCK0 |  | Serial clock input/output pin for UARTO. Valid only when serial clock input/ output setting on UARTO is "enabled." |
| 44 | P32 | H | General-purpose input/output port. |
|  | SIN0 |  | Serial data input/output pin for UART0. Use the pin by setting as input port. |
| 45 | P33 | D | General-purpose input/output port. |
| 46 | X0A* | A | Pin for low-rate oscillation. |
|  | P35* |  | General-purpose input/output port. |
| 47 | X1A* | A | Pin for low-rate oscillation. |
|  | P36* |  | General-purpose input/output port. |
| 48 | AVss | - | Vss power supply input pin for A/D converter. |

[^0]
## MB90895 Series

## I/O CIRCUIT TYPE

| Type |  | Remarks <br> • High-rate oscillation feedback <br> resistor, approx. $1 \mathrm{M} \Omega$ |
| :---: | :---: | :---: | :---: |
| • Low-rate oscillation feedback |  |  |
| resistor, approx. $10 \mathrm{M} \Omega$ |  |  |

(Continued)
|

## MB90895 Series

## - Caution on Operations during PLL Clock Mode

- If the PLL clock mode is selected, the microcontroller attempt to be working with the self-oscillating circuit even when there is no external oscillator or external clock input is stopped. Performance of this operation, however, cannot be guaranteed.


## - Sequence of Turning on Power of A/D Converter and Applying Analog Input

- Be sure to turn on digital power (Vcc) before applying signals to the A/D converter and applying analog input signals (AN0 to AN7 pins).
- Be sure to turn off the power of $A / D$ converter and analog input before turning off the digital power supply.
- Be sure not to apply AVR exceeding AVcc when turning on and off. (No problems occur if analog and digital power is turned on and off simultaneously.)
- Handling Pins When A/D Converter is Not Used
- If the $A / D$ converter is not used, connect the pins under the following conditions: "AVcc=AVR=Vcc," and "AVss=Vss".
- Note on Turning on Power
- For preventing malfunctions on built-in step-down circuit, maintain a minimum of $50 \mu$ s of voltage rising time (between 0.2 V and 2.7 V ) when turning on the power.
- Stabilization of supply voltage
- A sudden change in the supply voltage may cause the device to malfunction even within the specified $\mathrm{V}_{\mathrm{cc}}$ supply voltage operating range. Therefore, the Vcc supply voltage should be stabilized.
For reference, the supply voltage should be controlled so that Vcc ripple variations (peak-to-peak values) at commercial frequencies ( $50 / 60 \mathrm{~Hz}$ ) fall below $10 \%$ of the standard V cc supply voltage and the coefficient of fluctuation does not exceed $0.1 \mathrm{~V} / \mathrm{ms}$ at instantaneous power switching.
- Support for $+\mathbf{1 2 5}^{\circ} \mathrm{C} /+150^{\circ} \mathrm{C}$
- Users considering application exceeding $\mathrm{T}_{\mathrm{A}}=+105^{\circ} \mathrm{C}$ are advised to contact their representatives beforehand for reliability limitations.


## MB90895 Series

## BLOCK DIAGRAM



## MB90895 Series

## MEMORY MAP

## 1. Memory allocation of MB90895

MB90895 series model outputs 24-bit wide internal address bus and up to 24 -bit of external address bus. A maximum of 16 Mbyte memory space of external access memory is accessible.

## 2. Memory map


: Internal access memory
: Access disallowed

* : On MB90F897/S/Y/YS, to read "FE0000н" to "FEFFFFн" is to read out "FF0000" to "FFFFFFн".

Note : When internal ROM is operating, F²MC-16LX allows viewing ROM data image on FF bank at upper-level of 00 bank. This function is called "mirroring ROM," which allows effective use of $C$ compiler small model. $\mathrm{F}^{2} \mathrm{MC}-16 \mathrm{LX}$ assigns the same low order 16 -bit address to FF bank and 00 bank, which allows referencing table in ROM without specifying "far" using pointer.
For example, when accessing to " 00 C 000 h ", ROM data at "FFC000н" is accessed actually. However, because ROM area of FF bank exceeds 48 Kbytes, viewing all areas is not possible on 00 bank image. Because ROM data of "FF4000н" to "FFFFFFF"" is viewed on " 004000 н" to " 00 FFFFF" image, store a ROM data table in area "FF4000н" to "FFFFFFн."

## MB90895 Series

## I/O MAP

| Address | Register abbreviation | Register | Read/ Write | Resource | Initial value |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 000000н | (Reserved area) * |  |  |  |  |
| 000001н | PDR1 | Port 1 data register | R/W | Port 1 | XXXXXXXX |
| 000002н | PDR2 | Port 2 data register | R/W | Port 2 | XXXXXXXX |
| 000003н | PDR3 | Port 3 data register | R/W | Port 3 | ХХХХХХХХХв |
| 000004н | PDR4 | Port 4 data register | R/W | Port 4 | XXXXXXXX |
| 000005н | PDR5 | Port 5 data register | R/W | Port 5 | XXXXXXXX |
| $\begin{array}{\|c\|} \hline 00000 \mathrm{H}_{\mathrm{H}} \\ \text { to } \\ 000010_{\mathrm{H}} \end{array}$ | (Reserved area) * |  |  |  |  |
| 000011н | DDR1 | Port 1 direction data register | R/W | Port 1 | 00000000в |
| 000012н | DDR2 | Port 2 direction data register | R/W | Port 2 | 00000000в |
| 000013н | DDR3 | Port 3 direction data register | R/W | Port 3 | 000X0000в |
| 000014н | DDR4 | Port 4 direction data register | R/W | Port 4 | XXX00000в |
| 000015 ${ }^{\text {H }}$ | DDR5 | Port 5 direction data register | R/W | Port 5 | 00000000в |
| $\begin{array}{\|c\|} \hline 000016 н \\ \text { to } \\ 00001 \text { A }_{H} \end{array}$ | (Reserved area) * |  |  |  |  |
| 00001Bн | ADER | Analog input permission register | R/W | 8/10-bit <br> A/D converter | 1111111в |
| $\begin{array}{\|c\|} \hline 00001 \mathrm{C}_{\mathrm{H}} \\ \text { to } \\ 00001 \mathrm{~F}_{\mathrm{H}} \end{array}$ | (Reserved area) * |  |  |  |  |
| 000020н | SMR0 | Serial mode register 0 | R/W | UARTO | 00000000в |
| 000021н | SCR0 | Serial control register 0 | R/W, W |  | 00000100в |
| 000022н | $\begin{aligned} & \hline \text { SIDR0/ } \\ & \text { SODRO } \end{aligned}$ | Serial input data register $0 /$ Serial output data register 0 | R, W |  | ХХХХХХХХХв |
| 000023н | SSR0 | Serial status register 0 | R, R/W |  | 00001X00в |
| 000024н | CDCR0 | Communication prescaler control register 0 | R/W |  | 0XXX1111в |
| 000025н | SES0 | Serial edge selection register 0 | R/W |  | XXXXXXX0в |
| 000026н | SMR1 | Serial mode register 1 | R/W | UART1 | 00000000в |
| 000027H | SCR1 | Serial control register 1 | R/W, W |  | 00000100 в |
| 000028H | $\begin{aligned} & \hline \text { SIDR1/ } \\ & \text { SODR1 } \end{aligned}$ | Serial input data register 1/ Serial output data register 1 | R, W |  | ХХХХХХХХХв |
| 000029н | SSR1 | Serial status data register 1 | R, R/W |  | 00001000в |
| 00002Ан | (Reserved area) * |  |  |  |  |
| 00002Bн | CDCR1 | Communication prescaler control register 1 | R/W | UART1 | 0XXX0000в |

(Continued)

## MB90895 Series

| Address | Register abbreviation | Register | Read/ Write | Resource | Initial value |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\begin{aligned} & \hline 00002 \mathrm{C}_{\mathrm{H}} \\ & \text { to } \\ & 00002 \mathrm{~F}_{\mathrm{H}} \end{aligned}$ | (Reserved area) * |  |  |  |  |
| 000030н | ENIR | DTP/External interrupt permission register | R/W | DTP/External interrupt | 00000000в |
| 000031н | EIRR | DTP/External interrupt source register | R/W |  | ХХХХХХХХХв |
| 000032н | ELVR | Detection level setting register | R/W |  | 00000000в |
| 000033н |  |  | R/W |  | 00000000в |
| 000034н | ADCS | A/D control status register | R/W | 8/10-bit <br> A/D converter | 00000000в |
| 000035н |  |  | R/W, W |  | 00000000в |
| 000036н | ADCR | A/D data register | W, R |  | Х XXXXXXX $^{\text {¢ }}$ |
| 000037н |  |  | R |  | 00101XXX |
| $\begin{gathered} 000038 \text { н } \\ \text { to } \\ 00003 \text { Eн }^{2} \end{gathered}$ | (Reserved area) * |  |  |  |  |
| 00003FH | PSCCR | PLL/Subclock control register | R/W, W | Clock | XXXX0000в |
| 000040н | PPGC0 | PPG0 operation mode control register | R/W, W | 8/16-bit PPG timer 0/1 | 0X000XX1в |
| 000041н | PPGC1 | PPG1 operation mode control register | R/W, W |  | 0X000001в |
| 000042н | PPG01 | PPG0/1 count clock selection register | R/W |  | 000000XХв |
| 000043н | (Reserved area) * |  |  |  |  |
| 000044н | PPGC2 | PPG2 operation mode control register | R/W, W | 8/16-bit PPG timer 2/3 | 0X000XX1в |
| 000045 ${ }^{\text {H }}$ | PPGC3 | PPG3 operation mode control register | R/W, W |  | 0X000001в |
| 000046H | PPG23 | PPG2/3 count clock selection register | R/W |  | 000000XХв |
| $\begin{array}{\|c\|} \hline 000047 \mathrm{H} \\ \text { to } \\ 00004 \mathrm{~F}_{\mathrm{H}} \end{array}$ | (Reserved area) * |  |  |  |  |

(Continued)

## MB90895 Series

| Address | Register abbreviation | Register | Read/ Write | Resource | Initial value |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 000050н | IPCP0 | Input capture data register 0 | R | 16-bit input/output timer | ХХХХХХХХВ |
| 000051н |  |  |  |  | ХХХХХХХХХв |
| 000052 H | IPCP1 | Input capture data register 1 | R |  | ХХХХХХХХХ |
| 000053н |  |  |  |  | XXXXXXXX |
| 000054н | ICS01 | Input capture control status register | R/W |  | 00000000в |
| 000055 ${ }^{\text {H }}$ | ICS23 |  |  |  | 00000000в |
| 000056н | TCDT | Timer counter data register | R/W |  | 00000000в |
| 000057H |  |  |  |  | 00000000в |
| 000058 H | TCCS | Timer counter control status register | R/W |  | 00000000в |
| 000059н |  | (Reserved | d area) * |  |  |
| 00005Ан | IPCP2 | Input capture data register 2 | R | 16-bit input/output timer | XXXXXXXX ${ }_{\text {¢ }}$ |
| 00005Вн |  |  |  |  | XXXXXXXX |
| 00005CH | IPCP3 | Input capture data register 3 | R |  | XXXXXXXX |
| 00005D |  |  |  |  | ХХХХХХХХХв |
| $\begin{gathered} 00005 \text { Ен } \\ \text { to } \\ 000065 \text { H } \end{gathered}$ | (Reserved area) * |  |  |  |  |
| 000066н | TMCSR0 | Timer control status register | R/W | 16-bit reload timer 0 | 00000000в |
| 000067H |  |  | R/W |  | XXXX0000в |
| 000068н | TMCSR1 |  | R/W | 16-bit reload timer 1 | 00000000в |
| 000069н |  |  | R/W |  | XXXX0000в |
| $\begin{aligned} & 00006 \text { Ан } \\ & \text { to } \\ & 00006 \mathrm{E} \end{aligned}$ | (Reserved area) * |  |  |  |  |
| 00006F ${ }_{\text {H }}$ | ROMM | ROM mirroring function selection register | W | ROM mirroring function selection module | XXXXXXX1в |
| $\begin{gathered} \text { 000070н } \\ \text { to } \\ 00007 \mathrm{~F}_{\mathrm{H}} \end{gathered}$ | (Reserved area) * |  |  |  |  |
| 000080н | BVALR | Message buffer enabling register | R/W | CAN controller | 00000000в |
| 000081н | (Reserved area) * |  |  |  |  |
| 000082н | TREQR | Send request register | R/W | CAN controller | 00000000в |
| 000083н | (Reserved area) * |  |  |  |  |
| 000084н | TCANR | Send cancel register | W | CAN controller | 00000000в |
| 000085 ${ }^{\text {H }}$ | (Reserved area) * |  |  |  |  |
| 000086н | TCR | Send completion register | R/W | CAN controller | 00000000в |

(Continued)

## MB90895 Series

| Address | Register abbreviation | Register | Read/ Write | Resource | Initial value |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 000087н | (Reserved area) * |  |  |  |  |
| 000088н | RCR | Receive completion register | R/W | CAN controller | 00000000в |
| 000089н | (Reserved area) * |  |  |  |  |
| 00008Ан | RRTRR | Receive RTR register | R/W | CAN controller | 00000000в |
| 00008Вн | (Reserved area) * |  |  |  |  |
| 00008CH | ROVRR | Receive overrun register | R/W | CAN controller | 00000000в |
| 00008D | (Reserved area) * |  |  |  |  |
| 00008Ен | RIER | Receive completion interrupt permission register | R/W | CAN controller | 00000000в |
| $\begin{array}{\|l} \hline 00008 \mathrm{~F}_{\mathrm{H}} \\ \text { to } \\ 00009 \mathrm{D}_{\mathrm{H}} \end{array}$ | (Reserved area) * |  |  |  |  |
| 00009Ен | PACSR | Address detection control register | R/W | Address matching detection function | 00000000в |
| 00009Fн | DIRR | Delay interrupt request generation/ release register | R/W | Delay interrupt generation module | XXXXXXX0в |
| 0000AOH | LPMCR | Lower power consumption mode control register | W,R/W | Lower power consumption mode | 00011000в |
| 0000A1н | CKSCR | Clock selection register | R,R/W | Clock | 11111100в |
| 0000A2н | PILR | Port input level selection register | R/W | I/O | 0000000Хв |
| $\begin{aligned} & \text { 0000АЗ } \\ & \text { to } \\ & 0000 \mathrm{~A} 7 \mathrm{H} \end{aligned}$ | (Reserved area) * |  |  |  |  |
| 0000A8н | WDTC | Watchdog timer control register | R,W | Watchdog timer | XXXXX111в |
| 0000A9н | TBTC | Time-base timer control register | R/W,W | Time-base timer | 1XX00100в |
| 0000ААн | WTC | Watch timer control register | R,R/W | Watch timer | 1X001000в |
| $\begin{aligned} & \hline 0000 \mathrm{ABH}_{\mathrm{H}} \text { to } \\ & 0000 \mathrm{ADH} \end{aligned}$ | (Reserved area) * |  |  |  |  |
| 0000АЕн | FMCS | Flash memory control status register | R,W,R/W | 512K-bit flash memory | 000X0000в |
| 0000AFH | (Reserved area) * |  |  |  |  |

(Continued)

## MB90895 Series

| Address | Register abbreviation | Register | Read/ Write | Resource | Initial value |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 0000ВОн | ICR00 | Interrupt control register 00 | R/W | Interrupt controller | 00000111в |
| 0000В1н | ICR01 | Interrupt control register 01 |  |  | 00000111в |
| 0000В2н | ICR02 | Interrupt control register 02 |  |  | 00000111в |
| 0000В3н | ICR03 | Interrupt control register 03 |  |  | 00000111в |
| 0000B4н | ICR04 | Interrupt control register 04 |  |  | 00000111в |
| 0000B5 | ICR05 | Interrupt control register 05 |  |  | 00000111в |
| 0000В6н | ICR06 | Interrupt control register 06 |  |  | 00000111в |
| 0000B7 ${ }_{\text {H }}$ | ICR07 | Interrupt control register 07 |  |  | 00000111в |
| 0000В8н | ICR08 | Interrupt control register 08 |  |  | 00000111в |
|  | ICR09 | Interrupt control register 09 |  |  | 00000111в |
| 0000ВАн | ICR10 | Interrupt control register 10 |  |  | 00000111в |
| 0000ВВн | ICR11 | Interrupt control register 11 |  |  | 00000111в |
| 0000BCH | ICR12 | Interrupt control register 12 |  |  | 00000111в |
| 0000BDн | ICR13 | Interrupt control register 13 |  |  | 00000111в |
| 0000ВЕн | ICR14 | Interrupt control register 14 |  |  | 00000111 ${ }_{\text {b }}$ |
| 0000BFн | ICR15 | Interrupt control register 15 |  |  | 00000111в |
| $\begin{array}{\|c\|} \hline 0000 \mathrm{C} 0_{H} \\ \text { to } \\ 0000 \mathrm{FF}_{\mathrm{H}} \end{array}$ | (Reserved area) * |  |  |  |  |
| 001FFOH | PADR0 | Detection address setting register 0 (low-order) | R/W | Address matching detection function | ХХХХХХХХХв |
| 001FF1H |  | Detection address setting register 0 (middle-order) |  |  | ХХХХХХХХв |
| 001FF2н |  | Detection address setting register 0 (high-order) |  |  | ХХХХХХХХХв |
| 001FF3н | PADR1 | Detection address setting register 1 (low-order) | R/W |  | ХХХХХХХХХв |
| 001FF4H |  | Detection address setting register 1 (middle-order) |  |  | XXXXXXXX |
| 001FF5 ${ }_{\text {H }}$ |  | Detection address setting register 1 (high-order) |  |  | XXXXXXXX |
| 003900н | TMR0/ <br> TMRLR0 | 16-bit timer register 0/16-bit reload register 0 | R,W | 16-bit reload timer 0 | ХХХХХХХХХв |
| 003901н |  |  |  |  | ХХХХХХХХ ${ }_{\text {¢ }}$ |
| 003902н | TMR1/ TMRLR1 | 16-bit timer register 1/16-bit reload register 1 | R,W | 16-bit reload timer 1 | ХХХХХХХХв |
| 003903н |  |  |  |  | ХХХХХХХХв |
| $\begin{gathered} \hline 003904 \text { н } \\ \text { to } \\ 003909 \text { н } \end{gathered}$ | (Reserved area) * |  |  |  |  |

(Continued)

## MB90895 Series

| Address | Register abbreviation | Register | Read/ Write | Resource | Initial value |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\begin{gathered} \hline 003 \mathrm{C} 2 \mathrm{CH}_{\mathrm{H}} \\ \text { to } \\ 003 \mathrm{C} 2 \mathrm{~F}_{\mathrm{H}} \end{gathered}$ | IDR7 | ID register 7 | R/W | CAN controller | $\begin{gathered} \hline \text { XXXXXXXXв } \\ \text { to } \\ \text { XXXXXXX } \end{gathered}$ |
| $\begin{aligned} & 003 \mathrm{C} 3 \mathrm{H}_{\mathrm{H}} \\ & 003 \mathrm{C} 31 \mathrm{H} \end{aligned}$ | DLCR0 | DLC register 0 | R/W |  | $\begin{aligned} & \text { ХХХХХХХХв } \\ & \text { XXXXXXXXB } \end{aligned}$ |
| $\begin{aligned} & \text { 003С32н } \\ & 003 \mathrm{C} 33 \mathrm{H} \end{aligned}$ | DLCR1 | DLC register 1 | R/W |  | $\begin{aligned} & \text { XXXXXXXXB }_{\text {BXXX }} \\ & \text { XXXXXX } \end{aligned}$ |
| $\begin{aligned} & 003 \mathrm{C} 34 \mathrm{H} \\ & 003 \mathrm{C} 35 \end{aligned}$ | DLCR2 | DLC register 2 | R/W |  | $\begin{aligned} & \text { ХХХХХХХХв } \\ & \text { XXXXXXXXB } \end{aligned}$ |
| $\begin{aligned} & 003 \mathrm{C} 36 \mathrm{H} \\ & 003 \mathrm{C} 37 \mathrm{H} \end{aligned}$ | DLCR3 | DLC register 3 | R/W |  | $\begin{aligned} & \text { XXXXXXXX } \\ & \text { XXXXXXXX } \end{aligned}$ |
| $\begin{aligned} & 003 \mathrm{C} 38 \mathrm{H} \\ & 003 \mathrm{C} 39_{\mathrm{H}} \end{aligned}$ | DLCR4 | DLC register 4 | R/W |  | $\begin{aligned} & \text { ХХХХХХХХв } \\ & \text { XXXXXXXXB } \end{aligned}$ |
| $\begin{aligned} & 003 \mathrm{C} 3 А н \\ & 003 \mathrm{C} 3 \mathrm{~B} \end{aligned}$ | DLCR5 | DLC register 5 | R/W |  | $\begin{aligned} & \text { XXXXXXXXB } \\ & \text { XXXXXXXX } \end{aligned}$ |
| $\begin{aligned} & \hline 003 \mathrm{C3CH} \\ & 003 \mathrm{C} 3 \mathrm{D} \end{aligned}$ | DLCR6 | DLC register 6 | R/W |  |  |
| $\begin{aligned} & \text { 003С3Ен } \\ & 003 \mathrm{C} 3 \mathrm{~F}_{\mathrm{H}} \end{aligned}$ | DLCR7 | DLC register 7 | R/W |  | $\begin{aligned} & \text { XXXXXXXX } \\ & \text { XXXXXXXX } \end{aligned}$ |
| $\begin{gathered} \text { 003C40н } \\ \text { to } \\ 003 \mathrm{C} 47 \mathrm{H} \end{gathered}$ | DTR0 | Data register 0 | R/W |  | $\begin{gathered} \text { XXXXXXXX } \\ \text { to } \\ \text { XXXXXXX } \end{gathered}$ |
| $\begin{gathered} \text { 003C48н } \\ \text { to } \\ 003 \mathrm{C} 4 \mathrm{~F}_{\mathrm{H}} \end{gathered}$ | DTR1 | Data register 1 | R/W |  | $\begin{gathered} \text { XXXXXXXX } \\ \text { to } \\ \text { XXXXXXX } \end{gathered}$ |
| $\begin{gathered} \text { 003C50н } \\ \text { to } \\ 003 \mathrm{C} 57 \mathrm{H} \end{gathered}$ | DTR2 | Data register 2 | R/W |  | $\begin{gathered} \text { XXXXXXXX } \\ \text { to } \\ \text { XXXXXXX } \end{gathered}$ |
| $\begin{gathered} \text { 003C58H } \\ \text { to } \\ 003 \mathrm{C} 5 \mathrm{FH} \end{gathered}$ | DTR3 | Data register 3 | R/W |  | $\begin{gathered} \text { XXXXXXXXв } \\ \text { to } \\ \text { XXXXXXX } \end{gathered}$ |
| $\begin{gathered} \text { 003C60н } \\ \text { to } \\ 003 \mathrm{C} 67 \mathrm{H} \end{gathered}$ | DTR4 | Data register 4 | R/W |  | $\begin{gathered} \text { XXXXXXXXв } \\ \text { to } \\ \text { XXXXXXX } \end{gathered}$ |
| $\begin{gathered} 003 \mathrm{C} 68 \mathrm{H} \\ \text { to } \\ 003 \mathrm{C} 6 \mathrm{FH} \end{gathered}$ | DTR5 | Data register 5 | R/W |  | $\begin{gathered} \text { XXXXXXXXB } \\ \text { to } \\ \text { XXXXXXXB } \end{gathered}$ |
| $\begin{gathered} 003 \mathrm{C} 70_{\mathrm{H}} \\ \text { to } \\ 003 \mathrm{C} 7 \mathrm{H}_{\mathrm{H}} \end{gathered}$ | DTR6 | Data register 6 | R/W |  | $\begin{gathered} \text { XXXXXXXX } \\ \text { to } \\ \text { XXXXXXX } \end{gathered}$ |
| $\begin{aligned} & \text { 003C78H } \\ & \text { to } \\ & 003 \mathrm{C} 7 \mathrm{FH} \end{aligned}$ | DTR7 | Data register 7 | R/W |  | $\begin{gathered} \text { XXXXXXXX } \\ \text { to } \\ \text { XXXXXXX } \end{gathered}$ |

(Continued)

## MB90895 Series

(Continued)

| Address | Register abbreviation | Register | Read/ Write | Resource | Initial value |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\begin{array}{\|c\|} \hline 003 \mathrm{C} 80_{\mathrm{H}} \\ \text { to } \\ 003 \mathrm{CFFF}_{\mathrm{H}} \\ \hline \end{array}$ | (Reserved area) * |  |  |  |  |
| $\begin{array}{l\|} \hline 003 \mathrm{DOOH} \\ \text { 003D01н } \end{array}$ | CSR | Control status register | R/W, R | CAN controller | $\begin{aligned} & \text { 0XXXX001в } \\ & \text { 00XXX000в } \end{aligned}$ |
| 003D02н | LEIR | Last event display register | R/W |  | 000XX000в |
| 003D03н | (Reserved area) * |  |  |  |  |
| $\begin{array}{\|l\|} \hline \text { 003D04н } \\ \text { 003D05н } \end{array}$ | RTEC | Send/receive error counter | R | CAN controller | $\begin{aligned} & \hline 00000000_{\text {в }} \\ & 00000000_{\text {в }} \end{aligned}$ |
| $\begin{array}{\|l\|} \hline 003 \mathrm{DO6H} \\ \text { 003D07H } \end{array}$ | BTR | Bit timing register | R/W |  | $\begin{aligned} & \text { 11111111в } \\ & \text { X1111111в } \end{aligned}$ |
| 003D08н | IDER | IDE register | R/W |  | ХХХХХХХХв |
| 003D09н | (Reserved area) * |  |  |  |  |
| 003D0Ан | TRTRR | Send RTR register | R/W |  | 00000000в |
| 003D0Bн | (Reserved area) * |  |  |  |  |
| 003D0CH | RFWTR | Remote frame receive wait register | R/W | CAN controller | ХХХХХХХХв |
| 003D0Dн | (Reserved area) * |  |  |  |  |
| 003D0Eн | TIER | Send completion interrupt permission register | R/W | CAN controller | 00000000 ${ }_{\text {B }}$ |
| 003D0F ${ }^{\text {¢ }}$ | (Reserved area) * |  |  |  |  |
| $\begin{array}{\|l\|} \hline \text { 003D10н } \\ \text { 003D11н } \end{array}$ | AMSR | Acceptance mask selection register | R/W | CAN controller | $\begin{aligned} & \text { XXXXXXXXB } \\ & \text { XXXXXXXXB }^{\text {( }} \end{aligned}$ |
| $\begin{array}{\|l\|} \hline \text { 003D12н } \\ \text { 003D13н } \end{array}$ | (Reserved area) * |  |  |  |  |
| $\begin{array}{\|c\|} \hline \text { 003D14H } \\ \text { to } \\ \text { 003D17H } \end{array}$ | AMR0 | Acceptance mask register 0 | R/W | CAN controller | $\begin{gathered} \hline \text { XXXXXXXX } \\ \text { to } \\ \text { XXXXXXXX } \end{gathered}$ |
| $\begin{array}{\|c\|} \hline \text { 003D18н } \\ \text { to } \\ 003 \mathrm{D} 1 \mathrm{BH} \end{array}$ | AMR1 | Acceptance mask register 1 | R/W | CAN controller | $\begin{gathered} \hline \text { XXXXXXXX } \\ \text { to } \\ \text { XXXXXXXXB } \\ \hline \end{gathered}$ |
| $\left\|\begin{array}{c} 003 \mathrm{D} 1 \mathrm{C}_{\mathrm{H}} \\ \text { to } \\ 003 \mathrm{DFF}_{\mathrm{H}} \end{array}\right\|$ | (Reserved area) * |  |  |  |  |
| $\begin{gathered} \hline 003 \mathrm{E} 00_{\mathrm{H}} \\ \text { to } \\ 003 \mathrm{EFF}_{\mathrm{H}} \end{gathered}$ | (Reserved area) * |  |  |  |  |
| $\begin{array}{\|c\|} \hline 003 F F O_{H} \\ \text { to } \\ 003 F F F_{H} \end{array}$ | (Reserved area) * |  |  |  |  |

Initial values :
0 : Initial value of this bit is " 0 ."
1 : Initial value of this bit is " 1 ."
$X$ : Initial value of this bit is undefined.
*: "Reserved area" should not be written anything. Result of reading from "Reserved area" is undefined.

## MB90895 Series

■ INTERRUPT SOURCES, INTERRUPT VECTORS, AND INTERRUPT CONTROL REGISTERS

| Interrupt source | $\mathrm{El}^{2} \mathrm{OS}$ readiness | Interrupt vector |  |  | Interrupt control register |  | Priority*3 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Num | ber | Address | ICR | Address |  |
| Reset | $\times$ | \#08 | 08н | FFFFDCH | - | - | High |
| INT 9 instruction | $\times$ | \#09 | 09н | FFFFD8н | - | - | $\uparrow$ |
| Exceptional treatment | $\times$ | \#10 | 0Ан | FFFFD4н | - | - |  |
| CAN controller reception completed (RX) | $\times$ | \#11 | OBн | FFFFD0н | ICR00 | $0000 \mathrm{B0} \mathrm{H}^{* 1}$ |  |
| CAN controller transmission completed (TX) / Node status transition (NS) | $\times$ | \#12 | OCH | FFFFCCC |  |  |  |
| Reserved | $\times$ | \#13 | 0D | FFFFC8\% | ICR01 | 0000B1н |  |
| Reserved | $\times$ | \#14 | ОЕн | FFFFC4 ${ }_{\text {¢ }}$ |  |  |  |
| CAN wakeup | $\Delta$ | \#15 | OFH | FFFFC0\% | ICR02 | 0000B2 ${ }^{* 1}$ |  |
| Time-base timer | $\times$ | \#16 | 10 H | FFFFBCH |  |  |  |
| 16-bit reload timer 0 | $\Delta$ | \#17 | 11н | FFFFB8 | ICR03 | 0000B3 ${ }^{* 1}$ |  |
| 8/10-bit A/D converter | $\Delta$ | \#18 | 12н | FFFFB4 ${ }_{\text {¢ }}$ |  |  |  |
| 16-bit free-run timer overflow | $\Delta$ | \#19 | 13н | FFFFB0н | ICR04 | 0000B4 ${ }^{* *}$ |  |
| Reserved | $\times$ | \#20 | 14н | FFFFACH |  |  |  |
| Reserved | $\times$ | \#21 | 15н | FFFFA8н | ICR05 | 0000B5 ${ }^{* 1}$ |  |
| PPG timer ch.0, ch. 1 underflow | $\times$ | \#22 | 16н | FFFFA4 |  |  |  |
| Input capture 0-input | $\Delta$ | \#23 | 17\% | FFFFA0н | ICR06 | 0000B6 ${ }^{* 1}$ |  |
| External interrupt (INT4/INT5) | $\Delta$ | \#24 | 18н | FFFF9C ${ }_{\text {н }}$ |  |  |  |
| Input capture 1-input | $\Delta$ | \#25 | 19н | FFFF98 | ICR07 | 0000B7 ${ }^{* 2}$ |  |
| PPG timer ch.2, ch. 3 underflow | $\times$ | \#26 | 1Ан | FFFF94 ${ }_{\text {¢ }}$ |  |  |  |
| External interrupt (INT6/INT7) | $\Delta$ | \#27 | 1Вн | FFFF90 ${ }_{\text {н }}$ | ICR08 | 0000B8 ${ }^{* 1}$ |  |
| Watch timer | $\Delta$ | \#28 | $1 \mathrm{CH}_{\mathrm{H}}$ | FFFF8CH |  |  |  |
| Reserved | $\times$ | \#29 | 1Dн | FFFF88 ${ }_{\text {¢ }}$ | ICR09 | 0000B9 ${ }^{* 1}$ |  |
| Input capture 2-input Input capture 3-input | $\times$ | \#30 | 1Ен | FFFF84 |  |  |  |
| Reserved | $\times$ | \#31 | 1FH | FFFF80 ${ }_{\text {н }}$ | ICR10 | $0000 \mathrm{BA}{ }^{* 1}$ |  |
| Reserved | $\times$ | \#32 | 20H | FFFF7C ${ }_{\text {H }}$ |  |  |  |
| Reserved | $\times$ | \#33 | 21н | FFFF78 | ICR11 | $0000 \mathrm{BB}^{* 1}$ |  |
| Reserved | $\times$ | \#34 | 22н | FFFF74 |  |  |  |
| Reserved | $\times$ | \#35 | 23H | FFFF70н | ICR12 | $0000 \mathrm{BCH}^{* 1}$ | $\downarrow$ |
| 16-bit reload timer 1 | $\bigcirc$ | \#36 | 24н | FFFF6C ${ }_{\text {н }}$ |  |  |  |

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## MB90895 Series

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| Interrupt source | El2OS readiness | Interrupt vector |  |  | Interrupt control register |  | Priority*3 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Nu | ber | Address | ICR | Address |  |
| UART1 reception completed | $\bigcirc$ | \#37 | 25- | FFFF68 ${ }_{\text {H }}$ | ICR13 | $0000 \mathrm{BD}{ }^{* 1}$ | $\begin{gathered} \text { High } \\ \uparrow \end{gathered}$ |
| UART1 transmission completed | $\Delta$ | \#38 | 26н | FFFFF64 |  |  |  |
| UARTO reception completed | $\bigcirc$ | \#39 | 27 ${ }^{\text {H }}$ | FFFF60 ${ }_{\text {н }}$ | ICR14 | $0000 \mathrm{BE} \mathrm{r}^{* 1}$ |  |
| UART0 transmission completed | $\Delta$ | \#40 | 28H | FFFF55 ${ }_{\text {н }}$ |  |  |  |
| Flash memory | $\times$ | \#41 | 29н | FFFF58 ${ }^{\text {H }}$ | ICR15 | $0000 \mathrm{BFH}^{*}{ }^{* 1}$ |  |
| Delay interrupt generation module | $\times$ | \#42 | 2 Ан | FFFF54 |  |  | $\begin{gathered} \downarrow \\ \text { Low } \end{gathered}$ |

$\bigcirc$ : Available
$\times$ : Unavailable
© : Available, El²OS stop function is provided.
$\Delta$ : Available when a cause of interrupt sharing a same ICR is not used.
*1 : • Peripheral functions sharing an ICR register have the same interrupt level.

- If peripheral functions share an ICR register, only one function is available when using extended intelligent I/O service.
- If peripheral functions share an ICR register, a function using extended intelligent I/O service does not allow interrupt by another function.
*2 : Only input capture 1 is ready for $\mathrm{El}^{2} \mathrm{OS}$. Because PPG is not ready for $\mathrm{El}^{2} \mathrm{OS}$, disable PPG interrupt when using El²OS with Input capture 1.
*3 : Priority when two or more interrupts of a same level occur simultaneously.


## MB90895 Series

## FLASH MEMORY CONFIGURATION

## - Sector configuration of 512 Kbit flash memory

| Flash memory | CPU address | Writer address* |
| :---: | :---: | :---: |
| SA0 (4 Kbytes) | FFOOOOH <br> FF0FFFH | $70000 \mathrm{H}$ <br> 70FFFH |
| SA1 (4 Kbytes) | FF1000н <br> FF1FFFH | $71000 \mathrm{H}$ <br> 71FFFH |
| SA2 (4 Kbytes) | FF2000H <br> FF2FFFH | $72000 \mathrm{H}$ <br> 72FFFH |
| SA3 (4 Kbytes) | FF3000H <br> FF3FFFH | $73000 \mathrm{H}$ <br> 73FFFH |
| SA4 (16 Kbytes) | FF4000H <br> FF7FFFH | $74000 \mathrm{H}$ <br> 77FFFH |
| SA5 (16 Kbytes) | FF8000H <br> FFBFFFн | $78000 \mathrm{H}$ <br> 7BFFFH |
| SA6 (4 Kbytes) | FFCOOOH <br> FFCFFFH | 7 COOOH <br> 7CFFFH |
| SA7 (4 Kbytes) | FFDOOOH <br> FFDFFFH | 7D000н <br> 7DFFF |
| SA8 (4 Kbytes) | FFE000н <br> FFEFFFH | 7 EOOOH <br> 7EFFFh |
| SA9 (4 Kbytes) | FFFOOOH <br> FFFFFFH | $7 \mathrm{FOOOH}$ <br> 7FFFFH |

*: "Writer address" is an address equivalent to CPU address, which is used when data is written on flash memory, using parallel writer. When writing/ deleting data with general-purpose writer, the writer address is used for writing and deleting.

## MB90895 Series

## ■ ELECTRIC CHARACTERISTICS

1. Absolute Maximum Rating

| Parameter | Symbol | Rating |  | Unit | Remarks |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Max |  |  |
| Power supply voltage*1 | V cc | Vss -0.3 | Vss +6.0 | V |  |
|  | AV cc | Vss -0.3 | Vss +6.0 | V | $\mathrm{V} \mathrm{cc}=\mathrm{AV}_{\text {cc }}{ }^{\text {2 }}$ |
|  | AVR | Vss -0.3 | Vss +6.0 | V | AV cc $\geq \mathrm{AVR}^{* 2}$ |
| Input voltage ${ }^{* 1}$ | $V_{1}$ | Vss -0.3 | Vss +6.0 | V | *3 |
| Output voltage* ${ }^{*}$ | Vo | Vss -0.3 | Vss +6.0 | V | *3 |
| Maximum clamp current | Iclamp | -2.0 | + 2.0 | mA | *7 |
| Total maximum clamp current | $\Sigma \mid$ Ilcamp \| | - | 20 | mA | *7 |
| "L" level maximum output current | loL1 | - | 15 | mA | Normal output*4 |
|  | loL2 | - | 40 | mA | High-current output*4 |
| "L" level average output current | lolav1 | - | 4 | mA | Normal output*5 |
|  | lolav2 | - | 30 | mA | High-current output*5 |
| "L" level maximum total output current | EloL1 | - | 125 | mA | Normal output |
|  | EloL2 | - | 160 | mA | High-current output |
| "L" level average total output current | Elolavi | - | 40 | mA | Normal output* |
|  | Eloav2 | - | 40 | mA | High-current output*6 |
| "H" level maximum output current | І ${ }_{\text {OH1 }}$ | - | -15 | mA | Normal output* |
|  | Іон2 | - | -40 | mA | High-current output*4 |
| "H" level average output current | lohav1 | - | -4 | mA | Normal output*5 |
|  | Іоhav2 | - | -30 | mA | High-current output*5 |
| "H" level maximum total output current | Eloh1 | - | -125 | mA | Normal output |
|  | इloн2 | - | -160 | mA | High-current output |
| "H" level average total output current | Elohav1 | - | -40 | mA | Normal output* ${ }^{\text {¢ }}$ |
|  | Elohav2 | - | -40 | mA | High-current output* ${ }^{*}$ |
| Power consumption | PD | - | 297 | mW |  |
| Operating temperature | TA | -40 | +105 | ${ }^{\circ} \mathrm{C}$ | Other than MB90F897Y/YS |
|  |  | -40 | +125 | ${ }^{\circ} \mathrm{C}$ | *8 <br> Other than MB90F897Y/YS |
|  |  | -40 | +150 | ${ }^{\circ} \mathrm{C}$ | $\begin{aligned} & \text { *8, *9 } \\ & \text { MB90F897Y/YS } \end{aligned}$ |
| Storage temperature | Tstg | -55 | +150 | ${ }^{\circ} \mathrm{C}$ |  |

*1: The parameter is based on $\mathrm{V}_{\mathrm{ss}}=\mathrm{AV}$ ss $=0.0 \mathrm{~V}$.
*2 : AVcc and AVR should not exceed Vcc.
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## MB90895 Series

(Continued)
*3: Vi and Vo should not exceed Vcc +0.3 V . However, if the maximum current to/from an input is limited by some means with external components, the Iclamp rating supersedes the $V_{1}$ rating.
*4: A peak value of an applicable one pin is specified as a maximum output current.
*5: An average current value of an applicable one pin within 100 ms is specified as an average output current. (Average value is found by multiplying operating current by operating rate.)
*6: An average current value of all pins within 100 ms is specified as an average total output current. (Average value is found by multiplying operating current by operating rate.)
*7 : • Applicable to pins: P10 to P17, P20 to P27, P30 to P33, P35, P36, P37, P40 to P44, P50 to P57 Note: P35 and P36 are MB90F897S/YS only.

- Use within recommended operating conditions.
- Use at DC voltage (current) .
- The +B signal should always be applied a limiting resistance placed between the +B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the $\mathrm{V}_{\mathrm{cc}}$ pin, and this may affect other devices.
- Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V ), the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the power-on reset.
- Care must be taken not to leave the +B input pin open.
- Note that analog system input/output pins other than the A/D input pins (LCD drive pins, comparator input pins, etc.) cannot accept +B signal input.
- Sample recommended circuits:
- Input/Output Equivalent circuits
+B input ( 0 V to 16 V )

*8 : Users considering application exceeding $\mathrm{T}_{\mathrm{A}}=+105^{\circ} \mathrm{C}$ are advised to contact their FUJITSU MICROELECTRONICS representatives beforehand for reliability limitations.
*9 : Use the PB circuit board which has 4 or more layers.
WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.


## MB90895 Series

2. Recommended Operating Conditions

| Parameter | Symbol | Value |  |  | Unit | Remarks |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |  |
| Power supply voltage | Vcc | 3.5 | 5.0 | 5.5 | V | Under normal operation |
|  |  | 3.0 | - | 5.5 | V | Retain status of stop operation |
|  |  | 4.0 | - | 5.5 | V | Accuracy guarantee voltage of $A / D$ converter |
| Smoothing capacitor | Cs | 0.1 | - | 1.0 | $\mu \mathrm{F}$ | *1 |
| Operating temperature | TA | -40 | - | +105 | ${ }^{\circ} \mathrm{C}$ | Other than MB90F897Y/YS |
|  |  | -40 | - | +125 | ${ }^{\circ} \mathrm{C}$ | *2 <br> Other than MB90F897Y/YS |
|  |  | -40 | - | +150 | ${ }^{\circ} \mathrm{C}$ | *2, *3 <br> MB90F897Y/YS |

*1 : Use a ceramic capacitor, or a capacitor of similar frequency characteristics. On the Vcc pin, use a bypass capacitor that has a larger capacity than that of Cs.
Refer to the following figure for connection of smoothing capacitor Cs.
*2: Users considering application exceeding $\mathrm{T}_{\mathrm{A}}=+105^{\circ} \mathrm{C}$ are advised to contact their FUJITSU MICROELECTRONICS representatives beforehand for reliability limitations.
*3 : Use the PB circuit board which has 4 or more layers.

- C pin connection diagram


WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.
Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.
No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

## MB90895 Series

## 3. DC Characteristics

- MB90F897/S (Models that support + $125{ }^{\circ} \mathrm{C}$ )
$\left(\mathrm{V} c \mathrm{cc}=5.0 \mathrm{~V} \pm 10 \%, \mathrm{~V}_{\mathrm{ss}}=\mathrm{AV} \mathrm{ss}=0.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}\right.$ to $\left.+125^{\circ} \mathrm{C}\right)$

| Parame ter | Sym bol | Pin name | Conditions | Value |  |  | Unit | Remarks |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | Min | Typ | Max |  |  |
| "H" level input voltage | V ${ }_{\text {не }}$ | CMOS hysteresis input pin | - | 0.8 Vcc | - | V cc +0.3 | V | When selected CMOS hysteresis |
|  | VIHA | Automotive input pin | - | 0.8 Vcc | - | V cc +0.3 | V | When selected Automotive |
|  | V нс $^{\text {c }}$ | CMOS input pin (P32, P40) | - | 0.7 Vcc | - | $\mathrm{Vcc}+0.3$ | V | When selected CMOS |
|  | Vінм | MD input pin | - | V cc -0.3 | - | $\mathrm{V}_{\mathrm{cc}}+0.3$ | V |  |
| "L" level input voltage | VıLS | CMOS <br> hysteresis input pin | - | Vss - 0.3 | - | 0.2 Vcc | V | When selected CMOS hysteresis |
|  | VILA | Automotive input pin | - | Vss - 0.3 | - | 0.5 Vcc | V | When selected Automotive |
|  | VILC | CMOS input pin (P32, P40) | - | Vss - 0.3 | - | 0.3 Vcc | V | When selected CMOS |
|  | VILM | MD input pin | - | Vss -0.3 | - | Vss +0.3 | V |  |
| "H" level output voltage | Vон1 | Pins other than P14 to P17 | $\begin{aligned} & \mathrm{V} \mathrm{cc}=4.5 \mathrm{~V}, \\ & \mathrm{loH}=-4.0 \mathrm{~mA} \end{aligned}$ | $\mathrm{Vcc}-0.5$ | - | - | V |  |
|  | Vон2 | P14 to P17 | $\begin{aligned} & \mathrm{V} \mathrm{cc}=4.5 \mathrm{~V}, \\ & \mathrm{loH}=-14.0 \mathrm{~mA} \end{aligned}$ | $\mathrm{Vcc}-0.5$ | - | - | V |  |
| "L" level output voltage | Vol1 | Pins other than P14 to P17 | $\begin{aligned} & \mathrm{V} \mathrm{cc}=4.5 \mathrm{~V}, \\ & \mathrm{loL}=4.0 \mathrm{~mA} \end{aligned}$ | - | - | 0.4 | V |  |
|  | Vol2 | P14 to P17 | $\begin{aligned} & \mathrm{V} \mathrm{cc}=4.5 \mathrm{~V}, \\ & \mathrm{loL}=20.0 \mathrm{~mA} \end{aligned}$ | - | - | 0.4 | V |  |
| Input leak current | IIL | All input pins | $\begin{aligned} & \mathrm{V}_{\mathrm{cc}}=5.5 \mathrm{~V}, \\ & \mathrm{~V}_{\mathrm{ss}}<\mathrm{V}_{1}<\mathrm{V}_{\mathrm{cc}} \end{aligned}$ | -5 | - | +5 | $\mu \mathrm{A}$ |  |
| Power supply current* | Icc | Vcc | $\mathrm{V}_{\mathrm{cc}}=5.0 \mathrm{~V} \text {, }$ <br> Internally operating at 16 MHz , normal operation. | - | 25 | 30 | mA |  |
|  |  |  | $\mathrm{V}_{\mathrm{cc}}=5.0 \mathrm{~V},$ <br> Internally operating at 16 MHz , writing on flash memory. | - | 45 | 50 | mA | MB90F897/S |
|  |  |  | $\mathrm{V}_{\mathrm{cc}}=5.0 \mathrm{~V}$, Internally operating at 16 MHz , deleting on flash memory. | - | 45 | 50 | mA | MB90F897/S |

[^1](Continued)

## MB90895 Series

(Continued)
$\left(\mathrm{Vcc}=5.0 \mathrm{~V} \pm 10 \%, \mathrm{~V}_{\mathrm{ss}}=\mathrm{AV} \mathrm{ss}=0.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}\right.$ to $\left.+125^{\circ} \mathrm{C}\right)$

| Parameter | Symbol | Pin name | Conditions | Value |  |  | Unit | Remarks |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | Min | Typ | Max |  |  |
| $\begin{aligned} & \text { Power } \\ & \text { supply } \\ & \text { current } \end{aligned}$ | Icos | Voc | $\mathrm{V}_{\mathrm{cc}}=5.0 \mathrm{~V},$ <br> Internally operating at 16 MHz , sleeping. | - | 8 | 12 | mA |  |
|  | Icts |  | $V_{c c}=5.0 \mathrm{~V},$ <br> Internally operating at 2 MHz , transition from main clock mode, in time-base timer mode. | - | 0.2 | 0.35 | mA |  |
|  | IcTsPII |  | $\mathrm{V}_{\mathrm{cc}}=5.0 \mathrm{~V},$ <br> Internally operating at 16 MHz , transition from PLL clock mode, in time-base timer mode. | - | 3 | 5 | mA |  |
|  | Iccl |  | $\mathrm{V}_{\mathrm{cc}}=5.0 \mathrm{~V},$ <br> Internally operating at 8 kHz , subclock operation, $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ | - | 40 | 100 | $\mu \mathrm{A}$ |  |
|  | Iccıs |  | $\mathrm{V}_{\mathrm{cc}}=5.0 \mathrm{~V},$ <br> Internally operating at 8 kHz , subclock, sleep mode, $T_{A}=+25^{\circ} \mathrm{C}$ | - | 10 | 50 | $\mu \mathrm{A}$ |  |
|  | Ісст |  | $\mathrm{V}_{\mathrm{cc}}=5.0 \mathrm{~V},$ <br> Internally operating at 8 kHz , watch mode, $T_{A}=+25^{\circ} \mathrm{C}$ | - | 8 | 30 | $\mu \mathrm{A}$ |  |
|  | Icch |  | Stopping, $T_{A}=+25^{\circ} \mathrm{C}$ | - | 5 | 25 | $\mu \mathrm{A}$ |  |
| Input capacity | Cin | Other than AV cc, AV ss, AVR, C, Vcc, Vss | - | - | 5 | 15 | pF |  |
| $\begin{array}{\|l\|} \hline \begin{array}{l} \text { Pull-up } \\ \text { resistor } \end{array} \end{array}$ | Rup | $\overline{\mathrm{RST}}$ | - | 25 | 50 | 100 | $\mathrm{k} \Omega$ |  |
| Pull-down resistor | Roown | MD2 | - | 25 | 50 | 100 | $\mathrm{k} \Omega$ | FLASH product is not provided with pull-down resistor |

* : Test conditions of power supply current are based on a device using external clock.


## MB90895 Series

- MB90F897Y/YS (Models that support $+\mathbf{1 5 0}^{\circ} \mathrm{C}$ ) (Under development)

| Parameter | Symbol | Pin name | Conditions | Value |  |  | Unit | Remarks |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | Min | Typ | Max |  |  |
| " H " levelinputvoltage | Vihs | CMOS hysteresis input pin | - | 0.8 Vcc | - | $\mathrm{Vcc}+0.3$ | V | When selected CMOS hysteresis |
|  | Viha | Automotive input pin | - | 0.8 Vcc | - | $\mathrm{Vcc}+0.3$ | V | When selected Automotive |
|  | Vінс | CMOS input pin (P32, P40) | - | 0.7 Vcc | - | $\mathrm{Vcc}+0.3$ | V | When selected CMOS |
|  | Vнм | MD input pin | - | Vcc - 0.3 | - | V cc +0.3 | V |  |
| "L" levelinputvoltage | VILs | CMOS hysteresis input pin | - | Vss - 0.3 | - | 0.2 Vcc | V | When selected CMOS hysteresis |
|  | VILA | Automotive input pin | - | Vss - 0.3 | - | 0.5 Vcc | V | When selected Automotive |
|  | Vilc | CMOS input pin (P32, P40) | - | Vss - 0.3 | - | 0.3 Vcc | V | When selected CMOS |
|  | VILM | MD input pin | - | Vss -0.3 | - | Vss +0.3 | V |  |
| "H" level output voltage | Vон1 | Pins other than P14 to P17 | $\begin{aligned} & \mathrm{V} \mathrm{Cc}=4.5 \mathrm{~V}, \\ & \mathrm{IOH}=-3.0 \mathrm{~mA} \end{aligned}$ | Vcc-0.5 | - | - | V |  |
|  | Vон2 | P14 to P17 | $\begin{aligned} & \mathrm{V}_{\mathrm{cc}}=4.5 \mathrm{~V}, \\ & \mathrm{loH}=-12.0 \mathrm{~mA} \end{aligned}$ | Vcc - 0.5 | - | - | V |  |
| "L" level output voltage | VoL1 | Pins other than P14 to P17 | $\begin{aligned} & \mathrm{V} \mathrm{cc}=4.5 \mathrm{~V}, \\ & \mathrm{loL}=3.0 \mathrm{~mA} \end{aligned}$ | - | - | 0.4 | V |  |
|  | VoL2 | P14 to P17 | $\begin{aligned} & \mathrm{V} \mathrm{Cc}=4.5 \mathrm{~V}, \\ & \mathrm{loL}=16 \mathrm{~mA} \end{aligned}$ | - | - | 0.4 | V |  |
| Input leak current | ILL | All input pins | $\begin{aligned} & \mathrm{V}_{\mathrm{cc}}=5.5 \mathrm{~V}, \\ & \mathrm{~V}_{\mathrm{ss}}<\mathrm{V}_{1}<\mathrm{V}_{\mathrm{cc}} \end{aligned}$ | -5 | - | +5 | $\mu \mathrm{A}$ |  |
| $\begin{aligned} & \text { Power } \\ & \text { supply } \\ & \text { current** } \end{aligned}$ | Icc | V cc | $\mathrm{V}_{\mathrm{cc}}=5.0 \mathrm{~V}$, Internally operating at 16 MHz , normal operation. | - | 25 | 32 | mA |  |
|  |  |  | $\mathrm{V}_{\mathrm{cc}}=5.0 \mathrm{~V},$ <br> Internally operating at 16 MHz , writing on flash memory. $\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C} \text { to }+125^{\circ} \mathrm{C}$ | - | 45 | 50 | mA | Up to $+125^{\circ} \mathrm{C}$ |
|  |  |  | $\mathrm{V}_{\mathrm{cc}}=5.0 \mathrm{~V},$ <br> Internally operating at 16 MHz , deleting on flash memory. $\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C} \text { to }+125^{\circ} \mathrm{C}$ | - | 45 | 50 | mA | Up to $+125^{\circ} \mathrm{C}$ |

*: Test conditions of power supply current are based on a device using external clock.
(Continued)

## MB90895 Series

(Continued)
$\left(\mathrm{V} \mathrm{Cc}=5.0 \mathrm{~V} \pm 10 \%, \mathrm{~V}\right.$ ss $=\mathrm{AV}$ ss $=0.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ )

| Parameter | $\begin{gathered} \text { Sym- } \\ \text { bol } \end{gathered}$ | Pin name | Conditions | Value |  |  | Unit | Remarks |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | Min | Typ | Max |  |  |
| Power supply current* | Iccs | Voc | $\mathrm{Vcc}=5.0 \mathrm{~V}$, Internally operating at 16 MHz , sleeping. | - | 8 | 14 | mA |  |
|  |  |  | $\mathrm{V}_{\mathrm{cc}}=5.0 \mathrm{~V}$, Internally operating at 2 MHz , transition from main clock mode, in time-base timer mode. $\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ | - | 0.2 | 0.35 | mA | Up to $+125^{\circ} \mathrm{C}$ |
|  | Icts |  | $\mathrm{V}_{\mathrm{cc}}=5.0 \mathrm{~V}$, Internally operating at 2 MHz , transition from main clock mode, in time-base timer mode. $\mathrm{T}_{\mathrm{A}}=+125^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ | - | 0.2 | T.B.D | mA |  |
|  | IctspII |  | $\mathrm{V}_{\mathrm{cc}}=5.0 \mathrm{~V}$, Internally operating at 16 MHz , transition from PLL clock mode, in time-base timer mode. | - | 3 | 7 | mA |  |
|  | Iccl |  | $\mathrm{V} \mathrm{cc}=5.0 \mathrm{~V},$ <br> Internally operating at 8 kHz , subclock operation, $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ | - | 40 | 100 | $\mu \mathrm{A}$ |  |
|  | Iccls |  | $\mathrm{V}_{\mathrm{cc}}=5.0 \mathrm{~V}$, Internally operating at 8 kHz , subclock, sleep mode, $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ | - | 10 | 50 | $\mu \mathrm{A}$ |  |
|  | Ісст |  | $\mathrm{V}_{\mathrm{cc}}=5.0 \mathrm{~V}$, Internally operating at 8 kHz , watch mode, $T_{A}=+25^{\circ} \mathrm{C}$ | - | 8 | 30 | $\mu \mathrm{A}$ |  |
|  | Іссн |  | Stopping, $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ | - | 5 | 25 | $\mu \mathrm{A}$ |  |
| Input capacity | Cin | Other than AVcc, AVss, AVR, C, Vcc, Vss | - | - | 5 | 15 | pF |  |
| $\begin{array}{\|l\|} \hline \text { Pull-up } \\ \text { resistor } \end{array}$ | Rup | RST | - | 25 | 50 | 100 | k $\Omega$ |  |
| Pull-down resistor | Roown | MD2 | - | 25 | 50 | 100 | k $\Omega$ | FLASH product is not provided with pull-down resistor |

*: Test conditions of power supply current are based on a device using external clock.
FUjITSU

## MB90895 Series

## 4. AC Characteristics

## (1) Clock timing

$\left(\mathrm{Vcc}=5.0 \mathrm{~V} \pm 10 \%, \mathrm{~V} s \mathrm{ss}=\mathrm{AV}\right.$ ss $=0.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C} /+150^{\circ} \mathrm{C}$ (only MB90F897Y/YS))

| Parameter | Symbol | Pin name | Value |  |  | Unit | Remarks |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Typ | Max |  |  |
| Clock frequency | fc | X0, X1 | 3 | - | 8 | MHz | When crystal or ceramic resonator is used |
|  |  |  | 3 | - | 16 | MHz | External clock |
|  |  |  | 4 | - | 16 | MHz | PLL multiplied by 1 |
|  |  |  | 4 | - | 8 | MHz | PLL multiplied by 2 |
|  |  |  | 4 | - | 5.33 | MHz | PLL multiplied by 3 |
|  |  |  | 4 | - | 4 | MHz | PLL multiplied by 4 |
|  | fct | X0A, X1A | - | 32.768 | - | kHz | MB90F897/Y only |
| Clock cycle time | thcyl | X0, X1 | 125 | - | 333 | ns |  |
|  | tLCyL | X0A, X1A | - | 30.5 | - | $\mu \mathrm{s}$ | MB90F897/Y only |
| Input clock pulse width | Рwh, Pwı | X0 | 10 | - | - | ns | Set duty factor at $30 \%$ to $70 \%$ as a guideline. |
|  | Pwır,Pwlı | X0A | - | 15.2 | - | $\mu \mathrm{s}$ | MB90F897/Y only |
| Input clock rise time and fall time | tcr, tcF | X0 | - | - | 5 | ns | When external clock is used |
| Internal operation clock frequency | fcp | - | 1.5 | - | 16 | MHz | When main clock is used |
|  | flcp | - | - | 8.192 | - | kHz | When sub clock is used, MB90F897/Y only |
| Internal operation clock cycle time | tcp | - | 62.5 | - | 666 | ns | When main clock is used |
|  | tıcp | - | - | 122.1 | - | $\mu \mathrm{s}$ | When sub clock is used, MB90F897/Y only |

- Clock timing



## MB90895 Series

- PLL operation guarantee range

> Relation between internal operation clock frequency and power supply voltage

Operation guarantee range of MB90F897/S/Y/YS


Relation among external clock frequency and internal clock frequency


* : fc is 8 MHz at maximum when crystal or ceramic resonator circuit is used.


## MB90895 Series

Rating values of alternating current is defined by the measurement reference voltage values shown below:

- Input signal waveform

Hysteresis input pin
VIH
VIL


- Output signal waveform

Output pin

(2) Reset input timing

| Parameter | Symbol | $\begin{gathered} \text { Pin } \\ \text { name } \end{gathered}$ | Conditions | Value |  | Unit | Remarks |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | Min | Max |  |  |
| Reset input time | trsti | $\overline{\mathrm{RST}}$ | - | 16 tcp*3 | - | ns | Normal operation |
|  |  |  |  | $\begin{aligned} & \text { Oscillation time } \\ & \text { of oscillator }{ }^{* 1}+ \\ & 100 \mu \mathrm{~s}+16 \text { tcp }^{* 3} \end{aligned}$ | - | - | In sub clock ${ }^{* 2}$, sub sleep ${ }^{* 2}$, watch ${ }^{\star 2}$ and stop mode |
|  |  |  |  | 100 | - | $\mu \mathrm{s}$ | In timebase timer |

*1 : Oscillation time of oscillator is time that the amplitude reached the $90 \%$. In the crystal oscillator, the oscillation time is between several ms to tens of ms . In ceramic oscillator, the oscillation time is between hundreds of $\mu \mathrm{s}$ to several ms . In the external clock, the oscillation time is 0 ms .
*2 : Except for MB90F897S/YS.
*3 : Refer to "(1) Clock timing" ratings for tcp (internal operation clock cycle time).

- In sub clock, sub sleep, watch and stop mode



## MB90895 Series

## (3) Power-on reset

| Parameter | Symbol | Pin name | Conditions | Value |  | Unit | Remarks |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | Min | Max |  |  |
| Power supply rise time | tR | Vcc | - | 0.05 | 30 | ms |  |
| Power supply shutdown time | toff | Vcc |  | 1 | - | ms | Repeated operation |



Note : Sudden change of power supply voltage may activate the power-on reset function. When changing power supply voltages during operation, raise the power smoothly by suppressing variation of voltages as shown below. When raising the power, do not use PLL clock. However, if voltage drop is $1 \mathrm{~V} /$ s or less, use of PLL clock is allowed during operation.


## MB90895 Series

- Internal shift clock mode

- External shift clock mode



## MB90895 Series

## 5. A/D converter

$\left(\mathrm{V}_{\mathrm{cc}}=\mathrm{A} \mathrm{V}_{\mathrm{cc}}=5.0 \mathrm{~V} \pm 10 \%, 3.0 \mathrm{~V} \leq \mathrm{AVR}-\mathrm{A} \mathrm{V}_{\mathrm{ss}}, \mathrm{V}_{\mathrm{ss}}=\mathrm{A} \mathrm{Vss}=0.0 \mathrm{~V}\right.$, $\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C} /+150^{\circ} \mathrm{C}$ (only MB90F897Y/YS)

| Parameter | Symbol | Pin name | Value |  |  | Unit | Remarks |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Typ | Max |  |  |
| Resolution | - | - | - | - | 10 | bit |  |
| Total error | - | - | - | - | $\pm 3.0$ | LSB |  |
| Nonlinear error | - | - | - | - | $\pm 2.5$ | LSB |  |
| Differential linear error | - | - | - | - | $\pm 1.9$ | LSB |  |
| Zero transition voltage | Vот | ANO to AN7 | $\begin{aligned} & \hline \mathrm{AV} \mathrm{ss}^{-} \\ & 1.5 \mathrm{LSB} \end{aligned}$ | $\begin{gathered} \mathrm{AVss}+ \\ 0.5 \mathrm{LSB} \end{gathered}$ | $\begin{gathered} \hline \mathrm{AV} \text { ss + } \\ 2.5 \mathrm{LSB} \end{gathered}$ | V | $1 \mathrm{LSB}=(\mathrm{AVR}-$ |
| Full-scale transition voltage | $V_{\text {fst }}$ | AN0 to AN7 | $\begin{gathered} \text { AVR - } \\ \text { 3.5 LSB } \end{gathered}$ | $\begin{gathered} \text { AVR - } \\ \text { 1.5 LSB } \end{gathered}$ | $\begin{gathered} \text { AVR + } \\ \text { 0.5 LSB } \end{gathered}$ | V | AVss) /1024 |
| Compare time | - | - | 66 tcp *1 | - | - | ns | With 16 MHz machine clock $5.5 \mathrm{~V} \geq \mathrm{AVcc} \geq 4.5 \mathrm{~V}$ |
|  |  |  | 88 tcp *1 | - | - | ns | With 16 MHz machine clock $4.5 \mathrm{~V}>\mathrm{AVcc} \geq 4.0 \mathrm{~V}$ |
| Sampling time | - | - | 32 tcp *1 | - | - | ns | With 16 MHz machine clock <br> $5.5 \mathrm{~V} \geq \mathrm{AVcc} \geq 4.5 \mathrm{~V}$ |
|  |  |  | 128 tcp*1 | - | - | ns | With 16 MHz machine clock $4.5 \mathrm{~V}>\mathrm{AV}$ cc $\geq 4.0 \mathrm{~V}$ |
| Analog port input current | lain | ANO to AN7 | - | - | 10 | $\mu \mathrm{A}$ |  |
| Analog input voltage | Vain | ANO to AN7 | AVss | - | AVR | V |  |
| Reference voltage | - | AVR | AV ss + 2.7 | - | AVcc | V |  |
| Power supply current | IA | AVcc | - | 3.5 | 7.5 | mA |  |
|  | IA | AV ${ }_{\text {cc }}$ | - | - | 5 | $\mu \mathrm{A}$ | *2 |
| Reference voltage supplying current | IR | AVR | - | 165 | 250 | $\mu \mathrm{A}$ |  |
|  | IRH | AVR | - | - | 5 | $\mu \mathrm{A}$ | *2 |
| Variation among channels | - | AN0 to AN7 | - | - | 4 | LSB |  |

*1 : Refer to "(1) Clock timing" ratings for tcp (internal operation clock cycle time).
*2 : If $A / D$ converter is not operating, a current when CPU is stopped is applicable (Vcc=AVcc=AVR=5.0 V).

## MB90895 Series

## 6. Definition of A/D Converter Terms

Resolution : Analog variation that is recognized by an A/D converter.
Linear error : Deviation between a line across zero-transition line ("00 00000000 " $\leftarrow \rightarrow$ "00 00000001 ") and full-scale transition line ("11 11111110 " $\hookleftarrow$ "11 11111111") and actual conversion characteristics.
Differential linear : Deviation of input voltage, which is required for changing output code by 1 LSB, from an error ideal value.

Total error : Difference between an actual value and an ideal value. A total error includes zero transition error, full-scale transition error, and linear error.

(Continued)

## MB90895 Series

## 7. Notes on A/D Converter Section

<About the external impedance of the analog input and its sampling time>

- A/D converter with sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting A/D conversion precision.

Analog input circuit model


Note : The values are reference values.
(Continued)

## MB90895 Series

(Continued)

- To satisfy the A/D conversion precision standard, consider the relationship between the external impedance and minimum sampling time and either adjust the resistor value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value.


The relationship between the external impedance and minimum sampling time

- If the sampling time cannot be sufficient, connect a capacitor of about $0.1 \mu \mathrm{~F}$ to the analog input pin.
<About errors>
- As $\mid$ AVR - AVss $\mid$ become smaller, values of relative errors grow larger.


## MB90895 Series

8. Flash Memory Program/Erase Characteristics*1

| Parameter | Conditions | Value |  |  | Unit | Remarks |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |  |
| Sector erase time <br> ( 4 KB sector) | $\begin{gathered} \mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}, \\ \mathrm{~V}_{\mathrm{CC}}=5.0 \mathrm{~V} \end{gathered}$ | - | 0.2 | 0.5 | s | Excludes 00 н programming prior to erasure |
| Sector erase time ( 16 KB sector) |  | - | 0.5 | 7.5 | s | Excludes 00 н programming prior to erasure |
| Chip erase time |  | - | 2.6 | - | s | Excludes 00 н programming prior to erasure |
| Word (16 bit width) programming time |  | - | 16 | 3,600 | $\mu \mathrm{s}$ | Except for the over head time of the system |
| Program/Erase cycle | - | 10,000 | - | - | cycle |  |
| Flash Data Retention Time | Average $\mathrm{T}_{\mathrm{A}}=+85^{\circ} \mathrm{C}$ | 20 | - | - | Years | *2 |

*1: For MB90F897Y/YS, it is prohibited to write or erase data in the range of $\mathrm{T}_{\mathrm{A}}=+125^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$.
*2: This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at $+85^{\circ} \mathrm{C}$ ).

## MB90895 Series

## EXAMPLE CHARACTERISTICS

## - MB90F897

$$
\mathrm{Icc}-\mathrm{Vcc}
$$

$\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$, In external clock operation $\mathrm{f}=$ Internal operating frequency



Iccl-Vcc
$\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$, In external clock operation $f=$ Internal operating frequency


## MB90895 Series

(Continued)
(Vсс - Vон) - Іон

$$
\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}, \mathrm{~V}_{\mathrm{cc}}=4.5 \mathrm{~V}
$$


Vol - lol

$$
\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}, \mathrm{~V}_{\mathrm{cc}}=4.5 \mathrm{~V}
$$


"H" level input voltage/ "L" level input voltage
Vin - Vcc

$$
\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}
$$



## MB90895 Series

## ■ ORDERING INFORMATION

| Part number | Package | Remarks |
| :--- | :---: | :---: |
| MB90F897PMT | 48-pin plastic LQFP |  |
| MB90F897SPMT | (FPT-48P-M26) |  |
| MB90F897YPMT |  |  |
| MB90F897YSPMT |  |  |

## MB90895 Series

## MAIN CHANGES IN THIS EDITION

| Page | Section | Change Results |
| :---: | :---: | :---: |
| - | - | Added the following part numbers under development. MB90F897Y, MB90F897YS |
| 1 | ■ FEATURES | Added as follows. <br> - Models that support $+150^{\circ} \mathrm{C}$ (MB90F897Y/YS) |
| 8 | - PIN DESCRIPTION | Corrected the function of pin SCKO on pin number 43. UART1 $\rightarrow$ UART0 |
| 11 | - HANDLING DEVICES | Corrected the description for "• Handling Unused Pins". unused input pins $\rightarrow$ unused I/O pins |
| 12 |  | "• Support for $+125^{\circ} \mathrm{C}$ " $\rightarrow$ <br> "• Support for $+125^{\circ} \mathrm{C} /+150^{\circ} \mathrm{C}$ " |
| 13 | - BLOCK DIAGRAM | Corrected the arrow for "pin X0 and X1" in the clock control circuit. <br> "input $\rightarrow$ " $\rightarrow$ "input/output $\longleftrightarrow$ " |
|  |  | Corrected the arrow for "pin TIN0 and pin TIN1" in 16-bit reload timer (2ch). <br> "output $\rightarrow$ " $\rightarrow$ "input $\leftarrow$ " |
| 23 | ■ INTERRUPT SOURCES, INTERRUPT VECTORS, AND INTERRUPT CONTROL REGISTERS | Corrected footnotes in the address column for ICR05 and ICR07 of the interrupt control register. $\begin{aligned} & 0000 \mathrm{~B} 5 \mathrm{H}^{* 2} \rightarrow 0000 \mathrm{~B} 5 \mathrm{H}^{\star 1} \\ & 10000 \mathrm{~B} 7 \mathrm{H}^{* 1} \rightarrow 0000 \mathrm{~B} 7 \mathrm{H}^{* 2} \end{aligned}$ |
| 24 |  | Corrected the description for footnote *2. 16-bit reload timer $\rightarrow$ Input capture 1 |
| - | ■ PERIPHERAL RESOURCES | Deleted the section <br> Refer to the hardware manual, for details of peripheral resources. |
| 25 | ■ FLASH MEMORY CONFIGURATION | Changed the item name from "PERIPHERAL RESOURCES" to "FLASH MEMORY CONFIGURATION". |
| 26 | - ELECTRIC CHARACTERISTICS <br> 1. Absolute Maximum Rating | Item: Added the rating value for MB90F897Y/YS to the operating temperature. <br> Min: - $40^{\circ} \mathrm{C}$, Max: $+150^{\circ} \mathrm{C}$ |
| 27 |  | Added footnote*9. |
| 28 | 2. Recommended Operating Conditions | Item: Added the rating value for MB90F897Y/YS to the operating temperature. <br> Min: - $40^{\circ} \mathrm{C}$,Max: $+150^{\circ} \mathrm{C}$ |
|  |  | Added footnote *3. |
| 31, 32 | 3. DC Characteristics | Added DC characteristics for "MB90F897Y/YS". |
| 33 to 40 | 4. AC Characteristics | Changed the condition description in the upper right of the table.$\begin{aligned} & \mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C} \text { to }+125^{\circ} \mathrm{C} \rightarrow \\ & \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \mathrm{C} \text { to }+125^{\circ} \mathrm{C} /+150^{\circ} \mathrm{C} \text { (Only MB90F897Y/YS) } \end{aligned}$ |
|  | 5. A/D converter |  |
| 49 | ■ ORDERING INFORMATION | Added the following part numbers. MB90F897YPMT, MB90F897YSPMT |

The vertical lines marked in the left side of the page show the changes.

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[^0]:    *: MB90F897/Y : X1A, X0A
    MB90F897S/YS : P36, P35

[^1]:    * : Test conditions of power supply current are based on a device using external clock.

