NEC Electronics Inc.

μPB100470
4,096 x 1-BIT
100K ECL RAM

T-46-23-05

Description

The μPB100470 is a very high-speed 100K interface ECL RAM with full voltage and temperature compensation. The device is organized as 4K words by 1 bit, and is designed with an open emitter output (noninverted) for low power consumption. Two fast access time versions are available: 10 ns maximum and 15 ns maximum. The μPB100470 is available in a hermetic, 300-mil, 18-pin cerdip.

Features

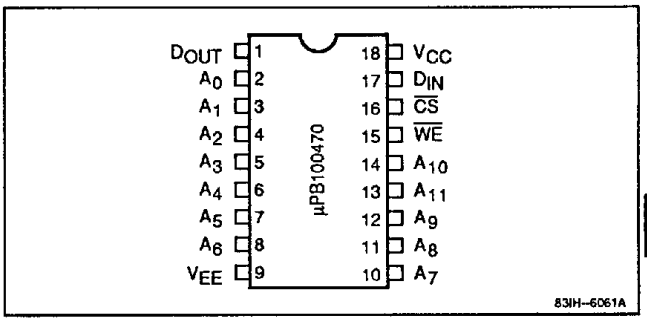
- 4,096-word x 1-bit organization
- 100K ECL interface with full voltage and temperature compensation
- Open emitter output (noninverted)
- Fast access times
- Low power consumption
- 300-mil, 18-pin cerdip packaging

Ordering Information

Part Number	Access Time (max)	Package
μPB100470D-10	10 ns	18-pin cerdip
D-15	15 ns	

Pin Configuration

18-Pin Cerdip



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Pin Identification

Symbol	Function
A_0 - A_{11}	Address Inputs
D_{IN}	Data input
D_{OUT}	Data output
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
V_{CC}	Ground
V_{EE}	−4.5-volt power supply

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Absolute Maximum Ratings

Supply voltage, V_{EE} to V_{CC}	−7.0 to +0.5 V
Input voltage, V_{IN}	V_{EE} to +0.5 V
Output current, I_{OUT}	−30 to +0.1 mA
Storage temperature, T_{STG}	−65 to +150°C
Storage temperature under bias, T_{STG} (bias)	−55 to +125°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_{IN}		4		pF
Output capacitance	C_{OUT}		5		pF

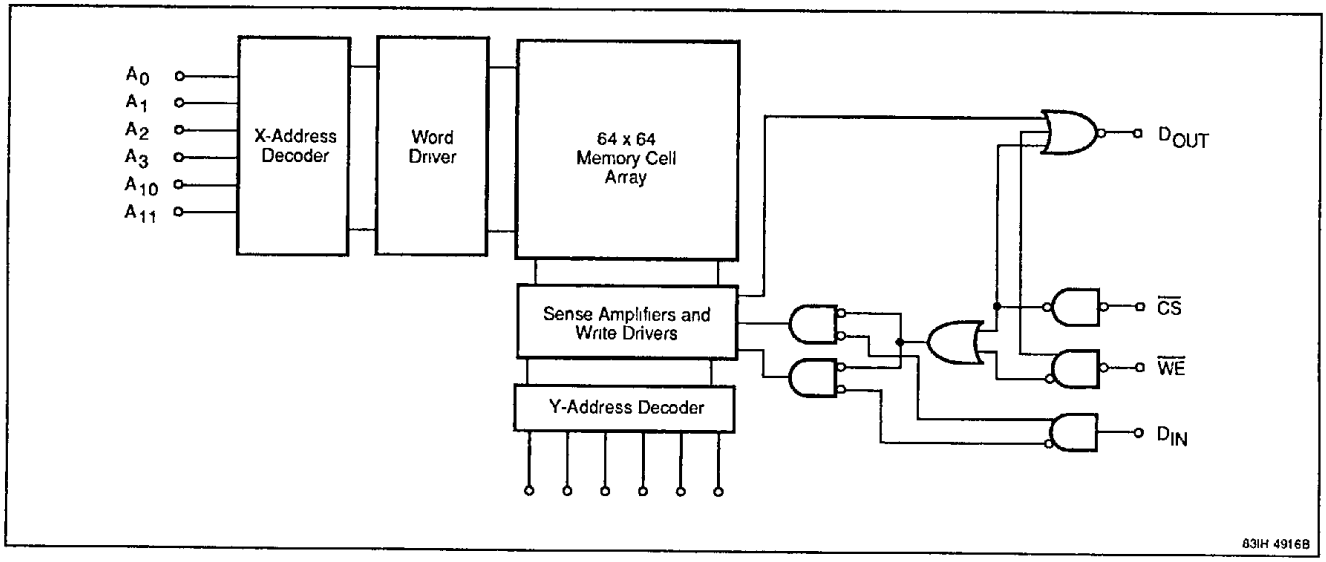
Truth Table

$\overline{CS}$	$\overline{WE}$	D_{IN}	Function	Output
H	X	X	Not selected	L
L	L	L	Write 0	L
L	L	H	Write 1	L
L	H	X	Read	D_{OUT}

Notes:

(1) X = don't care.

Block Diagram



DC Characteristics

T_A = 0 to +85°C; V_{EE} = −4.5 V; output load = 50 Ω to −2.0 V

Parameter	Symbol	Min	Max	Unit	Test Conditions
Output voltage, high	V_{OH}	−1025	−880	mV	V_{IN} = V_{IH} (max) or V_{IL} (min)
Output voltage, low	V_{OL}	−1810	−1620	mV	
Output threshold voltage, high	V_{OHC}	−1035		mV	V_{IN} = V_{IH} (min) or V_{IL} (max)
Output threshold voltage, low	V_{OLC}		−1610	mV	
Input voltage, high	V_{IH}	−1165	−880	mV	Guaranteed input voltage high for all inputs
Input voltage, low	V_{IL}	−1810	−1475	mV	Guaranteed input voltage low for all inputs
Input current, high	I_{IH}		220	μA	V_{IN} = V_{IH} (max)
Input current, low	I_{IL}	0.5	170	μA	For $\overline{CS}$: V_{IN} = V_{IL} (min)
		−50		μA	For all others: V_{IN} = V_{IL} (min)
Supply current	I_{EE}	−220		mA	All inputs and outputs open

Notes:

(1) The device under test (DUT) is mounted in a test socket and is measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

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AC Characteristics

T_A = 0 to +85°C; V_{EE} = −4.5 V ± 5%

		μPB100470-10			μPB100470-15				
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions
Read Operation									
Address access time	t_{AA}			10			15	ns	
Chip select access time	t_{ACS}			6			8	ns	
Chip select recovery time	t_{RCS}			6			8	ns	
Write Operation									
Write pulse width	t_W	10			15			ns	
Data setup time	t_{WSD}	2			2			ns	
Data hold time	t_{WHD}	2			2			ns	
Address setup time	t_{WSA}	3			3			ns	
Address hold time	t_{WHA}	2			2			ns	
Chip select setup time	t_{WSCS}	2			2			ns	
Chip select hold time	t_{WHCS}	2			2			ns	
Write disable time	t_{WS}			6			8	ns	
Write recovery time	t_{WR}			10			10	ns	
Output Rise and Fall Times									
Rise time	t_R		2			2		ns	
Fall time	t_F		2			2		ns	

Notes:

(1) The device under test (DUT) is mounted in a test socket and is measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

Figure 1. Loading Conditions Test Circuit

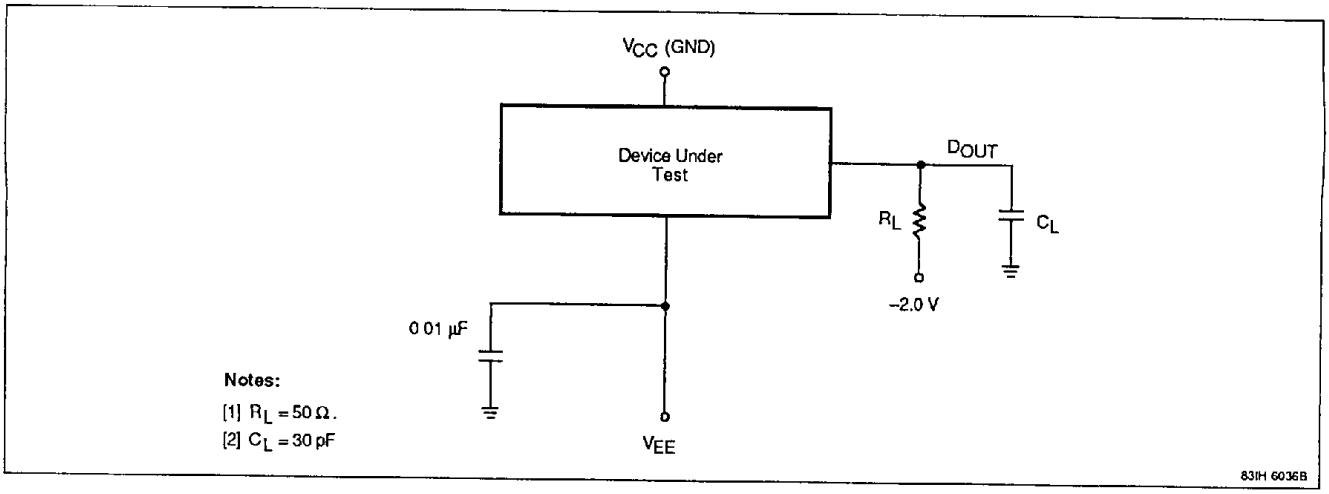
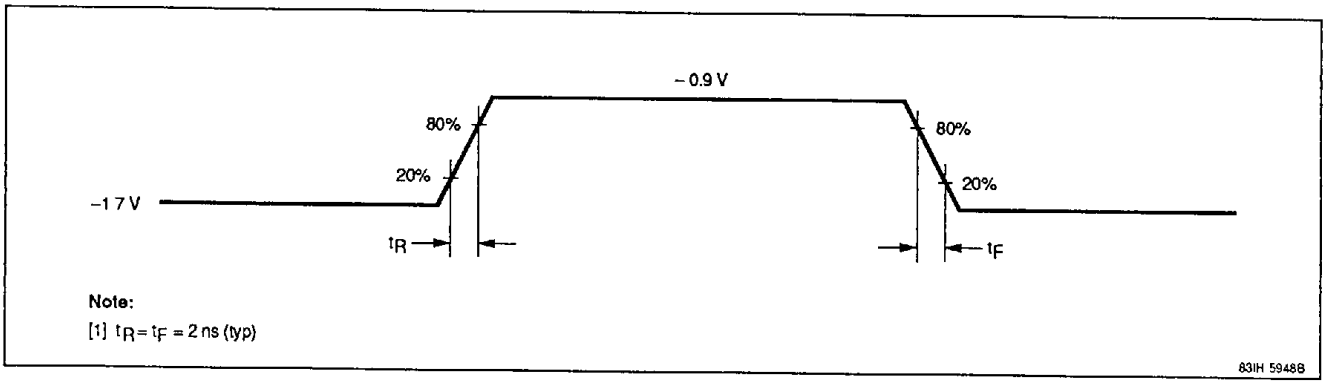
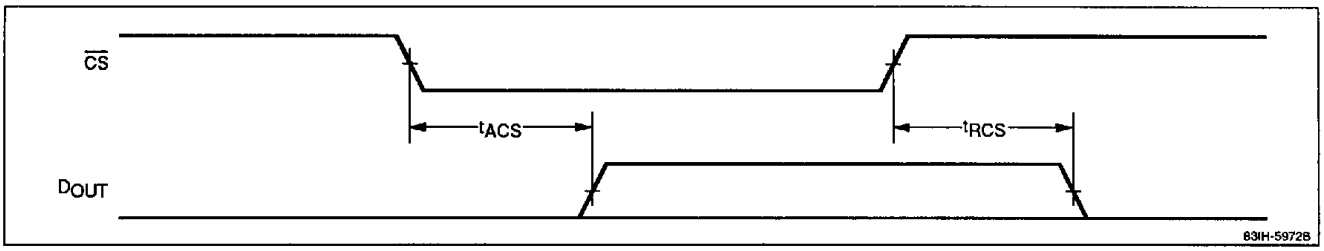


Figure 2. Input Pulse

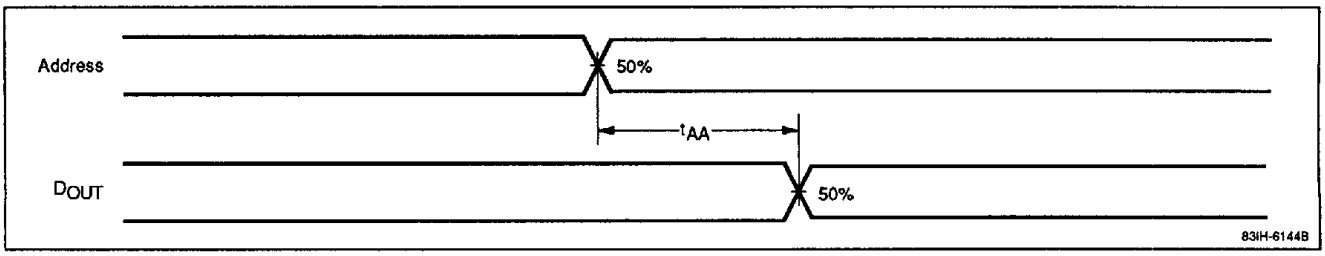


Timing Waveforms

Chip Select Access Cycle



Address Access Cycle



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Write Cycle