

# 74VHC08-Q100; 74VHCT08-Q100

Quad 2-input AND gate

Rev. 1 — 20 December 2013

Product data sheet

## 1. General description

The 74VHC08-Q100; 74VHCT08-Q100 are high-speed Si-gate CMOS devices and are pin compatible with Low-power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard JESD7-A.

The 74VHC08-Q100; 74VHCT08-Q100 provide the quad 2-input AND function.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

## 2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - ◆ Specified from  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$  and from  $-40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$
- Balanced propagation delays
- All inputs have a Schmitt-trigger action
- Inputs accept voltages higher than  $V_{CC}$
- Input levels:
  - ◆ The 74VHC08-Q100 operates with CMOS logic levels
  - ◆ The 74VHCT08-Q100 operates with TTL logic levels
- ESD protection:
  - ◆ MIL-STD-883, method 3015 exceeds 2000 V
  - ◆ HBM JESD22-A114F exceeds 2000 V
  - ◆ MM JESD22-A115-A exceeds 200 V ( $C = 200\text{ pf}$ ,  $R = 0\text{ }\Omega$ )
- Multiple package options

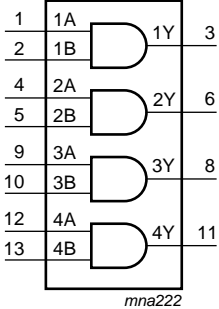


3. Ordering information

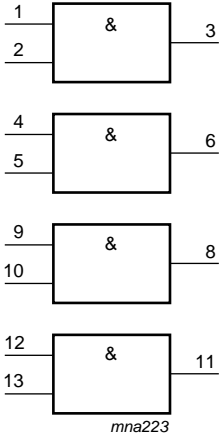
Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74VHC08D-Q100 74VHCT08D-Q100	−40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74VHC08PW-Q100 74VHCT08PW-Q100	−40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74VHC08BQ-Q100 74VHCT08BQ-Q100	−40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1

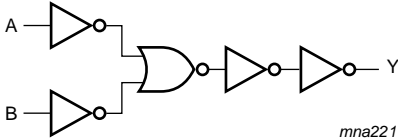
4. Functional diagram



**Fig 1. Logic symbol**



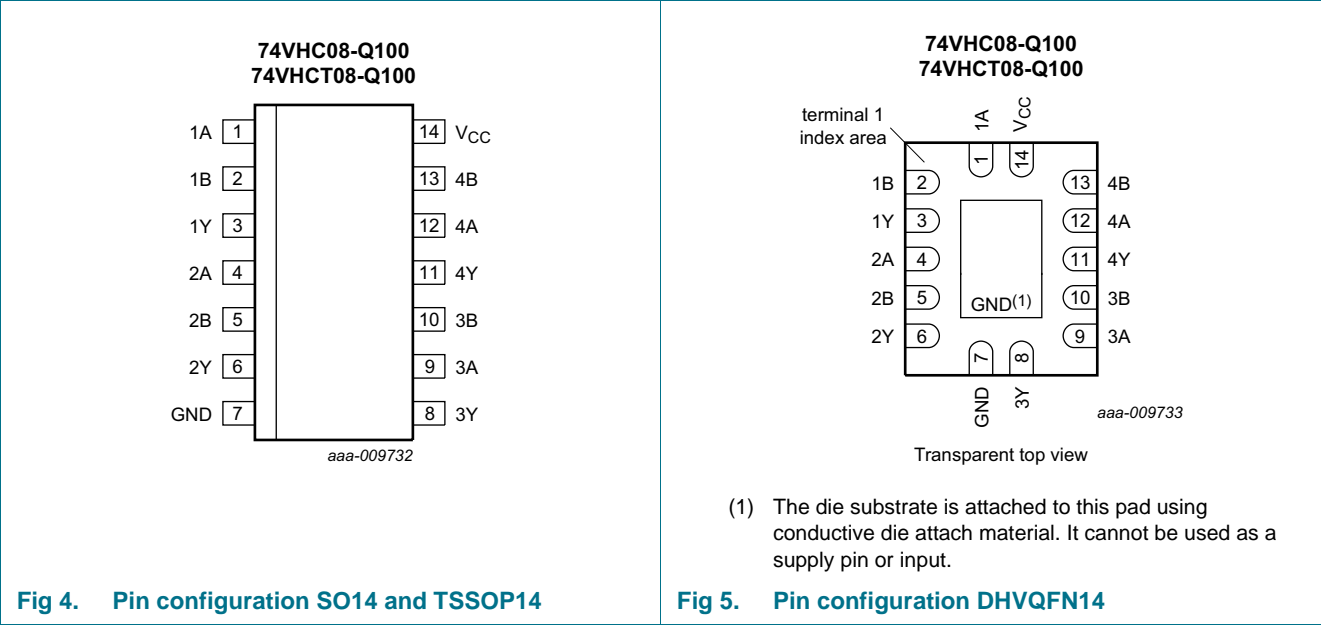
**Fig 2. IEC logic symbol**



**Fig 3. Logic diagram (one gate)**

5. Pinning information

5.1 Pinning



5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1A	1	data input
1B	2	data input
1Y	3	data output
2A	4	data input
2B	5	data input
2Y	6	data output
GND	7	ground (0 V)
3Y	8	data output
3A	9	data input
3B	10	data input
4Y	11	data output
4A	12	data input
4B	13	data input
V <sub>CC</sub>	14	supply voltage

## 6. Functional description

Table 3. Function selection<sup>[1]</sup>

Input		Output
nA	nB	nY
L	X	L
X	L	L
H	H	H

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care

## 7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+7.0	V
$V_I$	input voltage		-0.5	+7.0	V
$I_{IK}$	input clamping current	$V_I < -0.5$ V	<sup>[1]</sup> -20	-	mA
$I_{OK}$	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V	<sup>[1]</sup> -	±20	mA
$I_O$	output current	$V_O = -0.5$ V to $(V_{CC} + 0.5$ V)	-	±25	mA
$I_{CC}$	supply current		-	75	mA
$I_{GND}$	ground current		-75	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40$ °C to +125 °C			
	SO14 package		<sup>[2]</sup> -	500	mW
	TSSOP14 package		<sup>[3]</sup> -	500	mW
	DHVQFN14 package		<sup>[4]</sup> -	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2]  $P_{tot}$  derates linearly with 8 mW/K above 70 °C.

[3]  $P_{tot}$  derates linearly with 5.5 mW/K above 60 °C.

[4]  $P_{tot}$  derates linearly with 4.5 mW/K above 60 °C.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	74VHC08-Q100			74VHCT08-Q100			Unit
			Min	Typ	Max	Min	Typ	Max	
V <sub>CC</sub>	supply voltage		2.0	5.0	5.5	4.5	5.0	5.5	V
V <sub>I</sub>	input voltage		0	-	5.5	0	-	5.5	V
V <sub>O</sub>	output voltage		0	-	V <sub>CC</sub>	0	-	V <sub>CC</sub>	V
T <sub>amb</sub>	ambient temperature		-40	+25	+125	-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V <sub>CC</sub> = 3.3 V ± 0.3 V	-	-	100	-	-	-	ns/V
		V <sub>CC</sub> = 5.0 V ± 0.5 V	-	-	20	-	-	20	ns/V

## 9. Static characteristics

**Table 6. Static characteristics**

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	

### For type 74VHC08-Q100

V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 2.0 V	1.5	-	-	1.5	-	1.5	-	V
		V <sub>CC</sub> = 3.0 V	2.1	-	-	2.1	-	2.1	-	V
		V <sub>CC</sub> = 5.5 V	3.85	-	-	3.85	-	3.85	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 2.0 V	-	-	0.5	-	0.5	-	0.5	V
		V <sub>CC</sub> = 3.0 V	-	-	0.9	-	0.9	-	0.9	V
		V <sub>CC</sub> = 5.5 V	-	-	1.65	-	1.65	-	1.65	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
		I <sub>O</sub> = -50 µA; V <sub>CC</sub> = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I <sub>O</sub> = -50 µA; V <sub>CC</sub> = 3.0 V	2.9	3.0	-	2.9	-	2.9	-	V
		I <sub>O</sub> = -50 µA; V <sub>CC</sub> = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I <sub>O</sub> = -4.0 mA; V <sub>CC</sub> = 3.0 V	2.58	-	-	2.48	-	2.4	-	V
V <sub>OL</sub>	LOW-level output voltage	I <sub>O</sub> = -8.0 mA; V <sub>CC</sub> = 4.5 V	3.94	-	-	3.8	-	3.7	-	V
		V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
		I <sub>O</sub> = 50 µA; V <sub>CC</sub> = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 50 µA; V <sub>CC</sub> = 3.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 50 µA; V <sub>CC</sub> = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
I <sub>I</sub>	input leakage current	I <sub>O</sub> = 4.0 mA; V <sub>CC</sub> = 3.0 V	-	-	0.36	-	0.44	-	0.55	V
		I <sub>O</sub> = 8.0 mA; V <sub>CC</sub> = 4.5 V	-	-	0.36	-	0.44	-	0.55	V
		V <sub>I</sub> = 5.5 V or GND; V <sub>CC</sub> = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	µA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 5.5 V	-	-	2.0	-	20	-	40	µA
C <sub>I</sub>	input capacitance		-	3.0	10	-	10	-	10	pF

**Table 6. Static characteristics ...continued**  
 Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
For type 74VHCT08-Q100										
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	2.0	-	-	2.0	-	2.0	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	-	-	0.8	-	0.8	-	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 4.5 V								
		I <sub>O</sub> = –50 µA	4.4	4.5	-	4.4	-	4.4	-	V
		I <sub>O</sub> = –8.0 mA	3.94	-	-	3.8	-	3.7	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 4.5 V								
		I <sub>O</sub> = 50 µA	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 8.0 mA	-	-	0.36	-	0.44	-	0.55	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND; V <sub>CC</sub> = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	µA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 5.5 V	-	-	2.0	-	20	-	40	µA
ΔI <sub>CC</sub>	additional supply current	per input pin; V <sub>I</sub> = V <sub>CC</sub> – 2.1 V; I <sub>O</sub> = 0 A; other pins at V <sub>CC</sub> or GND; V <sub>CC</sub> = 4.5 V to 5.5 V	-	-	1.35	-	1.5	-	1.5	mA
C <sub>I</sub>	input capacitance		-	3.0	10	-	10	-	10	pF

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**  
 GND = 0 V; For test circuit, see [Figure 7](#).

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	Min	Max	
For type 74VHC08-Q100										
t <sub>pd</sub>	propagation delay	nA, nB to nY; see <a href="#">Figure 6</a> <sup>[2]</sup>								
		V <sub>CC</sub> = 3.0 V to 3.6 V								
		C <sub>L</sub> = 15 pF	-	4.0	8.8	1.0	10.5	1.0	11.0	ns
		C <sub>L</sub> = 50 pF	-	5.6	12.3	1.0	14	1.0	15.5	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V								
		C <sub>L</sub> = 15 pF	-	3.0	5.9	1.0	7.0	1.0	7.5	ns
		C <sub>L</sub> = 50 pF		4.2	7.9	1.0	9.0	1.0	10.0	ns
C <sub>PD</sub>	power dissipation capacitance	C <sub>L</sub> = 50 pF; f <sub>i</sub> = 1 MHz; V <sub>I</sub> = GND to V <sub>CC</sub> <sup>[3]</sup>	-	10.0	-	-	-	-	-	pF

**Table 7. Dynamic characteristics ...continued**GND = 0 V; For test circuit, see [Figure 7](#).

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	Min	Max	
For type 74VHCT08-Q100										
t <sub>pd</sub>	propagation delay	nA, nB to nY; see <a href="#">Figure 6</a>	<a href="#">[2]</a>							
		V <sub>CC</sub> = 4.5 V to 5.5 V								
		C <sub>L</sub> = 15 pF	-	3.2	6.9	1.0	8.0	1.0	9.0	ns
		C <sub>L</sub> = 50 pF	-	4.2	7.9	1.0	9.0	1.0	10.0	ns
C <sub>PD</sub>	power dissipation capacitance	C <sub>L</sub> = 50 pF; f <sub>i</sub> = 1 MHz; V <sub>I</sub> = GND to V <sub>CC</sub>	<a href="#">[3]</a>	-	12.0	-	-	-	-	pF

[1] Typical values are measured at nominal supply voltage ( $V_{CC} = 3.3\text{ V}$  and  $V_{CC} = 5.0\text{ V}$ ).

[2]  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ .

[3]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$  where:

$f_i$  = input frequency in MHz,  $f_o$  = output frequency in MHz

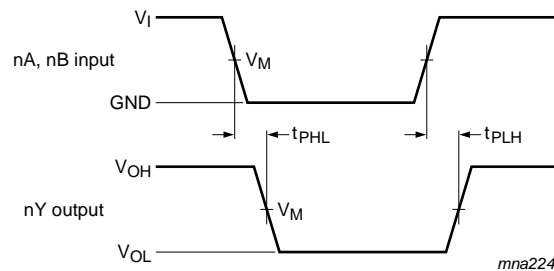
$C_L$  = output load capacitance in pF

$V_{CC}$  = supply voltage in Volts

$N$  = number of inputs switching

$\Sigma(C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.

## 11. Waveforms



Measurement points are given in [Table 8](#).

$V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

**Fig 6. The input (nA, nB) to output (nY) propagation delays****Table 8. Measurement points**

Type	Input	Output
	$V_M$	$V_M$
74VHC08-Q100	$0.5V_{CC}$	$0.5V_{CC}$
74VHCT08-Q100	1.5 V	$0.5V_{CC}$

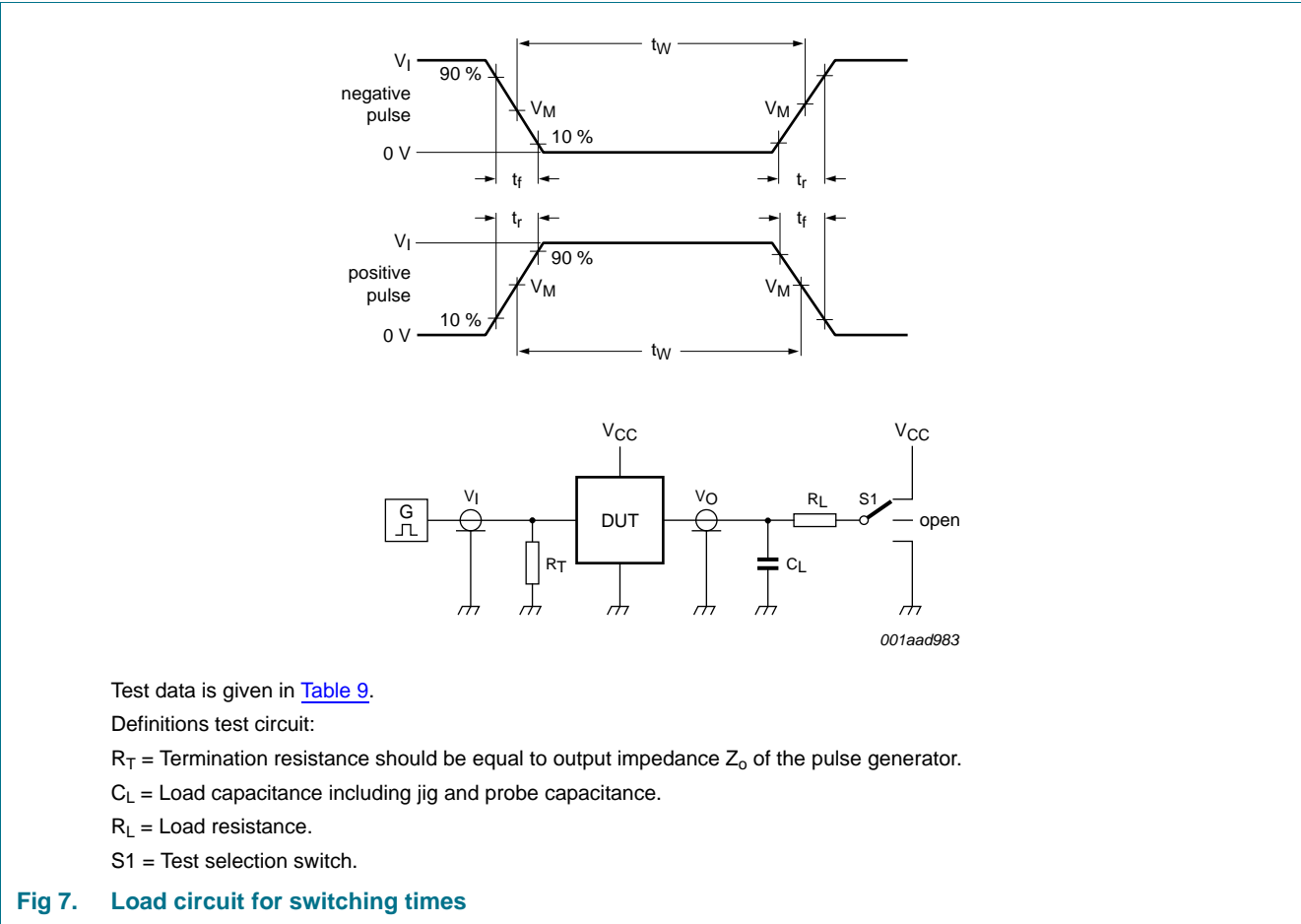


Table 9. Test data

Type	Input		Load		S1 position		
	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PHL}, t_{PLH}$	$t_{PZH}, t_{PHZ}$	$t_{PZL}, t_{PLZ}$
74VHC08-Q100	$V_{CC}$	$\leq 3.0 \text{ ns}$	15 pF, 50 pF	1 k $\Omega$	open	GND	$V_{CC}$
74VHCT08-Q100	3.0 V	$\leq 3.0 \text{ ns}$	15 pF, 50 pF	1 k $\Omega$	open	GND	$V_{CC}$



12. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

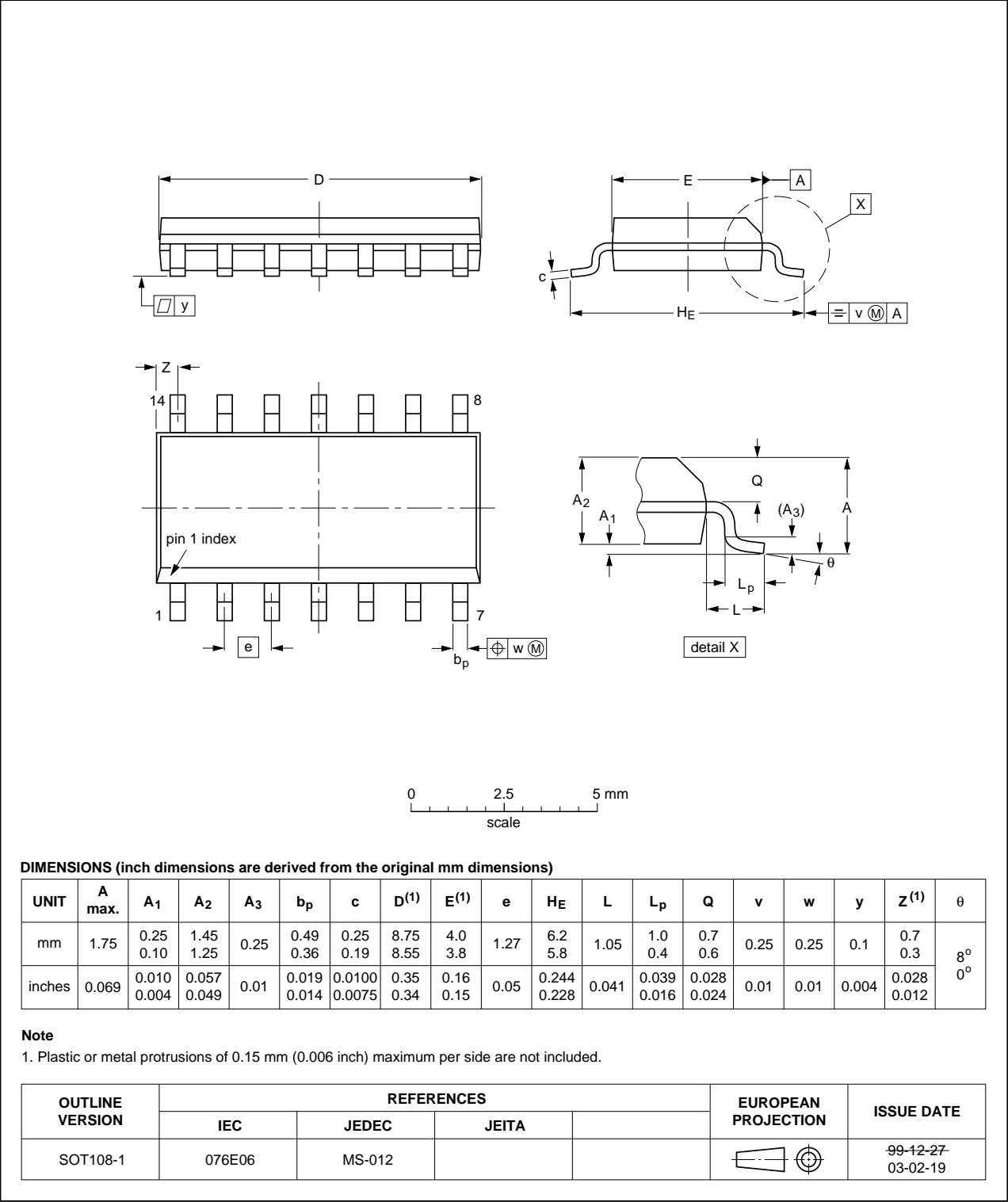


Fig 8. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

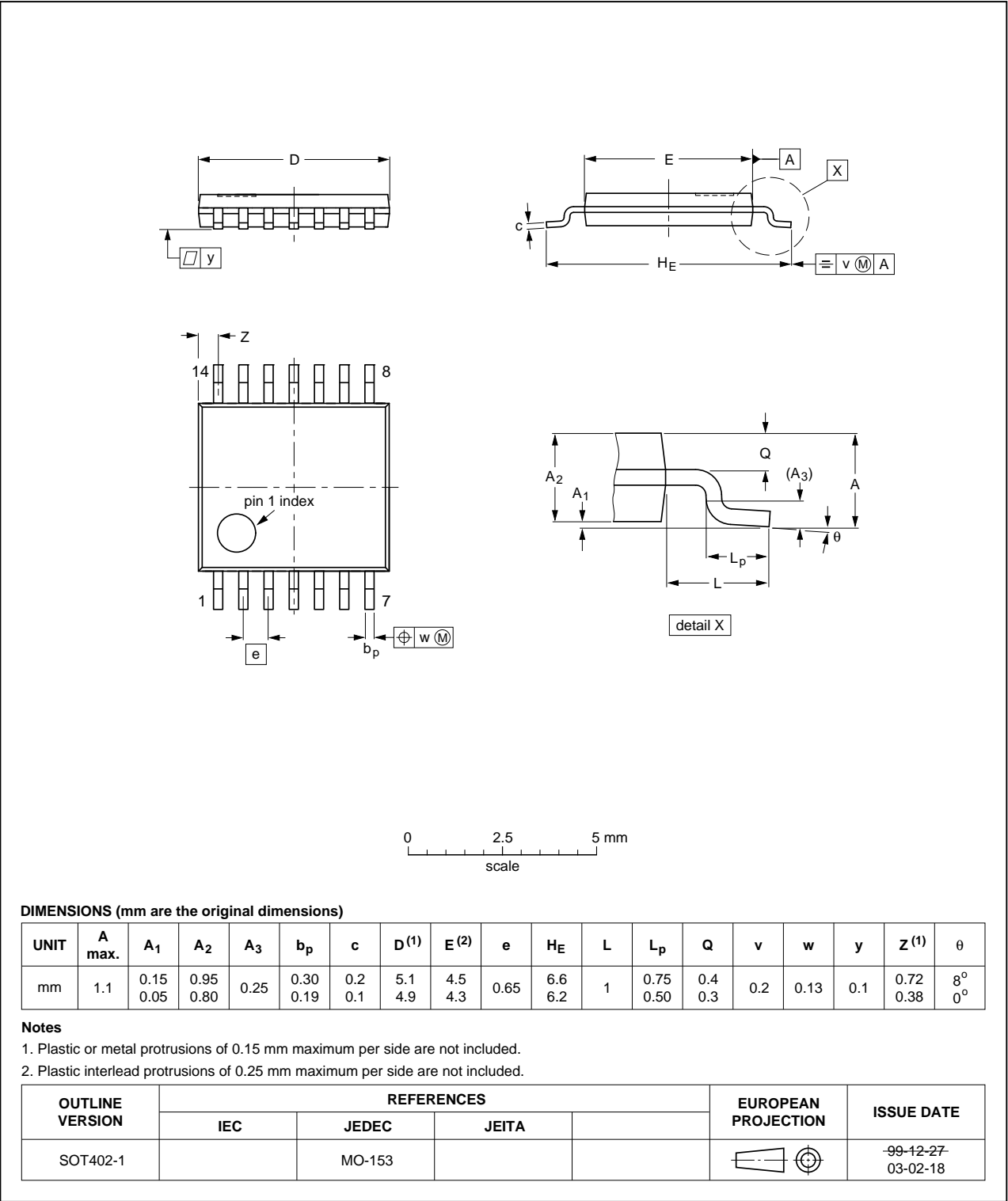


Fig 9. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm

SOT762-1

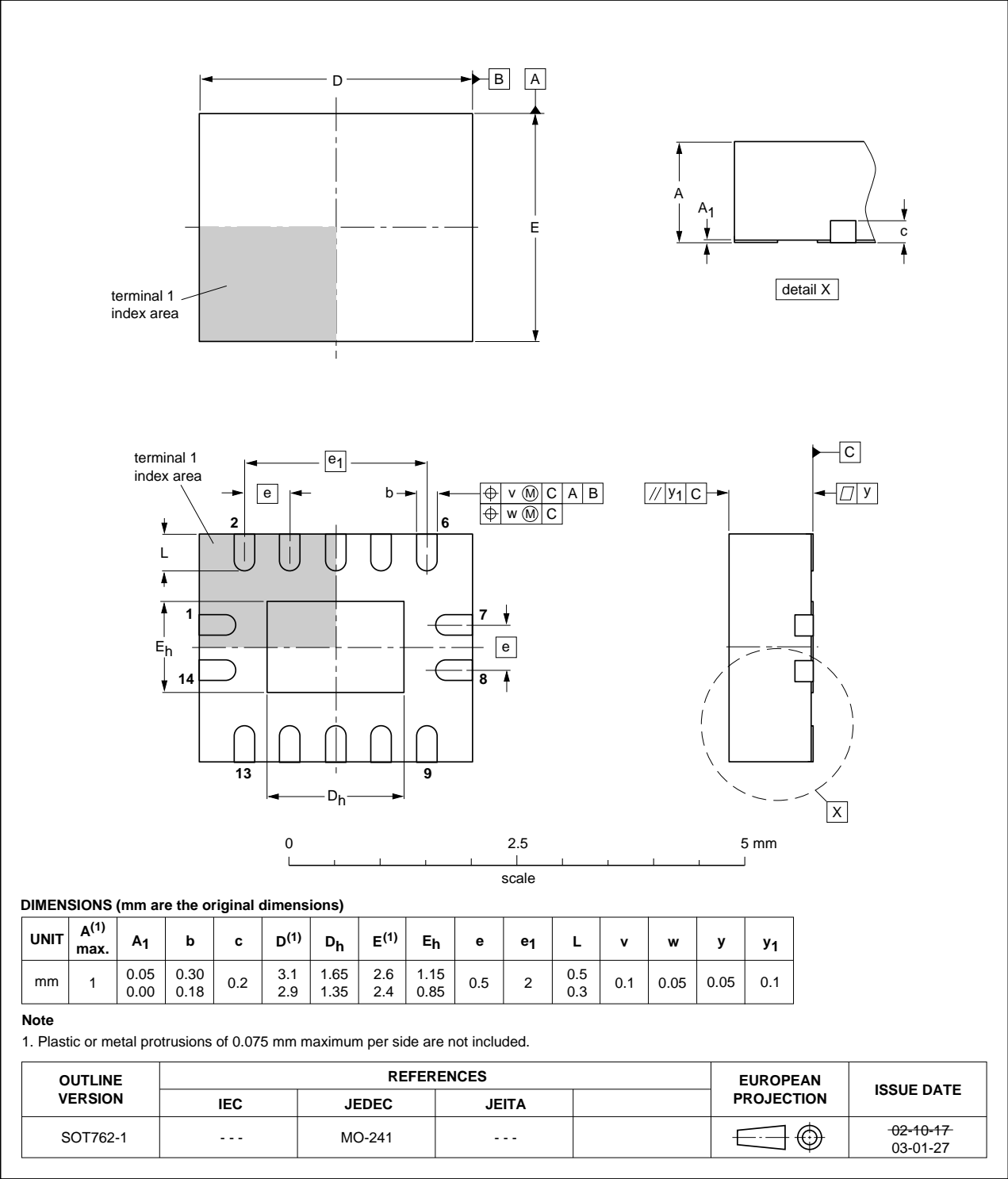


Fig 10. Package outline SOT762-1 (DHVQFN14)

## 13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
LSTTL	Low-power Schottky Transistor-Transistor Logic
MIL	Military
MM	Machine Model

## 14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74VHC_VHCT08_Q100 v.1	20131220	Product data sheet	-	-

## 15. Legal information

### 15.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

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