71-86GHz Low Noise Amplifier

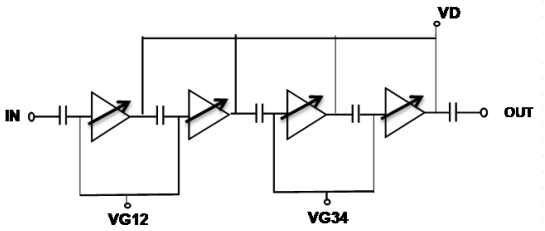
GaAs Monolithic Microwave IC

Description

The CHA2080-98F is a Low Noise Amplifier with variable gain. This circuit integrates four stages and provides 3.5dB Noise Figure associated to 22dB Gain and +10dBm Output Power at 1dB compression.

This amplifier is dedicated to telecommunication, particularly well suited for the two main E-Bands used in new generation of High Capacity Backhaul.

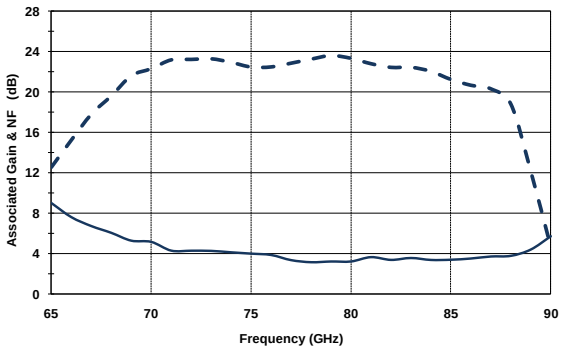
It is manufactured with a pHEMT process, 0.1µm gate length, via holes through the substrate, air bridges, electron beam gate lithography and is available in chip form with BCB Layer protection.



Functional diagram

Main Features

- Broadband performances: 71-86GHz
- Very low Noise Figure: 3.5dB
- High Gain: 22dB
- Dynamic Gain control: 12dB
- 10dBm Pout@1dB compression
- BCB Layer protection
- DC bias: Vd=3.5Volt@Id=75mA
- Chip size 3.35x1.12x0.07mm



Typical Linear gain and Noise Figure

Main Electrical Characteristics

Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	71		86	GHz
Gain	Linear Gain		22		dB
NF	Noise Figure		3.5		dB
Pout	Output Power @1dB compression		10		dBm

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Electrical Characteristics

Tamb.=+25°C, Vd=+3.5V, Id=75mA

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Frequency range	71		86	GHz
Gain*	Linear Gain		22		dB
ΔGain(Fop)	Gain variation: Low Band [71-76 GHz] High Band [81-86 GHz]		 ±0.2 ±0.8		 dB dB
Dyn_Gain	Gain Dynamic with VGx [-3; -2V]		12		dB
NF*	Noise Figure@ nominal gain Low Band [71-76 GHz] High Band [81-86 GHz]		 4 3.5		 dB dB
Pout@1dB comp.*	Output power at 1 dB compression Low Band [71-76 GHz] High Band [81-86 GHz]		 12 10		 dBm dBm
VSWR_in*	VSWR at input port		2:1		
VSWR_out*	VSWR at output port		2:1		
VG12 & VG34	Negative supply voltage		-2		V
Ig	Negative supply current		0.6		mA
Id	Positive supply current		75		mA

*Nominal conditions: VG12=VG34 are tuned to obtain Id=75mA (#-2V)

These values are representative of on-wafer measurements that are made without bonding wires at the RF ports.

A ribbon (75 µm wide) connection at the input and the output of the MMIC amplifier (see chapter recommended chip assembly) could improve the results.

Absolute Maximum Ratings (1)

Tamb.= +25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	4	V
Id	Drain bias current	95	mA
Vg	Gate bias voltage	-3 to +0.4	V
Pin	Maximum peak input power overdrive (2)	+0	dBm
Tj	Junction temperature	175	°C
Ta	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +150	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.

(2) Duration < 1s.

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Typical on-wafer Sij parameters

Tamb.=+25°C, Vd=+3.5V, Id=75mA

Freq (GHz)	S11 (dB)	PhS11 (°)	S12 (dB)	PhS12 (°)	S21 (dB)	PhS21 (°)	S22 (dB)	PhS22 (°)
68	-3.3	9	-39.7	152	19.5	106	-10.3	73
68.5	-4.3	-5	-45.9	160	19.9	86	-9.6	58
69	-5.4	-21	-45	159	20.8	63	-8.7	59
69.5	-6.8	-36	-47.7	166	21.2	42	-9.8	63
70	-8.1	-51	-42.8	160	21.5	21	-11.6	62
70.5	-9.3	-66	-42.3	144	21.7	0	-12.8	57
71	-10.4	-82	-44.5	132	21.8	-19	-12.8	52
71.5	-11.6	-98	-43.8	119	21.7	-39	-11.3	47
72	-12.7	-115	-44.5	123	21.6	-58	-10.4	45
72.5	-14.5	-135	-44.7	111	21.6	-77	-11	44
73	-14.9	-151	-46.4	98	21.5	-97	-12.4	33
73.5	-15.7	-158	-48.5	95	21.3	-115	-13	20
74	-16.5	-164	-47.7	66	21.3	-131	-13.3	10
74.5	-17.3	-175	-50.5	53	21.5	-146	-12.8	4
75	-16.5	172	-53.6	2	21.4	-164	-12.9	-4
75.5	-17	160	-52.2	1	21.5	180	-14.5	-13
76	-17	151	-54.4	-34	21.5	163	-14.9	-32
76.5	-17.2	139	-56.9	-65	21.6	146	-15.3	-48
77	-17.6	123	-53.5	-86	21.7	128	-15.3	-57
77.5	-19.4	107	-51.8	-101	21.7	110	-15.5	-71
78	-20.6	87	-50.1	-131	21.9	91	-15.7	-94
78.5	-24.8	55	-48.8	-158	22.1	74	-15.7	-117
79	-30.8	16	-49.4	-174	22.1	55	-15	-139
79.5	-29.3	-56	-50.1	165	22.1	34	-15.2	-160
80	-28.6	-109	-50.8	145	22	15	-16	-177
80.5	-24.2	-130	-49.7	143	21.8	-3	-15.8	164
81	-21.4	-154	-50.2	113	21.5	-22	-15.4	146
81.5	-19.6	-172	-53.8	88	21.3	-40	-15.1	131
82	-18.1	173	-53.2	70	21.2	-58	-15	118
82.5	-17	156	-64.1	43	21	-78	-15.4	102
83	-15.7	139	-59.5	88	20.9	-96	-15.4	86
83.5	-14.3	122	-61.6	85	20.9	-115	-15.2	72
84	-12.8	101	-59.4	29	20.8	-136	-14.5	60
84.5	-11.3	82	-60.9	15	20.5	-157	-13.7	41
85	-10	60	-53.3	-39	20.5	-180	-14.6	30
85.5	-8.8	42	-51.4	-73	20.4	159	-15	18
86	-7.7	24	-51	-108	19.9	136	-15.6	0
86.5	-6.6	7	-51.5	-130	19.9	109	-16.8	-8
87	-5.7	-9	-50.9	-148	19.6	84	-17	-1
87.5	-4.9	-24	-50.8	-165	18.6	51	-16.7	1
88	-4.3	-40	-50	171	17	18	-15.2	2
88.5	-4	-54	-51.2	137	14.2	-12	-13.9	-7
89	-3.9	-67	-51.7	110	10.8	-41	-12.7	-18

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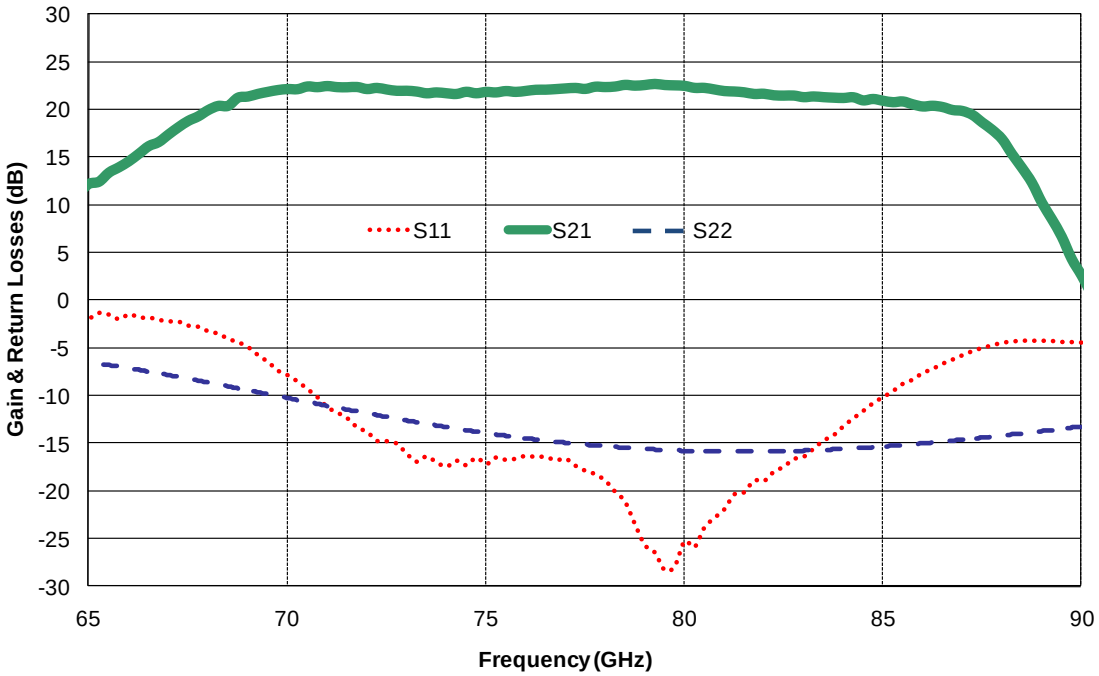
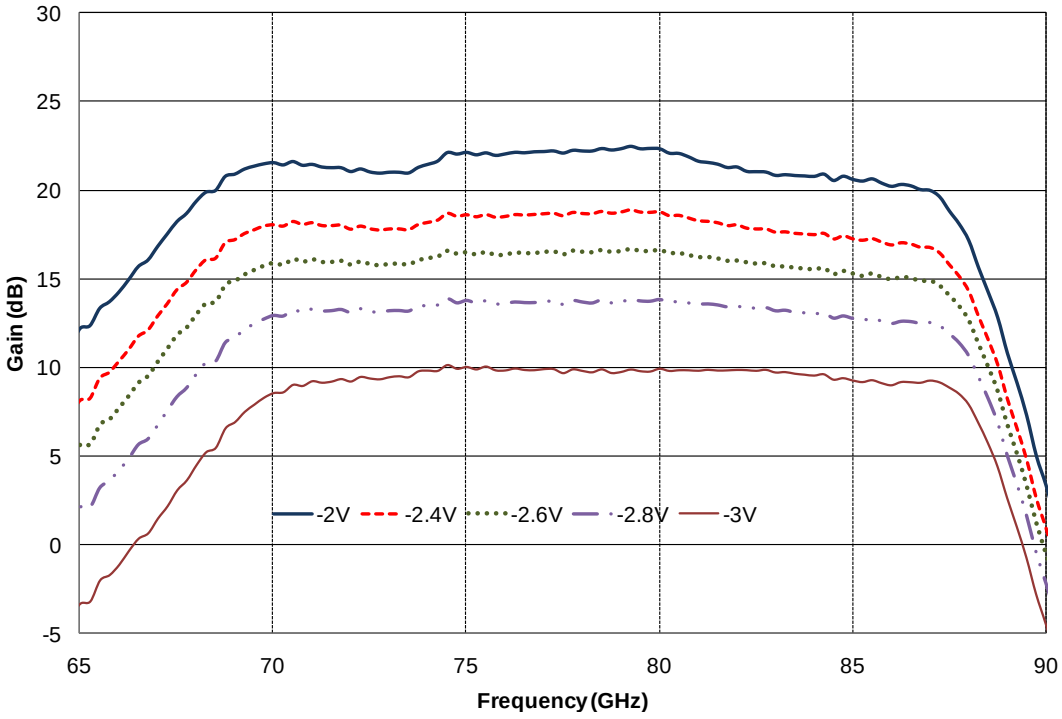
Typical on wafer Measurements

Tamb.=+25°C, Vd =+3.5V, Id=75mA

Linear Gain & return losses versus frequency



Linear Gain versus Vg voltage



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Typical on wafer Measurements

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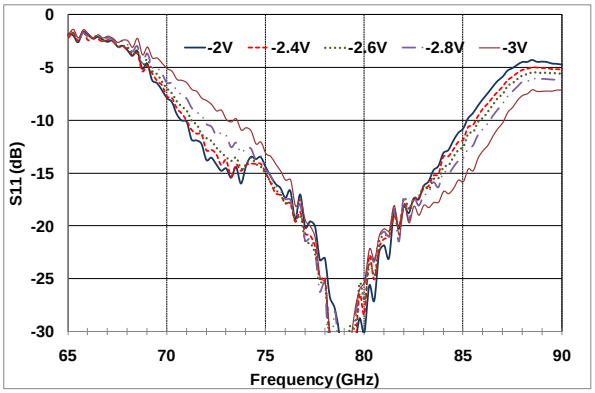
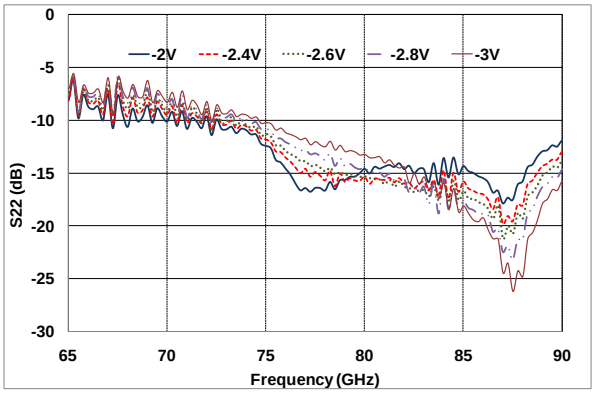
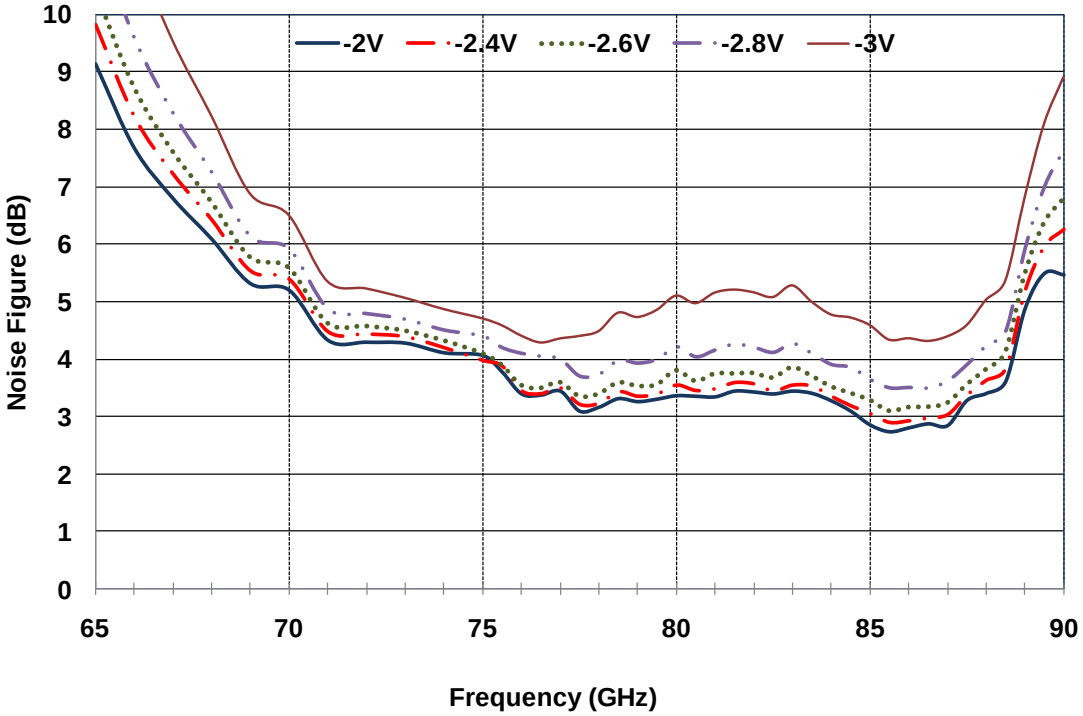
Input Return loss versus vg voltage



Output Return loss versus vg Voltage



Noise Figure versus Vg voltage



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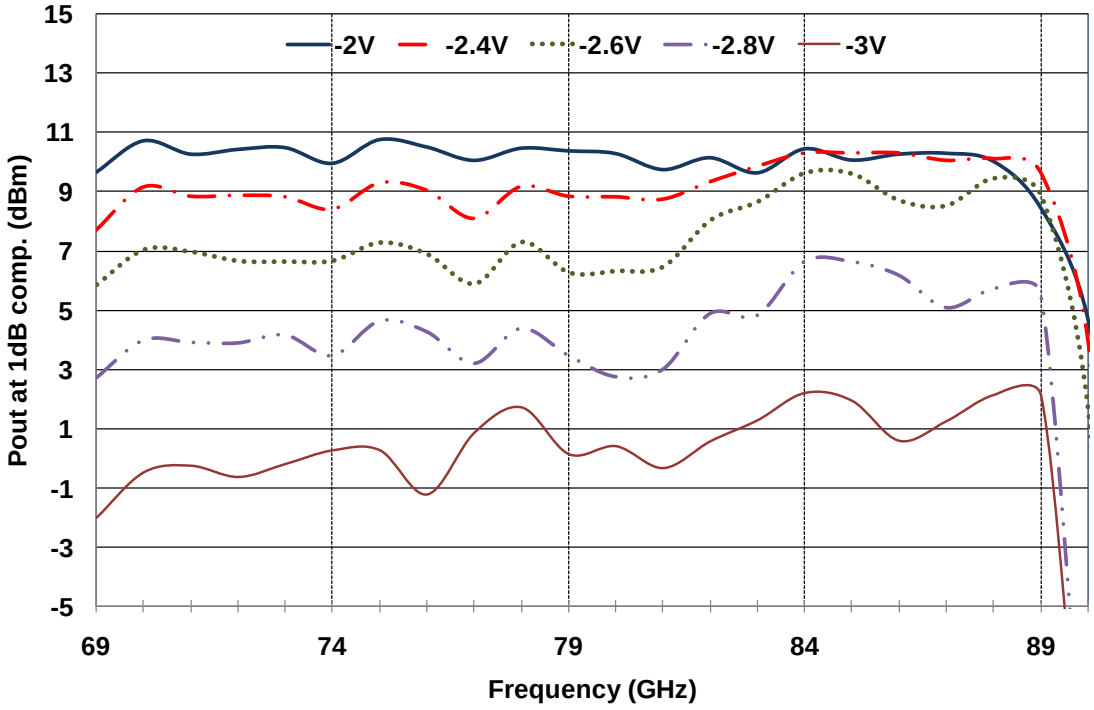
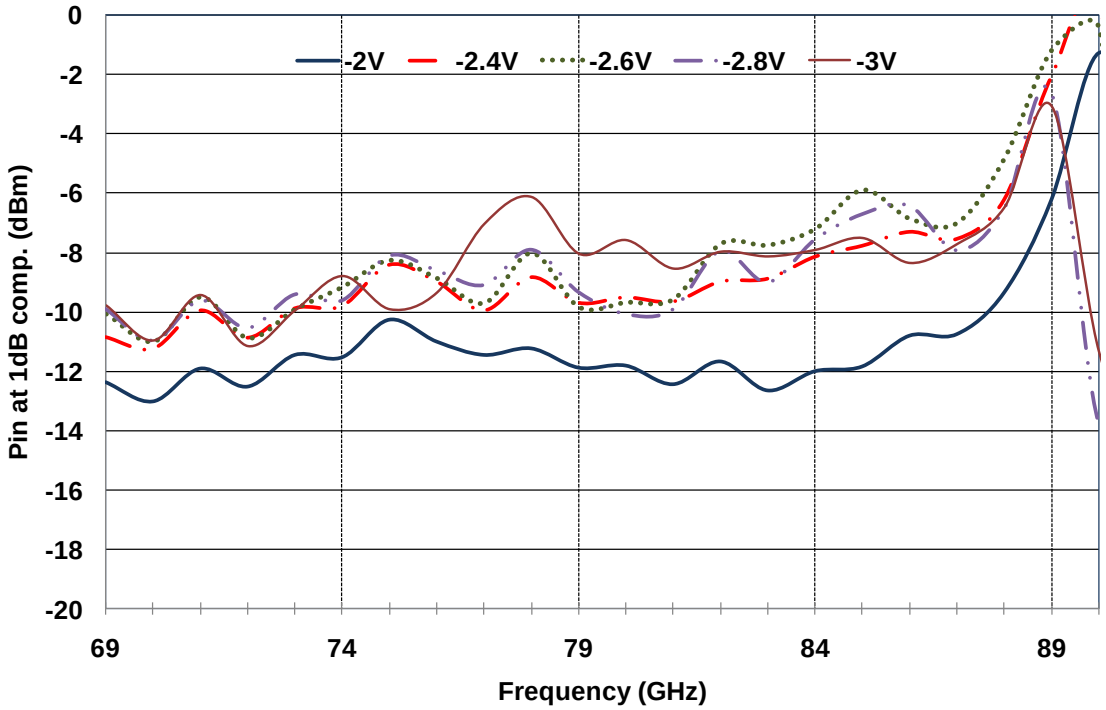
Typical on wafer Measurements

Tamb.=+25°C, Vd=+3.5V, Id=75mA

Output power at 1 dB compression versus Vg voltage



Input power at 1 dB compression versus Vg voltage



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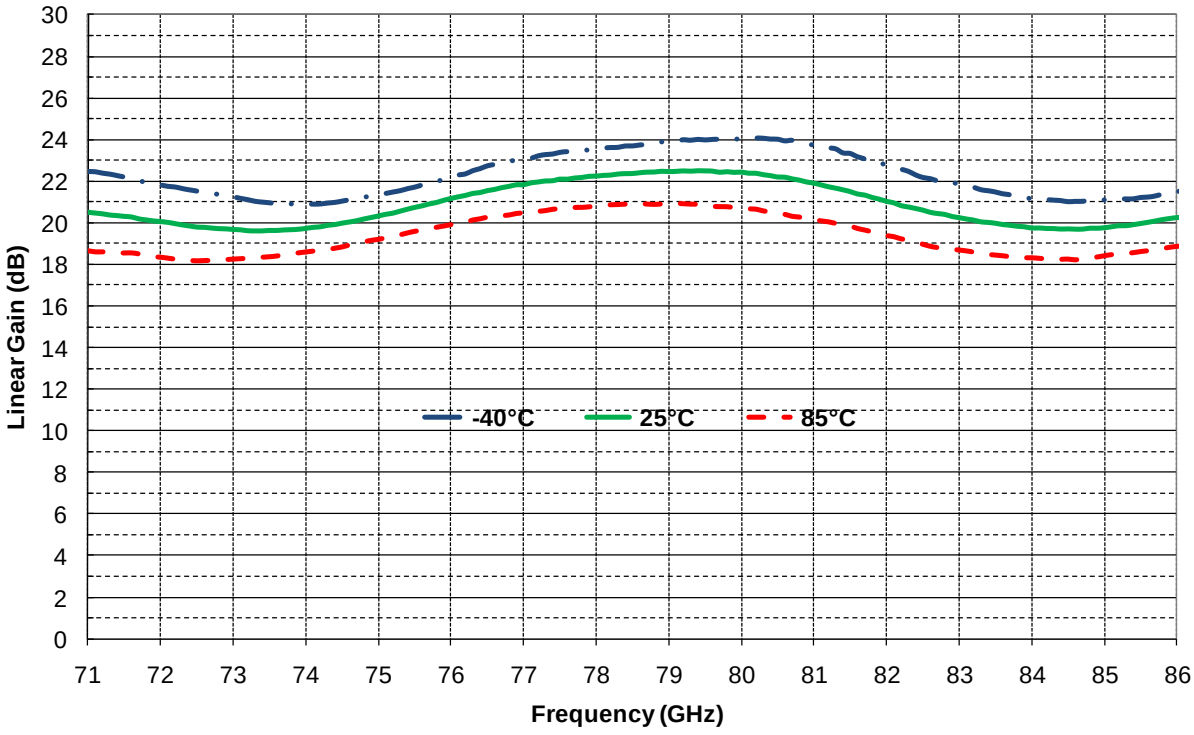
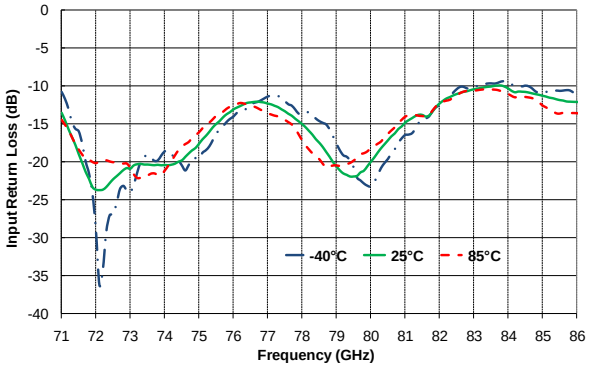
Typical Test Fixture Measurements

Tamb.=-40°C / +25°C / +85°C, Vd=+3.5V
Id=75 mA @ +25°C
Measurements are given in the test fixture access plans

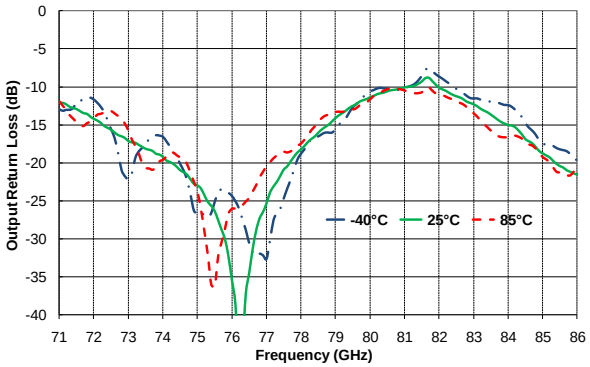
Linear Gain versus Temperature



Input Return Loss versus Temperature



Output Return Loss versus Temperature



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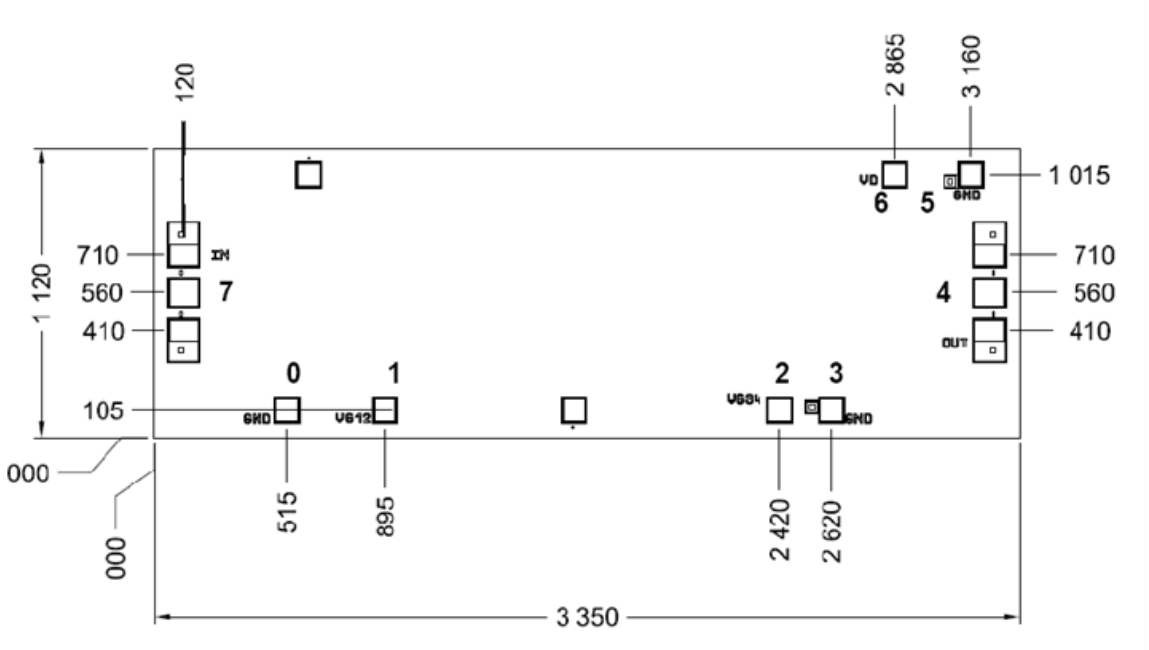
Mechanical data



Chip thickness: 70µm. ±10µm
Chip size: 3350x1120 ±35µm
All dimensions are in micrometers

RF Pads (4,7) = 108 x 106 (BCB opening)
DC Pads = 86 x 83 (BCB opening)

Pin number	Pin name	Description
0, 3, 5	**GND**	Ground: should not be bonded
4	**OUT**	RF output port
7	**IN**	RF input port
6	**VD**	Positive supply voltage
1	**VG12**	Negative supply voltage for the first & second stage
2	**VG34**	Negative supply voltage for the third and fourth stage

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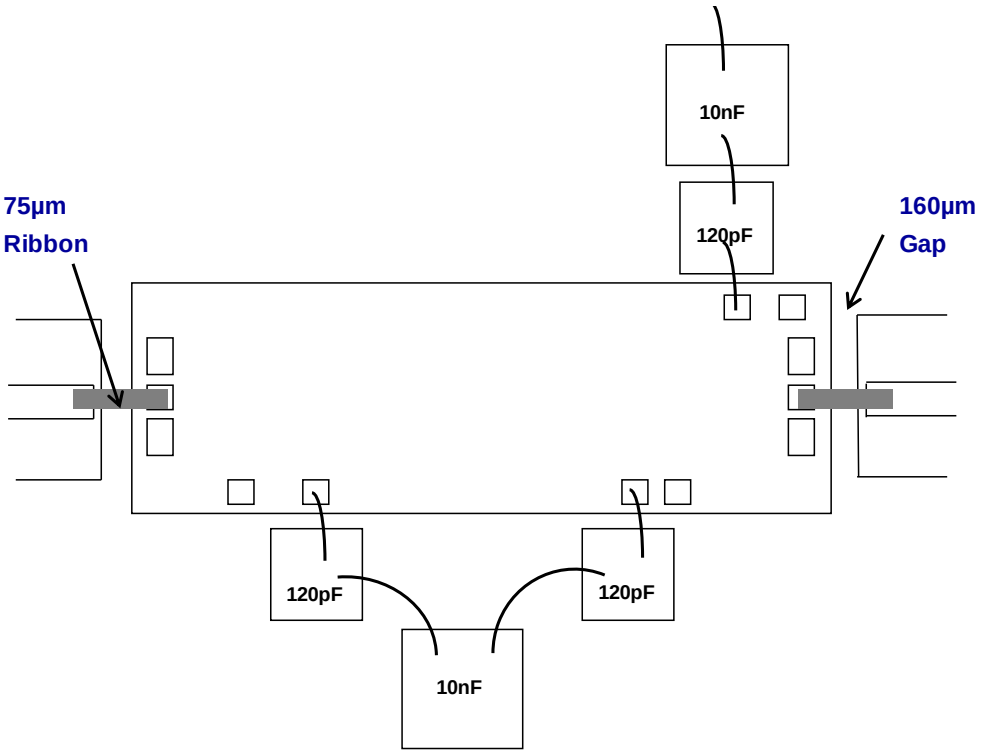
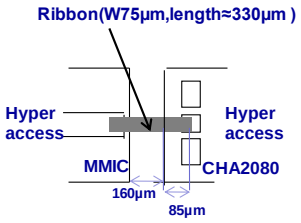
Recommended chip assembly



The design of the circuit integrates a half ribbon (75µm wide) connection at the input and the output of the MMIC amplifier compliant with a 50 Ohm line on GaAs MMIC.

Circuits having to be as close as possible to each other, the ribbon length must be reduced to the achievable minimum (160µm gap between two chips is considered) and the loop height must also be the smallest realizable (80µm).



A second solution is the use of double wires (Ø 25µm). In this case, a minimum of two wires and the same chip to chip distance than ribbon solution are necessary to reduce the inductance effect. Nevertheless, simulations have demonstrated an improvement of RF performance for E-band frequency range with the use of ribbon connection instead of wire.

Regarding the connection of the DC pads, a 25µm wedge bonding is preferred.

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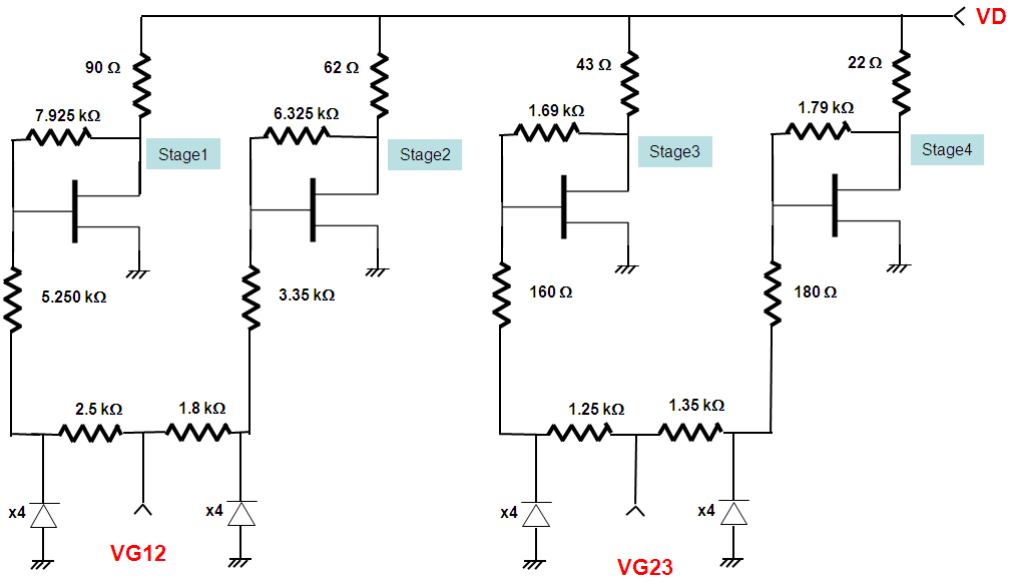
DC Schematic



LNA: 3.5V, 75mA

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Recommended ESD management

Refer to the application note AN0020 available at http://www.ums-gaas.com for ESD sensitivity and handling recommendations for the UMS products.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at http://www.ums-gaas.com.

Ordering Information

Chip form:	CHA2080-98F/00

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