DS32506/DS32508/DS32512
6-/8-/12-Port DS3/E3/STS-1 LIU

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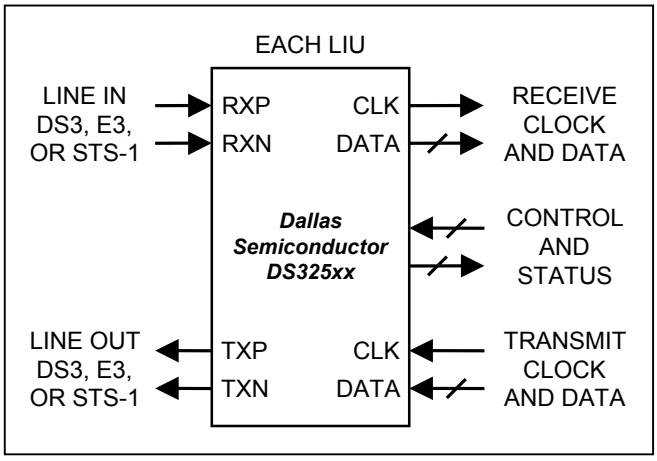
GENERAL DESCRIPTION

The DS32506 (6 port), DS32508 (8 port), and DS32512 (12 port) line interface units (LIUs) are highly integrated, low-power, feature-rich LIUs for DS3, E3, and STS-1 applications. Each LIU port in these devices has independent receive and transmit paths, a jitter attenuator, full-featured pattern generator and detector, performance-monitoring counters, and a complete set of loopbacks. An on-chip clock adapter generates all line-rate clocks from a single input clock. Ports are independently software configurable for DS3, E3, and STS-1 and can be individually powered down. Control interface options include 8-bit parallel, SPI™, and hardware mode.

APPLICATIONS

SONET/SDH and PDH Multiplexers
ATM and Frame Relay Equipment
WAN Routers and Switches
Digital Cross-Connects
Access Concentrators
CSUs/DSUs
PBXs
DSLAMs

FUNCTIONAL DIAGRAM



FEATURES

- **Pin-Compatible Family of Products**
- **Each Port Independently Configurable**
- **Receive Clock and Data Recovery for Up to 457 meters (1500 feet) of 75Ω Coaxial Cable**
- **Standards-Compliant Transmit Waveshaping**
- **Uses 1:1 Transformers on Both Tx and Rx**
- **Three Control Interface Options: 8/16-Bit Parallel, SPI, and Hardware Mode**
- **Jitter Attenuators (One Per Port) Can be Placed in the Receive Path or the Transmit Path**
- **Jitter Attenuators Have Provisionable Buffer Depth: 16, 32, 64, or 128 Bits**
- **Built-In Clock Adapter Generates All Line-Rate Clocks from a Single Input Clock (DS3, E3, STS-1, 12.8MHz, 19.44MHz, 38.88MHz, 77.76MHz)**
- **Per-Port Programmable Internal Line Termination Requiring Only External Transformers**
- **High-Impedance Tx and Rx, Even When V_{DD} = 0, Enables Hot-Swappable, 1:1 and 1+1 Board Redundancy Without Relays**
- **Per-Port BERT for PRBS and Repetitive Pattern Generation and Detection**
- **Tx and Rx Open and Short Detection Circuitry**
- **Transmit Driver Monitor Circuitry**
- **Receive Loss-of-Signal (LOS) Monitoring Compliant with ANSI T1.231 and ITU G.775**
- **Automatic Data Squelching on Receive LOS**
- **Large Line Code Performance-Monitoring Counters for Accumulation Intervals Up to 1s**
- **Local and Remote Loopbacks**
- **Transmit Common Clock Option**
- **Power-Down Capability for Unused Ports**
- **Low-Power 1.8V/3.3V Operation (5V Tolerant I/O)**
- **Industrial Temperature Range: -40°C to +85°C**
- **Small Package: 23mm x 23mm, 484-Pin BGA**
- **IEEE 1149.1 JTAG Support**

ORDERING INFORMATION

PART	LIUs	TEMP RANGE	PIN-PACKAGE
DS32506	6	0°C to +70°C	484 BGA
DS32506N	6	-40°C to +85°C	484 BGA
DS32508	8	0°C to +70°C	484 BGA
DS32508N	8	-40°C to +85°C	484 BGA
DS32512	12	0°C to +70°C	484 BGA
DS32512N	12	-40°C to +85°C	484 BGA

Note: *Add the "+" suffix for the lead-free package option.*

Note: *Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, click here: www.maxim-ic.com/errata.*

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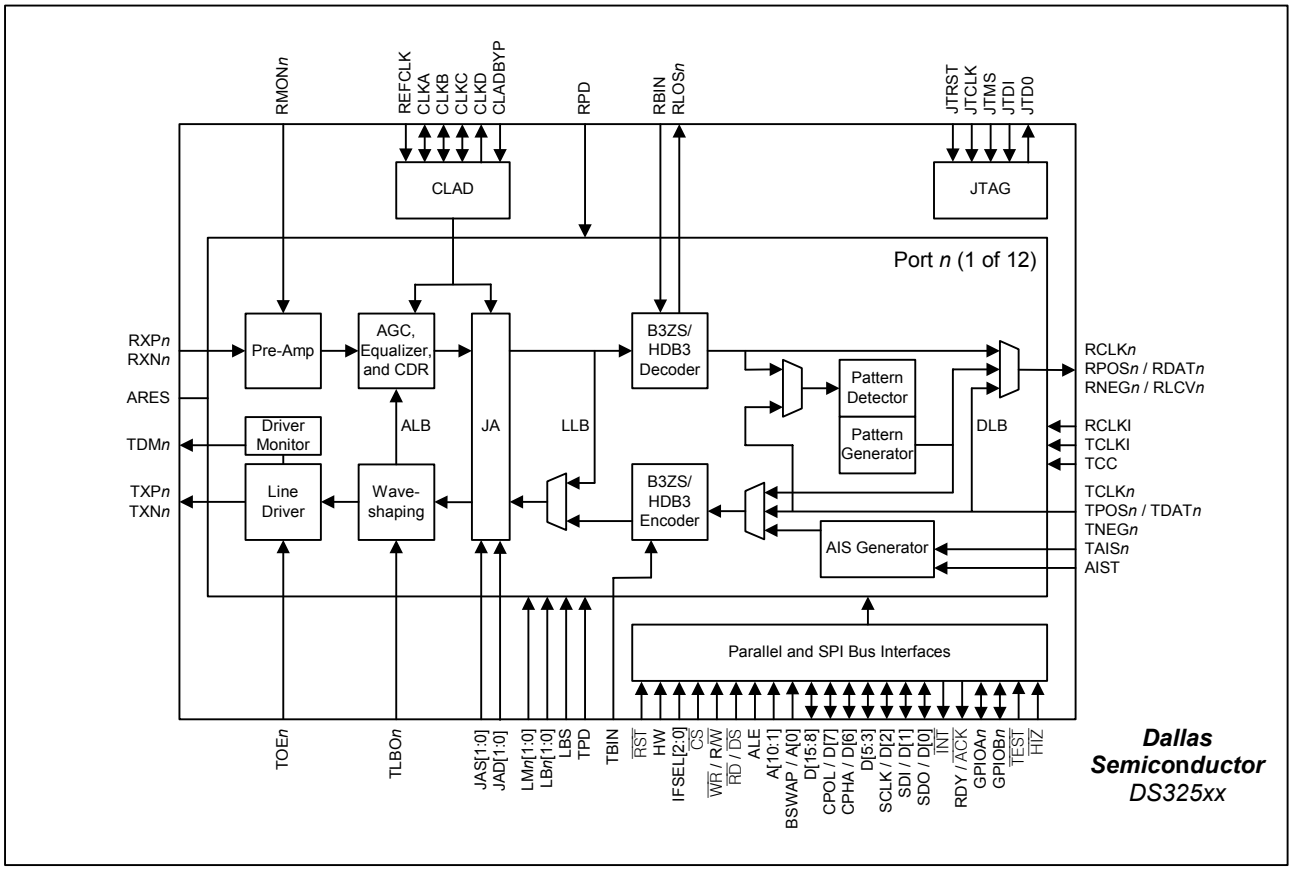
1. STANDARDS COMPLIANCE

Table 1-1. Applicable Telecommunications Standards

SPECIFICATION	SPECIFICATION TITLE
ANSI	
T1.102-1993	*Digital Hierarchy—Electrical Interfaces*
T1.231-2003	*Digital Hierarchy—Layer 1 In-Service Digital Transmission Performance Monitoring*
T1.404-2002	*Network-to-Customer Installation—DS3 Metallic Interface Specification*
AT&T	
TR54014	*ACCUNET® T45 Service Description and Interface Specification,* 05/92
ETSI	
EN 300 686	*Business TeleCommunications; 34Mbps and 140Mbps Digital Leased Lines (D34U, D34S, D140U, and D140S); Network Interface Presentation,* v1.2.1 February 2001
EN 300 687	*Business TeleCommunications; 34Mbps Digital Leased Lines (D34U and D34S); Connection Characteristics*, v1.2.1 February 2001
EN 300 689	*Access and Terminals (AT); 34Mbps Digital Leased Lines (D34U and D34S); Terminal equipment interface,* v1.2.1July 2001
TBR 24	*Business TeleCommunications; 34Mbps Digital Unstructured and Structured Lease Lines; Attachment Requirements for Terminal Equipment Interface*, July 1997
ITU-T	
G.703	*Physical/Electrical Characteristics of Hierarchical Digital Interfaces,* November 2001
G.751	*Digital Multiplex Equipment Operating at the Third-Order Bit Rate of 34,368kbps and the Fourth-Order Bit Rate of 139,264kbps and Using Positive Justification,* November 1988
G.755	*Digital Multiplex Equipment Operating at 139,264 kbit/s and Multiplexing Three Tributaries at 44,736 kbit/s*, November 1988
G.775	*Loss of Signal (LOS) and Alarm Indication Signal (AIS) Defect Detection and Clearance Criteria*, November 1994
G.823	*The Control of Jitter and Wander within Digital Networks that are Based on the 2048kbps Hierarchy*, March, 2000
G.824	*The Control of Jitter and Wander within Digital Networks that are Based on the 1544kbps Hierarchy*, March, 2000
O.151	*Error Performance Measuring Equipment Operating at the Primary Rate and Above*, October 1992
O.161	*In-Service Code Violation Monitors for Digital Systems*, November 1988
O.152	*Equipment To Perform In-Service Monitoring on 2048, 8448, 34,368 and 139,264 kbit/s Signals*, October 1992
TELCORDIA	
GR-253-CORE	*SONET Transport Systems: Common Generic Criteria*, Issue 3, September 2000
GR-499-CORE	*Transport Systems Generic Requirements (TSGR): Common Requirements,* Issue 2, December 1998
GR-820-CORE	*Generic Digital Transmission Surveillance*, Issue 2, December 1997

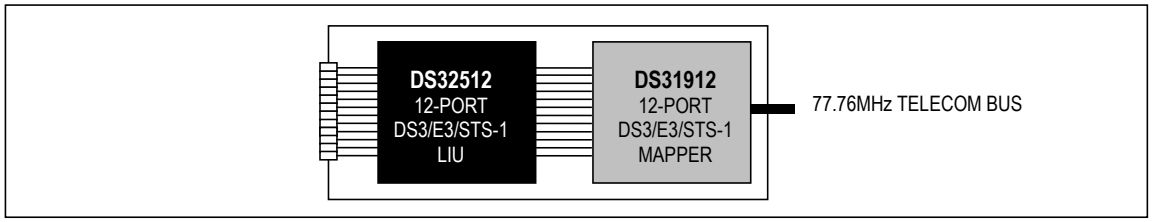
2. BLOCK DIAGRAM

Figure 2-1. Block Diagram



3. APPLICATION EXAMPLE

Figure 3-1. 12-Port Unchannelized DS3/E3 Card



4. DETAILED DESCRIPTION

The DS32506 (6 port), DS32508 (8 port), and DS32512 (12 port) LIUs perform the functions necessary for interfacing at the physical layer to DS3, E3, or STS-1 lines. Each LIU has independent receive and transmit paths and a built-in jitter attenuator. The receiver performs clock and data recovery from a B3ZS- or HDB3-coded alternate mark inversion (AMI) signal and monitors for loss of the incoming signal. The receiver optionally performs B3ZS/HDB3 decoding and outputs the recovered data in either binary (NRZ) or digital bipolar format. The transmitter accepts data in either binary (NRZ) or digital bipolar format, optionally performs B3ZS/HDB3 encoding, and drives standard pulse-shape waveforms onto 75Ω coaxial cable. Both transmitter and receiver are high-impedance when V_{DD} is out of spec to enable hot-swappable 1:1 and 1+1 board redundancy without relays. The jitter attenuator can be mapped into the receiver data path, mapped into the transmitter data path, or disabled. An on-chip clock adapter generates all line-rate clocks from a single input clock. Control interface options include 8- or 16-bit parallel, SPI, and hardware mode. The DS325xx LIUs conform to the telecommunications standards listed in Table 1-1. The external components required for proper operation are shown in Figure 4-1 and Figure 4-2.

Figure 4-1. External Connections, Internal Termination Enabled

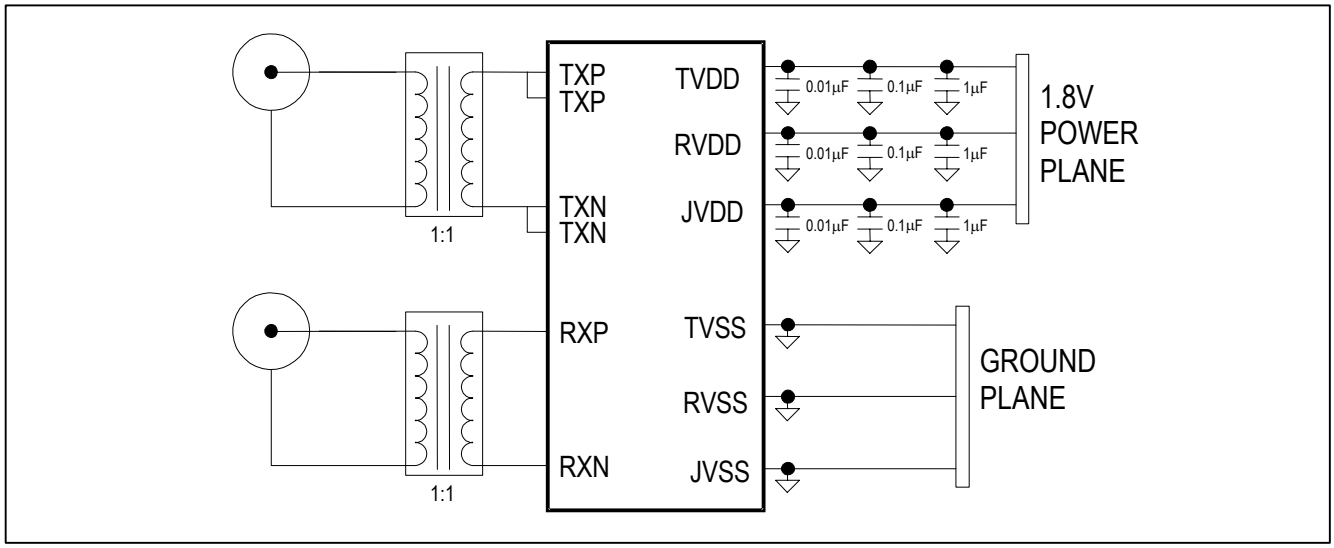
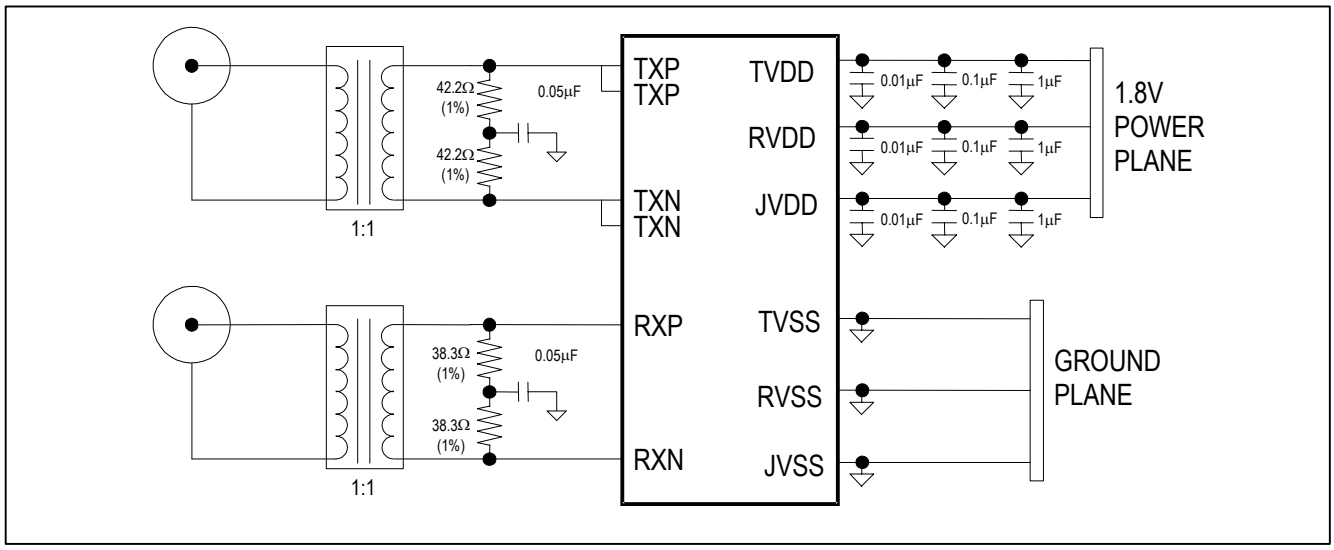


Figure 4-2. External Connections, Internal Termination Disabled



Shorthand Notations. The notation “DS325xx” throughout this data sheet refers to either the DS32506, DS32508, or DS32512. This data sheet is the specification for all three devices. The LIUs on the DS325xx devices are identical. For brevity, this document uses the pin name and register name shorthand “NAMEn,” where “n” stands in place of the LIU port number. For example, on the DS32506, TCLKn is shorthand notation for pins TCLK1, TCLK2, TCLK3, TCLK4, TCLK5 and TCLK6 on LIU ports 1, 2, 3, 4, 5 and 6, respectively. This document also uses generic pin and register names such as TCLK (without a number suffix) when describing LIU operation. When working with a specific LIU on the DS325xx devices, generic names like TCLK should be converted to actual pin names, such as TCLK1.

5. DETAILED FEATURES

5.1 Global Features

- Three interface modes: hardware, 8-/16-bit parallel bus, and SPI serial bus
- Independent per-port operation (e.g., line rate, jitter attenuator placement, or loopback type)
- Clock, data, and control signals can be inverted to allow a glueless interface to other devices
- Manual or automatic one-second update of performance monitoring counters
- Each port can be put into a low-power standby mode when not being used
- Requires only a single reference clock for all three LIU data rates using internal clock rate adapter
- Jitter attenuators can be used in either transmit or receive path
- Detection of loss-of-transmit clock
- Two programmable I/O pins per port
- Optional global write mode configures all LIUs at the same time
- Glueless interface to neighboring framer and mapper components

5.2 Receiver

- AGC/equalizer block handles from 0 to 22dB of cable loss
- Programmable internal termination resistor
- Loss-of-lock (LOL) PLL status indication
- Interfaces directly to a DSX monitor signal (~20dB flat loss) using built-in preamp
- Digital and analog loss-of-signal (LOS) detectors (compliant with ANSI T1.231 and ITU G.775)
- Software programmable B3ZS/HDB3 or AMI decoding
- Detection and accumulation of bipolar violations (BPV), code violations (CV), and excessive zeros occurrences (EXZ)
- Detection of receipt of B3ZS/HDB3 codewords
- Binary or bipolar framer interface
- On-board programmable PRBS detector
- Per-channel power-down control

5.3 Transmitter

- Standards-compliant waveshaping
- Programmable waveshaping
- Programmable internal termination resistor
- Binary or bipolar framer interface
- Gapped clock capable up to 78MHz with jitter attenuator in transmit path
- Wide 50 ±20% transmit clock duty cycle
- Transmit common clock option
- Software programmable B3ZS/HDB3 or AMI decoding
- Programmable insertion of bipolar violations (BPV), code violations (CV), and excessive zeros (EXZ)
- AIS generator: unframed all ones, framed DS3 AIS, and STS-1 AIS-L
- Line build-out (LBO) control
- High-impedance line-driver output mode to support protection-switching applications
- Per-channel power-down control
- Output driver monitor

5.4 Jitter Attenuator

- One jitter attenuator per port
- Fully integrated, requires no external components
- Meets all applicable ANSI, ITU, ETSI, and Telcordia jitter transfer and output jitter requirements
- Can be placed in the transmit path, receive path or disabled
- Programmable FIFO depth: 16, 32, 64, or 128 bits
- Overflow and underflow status indications

5.5 Bit Error-Rate Tester (BERT) Features

- One BERT per port
- Software programmable for insertion toward the transmit line interface or the receive system interface
- Generates and detects pseudo-random patterns of length 2^n - 1 (n = 1 to 32) and repetitive patterns from 1 to 32 bits in length
- Large 24-bit error counter and 32-bit bit counter allows testing to proceed for long periods without host intervention
- Errors can be inserted in the generated BERT patterns for diagnostic purposes (single bit errors or specific bit-error rates)
- Pattern synchronization even in the presence of 10^{-3} bit-error rate

5.6 Clock Adapter

- Creates DS3, E3, STS-1, and/or telecom bus clocks from single input reference clock
- Input reference clock can be DS3, E3, STS-1, 12.8MHz, 19.44MHz, 38.88MHz, or 77.76MHz
- Use of common system timing frequencies such as 19.44MHz eliminates the need for any local oscillators, reducing cost and board space
- Very small jitter gain and intrinsic jitter generation
- Derived clocks can be output for external system use
- Transmit signals using CLAD clocks meet Telcordia (DS3) and ITU (E3) jitter and wander requirements

5.7 Parallel Microprocessor Interface Features

- Multiplexed or nonmultiplexed 8- or 16-bit interface
- Configurable for Intel mode ($\overline{CS}$, $\overline{WR}$, $\overline{RD}$) or Motorola mode ($\overline{CS}$, $\overline{DS}$, R/W)
- Ready (RDY/$\overline{ACK}$) handshake output signal

5.8 SPI Serial Microprocessor Interface Features

- Operation up to 10Mbps
- Burst mode for multibyte read and write accesses
- Programmable clock polarity and phase
- Half-duplex operation gives option to tie SDI and SDO together externally to reduce wire count

5.9 Miscellaneous Features

- Global reset input pin
- Global interrupt output pin
- Two programmable I/O pins per port

5.10 Test Features

- Five pin JTAG port
- All functional pins are in-out pins in JTAG mode
- Standard JTAG instructions: SAMPLE/PRELOAD, BYPASS, EXTEST, CLAMP, HIGHZ, IDCODE
- $\overline{HIZ}$ pin to force all digital output and I/O pins into a high-impedance state
- $\overline{TEST}$ pin for manufacturing test modes

5.11 Loopback Features

- Analog local loopback—ALB (transmit line output to receive line input)
- Diagnostic local loopback—DLB (transmit framer interface to receive framer interface)
- Line loopback—LLB (receive clock and data recover to transmit waveshaping)
- Optional AIS generation on the line side of the loopback during diagnostic loopback

6. CONTROL INTERFACE MODES

The DS325xx devices can be controlled by hardware interface, by microprocessor interface, or by a combination of both interfaces at the same time. The hardware interface is configured (enabled or disabled) independently from the microprocessor interface (8-bit parallel, 16-bit parallel, SPI, or disabled).

When the hardware interface is enabled (HW = 1), device configuration can be controlled by input pins, while device status can be sensed on output pins. When the hardware interface is disabled (HW = 0), all the pins in Table 7-5 are disabled (inputs are ignored; outputs are placed in a high-impedance state).

The microprocessor interface provides access to features, configuration options, and device status information that the hardware interface does not support. The microprocessor interface is enabled and configured by the IFSEL pins. When IFSEL = 01X, the SPI serial interface is enabled. When IFSEL = 10X, the 8-bit parallel interface is enabled. When IFSEL = 11X, the 16-bit parallel interface is enabled. For both the 8- and 16-bit parallel interfaces, IFSEL[0] = 0 specifies an Intel-style bus ($\overline{CS}$, $\overline{RD}$, and $\overline{WR}$ control signals) while IFSEL[0] = 1 specifies a Motorola-style bus ($\overline{CS}$, R/W, and $\overline{DS}$ control signals). Through the microprocessor interface an external microprocessor can access a set of internal configuration and status registers inside the device. Pins that are not used by the selected microprocessor interface type but are used in other microprocessor interface modes are disabled (inputs are ignored and considered to be low and can be left floating or wired low or high; outputs are placed in a high-impedance state and can be left unconnected or wired low or high). When no microprocessor interface is selected (IFSEL = 000) all microprocessor interface inputs are ignored, and all microprocessor interface outputs are put in a high impedance state.

When both the hardware interface and the microprocessor interface are enabled at the same time, many internal settings of the device can be configured by both a hardware interface *pin* and a microprocessor interface register *bit* with identical names and functions. In this situation the actual internal device setting is the logical OR of pin assertion and register bit assertion. For example, the transmitter output driver is enabled when the *TOE pin* is high *OR* the TOE *register bit* is high. When both the hardware interface and the microprocessor interface are enabled at the same time, the following hardware interface pins are ignored and replaced by equivalent configuration register fields: LMn[1:0], JAS[1:0], JAD[1:0], LBn[1:0], and LBS.

7. PIN DESCRIPTIONS

Note: *All digital pins are I/O pins in JTAG mode. This feature is to increase the effectiveness of board-level ATPG patterns to isolate interconnect failures.*

7.1 Short Pin Descriptions

n = port number (1 to 12 for DS32512, 1 to 8 for DS32508, 1 to 6 for DS32506). I = input, Ipu = input with internal pullup resistor, Ipd = input with internal pulldown resistor, Ia = analog input, I/O = bidirectional in/out, I/Opd = bidirectional in/out with internal pulldown resistor, O = output, Oz = high-impedance output (needs an external pullup or pulldown resistor to keep the node from floating), Oa = analog output (high impedance), P = power supply or ground. All unused input pins without pullup should be tied low. Note: All internal pullup resistors are 50kΩ tied to approximately 2.2V DC. See Section 12 for pin assignments.

Table 7-1. Short Pin Descriptions

NAME	TYPE	FUNCTION
ANALOG LINE INTERFACE		
TXPn	Oa	Transmit Positive Analog (Port n)
TXNn	Oa	Transmit Negative Analog (Port n)
RXPn	Ia	Receive Positive Analog (Port n)
RXNn	Ia	Receive Negative Analog (Port n)
DIGITAL FRAMER INTERFACE		
TCLKn	I	Transmit Clock (Port n)
TPOSn/TDATn	I	Transmit Positive AMI/Transmit NRZ Data (Port n)
TNEGn	I	Transmit Negative AMI (Port n)
RCLKn	Oz	Receive Clock (Port n)
RPOSn/RDATn	Oz	Receive Positive AMI/Receive NRZ Data (Port n)
RNEGn/RLCVn	Oz	Receive Negative AMI/Receive Line Code Violation (Port n)
GLOBAL I/O		
IFSEL[2:0]	I	Microprocessor Interface Select
HW	Ipd	Hardware Interface Enable
$\overline{\text{TEST}}$	I	Factory Test Enable (Active Low)
$\overline{\text{HIZ}}$	I	High-Impedance Test Enable (Active Low)
$\overline{\text{RST}}$	Ipu	Reset (Active Low)
RESREF	Oa	Reference Resistor
HARDWARE INTERFACE		
LMn[1:0]	Ipd	LIU Mode Control (DS3, E3, or STS-1) (Port n)
AIST	Ipd	AIS Type Control (All Ports)
TAISn	Ipd	Transmit AIS Control (Port n)
TBIN	Ipd	Transmit Binary Interface Control (All Ports)
TCC	Ipd	Transmit Common Clock Control (All Ports)
TCLKI	Ipd	Transmit Clock Invert Control (All Ports)
TDMn	O	Transmit Driver Monitor Status (Port n)
TLBOn	Ipd	Transmit Line Build-Out Control (Port n)
TOEn	Ipd	Transmit Output-Enable Control (Port n)
TPD	Ipd	Transmit Power-Down (All Ports)
ITRE	I	Internal Termination Resistance Enable (Tx and Rx) (All Ports)
RBIN	Ipd	Receive Binary Interface Control (All Ports)
RCLKI	Ipd	Receive Clock Invert Control (All Ports)
RLOSn	O	Receive Loss-of-Signal Status (Port n)
RMONn	Ipd	Receive Monitor Preamp Control (Port n)

NAME	TYPE	FUNCTION
RPD	Ipd	Receive Power-Down (All Ports)
JAD[1:0]	Ipd	Jitter Attenuator Depth (All Ports)
JAS[1:0]	Ipd	Jitter Attenuator Select (Tx, Rx, or Disabled) (Port n)
LBn[1:0]	I	Loopback Control (Port n)
LBS	Ipd	Loopback Select (all ports)
8-/16-BIT PARALLEL INTERFACE		
$\overline{CS}$	I	Chip Select (Active Low)
$\overline{RD}$/$\overline{DS}$	I	Read Enable (Active Low)/Data Strobe (Active Low)
$\overline{WR}$/R/W	I	Write Enable (Active Low)/Read/Write Select
ALE	I	Address Latch Enable
A[10:1]	I	Address Bus (Excluding LSB)
A[0]/BSWAP	I	Address Bus LSB/Byte Swap
D[15:0]	I/O	Data Bus [15:0]
RDY/ACK	Oz	Ready/Acknowledge (Active Low)
$\overline{INT}$	Oz	Interrupt (Active Low)
GPIOAn	I/Opd	General-Purpose I/O A (Port n)
GPIOBn	I/Opd	General-Purpose I/O B (Port n)
SPI SERIAL INTERFACE		
$\overline{CS}$	I	Chip Select (Active Low)
SCLK	I	Serial Clock
SDI	I	Serial Data Input
SDO	O	Serial Data Output
CPHA	I	Clock Phase
CPOL	I	Clock Polarity
$\overline{INT}$	Oz	Interrupt Output (Active Low)
GPIOAn	I/Opd	General-Purpose I/O A (Port n)
GPIOBn	I/Opd	General-Purpose I/O B (Port n)
CLAD		
REFCLK	I	Reference Clock
CLKA	I/O	Clock A—DS3 44.736MHz
CLKB	I/O	Clock B—E3 34.368MHz
CLKC	I/O	Clock C—STS-1 51.84MHz
CLKD	O	Clock D—Telecom Bus 77.76MHz or 19.44MHz
CLADBYP	I	CLAD Bypass
JTAG		
JTCLK	I	JTAG Clock
JTMS	I_{PU}	JTAG Mode Select
JTDI	I_{PU}	JTAG Data Input
JTDO	Oz	JTAG Data Output
JTRST	I_{PU}	JTAG Reset (Active Low)
POWER SUPPLY AND GROUND PINS		
VDD18	P	Digital Core 1.8V Power, 1.8V ±5%
VDD33	P	I/O 3.3V Power, 3.3V ±5%
VSS	P	Ground for VDD18 and VDD33
JVDDn	P	Jitter Attenuator 1.8V Power, 1.8V ±5% (Port n)
JVSSn	P	Jitter Attenuator Ground (Port n)
RVDDn	P	Receive 1.8V Power, 1.8V ±5% (Port n)

NAME	TYPE	FUNCTION
RVSSn	P	Receive Ground (Port n)
TVDDn	P	Transmit 1.8V Power, 1.8V ±5% (Port n)
TVSSn	P	Transmit Ground (Port n)
CVDD	P	CLAD 1.8V ±5%
CVSS	P	CLAD Ground
MANUFACTURING TEST		
MT[10:0]	Test	Manufacturing Test Pins

7.2 Detailed Pin Descriptions

n = port number (1 to 12 for DS32512, 1 to 8 for DS32508, 1 to 6 for DS32506). I = input, Ipu = input with internal pullup resistor, Ipd = input with internal pulldown resistor, Ia = analog input, I/O = bidirectional in/out, I/Opd = bidirectional in/out with internal pulldown resistor, O = output, Oz = high-impedance output (needs an external pullup or pulldown resistor to keep the node from floating), Oa = analog output (high impedance), P= power supply or ground. All unused input pins without pullup should be tied low. Note: All internal pullup resistors are 50kΩ tied to 2.2V DC.

Table 7-2. Analog Line Interface Pin Descriptions

NAME	TYPE	FUNCTION
TXPn, TXNn	Oa	**Transmitter Analog Outputs.** These differential AMI outputs are coupled to the outbound 75Ω coaxial cable through a 1:1 transformer (Figure 4-1). These outputs can be disabled (high impedance) using the TOEn pin or the TOE or TPD configuration bits. See Section 8.2.8.
RXPn, RXNn	Ia	**Receiver Analog Inputs.** These differential AMI inputs are coupled to the inbound 75Ω coaxial cable through a 1:1 transformer (Figure 4-1). See Section 8.3.1.

Table 7-3. Digital Framer Interface Pin Descriptions

NAME	TYPE	FUNCTION
TCLKn	I	**Transmit Clock.** A DS3 (44.736MHz ±20ppm), E3 (34.368MHz ±20ppm), or STS-1 (51.840MHz ±20ppm) clock should be applied at this pin. Data to be transmitted is clocked into the device at TPOS/TDAT and TNEG either on the rising edge of TCLK (TCLKI = 0) or the falling edge of TCLK (TCLKI = 1). When pin TCC = 1, all ports are clocked by TCLK1, and TCLKx (x ≠ 1) are ignored. See Section 8.2.1 for additional details.
TPOSn/ TDATn	I	**Transmit Positive AMI/Transmit NRZ Data.** This pin is sampled either on the rising edge of TCLK (TCLKI = 0) or on the falling edge of TCLK (TCLKI = 1). See Section 8.2.2. *TPOSn*: When the transmitter is configured to have a bipolar interface (TBIN = 0), a positive pulse is transmitted on the line when TPOS is high. *TDATn*: When the transmitter is configured to have a binary interface (TBIN = 1), the data on TDAT is transmitted after B3ZS or HDB3 encoding.
TNEGn	I	**Transmit Negative AMI.** When the transmitter is configured to have a bipolar interface (TBIN = 0), a negative pulse is transmitted on the line when TNEG is high. When the transmitter is configured to have a binary interface (TBIN = 1), TNEG is ignored and should be wired either high or low. TNEG is sampled either on the rising edge of TCLK (TCLKI = 0) or the falling edge of TCLK (TCLKI = 1). See Section 8.2.2.
RCLKn	Oz	**Receive Clock.** The clock recovered from the receive signal is output on the RCLK pin. Recovered data is output on the RPOS/RDAT and RNEG/RLCV pins on the falling edge of RCLK (RCLKI = 0) or the rising edge of RCLK (RCLKI = 1). During a loss-of-signal condition (RLOSn = 0), the RCLK output signal is derived from the LIU's reference clock. See Section 8.3.6.
RPOSn/ RDATn	Oz	**Receive Positive AMI/Receive NRZ Data.** This pin is updated either on the falling edge of RCLK (RCLKI = 0) or the rising edge of RCLK (RCLKI = 1). See Section 8.3.6. *RPOSn*: When the receiver is configured to have a bipolar interface (RBIN = 0), RPOS pulses high for each positive AMI pulse received. *RDATn*: When the receiver is configured to have a binary interface (RBIN = 1), RDAT outputs decoded binary data.
RNEGn/ RLCVn	Oz	**Receive Negative AMI/Receive Line-Code Violation.** This pin is updated either on the falling edge of RCLK (RCLKI = 0) or the rising edge of RCLK (RCLKI = 1). See Section 8.3.6 for further details on code violations. *RNEGn*: When the receiver is configured to have a bipolar interface (RBIN = 0), RNEG pulses high for each negative AMI pulse received. *RLCVn:* When the receiver is configured to have a binary interface (RBIN = 1), RLCV pulses high to flag code violations.

Table 7-4. Global Pin Descriptions

NAME	TYPE	FUNCTION
IFSEL[2:0]	I	**Microprocessor Interface Select.** When no microprocessor interface is selected, all microprocessor interface inputs are ignored and internally pulled low, and all microprocessor interface outputs are put in a high-impedance state. See Section 6 for details. 000 = no microprocessor interface (must set HW = 1 and use hardware interface) 001 = reserved 010 = SPI serial interface, address and data MSB first 011 = SPI serial interface, address and data LSB first 100 = 8-bit parallel interface, Intel style ($\overline{CS}$, $\overline{RD}$, $\overline{WR}$ control signals) 101 = 8-bit parallel interface, Motorola style ($\overline{CS}$, R/W, $\overline{DS}$ control signals) 110 = 16-bit parallel interface, Intel style ($\overline{CS}$, $\overline{RD}$, $\overline{WR}$ control signals) 111 = 16- bit parallel interface, Motorola style ($\overline{CS}$, R/W, $\overline{DS}$ control signals)
HW	Ipd	**Hardware Interface Enable.** When the hardware interface pins are disabled, all hardware control inputs are ignored and internally pulled low, and all hardware status outputs are put in a high impedance state. See Section 6 for details. 0 = Hardware interface pins disabled 1 = Hardware interface pins enabled
$\overline{TEST}$	I	**Factory Test Enable (Active Low).** This pin enables the internal scan test mode when low. For normal operation tie high. This is an asynchronous input.
$\overline{HIZ}$	I	**High-Impedance Test Enable (Active Low).** This signal is used to enable testing. When this signal is low while $\overline{JTRST}$ is low, all the digital output and bidirectional pins are placed in the high-impedance state. For normal operation this signal is high. This is an asynchronous input.
$\overline{RST}$	Ipu	**Reset (Active Low, Open Drain).** When this global asynchronous reset is pulled low, all internal circuitry is reset and all internal registers are forced to their default values. The device is held in reset as long as $\overline{RST}$ is low. $\overline{RST}$ should be held low for at least two reference clock cycles. See Section 8.11.
RESREF	Oa	**Reference Resistor.** This pin is tied to VSS through a 10kΩ ±1% resistor. This accurate resistor is used to calibrate on-chip resistor values including internal transmit and receive termination resistors.

Table 7-5. Hardware Interface Pin Descriptions

NAME	TYPE	FUNCTION
LMn[1:0]	Ipd	**LIU Mode Control (Port n).** When only the hardware interface is enabled (IFSEL = 000 and HW = 1), these pins set the LIU mode for port n. See Section 8.1. 00 = DS3 01 = E3 10 = STS-1 11 = reserved
AIST	Ipd	**AIS Type Control (All Ports).** See Section 8.2.3. 0 = Unframed all ones 1 = Framed DS3 AIS (DS3 mode), unframed all ones (E3 mode), or AIS-L (STS-1 mode)
TAISn	Ipd	**Transmit AIS Control (Port n).** The type of AIS signal is specified by the LMn[1:0] and AIST pins. See Section 8.2.3. 0 = transmit normal data 1 = transmit AIS
TBIN	Ipd	**Transmit Binary Interface Control (All Ports).** See Section 8.2.2. 0 = Transmitter framer interface is bipolar on the TPOS and TNEG pins, and the B3ZS/HDB3 encoder is disabled. 1 = Transmitter framer interface is binary on the TDAT pin, and the B3ZS/HDB3 encoder is enabled.
TCC	Ipd	**Transmit Common Clock Control (All Ports).** When this pin is high, the transmit paths of all ports are clocked by the TCLK1 pin, and pins TCLKx ($x \neq 1$) are ignored. In designs where the transmit paths of all ports can be clocked synchronously with one another, this mode reduces wiring complexity between the LIU and the neighboring framer or mapper component. See Section 8.2.1.
TCLKI	Ipd	**Transmit Clock Invert control (All Ports).** See Section 8.2.1. 0 = TPOS/TDAT and TNEG are sampled on the rising edge of TCLK. 1 = TPOS/TDAT and TNEG are sampled on the falling edge of TCLK.
TDMn	O	**Transmit Driver Monitor Status (Port n).** This pin reports the status of the transmit driver monitor. See Section 8.2.9 for more information. 0 = Transmit line driver is operating properly. 1 = Transmit line driver is faulty.
TLBOn	Ipd	**Transmit Line Build-Out Control (Port n).** This pin specifies cable length for waveform shaping in DS3 and STS-1 modes. In E3 mode it is ignored and should be wired high or low. See Section 8.2.6. 0 = Cable length $\geq$ 225ft 1 = Cable length < 225ft
TOEn	Ipd	**Transmitter Output-Enable Control (Port n).** This pin enables and disables the transmitter outputs. The transmitter continues to operate internally when the outputs are disabled; only the line driver and driver monitor are disabled. See Section 8.2.7. 0 = TXPn/TXNn output drivers disabled (high impedance) 1 = TXPn/TXNn output drivers enabled
TPD	Ipd	**Transmit Power-Down (All Ports).** See Section 8.2.10. 0 = Enable all transmitters 1 = Power down all transmitters (drivers become high impedance)

NAME	TYPE	FUNCTION
ITRE	I	**Internal Termination Resistance Enable (Tx and Rx) (All Ports).** This bit indicates when the internal termination is enabled. See Section 8.2.8. 0 = Disabled. The transmitters and receivers are terminated externally. 1 = Enabled. The transmitters and receivers are terminated internally.
RBIN	Ipd	**Receive Binary Interface Control (All Ports).** See Section 8.3.6. 0 = Receiver framer interface is bipolar on the RPOS and RNEG pins, and the B3ZS/HDB3 encoder is disabled. 1 = Receiver framer interface is binary on the RDAT pin, and the B3ZS/HDB3 encoder is enabled.
RCLKI	Ipd	**Receive Clock Invert Control (All Ports).** See Section 8.3.6.3. 0 = RPOS/RDAT and RNEG/RLCV update on the falling edge of RCLK. 1 = RPOS/RDAT and RNEG/RLCV update on the rising edge of RCLK.
RLOSn	O	**Receive Loss-of-Signal Status (Port n).** This pin is asserted upon detection of 192 consecutive zeros in the receive data stream. It is deasserted when there are no excessive zero occurrences over a span of 192 clock periods. An excessive zero occurrence is defined as three or more consecutive zeros in DS3 and STS-1 modes or four or more zeros in E3 mode. See Section 8.3.5.
RMONn	Ipd	**Receive Monitor Preamp Control (Port n).** This pin determines whether or not the receiver preamp is enabled in port n to provide flat gain to the incoming signal before the AGC/equalizer block processes it. This feature should be enabled when the device is being used to monitor signals that have been resistively attenuated by a monitor jack. See Section 8.3.2 for more information. 0 = Disable the monitor preamp 1 = Enable the monitor preamp
RPD	Ipd	**Receive Power-Down (All Ports).** See Section 8.3.7. 0 = Enable all receivers 1 = Power down all receivers (RXPn/RXNn high impedance. RCLKn, RPOSn/RDATn, and RNEGn/RLCVn high impedance.)
JAD[1:0]	Ipd	**Jitter Attenuator Depth (All Ports).** These pins are ignored when a microprocessor interface is enabled (IFSEL ≠ 000). See Section 8.4. 00 = 16 bits 01 = 32 bits 10 = 64 bits 11 = 128 bits
JAS[1:0]	Ipd	**Jitter Attenuator Select (All Ports).** These pins select the location of the jitter attenuator. These pins are ignored when a microprocessor interface is enabled (IFSEL ≠ 000). See Section 8.4. 00 = Disabled 01 = Receive path 1X = Transmit path
LBn[1:0]	Ipd	**Loopback Control (Port n).** When only the hardware interface is enabled (IFSEL = 000 and HW = 1), these pins set the loopback mode for port n. See Section 8.6. 00 = No loopback 01 = Diagnostic loopback (DLB) 10 = Line loopback (LLB) 11 = (LBS = 0) Line loopback (LLB) and diagnostic loopback (DLB) simultaneously 11 = (LBS = 1) Analog loopback (ALB)
LBS	Ipd	**Loopback Select (All Ports).** This pin specifies how the device interprets the LBn[1:0] bits. This pin is ignored when a microprocessor interface is enabled (IFSEL ≠ 000). See Section 8.6.

Table 7-6. Parallel Interface Pin Descriptions

NAME	TYPE	FUNCTION
$\overline{CS}$	I	**Chip Select (Active Low).** This pin must be asserted to read or write internal registers. See Section 8.8.3.
$\overline{RD}/\overline{DS}$	I	**Read Enable (Active Low)/Data Strobe (Active Low)** *$\overline{RD}$:* For the Intel-style bus (IFSEL = 1X0), $\overline{RD}$ is asserted to read internal registers. *$\overline{DS}$:* For the Motorola-style bus (IFSEL = 1X1), $\overline{DS}$ is asserted to access internal registers while the R/W pin specifies whether the access is a read or a write. See Section 8.8.3.
$\overline{WR}$/R/$\overline{W}$	I	**Write Enable (Active Low)/Read/Write Select** *$\overline{WR}$:* For the Intel-style bus (IFSEL = 1X0), $\overline{WR}$ is asserted to write internal registers. R/W*:* For the Motorola-style bus (IFSEL = 1X1), R/W determines the type of bus transaction, with R/W = 1 indicating a read and R/W = 0 indicating a write. See Section 8.8.3.
ALE	I	**Address Latch Enable.** This pin controls a latch on the A[10:0] inputs. For a nonmultiplexed parallel bus, ALE is wired high to make the latch transparent. For a multiplexed parallel bus, the falling edge of ALE latches the address. See Section 8.8.3.
A[10:1]	I	**Address Bus (Excluding LSB).** These inputs specify the address of the internal 16-bit register to be accessed. A10 is not present on the DS32506. See Section 8.8.
A[0] / BSWAP	I	**Address Bus LSB/Byte Swap.** See Section 8.8.2. *A[0]:* This pin is connected to the lower address bit in 8-bit bus modes (IFSEL = 10X). 0 = Output register bits 7:0 on D[7:0]; D[15:8] high impedance 1 = Output register bits 15:8 on D[7:0]; D[15:8] high impedance *BSWAP:* This pin is tied high or low in 16-bit bus modes (IFSEL = 11X). 0 = Output register bits 15:8 on D[15:8] and bits 7:0 on D[7:0] 1 = Output register bits 7:0 on D[15:8] and bits 15:8 on D[7:0]
D[15:0]	I/O	**Data Bus.** A 8-bit or 16-bit bidirectional data bus. These pins are inputs during writes to internal registers and outputs during reads. D[15:8] are disabled (high impedance) in 8-bit bus modes (IFSEL = 10X). D[15:0] are disabled (high impedance) when $\overline{CS}$ = 1 or $\overline{RST}$ = 0. In 16-bit bus modes (IFSEL = 11X) the upper and lower bytes can be swapped by pulling the BSWAP pin high. See Section 8.8.
RDY/$\overline{ACK}$	Oz	**Ready Handshake (Tri-State)/Acknowledge Handshake (Tri-State, Active Low).** Tri-stated when $\overline{CS}$ = 1 or $\overline{RST}$ = 0. See Section 8.8. *RDY:* Intel Mode (IFSEL = 100 or 110): RDY goes high when the read or write cycle can progress. *$\overline{ACK}$:* Motorola Mode (IFSEL = 101 or 111): $\overline{ACK}$ goes low when the read or write cycle can progress.
$\overline{INT}$	Oz	**Interrupt Output (Active Low, Open Drain, or Push-Pull).** This pin is driven low in response to one or more unmasked, active interrupt sources within the device. $\overline{INT}$ remains low until the interrupt is serviced or masked. When GLOBAL.CR2:INTM = 0, $\overline{INT}$ is high impedance when inactive (default). When INTM = 1, $\overline{INT}$ is driven high when inactive. $\overline{INT}$ is high impedance when $\overline{RST}$ = 0. See Section 8.10.
GPIOAn	I/Opd	**General-Purpose I/O A.** When a microprocessor interface is enabled (IFSEL ≠ 000), this pin is the “A” general-purpose I/O pin for port n. See Section 8.7.3.
GPIOBn	I/Opd	**General-Purpose I/O B.** When a microprocessor interface is enabled (IFSEL ≠ 000), this pin is the “B” general-purpose I/O pin for port n. See Section 8.7.3. Note: GPIOB1, GPIOB2, and GPIOB3 can also be programmed as global control/status pins.

Table 7-7. SPI Serial Interface Pin Descriptions

NAME	TYPE	FUNCTION
$\overline{CS}$	I	**Chip Select (Active Low).** This pin must be asserted to read or write internal registers. See Section 8.9.
SCLK	I	**Serial Clock.** SCLK is always driven by the SPI bus master. See Section 8.9.
SDI	I	**Serial Data Input.** The SPI bus master transmits data to the device on this pin. See Section 8.9.
SDO	O	**Serial Data Output.** The device transmits data to the SPI bus master on this pin. See Section 8.9.
CPHA	I	**Clock Phase.** See Section 8.9. 0 = Data is latched on the leading edge of the SCLK pulse 1 = Data is latched on the trailing edge of the SCLK pulse
CPOL	I	**Clock Polarity.** See Section 8.9. 0 = SCLK is normally low and pulses high during bus transactions 1 = SCLK is normally high and pulses low during bus transactions
$\overline{INT}$	Oz	**Interrupt Output (Active Low, Open Drain).** See $\overline{INT}$ pin description in Table 7-6.
GPIOAn	I/Opd	**General-Purpose I/O A.** See GPIOAn pin description in Table 7-6.
GPIOBn	I/Opd	**General-Purpose I/O B.** See GPIOBn pin description in Table 7-6.

Table 7-8. CLAD Pin Descriptions

NAME	TYPE	FUNCTION
REFCLK	I	**Reference Clock.** The signal on this pin is the input reference clock to the CLAD and must be transmission quality (±20ppm, low jitter). In hardware mode, REFCLK must be 19.44MHz. In bus interface modes, REFCLK can be any of several frequencies. See Section 8.7.1.
CLKA	I/O	**Clock A—DS3 44.736MHz.** When the CLAD is bypassed, a transmission-quality DS3 clock (44.736MHz ±20ppm, low jitter) must be connected to this pin if any of the LIUs are to operate in DS3 mode. When the CLAD is enabled this pin can be configured to output the DS3 clock synthesized by PLL-A. See Section 8.7.1.
CLKB	I/O	**Clock B—E3 34.368MHz.** When the CLAD is bypassed, a transmission-quality E3 clock (34.368MHz ±20ppm, low jitter) must be connected to this pin if any of the LIUs are to operate in E3 mode. When the CLAD is enabled, this pin can be configured to output the E3 clock synthesized by PLL-B. See Section 8.7.1.
CLKC	I/O	**Clock C—STS-1 51.84MHz.** When the CLAD is bypassed, a transmission-quality STS-1 clock (51.84MHz ±20ppm, low jitter) must be connected to this pin if any of the LIUs are to operate in STS-1 mode. When the CLAD is enabled, this pin can be configured to output the STS-1 clock synthesized by PLL-C. See Section 8.7.1.
CLKD	O	**Clock D—Telecom Bus 77.76MHz or 19.44MHz.** When the CLAD is bypassed, this pin is driven low. When the CLAD is enabled this pin can output a 77.76MHz or 19.44MHz clock synthesized by PLL-D. See Section 8.7.1.
CLADBYP	I	**CLAD Bypass Control.** This pin controls whether the CLAD is used or bypassed. When a microprocessor interface is enabled (IFSEL ≠ 000), CLADBYP should be wired low to allow use of the GLOBAL.CR2:CLAD[6:0] field to control the CLAD. See Section 8.7.1. 0 = Synthesize the DS3, E3, and STS-1 clocks from the clock on the REFCLK pin. 1 = Source the DS3, E3, and STS-1 clocks from the CLKA, CLKB and CLKC pins.

Table 7-9. JTAG Pin Descriptions

NAME	TYPE	FUNCTION
JTCLK	I	**JTAG Clock.** This pin shifts data into JTDI on the rising edge and out of JTDO on the falling edge. JTCLK is typically a low frequency (less than 10MHz) 50% duty cycle clock signal. If boundary scan is not used, JTCLK should be pulled high. See Section 10.
JTMS	Ipu	**JTAG Mode Select.** This pin is used to control the JTAG controller state machine. JTMS is sampled on the rising edge of JTCLK. If boundary scan is not used, JTMS should be left unconnected or pulled high. See Section 10.
JTDI	Ipu	**JTAG Data Input.** This pin is used to input data into the register that is enabled by the JTAG controller state machine. JTDI is sampled on the rising edge of JTCLK. If boundary scan is not used, JTDI should be left unconnected or pulled high. See Section 10.
JTDO	Oz	**JTAG Data Output.** This pin is the output of an internal scan shift register enabled by the JTAG controller state machine. JTDO is updated on the falling edge of JTCLK. JTDO is in high-impedance mode when a register is not selected or when the $\overline{\text{JTRST}}$ pin is low. JTDO goes into and out of high-impedance mode after the falling edge of JTCLK. See Section 10.
$\overline{\text{JTRST}}$	Ipu	**JTAG Reset (Active Low).** When active, this pin forces the JTAG controller logic into the reset state and forces the JTDO pin into high-impedance mode. The JTAG controller is also reset when power is first applied via a power-on reset circuit. $\overline{\text{JTRST}}$ can be driven high or low for normal operation, but must be high for JTAG operation. See Section 10.

Table 7-10. Power-Supply Pin Descriptions

NAME	TYPE	FUNCTION
VDD18	P	**Digital Core 1.8V Power, 1.8V ±5%**
VDD33	P	**I/O 3.3V Power, 3.3V ±5%**
VSS	P	**Ground for VDD18 and VDD33**
JVDDn	P	**Jitter Attenuator 1.8V Power, 1.8V ±5%**
JVSSn	P	**Jitter Attenuator Ground**
RVDDn	P	**Receive 1.8V Power, 1.8V ±5%**
RVSSn	P	**Receive Ground**
TVDDn	P	**Transmit 1.8V Power, 1.8V ±5%**
TVSSn	P	**Transmit Ground**
CVDD	P	**CLAD 1.8V ±5%**
CVSS	P	**CLAD Ground**

Table 7-11. Manufacturing Test Pin Descriptions

NAME	TYPE	FUNCTION
MT[10:0]	Test	**Manufacturing Test Pins 10 to 0.** MT[0] and MT[2:10] must not be connected. MT[1] must be connected to digital ground (same as VSS pins).

8. FUNCTIONAL DESCRIPTION

8.1 LIU Mode

Each port is independently configurable for DS3, E3 or STS-1 operation. When only the hardware interface is enabled (IFSEL = 000 and HW = 1), the LMn[1:0] pins specify the LIU mode. When a microprocessor interface is enabled (IFSEL ≠ 000) the PORT.CR2:LM[1:0] control bits specify the LIU mode.

8.2 Transmitter

8.2.1 Transmit Clock

If the jitter attenuator is not enabled in the transmit path, the signal on TCLK is the transmit line clock and must be transmission quality (i.e., ±20ppm frequency accuracy and low jitter). If the jitter attenuator is enabled in the transmit path, the signal on TCLK can be jittery and/or periodically gapped, but must still have an average frequency within ±20ppm of the nominal line rate. When enabled in the transmit path, the jitter attenuator generates the transmit line clock. See Section 8.4 for more information about the jitter attenuator.

The polarity of TCLK can be inverted to support glueless interfacing to a variety of neighboring components. Normally data is sampled on the TPOS/TDAT and TNEG pins on the rising edge of TCLK. To sample these pins on the falling edge of TCLK, pull the TCLKI pin high or set the PORT.INV:TCLKI configuration bit.

8.2.1.1 Transmit Common Clock Mode

When the TCC pin is high, the transmit paths of all ports are clocked from TCLK1 and pins TCLKx (x ≠ 1) are ignored. When the TCC pin is low, the PORT.CR2:TCC register bit specifies whether the transmit clock for port n comes from TCLKn or TCLK1. In designs where the transmit paths of all ports can be clocked synchronously with one another, common transmit clocking reduces wiring complexity between the LIU and the neighboring framer or mapper component.

8.2.2 Framer Interface Format and the B3ZS/HDB3 Encoder

Data to be transmitted can be input in either bipolar or binary format.

8.2.2.1 Bipolar Interface Format

To select the bipolar interface format, pull the TBIN pin low and clear the PORT.CR2:TBIN configuration bit. In bipolar format, the B3ZS/HDB3 encoder is disabled and the data to be transmitted is sampled on the TPOS and TNEG pins. Positive-polarity pulses are indicated by TPOS = 1, while negative-polarity pulses are indicated by TNEG = 1. If TPOS and TNEG are high at the same time the transmitter generates an AMI pulse that is the opposite state of the pulse previously transmitted.

8.2.2.2 Binary Interface Format

To select the binary interface format, pull the TBIN pin high (all ports) or set the PORT.CR2:TBIN configuration bit (per port). In binary format, the B3ZS/HBD3 encoder is enabled, and the NRZ data to be transmitted is sampled on the TDAT pin. The TNEG pin is ignored in binary interface mode and should be wired low. In DS3 and STS-1 modes, B3ZS encoding is performed. In these modes, whenever three consecutive zeros are found in the transmit data stream they are replaced with a B3ZS codeword. In E3 mode HDB3 encoding is performed. In this mode, whenever four consecutive zeros are found in the transmit data stream they are replaced with an HDB3 codeword. In all three modes, the B3ZS or HDB3 codeword is constructed such that the last bit is a BPV with the opposite polarity of the most recently transmitted BPV.

8.2.3 Error Insertion

Bipolar violation (BPV) errors and excessive zeros (EXZ) errors can be inserted into the transmit data stream using the transmit manual error insert (TMEI) logic (see Section 8.7.5). Configuration bit LINE.TCR:BPVI enables the insertion of bipolar violations, while LINE.TCR:EXZI enables the insertion of excessive zero events. Note: BPV errors and EXZ errors can only be inserted in the binary interface format.

If the transmitter is configured for binary interface format (Section 8.2.2.2) and BPVI = 1 then when the configured manual error insert control goes from zero to one, the transmitter waits for the next occurrence of two consecutive

1s where the polarity of the first 1 is opposite the polarity of the BPV in the last B3ZS/HDB3 codeword. The first 1 is transmitted according to the normal AMI rule, but the second 1 is transmitted with the same polarity as the first 1, thus making the second 1 a bipolar violation.

If the transmitter is configured for binary interface format (Section 8.2.2.2) and EXZI = 1, then when the configured manual error insert control goes from zero to one, the transmitter waits for the next occurrence of three (four) consecutive zeros in the transmit data stream and inhibits the replacement of those zeros with a B3ZS (HDB3) codeword.

The transmitter ensures that there is at least one intervening 1 between consecutive BPV or EXZ errors. If a second error insertion request of a given type (BPV or EXZ) is initiated before a previous request has been completed, the second request is ignored.

8.2.4 AIS Generation

The transmitter can be configured to transmit an AIS signal by asserting the TAIS pin or the PORT.CR3:TAIS configuration bit. The type of AIS signal to be generated is specified by the LIU mode (LMn[1:0] pins or PORT.CR2:LM[1:0] configuration bits) and the AIS type (AIST pin or PORT.CR3:AIST configuration bit). When AIST = 0, the AIS signal is unframed all ones for DS3, E3 and STS-1 modes. When AIST = 1, the AIS signal is the framed DS3 AIS signal in DS3 mode, unframed all ones in E3 mode, and the AIS-L signal in STS-1 mode. The AIS-L signal is normally scrambled, but scrambling can be disabled by setting PORT.CR3:SCRD = 1.

8.2.5 Waveshaping

8.2.5.1 Standards-Compliant Waveshaping

Waveshaping converts the transmit clock, positive data, and negative data signals into a single analog AMI signal with the waveshape required for interfacing to DS3/E3/STS-1 lines. Figure 8-1 and Table 8-2 show the DS3 waveform equations and template. Figure 8-2 and Table 8-4 show the STS-1 waveform equations and template. Figure 8-3 shows the E3 waveform template.

8.2.5.2 Programmable Waveshaping

The transmit waveshape can be adjusted with the TWSC[19:0] bits in the LIU.TWSCR1 and LIU.TWSCR2 registers. These signals control the amplitude, slew rates and various other aspects of the waveform template. See the register descriptions for further details.

8.2.6 Line Build-Out

Because DS3 and STS-1 signals must meet the waveform templates at the cross-connect through any cable length from 0 to 450 feet, the waveshaping circuitry includes a selectable LBO feature. For cable lengths of 225 feet or greater, both the TLBO pin and the LIU.CR1:TLBO configuration bit should be low to disable the LBO circuitry. When the LBO circuitry is disabled, output pulses are driven onto the coaxial cable without any preattenuation. For cable lengths less than 225 feet, either the TLBO pin or the LIU.CR1:TLBO configuration bit should be high to enable the LBO circuitry. When the LBO circuitry is enabled, pulses are preattenuated by the LBO circuitry before being driven onto the coaxial cable to provide attenuation that mimics the attenuation of 225 feet of coaxial cable.

8.2.7 Line Driver

The transmit line driver can be disabled (TXP and TXN outputs high impedance) by deasserting the TOE pin and deasserting the LIU.CR1:TOE configuration bit. Powering down the transmitter through the TPD pin or the PORT.CR1:TPD configuration bit also disables the transmit line driver.

8.2.8 Interfacing to the Line

The transmitter interfaces to the outgoing DS3/E3/STS-1 coaxial cable (75Ω) through a 1:1 isolation transformer connected to the TXP and TXN pins. The transmit line termination can be internal to the device, external to the device, or a combination of both. Figure 4-1 shows the arrangement of the transformer when the internal termination is enabled (LIU.CR1:TTRE = 1) and no external termination resistors are used. Figure 4-2 shows the arrangement of the transformer and external termination resistors when the internal termination is disabled (LIU.CR1:TTRE = 0). The internal termination resistor value for the transmitter is specified in LIU.CR1:TRESADJ. Table 8-7 and Table 8-8 specify the required characteristics of the transformer and provide a list of recommended transformers.

8.2.9 Driver Monitor and Output Failure Detection

The transmit driver monitor compares the amplitude of the transmit waveform to thresholds V_{TXMIN} and V_{TXMAX}. If the amplitude is less than V_{TXMIN} or greater than V_{TXMAX} for approximately 32 MCLK cycles, then the monitor activates the TDM output pin (if the hardware interface is enabled) and sets the LIU.SR:TDM status bit. The setting of LIU.SR:TDM can cause an interrupt if enabled by LIU.SRIE:TDMIE. When the transmitter is disabled, the transmit driver monitor is also disabled. The transmit driver monitor is clocked by the LIU's reference clock.

Note that the transmit driver monitor can be affected by reflections caused by shorts and opens on the line. A short circuit at a distance less than a few inches (~11 inches for FR-4 material) can introduce inverted reflections that reduce the outgoing pulse amplitude below the V_{TXMIN} threshold and thereby activate the TDM pin and/or the TDM status bit. Similarly an open circuit a similar distance away can introduce noninverted reflections that increase the outgoing amplitude above the V_{TXMAX} threshold and thereby activate the TDM pin and/or the TDM status bit. Shorts and opens at larger distances away from TXP/TXN can also activate the TDM pin and/or the TDM status bit, but this effect is data-pattern dependent.

If either TXP or TXN is not connected (open), shorted to V_{DD}, or shorted to V_{SS}, then a transmit failure alarm is declared by setting the LIU.SR:TFAIL status bit. A change of state of the TFAIL status bit can cause an interrupt if enabled by LIU.SRIE:TFAILIE. TFAIL is cleared when activity is detected on both TXP and TXN.

8.2.10 Power-Down

To minimize power consumption when the transmitter is not being used, the TPD pin (all ports) or the PORT.CR1:TPD configuration bit (per port) can be asserted. When the transmitter is powered down, the TXP and TXN pins are put in a high-impedance state and the transmit drivers are powered down.

8.2.11 Jitter Generation (Intrinsic)

The transmitter meets the jitter generation requirements of all applicable standards in Table 8-1, with or without the jitter attenuator enabled. Generated jitter is measured with a jitter-free, 0ppm input clock.

Table 8-1. Jitter Generation

SIGNAL	STANDARD	REQUIREMENT	BANDWIDTH	DS325xx JITTER				UNITS
				WITHOUT CLAD		WITH CLAD		
				TYP	MAX	TYP	MAX	
DS3	GR-499	0.3 UI_{RMS}	10Hz to 400kHz	0.01	0.02	0.01	0.02	UI_{RMS}
DS3	T1.404	0.5 UI_{P-P}	10Hz to 400kHz	0.02	0.03	0.05	0.06	UI_{P-P}
DS3	T1.404	0.05 UI_{P-P}	30kHz to 400kHz	0.015	0.025	0.04	0.05	UI_{P-P}
E3	G.751	0.05 UI_{P-P}	100Hz to 800kHz	0.02	0.03	0.04	0.05	UI_{P-P}
STS-1	GR-253	0.01 UI_{RMS}	12kHz to 400kHz	0.005	0.008	0.007	0.01	UI_{RMS}
STS-1	GR-253	0.10 UI_{P-P}	12kHz to 400kHz	0.04	0.06	0.06	0.08	UI_{P-P}

8.2.12 Jitter Transfer

Without the jitter attenuator on the transmit side, the transmitter passes jitter through unchanged. With the jitter attenuator enabled on the transmit side, the transmitter meets the jitter transfer requirements of all applicable telecommunication standards in Table 1-1. See Figure 8-7.

Figure 8-1. DS3 Waveform Template

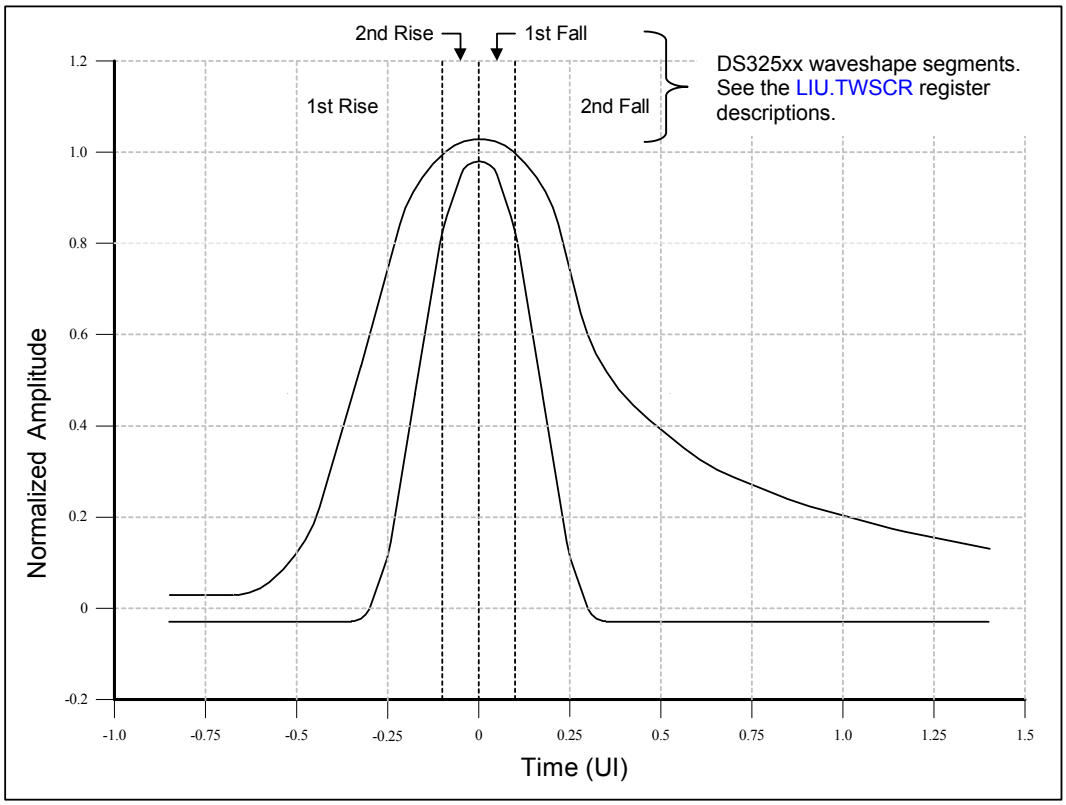


Table 8-2. DS3 Waveform Equations

TIME (IN UNIT INTERVALS)	NORMALIZED AMPLITUDE EQUATION
UPPER CURVE	
$-0.85 \le T \le -0.68$	0.03
$-0.68 \le T \le +0.36$	$0.5\{1 + \sin[(\pi / 2)(1 + T / 0.34)]\} + 0.03$
$0.36 \le T \le 1.4$	$0.08 + 0.407e^{-1.84(T - 0.36)}$
LOWER CURVE	
$-0.85 \le T \le -0.36$	-0.03
$-0.36 \le T \le +0.36$	$0.5\{1 + \sin[(\pi / 2)(1 + T / 0.18)]\} - 0.03$
$0.36 \le T \le 1.4$	-0.03

Table 8-3. DS3 Waveform Test Parameters and Limits

PARAMETER	SPECIFICATION
Rate	44.736Mbps (±20ppm)
Line Code	B3ZS
Transmission Medium	Coaxial cable (AT&T 734A or equivalent)
Test Measurement Point	At the end of 0 to 450ft of coaxial cable
Test Termination	75Ω (±1%) resistive
Pulse Amplitude	Between 0.36V and 0.85V
Pulse Shape	An isolated pulse (preceded by two zeros and followed by one zero) falls within the curves listed in Table 8-2.
Unframed All-Ones Power Level at 22.368MHz	Between -1.8dBm and +5.7dBm
Unframed All-Ones Power Level at 44.736MHz	At least 20dB less than the power at 22.368MHz
Pulse Imbalance of Isolated Pulses	Ratio of positive and negative pulses must be between 0.90 and 1.10

Figure 8-2. STS-1 Waveform Template

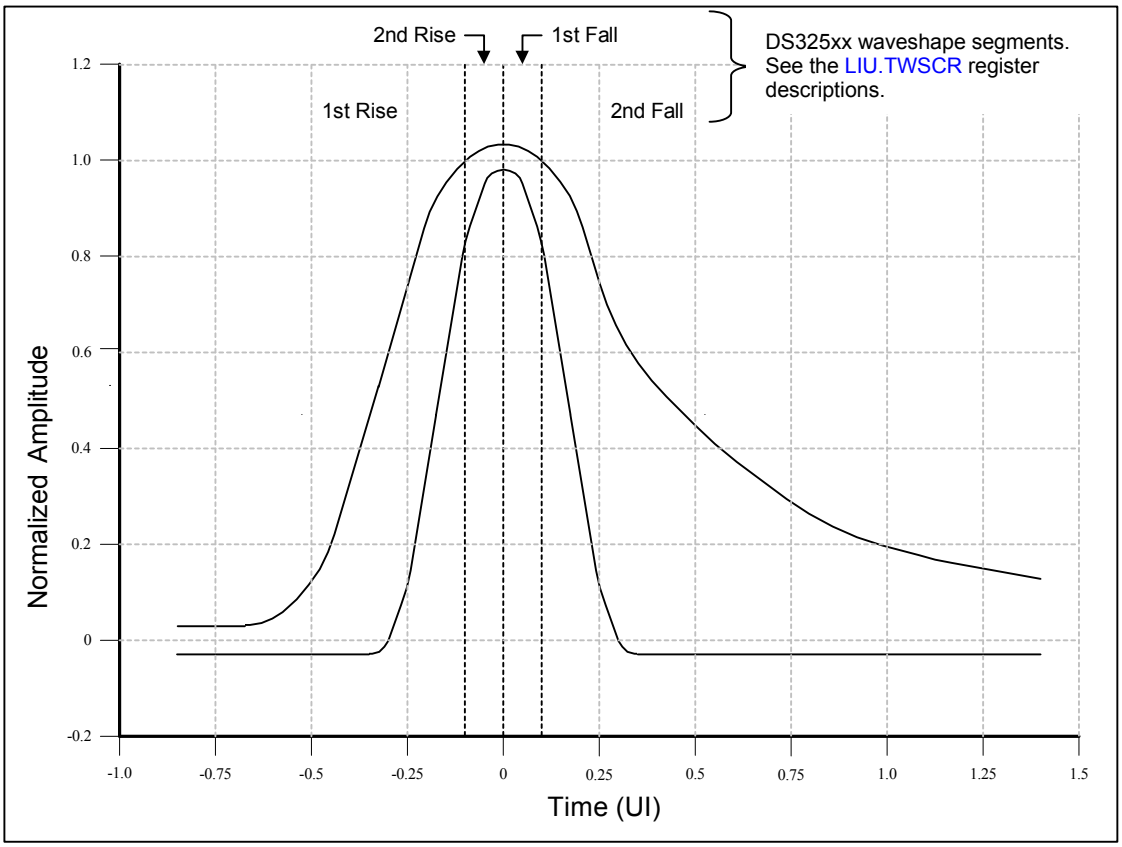


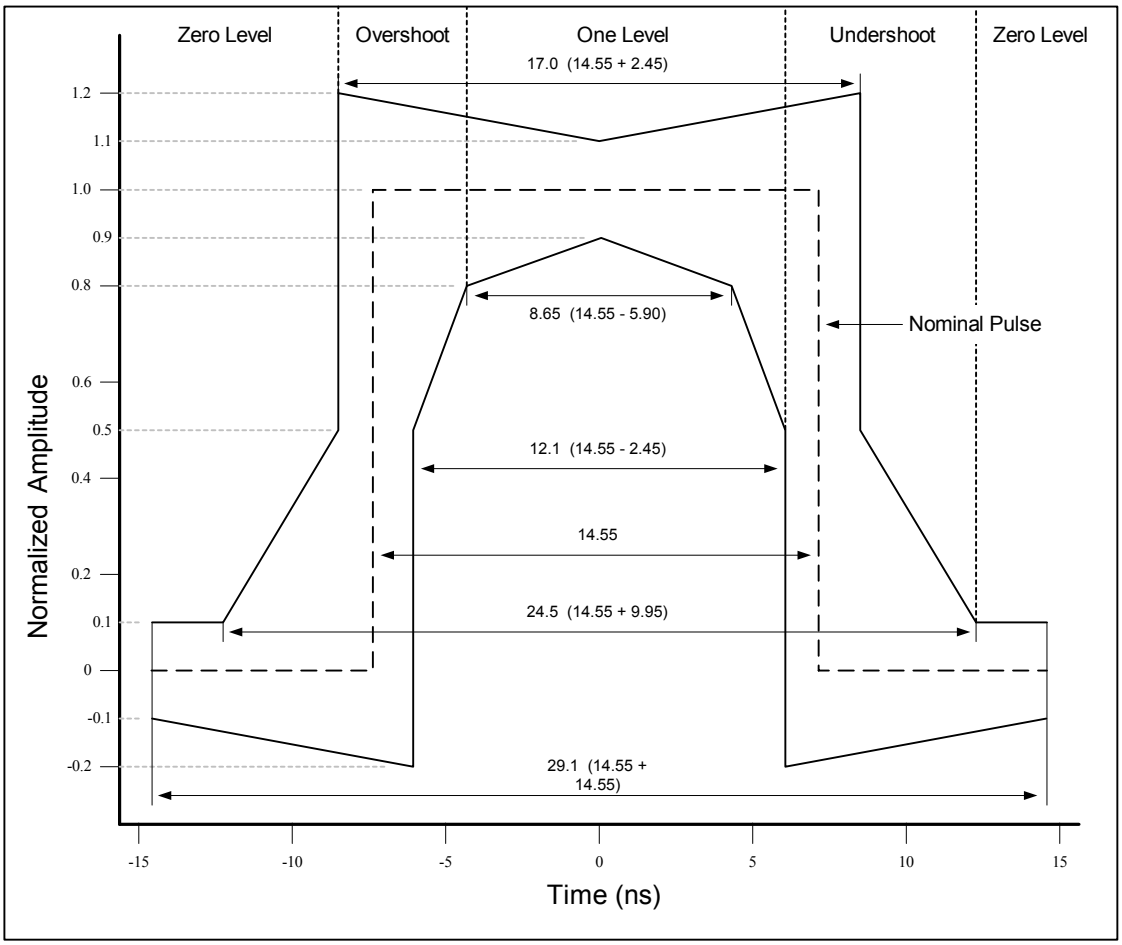
Table 8-4. STS-1 Waveform Equations

TIME (IN UNIT INTERVALS)	NORMALIZED AMPLITUDE EQUATIONS
UPPER CURVE	
$-0.85 \le T \le -0.68$	0.03
$-0.68 \le T \le +0.26$	$0.5 \{1 + \sin[(\pi / 2)(1 + T / 0.34)]\} + 0.03$
$0.26 \le T \le 1.4$	$0.1 + 0.61e^{-2.4(T - 0.26)}$
LOWER CURVE	
$-0.85 \le T \le -0.36$	-0.03
$-0.36 \le T \le +0.36$	$0.5 \{1 + \sin[(\pi / 2)(1 + T / 0.18)]\} - 0.03$
$0.36 \le T \le 1.4$	-0.03

Table 8-5. STS-1 Waveform Test Parameters and Limits

PARAMETER	SPECIFICATION
Rate	51.840Mbps (±20ppm)
Line Code	B3ZS
Transmission Medium	Coaxial cable (AT&T 734A or equivalent)
Test Measurement Point	At the end of 0 to 450ft of coaxial cable
Test Termination	75Ω (±1%) resistive
Pulse Amplitude	0.800V nominal (not covered in specs)
Pulse Shape	An isolated pulse (preceded by two zeros and followed by one zero) falls within the curved listed in Table 8-4.
Unframed All-Ones Power Level at 25.92MHz	Between -1.8dBm and +5.7dBm
Unframed All-Ones Power Level at 51.84MHz	At least 20dB less than the power at 25.92MHz

Figure 8-3. E3 Waveform Template



DS325xx waveshape segments. See the LIU.TWSCR register descriptions.

Table 8-6. E3 Waveform Test Parameters and Limits

PARAMETER	SPECIFICATION
Rate	34.368Mbps (±20ppm)
Line Code	HDB3
Transmission Medium	Coaxial cable (AT&T 734A or equivalent)
Test Measurement Point	At the transmitter
Test Termination	75Ω (±1%) resistive
Pulse Amplitude	1.0V (nominal)
Pulse Shape	An isolated pulse (preceded by two zeros and followed by one or more zeros) falls within the template shown in Figure 8-3.
Ratio of the Amplitudes of Positive and Negative Pulses at the Center of the Pulse Interval	0.95 to 1.05
Ratio of the Widths of Positive and Negative Pulses at the Nominal Half Amplitude	0.95 to 1.05

8.3 Receiver

8.3.1 Interfacing to the Line

The receiver can be transformer-coupled or capacitor-coupled to the line. Typically, the receiver interfaces to the incoming coaxial cable (75Ω) through a 1:1 isolation transformer. The receive line termination can be internal to the device, external to the device, or a combination of both. Figure 4-1 shows the arrangement of the transformer when the internal termination is enabled (LIU.CR2:RTRE = 1) and no external termination resistors are used. Figure 4-2 shows the arrangement of the transformer and external termination resistors when the internal termination is disabled (LIU.CR2:RTRE = 0). The internal termination resistor value is specified in LIU.CR2:RRESADJ[3:0]. Table 8-7 and Table 8-8 specify the required characteristics of the transformer and provide a list of recommended transformers. The receiver expects the incoming signal to be in B3ZS- or HDB3-coded AMI format.

Table 8-7. Transformer Characteristics

PARAMETER	VALUE
Turns Ratio	1:1 ±2%
Bandwidth 75Ω	0.200MHz to 340MHz (typ)
Primary Inductance	40µH (min)
Leakage Inductance	0.12µH (max)
Interwinding Capacitance	10pF (max)
Isolation Voltage	1500V_{RMS} (min)

Table 8-8. Recommended Transformers

MANUFACTURER	PART	TEMP RANGE	PIN-PACKAGE/ SCHEMATIC	OCL PRIMARY (µH) (min)	L_L (µH) (max)	BANDWIDTH 75Ω (MHz)
Pulse Engineering	PE-65967	0°C to +70°C	6 SMT LS-1/E	40	0.10	1500
Pulse Engineering	PE-65966	0°C to +70°C	6 THT LC-1/E	40	0.10	1500
Pulse Engineering	T3001	-40°C to +85°C	6 SMT LS-2/E	40	0.11	1500
Pulse Engineering	TX3025	-40°C to +85°C	16 SMT BH/3	100	0.120	1500
Pulse Engineering	TX3036	-40°C to +85°C	24 SMT	100	0.110	1500
Pulse Engineering	TX3047	-40°C to +85°C	32 SMT YB/1	100	0.150	1500
Pulse Engineering	TX3051	-40°C to +85°C	48 SMT	60	0.120	1500
Halo Electronics	TG01-0406NS	0°C to +70°C	6 SMT SMD/A	40	0.10	1500
Halo Electronics	TD01-0406NS	0°C to +70°C	6 DIP DIP/A	40	0.10	1500
Halo Electronics	TG01-0456NS	-40°C to +85°C	6 SMT SMD/A	45	0.12	1500
Halo Electronics	TD01-0456NE	-40°C to +85°C	6 DIP DIP/A	45	0.12	1500

Note: *Table subject to change. Multiport transformers are also available. Contact the manufacturers for details at www.pulseeng.com and www.haloelectronics.com.*

8.3.2 Optional Preamp

The receiver can be used in monitoring applications that typically have series resistors with a resistive loss of approximately 20dB. When the RMON pin is high or the LIU.CR2:RMON configuration bit is set, the receiver can compensate for this resistive loss by applying 14dB of additional flat gain to the incoming signal before sending the signal to the AGC/equalizer block (an additional 6dB of flat gain is applied in the AGC circuitry for a total gain of 20dB). When the preamp is enabled the receiver automatically determines whether or not to make use of the preamp's additional gain. Status bit LIU.SR:RPAS indicates whether or not the preamp is in use. A change of state of LIU.SR:RPAS can cause an interrupt if enabled by LIU.SRIE:RPASIE.

8.3.3 Automatic Gain Control (AGC) and Adaptive Equalizer

The AGC circuitry applies flat (frequency independent) gain to the incoming signal to compensate for flat losses in the transmission channel and variations in transmission power. Since the incoming signal also experiences frequency-dependent losses as it passes through the coaxial cable, the adaptive equalizer circuitry applies frequency-dependent gain to offset line losses and restore the signal. The AGC/equalizer circuitry automatically adapts to coaxial cable losses from 0 to 22dB, which translates into 0 to 457 meters (1500 feet) of coaxial cable

(AT&T 734A or equivalent). The AGC and the equalizer work simultaneously but independently to supply a signal of nominal amplitude and pulse shape to the clock and data recovery block. The AGC/equalizer block automatically handles direct (0 meters) monitoring of the transmitter output signal. The real-time receiver gain level can be read from the LIU.RGLR register. Note: When the receiver preamp is on (LIU.SR:RPAS = 1), the actual receiver gain level is the level read from the LIU.RGLR register plus 14dB.

8.3.4 Clock and Data Recovery (CDR)

The CDR block takes the amplified, equalized signal from the AGC/equalizer block and produces separate clock, positive data, and negative data signals. The CDR operates from the LIU's reference clock. See Section 8.7.1 for more information about reference clocks and clock selection.

The receiver locks onto the incoming signal using a clock recovery PLL. The PLL lock status is indicated in the LIU.SR:RLOL status bit. The RLOL bit is set when the difference between recovered clock frequency and reference clock frequency is greater than 7900ppm and cleared when the difference is less than 7700ppm. A change of state of the RLOL status bit can cause an interrupt if enabled by LIU.SRIE:RLOLIE. Note that if the reference clock is not present, RLOL is not set.

8.3.5 Loss-of-Signal (LOS) Detector

The receiver contains analog and digital LOS detectors. The analog LOS (ALOS) detector resides in the AGC/equalizer block. At approximately 23dB below nominal pulse amplitude ALOS is declared by setting the LIU.SR:ALOS status bit. A change of state of the ALOS status bit can cause an interrupt if enabled by LIU.SRIE:ALOSIE. When ALOS is declared the CDR block forces all zeros out of the data recovery circuit, causing digital LOS (DLOS), which is indicated by the RLOS pin and the LINE.RSR:LOS status bit. During ALOS the RCLK pin follows the LIU's reference clock, since no clock information is being received on RXP/RXN. ALOS is cleared at approximately 22dB below nominal pulse amplitude. When the preamp is enabled (Section 8.3.2) ALOS is declared at approximately 37dB below nominal and cleared at approximately 36dB below nominal.

The digital LOS detector declares DLOS when it detects 192 consecutive zeros in the recovered data stream. When DLOS occurs, the receiver asserts the RLOS pin (if the hardware interface is enabled) and the LINE.RSR:LOS status bit. DLOS is cleared when there are no EXZ occurrences over a span of 192 clock periods. An EXZ occurrence is defined as three or more consecutive zeros in DS3 and STS-1 modes and four or more consecutive zeros in E3 mode. The RLOS pin and the LOS status bit are deasserted when the DLOS condition is cleared. A change of state of the LINE.RSR:LOS status bit can cause an interrupt if enabled by LINE.RSRIE:LOSIE. DLOS is only declared when B3ZS/HDB3 decoding is enabled (LINE.RCR:RZSD = 0). When B3ZS/HDB3 decoding is disabled in the LIU, decoding should be enabled in the neighboring DS3/E3 framer, and DLOS should be detected and report by the framer.

The requirements of ANSI T1.231 and ITU-T G.775 for DS3 LOS defects are met by the DLOS detector, which asserts RLOS when it counts 192 consecutive zeros coming out of the CDR block and clears RLOS when it counts 192 consecutive pulse intervals without excessive zero occurrences.

The requirements of ITU-T G.775 for E3 LOS defects are met by a combination of the ALOS detector and the DLOS detector, as follows:

For E3 RLOS Assertion:

1) The ALOS detector in the AGC/equalizer block detects that the incoming signal is less than or equal to a signal level approximately 23dB below nominal, and mutes the data coming out of the clock and data recovery block. (23dB below nominal is in the "tolerance range" of G.775, where LOS may or may not be declared.)
2) The DLOS detector counts 192 consecutive zeros coming out of the CDR block and asserts RLOS. (192 meets the $10 \le N \le 255$ pulse-interval duration requirement of G.775.)

For E3 RLOS Clear:

1) The ALOS detector in the AGC/equalizer block detects that the incoming signal is greater than or equal to a signal level approximately 22dB below nominal, and enables data to come out of the CDR block. (22dB is in the "tolerance range" of G.775, where LOS may or may not be declared.)
2) The DLOS detector counts 192 consecutive pulse intervals without EXZ occurrences and deasserts RLOS. (192 meets the $10 \le N \le 255$ pulse-interval duration requirement of G.775.)

The DLOS detector supports the requirements of ANSI T1.231 for STS-1 LOS defects. At the STS-1 rate, the time required for the DLOS detector to count 192 consecutive zeros falls in the range of 2.3 ≤ T ≤ 100µs required by ANSI T1.231 for declaring an LOS defect. Although the time required for the DLOS detector to count 192 consecutive pulse intervals with no excessive zeros is less than the 125µs to 250µs period required by ANSI T1.231 for clearing an LOS defect, a period of this length where LOS is inactive can easily be timed in software.

During LOS, the RCLK output pin is derived from the LIU's reference clock. The ALOS detector has a longer time constant than the DLOS detector. Thus, when the incoming signal is lost, the DLOS detector activates first (asserting the RLOS pin and LOS status bit), followed by the ALOS detector. When a signal is restored, the DLOS detector does not get a valid signal that it can qualify for no EXZ occurrences until the ALOS detector has seen the signal rise above a signal level approximately 22dB below nominal.

8.3.6 Framer Interface Format and the B3ZS/HDB3 Decoder

The recovered data can be output in either bipolar or binary format. Reception of a B3ZS or HDB3 codeword is flagged by the LINE.RSRL:ZSCDL latched status bit.

8.3.6.1 Bipolar Interface Format

To select the bipolar interface format, pull the RBIN pin low and clear the PORT.CR2:RBIN configuration bit. In bipolar format, the B3ZS/HDB3 decoder is disabled and the recovered data is buffered and output on the RPOS and RNEG outputs for subsequent decoding by a downstream framer or mapper. Received positive-polarity pulses are indicated by RPOS = 1, while negative-polarity pulses are indicated by RNEG = 1.

In DS3 and STS-1 modes an excessive zeros error (EXZ) is declared whenever there is an occurrence of 3 or more zeros in a row in the receive data stream. In E3 mode, an EXZ error is declared whenever there is an occurrence of 4 or more zeros. EXZs are flagged by the LINE.RSRL:EXZL and EXZCL latched status bits and accumulated in the LINE.REXZCR register.

In all three modes (DS3, E3, and STS-1) a bipolar violation is declared if two positive pulses are received without an intervening negative pulse or if two negative pulses are received without an intervening positive pulse. Bipolar violations (BPVs) are flagged by the LINE.RSRL:BPVL and BPVCL latched status bits and accumulated in the LINE.RBPVCR register.

8.3.6.2 Binary Interface Format

To select the binary interface format, pull the RBIN pin high (all ports) or set the PORT.CR2:RBIN configuration bit (per port). In binary format, the B3ZS/HBD3 decoder is enabled, and the recovered data is decoded and output as a binary (NRZ) value on the RDAT pin, while bipolar violations, code violations, and excessive zero errors are detected and flagged on the RLCV pin.

In DS3 and STS-1 modes, B3ZS decoding is performed. In these modes, whenever a B3ZS codeword is found in the receive data stream it is replaced with three zeros. In E3 mode HDB3 decoding is performed. In this mode, whenever an HDB3 codeword is found in the receive data stream it is replaced with four zeros. The decoding search criteria for a B3ZS/HDB3 codeword is programmable using the LINE.RCR:RDZSF control bit.

An excessive zeros error (EXZ) is declared in DS3 and STS-1 modes whenever there is an occurrence of 3 or more zeros in a row in the receive data stream. In E3 mode, an EXZ error is declared whenever there is an occurrence of 4 or more zeros in a row. EXZs are flagged by the LINE.RSRL:EXZL and EXZCL latched status bits and accumulated in the LINE.REXZCR register.

A bipolar violation error (BPV error) is declared in DS3 and STS-1 modes if a BPV is detected that is not part of a valid B3ZS codeword. In E3 mode, a bipolar violation error is declared whenever a BPV is detected that is not part of a valid HDB3 codeword. In E3 mode if LINE.RCR:E3CVE = 1, code violations are detected rather than bipolar violation errors. A code violation is declared whenever consecutive BPVs (not BPV errors) have the same polarity (ITU O.161 definition). The error detection search criteria for a B3ZS/HDB3 codeword is programmable using the LINE.RCR:REZSF control bit. Bipolar violations (or code violations if LINE.RCR:E3CVE = 1) are flagged by the LINE.RSRL:BPVL and BPVCL latched status bits and accumulated in the LINE.RBPVCR register.

In the discussion that follows, a valid pulse that conforms to the AMI rule is denoted as B. A BPV pulse that violates the AMI rule is denoted as V.

In DS3 and STS-1 modes, B3ZS decoding is performed, and RLCV is asserted during any RCLK cycle where the data RDAT causes ones of the following code violations:

- When LINE.RCR:E3CVE = 0:
  - A BPV immediately preceded by a valid pulse (B, V).
  - A BPV with the same polarity as the last BPV.
  - The third zero in an EXZ.
- When LINE.RCR:E3CVE = 1:
  - A BPV immediately preceded by a valid pulse (B, V).
  - A BPV with the same polarity as the last BPV.

In E3 mode, HDB3 decoding is performed, and RLCV is asserted during any RCLK cycle where the data on RDAT causes one of the following code violations:

- When LINE.RCR:E3CVE = 0:
  - A BPV immediately preceded by a valid pulse (B, V) or by a valid pulse and a zero (B, 0, V).
  - A BPV with the same polarity as the last BPV.
  - The fourth zero in an EXZ.
- When LINE.RCR:E3CVE = 1:
  - A BPV with the same polarity as the last BPV.

In any cycle where RLCV is asserted to flag a BPV, the RDAT pin outputs a one. In any cycle where RLCV is asserted to flag an EXZ, the RDAT pin outputs a zero. The state bit that tracks the polarity of the last BPV is toggled on every BPV, whether part of a valid B3ZS/HDB3 codeword or not.

8.3.6.3 RCLK Inversion

The polarity of RCLK can be inverted to support a glueless interface to a variety of neighboring components. Normally, data is output on the RPOS/RDAT and RNEG/RLCV pins on the falling edge of RCLK. To output data on these pins on the rising edge of RCLK, pull the RCLKI pin high or set the PORT.INV:RCLKI configuration bit.

8.3.6.4 Receiver Output Disable

The RCLK, RPOS/RDAT and RNEG/RLCV pins can be disabled (put in a high-impedance state) to support protection switching and redundant-LIU applications. This capability supports system configurations where two or more LIUs are wire-ORed together and a system processor selects one to be active. To disable these pins, set the PORT.CR2:ROD configuration bit.

8.3.7 Power-Down

To minimize power consumption when the receiver is not being used, assert the RPD pin (all ports) or the PORT.CR1:RPD configuration bit (per port). When the receiver is powered down, the RCLK, RPOS/RDAT, and RNEG/RLCV pins are disabled (high impedance). In addition, the RXP and RXN pins become high impedance.

8.3.8 Input Failure Detection

The LIU receiver can detect opens and shorts on the RXP and RXN differential inputs. By default, the receiver detects the following problems, collectively labeled type 1 failures: open RXP connection, open RXN connection, common-mode RXP/RXN short to V_{DD}, and common-mode RXP/RXN short to V_{SS}. Type 1 failures are reported on LIU.SR:RFAIL1. RFAIL1 is cleared when activity is detected on both RXP and RXN.

If LIU.CR2:RFL2E = 1, the receiver also detects a type 2 failure, which is an open or high-impedance path between RXP and RXN. In a board with the external components shown in Figure 4-1 or Figure 4-2, the receive transformer normally presents a low-impedance path between RXP and RXN. To detect a type 2 failure, the receiver connects an 40µA DC current source to RXP and measures the impedance between RXP and RXN. When this impedance is greater than about 5kΩ the receiver declares a type 2 failure on LIU.SR:RFAIL2. When the type 2 failure detection circuitry is enabled, internal termination must be disabled (LIU.CR2:RTRE = 0) and external termination must not be present or a type 2 failure will not be detected because the impedance of the termination is below the type 2 failure threshold.

8.3.9 Jitter and Wander Tolerance

The receiver exceeds the input jitter tolerance requirements of all applicable telecommunication standards in Table 1-1. See Figure 8-4 for STS-1 and E3 jitter tolerance characteristics. See Figure 8-5 for DS3 jitter tolerance characteristics. See Figure 8-6 for DS3 and E3 wander tolerance characteristics. Note: Only G.823 and G.824 have wander tolerance requirements.

Figure 8-4. STS-1 and E3 Jitter Tolerance

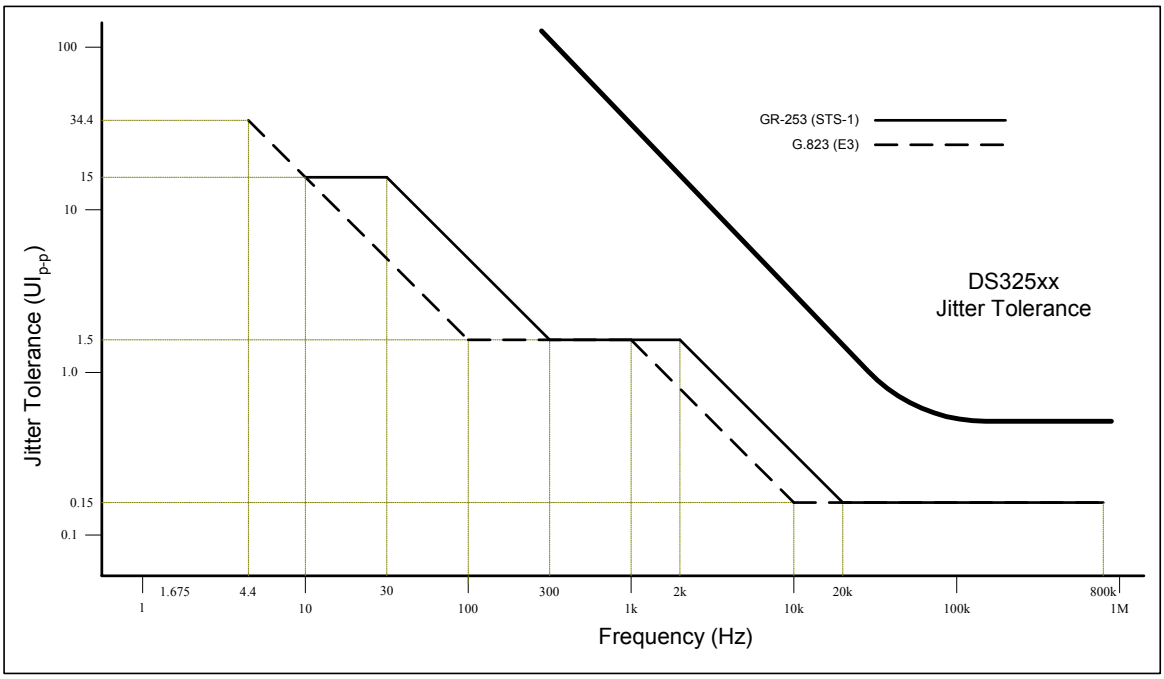


Figure 8-5. DS3 Jitter Tolerance

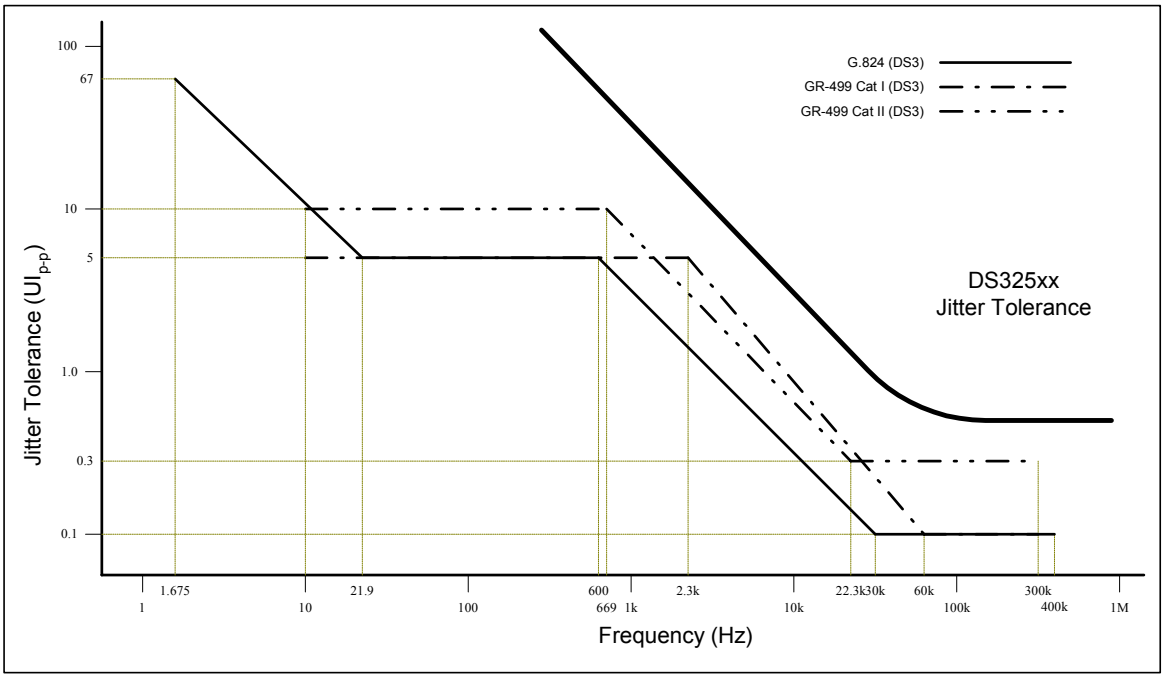
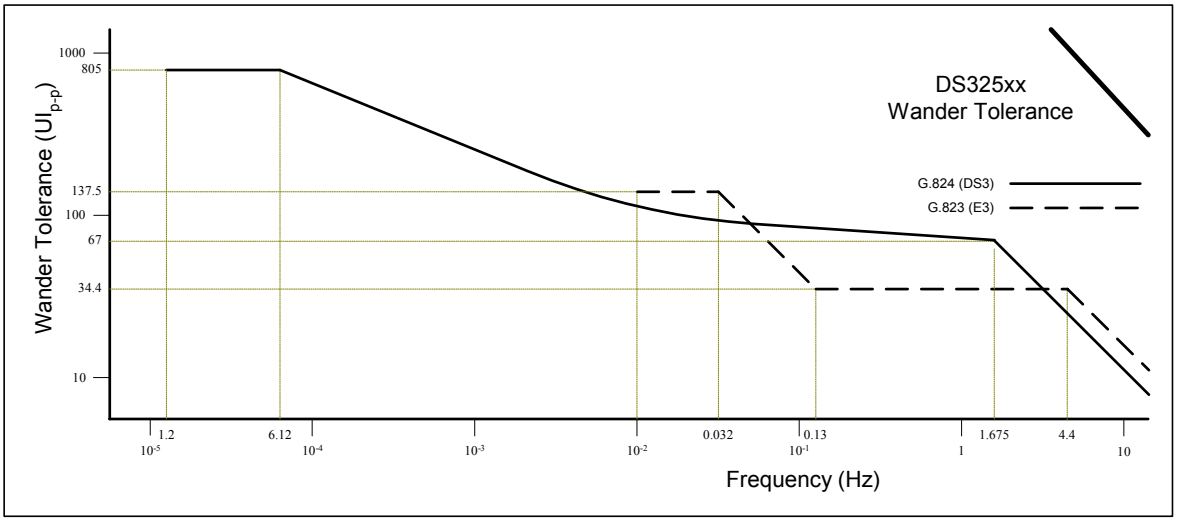


Figure 8-6. DS3 and E3 Wander Tolerance



8.3.10 Jitter Transfer

Without the jitter attenuator on the receive side, the receiver attenuates jitter at frequencies above its corner frequency (approximately 300kHz) and passes jitter at lower frequencies. With the jitter attenuator enabled on the receive side, the receiver meets the jitter transfer requirements of all applicable telecommunication standards in Table 1-1. See Figure 8-7.

8.4 Jitter Attenuator

Each LIU contains an on-board jitter attenuator that can be placed in the receive path or the transmit path or can be disabled. When only the hardware interface is enabled (IFSEL = 000 and HW = 1), the JAS[1:0] and JAD[1:0] pins specify the specify the JA location and buffer depth for all ports. When a microprocessor interface is enabled (IFSEL ≠ 000), the JAS[1:0] and JAD[1:0] pins are ignored, and the LIU.CR1:JAS[1:0] and JAD[1:0] configuration bits specify the JA location and buffer depth for each port individually. The JA buffer depth can be set to 16, 32, 64 or 128 bits. Figure 8-7 shows the minimum jitter attenuation for the device when the jitter attenuator is enabled. Figure 8-7 also shows the receive jitter transfer when the jitter attenuator is disabled.

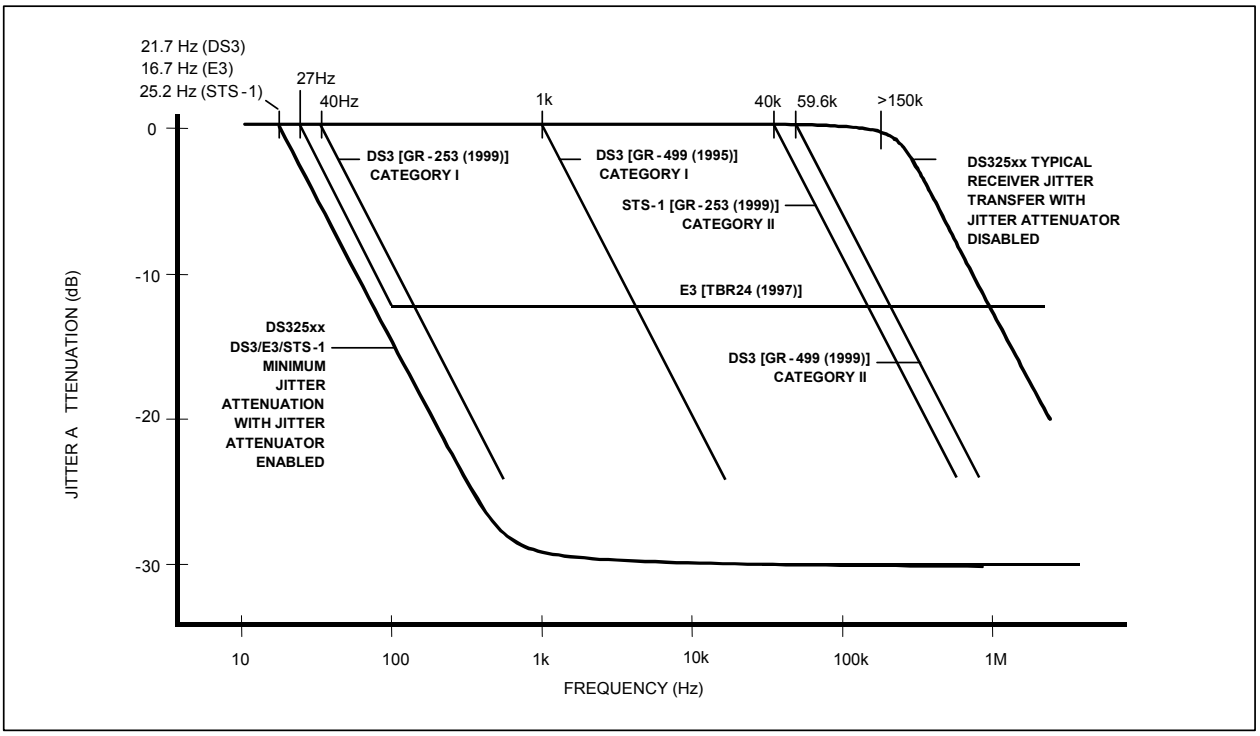
The jitter attenuator consists of a narrowband PLL to retime the selected clock, a FIFO to buffer the associated data while the clock is being retimed, and logic to prevent FIFO over/underflow in the presence of very large jitter amplitudes. The JA has a loop bandwidth of reference_clock ÷ 2,058,874 (see corner frequencies in Figure 8-7). The JA attenuates jitter at frequencies higher than the loop bandwidth, while allowing jitter (and wander) at lower frequencies to pass through relatively unaffected.

The jitter attenuator requires a transmission-quality reference clock (i.e., ±20ppm frequency accuracy and low jitter). See Section 8.7.1 for more information about reference clocks and clock selection.

When the microprocessor interface is enabled, the jitter attenuator indicates the fill status of its FIFO buffer in the LIU.SRL:JAFL (JA full) and LIU.SRL:JAEL (JA empty) status bits. When the buffer becomes full, the JA momentarily increases the frequency of the read clock by 6250ppm to avoid buffer overflow and consequent data errors. When the buffer becomes empty, the JA momentarily decreases the frequency of the read clock by 6250ppm to avoid buffer underflow and consequent data errors. During these momentary frequency adjustments, jitter is passed through the JA to avoid over/underflow. If the phase noise or frequency offset of the write clock is large enough to cause the buffer to overflow or underflow, the JA sets *both* the JAFL bit *and* the JAEL bit to indicate that data errors have occurred. JAFL and JAEL can cause an interrupt if enabled by the corresponding enable bits in the LIU.SRIE register.

As shown in Figure 8-7, the jitter attenuator meets the jitter transfer requirements of all applicable standards listed in Table 1-1.

Figure 8-7. Jitter Attenuation/Jitter Transfer



8.5 BERT

Each LIU port has a built-in bit error-rate tester (BERT). The BERT is a software-programmable test-pattern generator and monitor capable of meeting most error performance requirements for digital transmission equipment. It can generate and synchronize to pseudo-random patterns with a generation polynomial of the form $x^n + x^y + 1$, (where n and y can take on values from 1 to 32 with y < n) and to repetitive patterns of any length up to 32 bits. The pattern generator generates the programmable test pattern, and inserts the test pattern into the data stream. The pattern detector extracts the test pattern from the receive data stream and monitors it. Figure 2-1 shows the location of the BERT Block within the DS325xx devices.

8.5.1 Configuration and Monitoring

The pattern detector is always enabled. The pattern generator is enabled by setting the PORT.CR3:BERTE configuration bit. When the BERT is enabled and PORT.CR3:BERTD=0, the pattern is transmitted and received in the line direction, i.e. the pattern generator is the data source for the transmitter, and the receiver is the data source for the pattern detector. When the BERT is enabled and PORT.CR3:BERTD=1, the pattern is transmitted and received in the system direction, i.e. the pattern generator is the data source for the RPOS/RDAT and RNEG/RLCV pins, and the TPOS/TDAT and TNEG pins are the data source for the pattern detector. See Figure 2-1.

The I/O of the BERT are binary (NRZ) format. Thus while the BERT is enabled, both PORT.CR2:RBIN and PORT.CR2:TBIN must be set to 1 for proper operation. In addition, while transmitting/receiving BERT patterns in the system direction (PORT.CR3:BERTD = 1), the neighboring framer or mapper component must also be configured for binary interface mode to match the LIU. If the LIU interface is normally bipolar, the interface can be changed back to bipolar mode when the system is done using the BERT function (PORT.CR3:BERTE = 0).

The following tables show how to configure the BERT to send and receive common patterns.

Table 8-9. Pseudorandom Pattern Generation

PATTERN TYPE	BERT.PCR REGISTER				BERT.SPR2	BERT.SPR1	BERT.CR
	PTF[4:0] (hex)	PLF[4:0] (hex)	PTS	QRSS			TPIC, RPIC
2^9-1 O.153 (511 type)	04	08	0	0	0xFFFF	0xFFFF	0
2^{11}-1 O.152 and O.153 (2047 type)	08	0A	0	0	0xFFFF	0xFFFF	0
2^{15}-1 O.151	0D	0E	0	0	0xFFFF	0xFFFF	1
2^{20}-1 O.153	10	13	0	0	0xFFFF	0xFFFF	0
2^{20}-1 O.151 QRSS	02	13	0	1	0xFFFF	0xFFFF	0
2^{23}-1 O.151	11	16	0	0	0xFFFF	0xFFFF	1

Table 8-10. Repetitive Pattern Generation

PATTERN TYPE	BERT.PCR REGISTER				BERT.SPR2	BERT.SPR1
	PTF[4:0] (hex)	PLF[4:0] (hex)	PTS	QRSS		
All 1s	NA	00	1	0	0xFFFF	0xFFFF
All 0s	NA	00	1	0	0xFFFF	0xFFFE
Alternating 1s and 0s	NA	01	1	0	0xFFFF	0xFFFE
11001100...	NA	03	1	0	0xFFFF	0xFFFC
3 in 24	NA	17	1	0	0xFF20	0x0022
1 in 16	NA	0F	1	0	0xFFFF	0x0001
1 in 8	NA	07	1	0	0xFFFF	0xFF01
1 in 4	NA	03	1	0	0xFFFF	0xFFF1

After configuring these bits, the pattern must be loaded into the BERT. This is accomplished via a zero-to-one transition on BERT.CR.TNPL for the pattern generator and BERT.CR.RNPL for the pattern detector. The BERT must be enabled (PORT.CR3:BERTE = 1) before the pattern is loaded for the pattern load operation to take effect.

Monitoring the BERT requires reading the BERT.SR register, which contains the Bit-Error Count (BEC) bit and the Out of Synchronization (OOS) bit. The BEC bit is set to one when the bit error counter is one or more. The OOS bit is set to one when the pattern detector is not synchronized to the incoming pattern, which occurs when it receives 6 or more bit errors within a 64-bit window. The Receive BERT Bit Count Register (BERT.RBCR) and the Receive BERT Bit Error-Count Register (BERT.RBECR) are updated upon the reception of a Performance Monitor Update signal (e.g., BERT.CR.LPMU). This signal updates the registers with the bit and bit-error counts since the last update and then resets the counters. See Section 8.7.4 for more details about performance monitor updates.

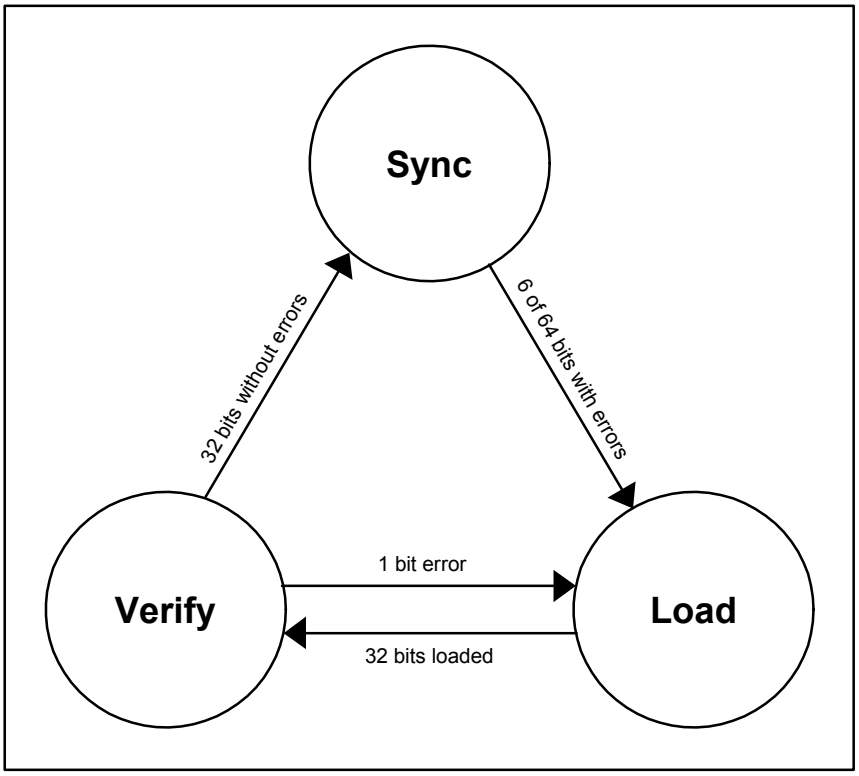
8.5.2 Receive Pattern Detection

The pattern detector synchronizes the receive pattern generator to the incoming pattern. The receive pattern generator is a 32-bit shift register that shifts data from the least significant bit (LSB) or bit 1 to the most significant bit (MSB) or bit 32. The input to bit 1 is the feedback. For a PRBS pattern (generating polynomial $x^n + x^y + 1$), the feedback is an XOR of bit n and bit y. For a repetitive pattern (length n), the feedback is bit n. The values for n and y are individually programmable (1 to 32 with y < n) in the BERT.PCR:PLF and PTF fields. The output of the receive pattern generator is the feedback. If QRSS is enabled (BERT.PCR:QRSS = 1), the feedback is forced to be an XOR of bits 17 and 20, and the output is forced to one if the next 14 bits are all zeros. For PRBS and QRSS patterns, the feedback is forced to one if bits 1 through 31 are all zeros. Depending on the type of pattern programmed, pattern detection performs either PRBS synchronization or repetitive pattern synchronization.

8.5.2.1 Receive PRBS Synchronization

PRBS synchronization synchronizes the receive pattern generator to the incoming PRBS or QRSS pattern. The receive pattern generator is synchronized by loading 32 data stream bits into the receive pattern generator, and then checking the next 32 data stream bits. Synchronization is achieved if all 32 bits match the incoming pattern. If at least six incoming bits in the current 64-bit window do not match the receive pattern generator, automatic pattern resynchronization is initiated. Automatic pattern resynchronization can be disabled by setting BERT.CR:APRD = 1. Pattern resynchronization can also be initiated manually by a zero-to-one transition of the Manual Pattern Resynchronization bit (BERT.CR:MPR). The incoming data stream can be inverted before comparison with the receive pattern generator by setting BERT.CR:RPIC. See Figure 8-8 for the PRBS synchronization diagram.

Figure 8-8. PRBS Synchronization State Diagram

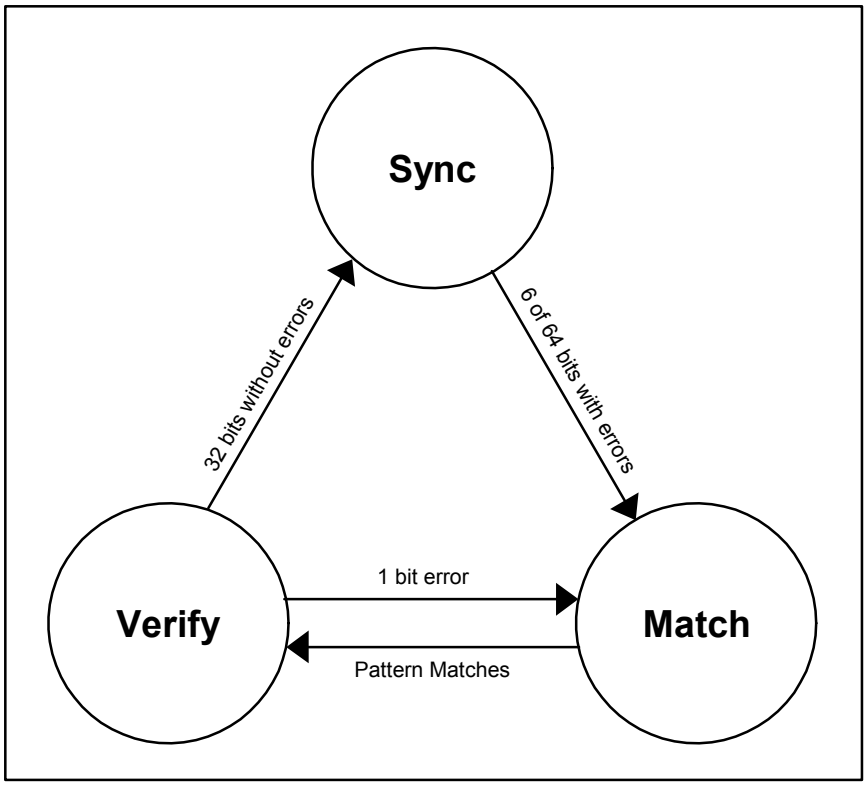


8.5.2.2 Receive Repetitive Pattern Synchronization

Repetitive pattern synchronization synchronizes the receive pattern generator to the incoming repetitive pattern. The receive pattern generator is synchronized by searching each incoming data stream bit position for the repetitive pattern, and then checking the next 32 data stream bits. Synchronization is achieved if all 32 bits match the incoming pattern. If at least six incoming bits in the current 64-bit window do not match the receive PRBS pattern generator, automatic pattern resynchronization is initiated. Automatic pattern re-synchronization can be disabled by setting BERT.CR:APRD = 1. Pattern resynchronization can also be initiated manually by a zero-to-one transition of the Manual Pattern Resynchronization bit (BERT.CR:MPR). The incoming data stream can be inverted before comparison with the receive pattern generator by setting BERT.CR:RPIC.

See Figure 8-9 for the repetitive pattern synchronization state diagram.

Figure 8-9. Repetitive Pattern Synchronization State Diagram



8.5.2.3 Receive Pattern Monitoring

Receive pattern monitoring monitors the incoming data stream for both an OOS condition and bit errors and counts the incoming bits. An Out Of Synchronization (BERT.SR:OOS = 1) condition is declared when the synchronization state machine is not in the “Sync” state. An OOS condition is terminated when the synchronization state machine is in the “Sync” state. A change of state of the OOS status bit sets the BERT.SRL:OOSL latched status bit and can cause an interrupt if enabled by BERT.SRIE:OOSIE.

Bit errors are determined by comparing the incoming data stream bit to the receive pattern generator output. If the two bits do not match, a bit error is declared (BERT.SRL:BEL = 1), and the bit error and bit counts are incremented (BERT.RBECR and BERT.RBCR, respectively). If the two bits do match, only the bit count is incremented. The bit count and bit error count are not incremented when an OOS condition exists. The setting of the BEL status bit can cause an interrupt if enabled by BERT.SRIE:BEIE.

8.5.3 Transmit Pattern Generation

The pattern generator generates the outgoing test pattern. The transmit pattern generator is a 32-bit shift register that shifts data from the least significant bit (LSB) or bit 1 to the most significant bit (MSB) or bit 32. The input to bit 1 is the feedback. For a PRBS pattern (generating polynomial $x^n + x^y + 1$), the feedback is an XOR of bit n and bit y. For a repetitive pattern (length n), the feedback is bit n. The values for n and y are individually programmable (1 to 32 with y < n) in the BERT.PCR:PLF and PTF fields. The output of the receive pattern generator is the feedback. If QRSS is enabled (BERT.PCR:QRSS = 1), the feedback is forced to be an XOR of bits 17 and 20, and the output is forced to one if the next 14 bits are all zeros. For PRBS and QRSS patterns, the feedback is forced to one if bits 1 through 31 are all zeros. When a new pattern is loaded, the pattern generator is loaded with a seed/pattern value before pattern generation starts. The seed/pattern value is programmable (0 - 2^n - 1) in the BERT.SPR registers. The generated pattern can be inverted by setting BERT.CR:TPIC.

8.5.3.1 Transmit Error Insertion

Errors can be inserted into the generated pattern one at a time or at a rate of one out of every 10^n bits. The value of n is programmable (1 to 7 or off) in the BERT.TEICR:TEIR[2:0] configuration field. Single bit error insertion is enabled by setting BERT.TEICR:BEI and can be initiated from the microprocessor interface or by the manual error insertion pin (GPIOB2). See Section 8.7.5 for more information about manual error insertion.

8.6 Loopbacks

Each LIU has three internal loopbacks. See Figure 2-1. When only the hardware interface is enabled (IFSEL = 000 and HW = 1), loopbacks are controlled by the LBn[1:0] and LBS pins. When a microprocessor interface is enabled (IFSEL ≠ 000), loopbacks are controlled by the LB[1:0] and LBS fields in the PORT.CR3 register.

Analog loopback (ALB) connects the outgoing transmit signal back to the receiver's analog front end. During ALB the transmit signal is output normally on TXP/TXN, but the received signal on RXP/RXN is ignored.

Line loopback (LLB) connects the output of the receiver to the input of the transmitter. The LLB path does not include the B3ZS/HDB3 decoder and encoder so that the signal looped back is exactly the same as the signal received, including bipolar violations and code violations. During LLB, recovered clock and data are output on RCLK, RPOS/RDAT, and RNEG/RLCV, but the TPOS/TDAT and TNEG pins are ignored.

Diagnostic loopback (DLB) connects the TCLK, TPOS/TDAT and TNEG pins to the RCLK, RPOS/RDAT, and RNEG/RLCV pins. During DLB (with LLB disabled), the signal on TXP/TXN can be the normal transmit signal or an AIS signal from the AIS generator. DLB and LLB can be enabled simultaneously to provide simultaneous remote and local loopbacks.

8.7 Global Resources

8.7.1 Clock Rate Adapter (CLAD)

The CLAD is used to create multiple transmission-quality reference clocks from a single transmission-quality (±20ppm, low jitter) clock input on the REFCLK pin. The LIUs in the device need up to three different reference clocks (DS3, E3, and STS-1) for use by the CDRs and jitter attenuators. Given one of these clock rates or any of several other clock frequencies on the REFCLK pin, the CLAD can generate all three LIU reference clocks. The internally generated reference clock signals can optionally be driven out on pins CLKA, CLKB, and CLKC for external use. In addition a fourth frequency, either 77.76MHz or 19.44MHz, can be generated and driven out on the CLKD pin for use in Telecom Bus applications.

When only the hardware interface is enabled (IFSEL = 000 and HW = 1), the CLAD is controlled by the CLADBYP pin, and the REFCLK frequency is fixed at 19.44MHz. When the CLADBYP pin is high all PLLs in the CLAD are bypassed and powered down, and the REFCLK pin is ignored. In this mode the CLKA, CLKB, and CLKC pins become inputs, and the DS3, E3, and STS-1 reference clocks, respectively, are sourced from these pins. Transmission-quality clocks (±20ppm, low jitter) must be provided to these pins for each line rate required by the LIUs. When CLADBYP is low, all four PLLs in the CLAD are enabled, and the generated DS3, E3, STS-1, and 77.76MHz clocks are always output on CLKA, CLKB, CLKC and CLKD, respectively.

When a microprocessor interface is enabled (IFSEL ≠ 000), the CLAD clock mode and the REFCLK frequency are set by the GLOBAL.CR2:CLAD[6:4] bits, as shown in Table 8-11. When CLAD[6:4] = 000, all PLLs in the CLAD are bypassed and powered down, and the REFCLK pin is ignored. In this mode the CLKA, CLKB, and CLKC pins become inputs, and the DS3, E3, and STS-1 reference clocks, respectively, are sourced from these pins. Transmission-quality clocks (±20ppm, low jitter) must be provided to these pins for each line rate required by the LIUs. CLAD[6:4] = 000 is equivalent to pulling the CLADBYP pin high. When CLAD[6:4] ≠ 000, the PLL circuits are enabled as needed to generate the required clocks, as determined by the CLAD[6:0] bits and the LIU mode bits (PORT.CR2:LM[1:0]). If a clock rate is not required as a reference clock, then the PLL used to generate that clock is automatically disabled and powered down. The CLAD[3:0] bits are output enable controls for CLKA, CLKB, CLKC and CLKD, respectively. Configuration bit GLOBAL.CR2:CLKD19 specifies the frequency to be output on the CLKD pin (77.76MHz or 19.44MHz). Status register GLOBAL.SRL provides activity status for the REFCLK, CLKA, CLKB and CLKC pins and lock status for the CLAD.

Each LIU block indicates the absence of the reference clock it requires by setting its LIU.SR:LOMC bit.

Table 8-11. CLAD Clock Source Settings

CLAD[6:4]	REFCLK	CLKA	CLKB	CLKC	CLKD
000	Don't Care	DS3 input	E3 input	STS-1 input	Low output
001	DS3 input	DS3 output	E3 output	STS-1 output	77.76 or 19.44MHz output
010	E3 input	DS3 output	E3 output	STS-1 output	77.76 or 19.44MHz output
011	STS-1 input	DS3 output	E3 output	STS-1 output	77.76 or 19.44MHz output
100	77.76MHz input	DS3 output	E3 output	STS-1 output	77.76 or 19.44MHz output
101	19.44MHz input	DS3 output	E3 output	STS-1 output	77.76 or 19.44MHz output
110	38.88MHz input	DS3 output	E3 output	STS-1 output	77.76 or 19.44MHz output
111	12.80MHz input	DS3 output	E3 output	STS-1 output	77.76 or 19.44MHz output

Table 8-12. CLAD Clock Pin Output Settings

CLAD[3:0]*	CLKA PIN	CLKB PIN	CLKC PIN	CLKD PIN
XXX0	Low output	—	—	—
XXX1	PLL-A output	—-	—	—
XX0X	—	Low output	—	—
XX1X	—	PLL-B output	—	—
X0XX	—	—	Low output	—
X1XX	—	—	PLL-C output	—
0XXX	—	—	—	Low output
1XXX	—	—	—	PLL-D output

**When CLAD[6:4] = 000, CLKA, CLKB, and CLKC are inputs and CLKD is held low.*

8.7.2 One-Second Reference Generator

The one-second reference signal can be used to update performance monitoring registers on a precise one-second interval. The generated internal signal is a 50% duty cycle signal that is divided down from the indicated reference signal. The low to high edge on this signal sets the GLOBAL.SRL:1SREFL latched one-second bit, which can generate an interrupt if enabled. The low to high edge is used to initiate a performance monitor register update when GLOBAL.CR1:GPM[1:0] = 1X. The internal one-second reference can be output on the GPIOB3 pin by setting GLOBAL.CR1:G1SROE. The source for the one second reference is set by GLOBAL.CR1:G1SRS[3:0]. The DS3, E3, and STS-1 reference clocks are sourced from the CLAD, if the CLAD is configured to generate them, or from the CLKA, CLKB ,and CLKC pins, respectively.

Table 8-13. Global One-Second Reference Source

G1SRS[3:0]	SOURCE
0000	Disabled
0001	DS3 reference clock
0010	E3 reference clock
0011	STS-1 reference clock
0100	Port 1 TCLK
0101	Port 2 TCLK
0110	Port 3 TCLK
0111	Port 4 TCLK
1000	Port 5 TCLK
1001	Port 6 TCLK
1010	Port 7 TCLK
1011	Port 8 TCLK
1100	Port 9 TCLK
1101	Port 10 TCLK
1110	Port 11 TCLK
1111	Port 12 TCLK

8.7.3 General-Purpose I/O Pins

When a microprocessor interface is enabled (IFSEL ≠ 000), there are two general-purpose I/O (GPIO) pins available per port, each of which can be used as a general-purpose input, general-purpose output, or loss-of-signal output. In addition, GPIOB1, GPIOB2, and GPIOB3 can be used as a global I/O signal. The GPIO pins are independently configurable using the GPIO*yn*S fields of the GLOBAL.GIOACR and GLOBAL.GIOBCR registers (see Table 8-15). When a GPIO pin is configured as an input, its value can be read from the GLOBAL.GIOARR or GLOBAL.GIOBRR registers. When a GPIO pins is configured as a loss-of-signal status output, its state mimics the state of the LINE.RSR:LOS status bit. When a port is powered down and a GPIO pin has been programmed as an associated loss-of-signal output, the pin is held low. Programming a GPIO pin as a global signal overrides the I/O settings specified by the GPIOynS field for that pin and configures the pin as an input or an output as shown in Table 8-14.

Table 8-14. GPIO Pin Global Signal Assignments

PIN	GLOBAL SIGNAL	
	FUNCTION	CONTROL BIT
GPIOA*n*	None	—
GPIOB1	Global PMU input	GLOBAL.CR1.GPM[1:0]
GPIOB2	Global TMEI input	GLOBAL.CR1.MEIMS
GPIOB3	1SREF output	GLOBAL.CR1.G1SROE
GPIOB*k*	None	—

Note: *n = 1 to 12, k = 4 to 12.*

Table 8-15. GPIO Pin Control

GPIO*yn*S[1:0]	FUNCTION
00	Input
01	Output LOS status for port n
10	Output logic 0
11	Output logic 1

Note: *n = 1 to 12, y = A or B.*

8.7.4 Performance Monitor Register Update

Each performance monitor counter can count at least one second of events before saturating at the maximum count. Each counter has an associated status bit that is set when the counter value is not zero, a latched status bit that is set when the counter value changes from zero to one, and a latched status bit that is set each time the counter is incremented.

There is a holding register for each performance monitor counter that is updated when a performance monitoring update is performed. A performance monitoring update causes the counter value to be loaded into the holding register and the counter to be cleared. If a counter increment occurs at the exact same time as the counter reset, the counter is loaded with a value of one, and the “counter is non-zero” latched status bit is set.

The performance monitor update (PMU) signal initiates a performance monitoring update. The PMU signal can be sourced from a general-purpose I/O pin (GPIOB1), the internal one-second reference, a global register bit (GLOBAL.CR1:GPMU), or a port register bit (PORT.CR1:PMU). Note: The BERT PMU can be sourced from a block level register bit (BERT.CR:LPMU). To use GPIOB1, GLOBAL.CR1.GPM[1:0] is set to 01, the appropriate PORT.CR1:PMUM bits are set to 1, and the appropriate BERT.CR:PMUM bits are set to 1. To use the internal one-second reference, GLOBAL.CR1:GPM[1:0] is set to 1X, the appropriate PORT.CR1:PMUM bits are set to 1, and the appropriate BERT.CR:PMUM bits are set to 1. To use the global PMU register bit, GLOBAL.CR1:GPM[1:0] is set to 00, the appropriate PORT.CR1:PMUM bits are set to 1, and the appropriate BERT.CR:PMUM bits are set to 1. To use the port PMU register bit, the associated PORT.CR1:PMUM bit is set to 0, and the appropriate BERT.CR:PMUM bits are set to 1. To use the BERT.CR:LPMU register bit, the appropriate BERT.CR:PMUM bit is set to 0.

When using the global or port PMU register bits, the PMU bit should be set to initiate the process and cleared when the associated PMS status bit (GLOBAL.SR:GPMS or PORT.SR:PMS) is set. When using the GPIO pin or internal one-second reference, the PMS bit is set shortly after the signal goes high, and cleared shortly after the signal

goes low. The PMS has an associated latched status bit that can generate an interrupt if enabled. The port PMS signal does not go high until an update of all the appropriately configured block-level performance monitoring counters in the port has been completed. The global PMS signal does not go high until an update of all the appropriately configured port-level performance monitoring counters in the entire chip has been completed.

8.7.5 Transmit Manual Error Insertion

Various types of errors can be inserted in the transmit data stream using the Transmit Manual Error Insertion (TMEI) signal, which can be sourced from a block-level register bit, a port register bit (PORT.CR1:TMEI), a global register bit (GLOBAL.CR1:TMEI), or a general-purpose I/O pin (GPIOB2). To use GPIOB2 as the TMEI signal, GLOBAL.CR1.MEIMS is set to 1, the appropriate PORT.CR1.MEIMS bits are set to 1, and the appropriate block-level MEIMS bits are set to 1. To use the global TMEI register bit, GLOBAL.CR1.MEIMS is set to 0, the appropriate PORT.CR1.MEIMS bits are set to 1, and the appropriate block-level MEIMS bits are set to 1. To use the port TMEI register bit, the associated PORT.CR1.MEIMS is set to 0 and the appropriate block-level MEIMS bits are set to 1. To use the block-level TSEI register bit, the associated block-level MEIMS bit is set to 0.

In order for an error of a particular type to be inserted, the error type must be enabled by setting the associated error insertion enable bit in the associated block's error insertion register. Once enabled, a single error is inserted at the next opportunity when the TMEI signal transitions from zero to one. Note: If the TMEI signal has multiple zero-to-one transitions between error insertion opportunities, only a single error is inserted.

8.8 8-/16-Bit Parallel Microprocessor Interface

See Table 11-8 and Figure 11-3 to Figure 11-10 for parallel interface timing diagrams and parameters.

8.8.1 8-Bit and 16-Bit Bus Widths

When the IFSEL pins are set to 1XX, the device presents a parallel microprocessor interface. In 8-bit modes (IFSEL = 10X), the address is composed of all the address bits including A[0], the lower 8 data lines D[7:0] are used, and the upper 8 data lines D[15:8] are disabled (high impedance). In 16-bit modes (IFSEL = 11X), the address does not include A[0], and all 16 data lines D[15:0] are used.

8.8.2 Byte Swap Mode

In 16-bit modes (IFSEL = 11X), the microprocessor interface can operate in byte swap mode. The BSWAP pin is used to determine whether byte swapping is enabled. This pin should be static and not change during operation. When the BSWAP pin is low the upper register bits REG[15:8] are mapped to the upper external data bus lines D[15:8], and the lower register bits REG[7:0] are mapped to the lower external data bus lines D[7:0]. When the BSWAP pin is high the upper register bits REG[15:8] are mapped to the lower external data bus lines D[7:0], and the lower register bits REG[7:0] are mapped to the upper external data bus lines D[15:8].

8.8.3 Read-Write And Data Strobe Modes

The processor interface can operate in either read-write strobe mode (also known as "Intel" mode) or data strobe mode (also known as "Motorola" mode). When IFSEL = 1X0 the read-write strobe mode is enabled. In this mode a negative pulse on $\overline{RD}$ performs a read cycle, and a negative pulse on $\overline{WR}$ performs a write cycle.

When IFSEL = 1X1 the data strobe mode is enabled. In this mode, a negative pulse on $\overline{DS}$ when R/W is high performs a read cycle, and a negative pulse on $\overline{DS}$ when R/W is low performs a write cycle.

8.8.4 Multiplexed and Nonmultiplexed Operation

In all parallel interface modes the interface supports both multiplexed and nonmultiplexed operation. For multiplexed operation in 8-bit modes, wire A[10:8] to the processor's A[10:8] pins, wire A[7:0] to D[7:0] and to the processor's multiplexed address/data bus, and connect the ALE pin to the appropriate pin on the processor. For nonmultiplexed 8-bit operation, wire ALE high and wire A[10:0] and D[7:0] to the appropriate pins on the processor.

For multiplexed operation in 16-bit modes, wire A[10:0] to D[10:0], wire D[15:0] to the CPU's multiplexed address/data bus, and connect the ALE pin to the appropriate pin on the processor. For nonmultiplexed 16-bit operation, wire ALE high and wire A[10:0] and D[15:0] to the appropriate pins on the processor.

8.8.5 Clear-On-Read And Clear-On-Write Modes

The latched status register bits can be programmed to clear on a read access or clear on a write access. The global control register bit GLOBAL.CR2.LSBCRE specifies the method used to clear all of the latched status registers. When LSBCRE = 0, latched status register bits are cleared when written with a 1. When LSBCRE = 1, latched status register bits are cleared when read.

The clear-on-write mode expects the user to use the following method: read the latched status register then write a 1 to the register bits to be cleared. This method is useful when multiple software tasks use the same latched status register. Each task can clear the bits it uses without affecting any of the latched status bits used by other tasks.

The clear-on-read mode clears all latched status bits in a register automatically when the latched status register is read. This method works well when no more than one software task uses any single latched status register. An event that occurs while the associated latched status register is being read results in the associated latched status bit being set after the read is completed.

8.8.6 Global Write Mode

When GLOBAL.CR2:GWRM = 1, a write to a register of any port causes the data to be written to the same register in all the ports on the device. In this mode register reads are not supported and result in undefined data.

8.9 SPI Serial Microprocessor Interface

When the IFSEL pins are set to 01X the device presents an SPI interface on the $\overline{CS}$, SCLK, SDI, and SDO pins. SPI is a widely-used master/slave bus protocol that allows a master device and one or more slave devices to communicate over a serial bus. The DS325xx is always a slave device. Masters are typically microprocessors, ASICs or FPGAs. Data transfers are always initiated by the master device, which also generates the SCLK signal. The DS325xx receives serial data on the SDI pin and transmits serial data on the SDO pin. SDO is high-impedance except when the DS325xx is transmitting data to the bus master. *Note that the ALE pin must be wired high for proper operation of the SPI interface.*

Bit Order. When IFSEL[2:0] = 010 the register address and all data bytes are transmitted MSB first on both SDI and SDO. When IFSEL[2:0] = 011, the register address and all data bytes are transmitted LSB first on both SDI and SDO. The Motorola SPI convention is MSB first.

Clock Polarity and Phase. The CPOL pin defines the polarity of SCLK. When CPOL = 0, SCLK is normally low and pulses high during bus transactions. When CPOL = 1, SCLK is normally high and pulses low during bus transactions. The CPHA pin sets the phase (active edge) of SCLK. When CPHA = 0, data is latched in on SDI on the leading edge of the SCLK pulse and updated on SDO on the trailing edge. When CPHA = 1, data is latched in on SDI on the trailing edge of the SCLK pulse and updated on SDO on the following leading edge. See Figure 8-10.

Device Selection. Each SPI device has its own chip-select line. To select the DS325xx, pull its $\overline{CS}$ pin low.

Control Word. After $\overline{CS}$ is pulled low, the bus master transmits the control word during the first 16 SCLK cycles. In MSB-first mode, the control word has the form:

R/$\overline{W}$ A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0 BURST

where A[13:0] is the register address, R/$\overline{W}$ is the data direction bit (1 = read, 0 = write), and BURST is the burst bit (1 = burst access, 0 = single-byte access). In LSB-first mode, the order of the 14 address bits is reversed. In the discussion that follows, a control word with R/$\overline{W}$ = 1 is a read control word, while a control word with R/$\overline{W}$ = 0 is a write control word. Note: The address range of the DS32512 is 000h–7FFh, so A[13:11] are ignored.

Single-Byte Writes. See Figure 8-11. After $\overline{CS}$ goes low, the bus master transmits a write control word with BURST = 0 followed by the data byte to be written. The bus master then terminates the transaction by pulling $\overline{CS}$ high.

Single-Byte Reads. See Figure 8-11. After $\overline{CS}$ goes low, the bus master transmits a read control word with BURST = 0. The DS325xx then responds with the requested data byte. The bus master then terminates the transaction by pulling $\overline{CS}$ high.

Burst Writes. See Figure 8-11. After $\overline{CS}$ goes low, the bus master transmits a write control word with BURST = 1 followed by the first data byte to be written. The DS325xx receives the first data byte on SDI, writes it to the specified register, increments its internal address register, and prepares to receive the next data byte. If the master

continues to transmit, the DS325xx continues to write the data received and increment its address counter. After the address counter reaches 7FFh it rolls over to address 000h and continues to increment.

Burst Reads. See Figure 8-11. After $\overline{CS}$ goes low, the bus master transmits a read control word with BURST = 1. The DS325xx then responds with the requested data byte on SDO, increments its address counter, and prefetches the next data byte. If the bus master continues to demand data, the DS325xx continues to provide the data on SDO, increment its address counter, and prefetch the following byte. After the address counter reaches 7FFh it rolls over to address 000h and continues to increment.

Early Termination of Bus Transactions. The bus master can terminate SPI bus transactions at any time by pulling $\overline{CS}$ high. In response to early terminations, the DS325xx resets its SPI interface logic and waits for the start of the next transaction. If a write transaction is terminated prior to the SCLK edge that latches the LSB of a data byte, the current data byte is not written.

Design Option: Wiring SDI and SDO Together. Because communication between the bus master and the DS325xx is half-duplex, the SDI and SDO pins can be wired together externally to reduce wire count. To support this option, the bus master must not drive the SDI/SDO line when the DS325xx is transmitting.

AC Timing. See Table 11-9 and Figure 11-11 for AC timing specifications for the SPI interface.

Figure 8-10. SPI Clock Polarity and Phase Options

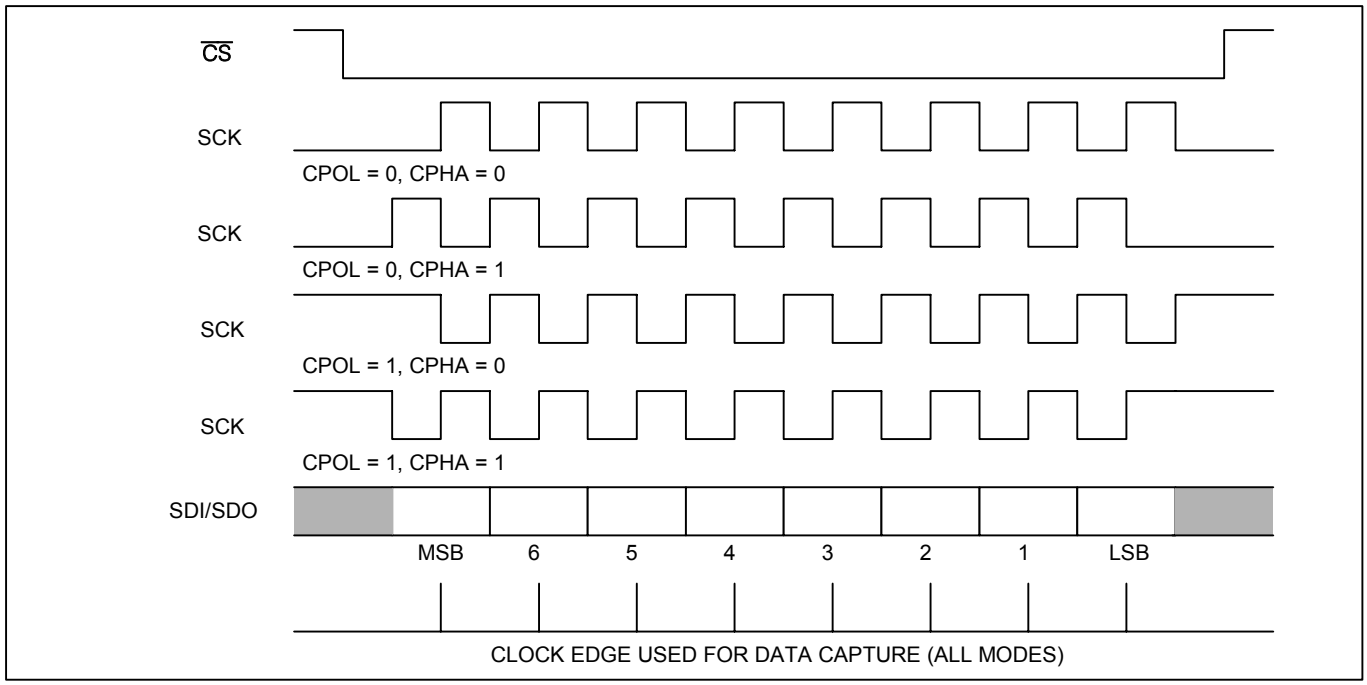
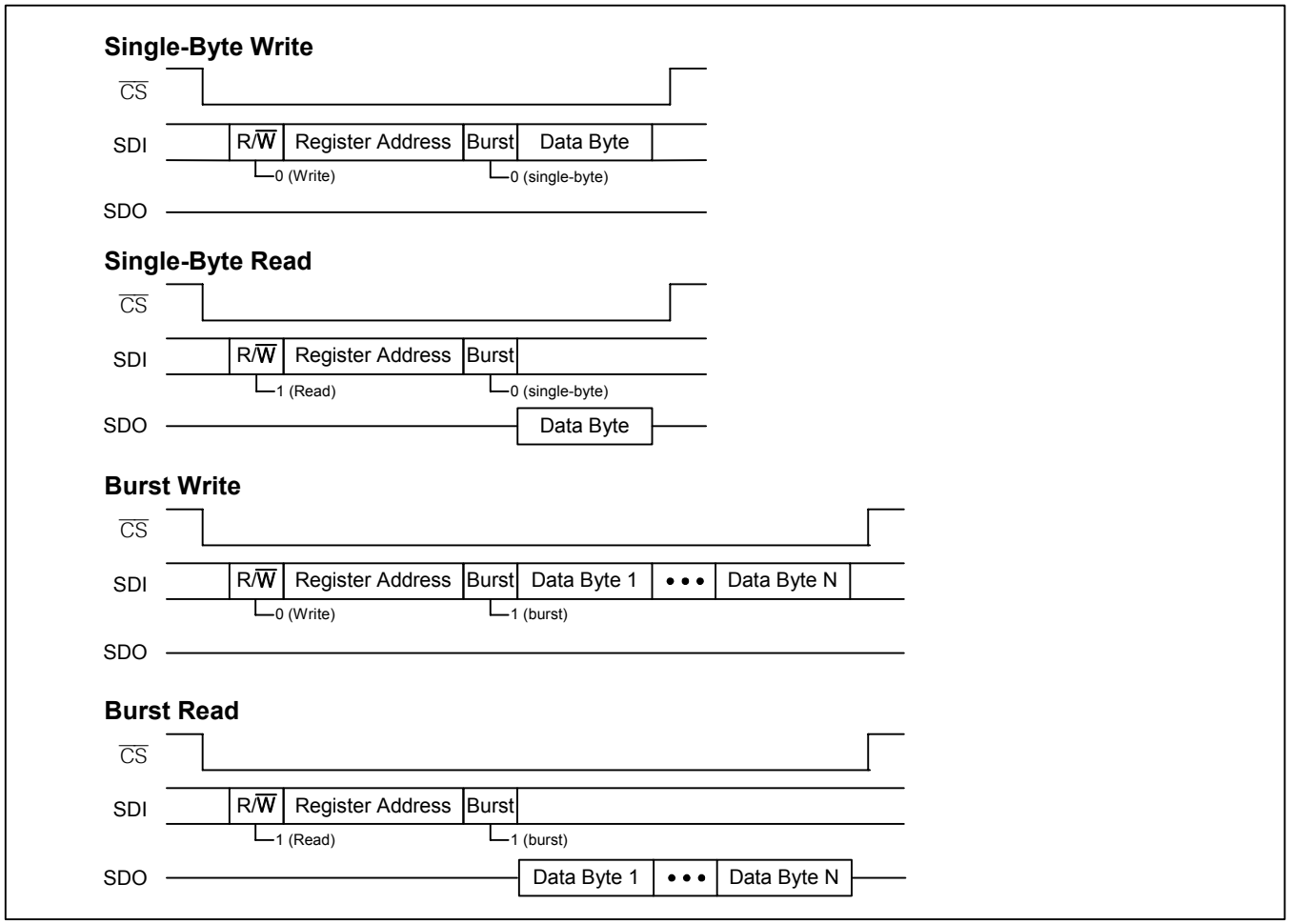


Figure 8-11. SPI Bus Transactions

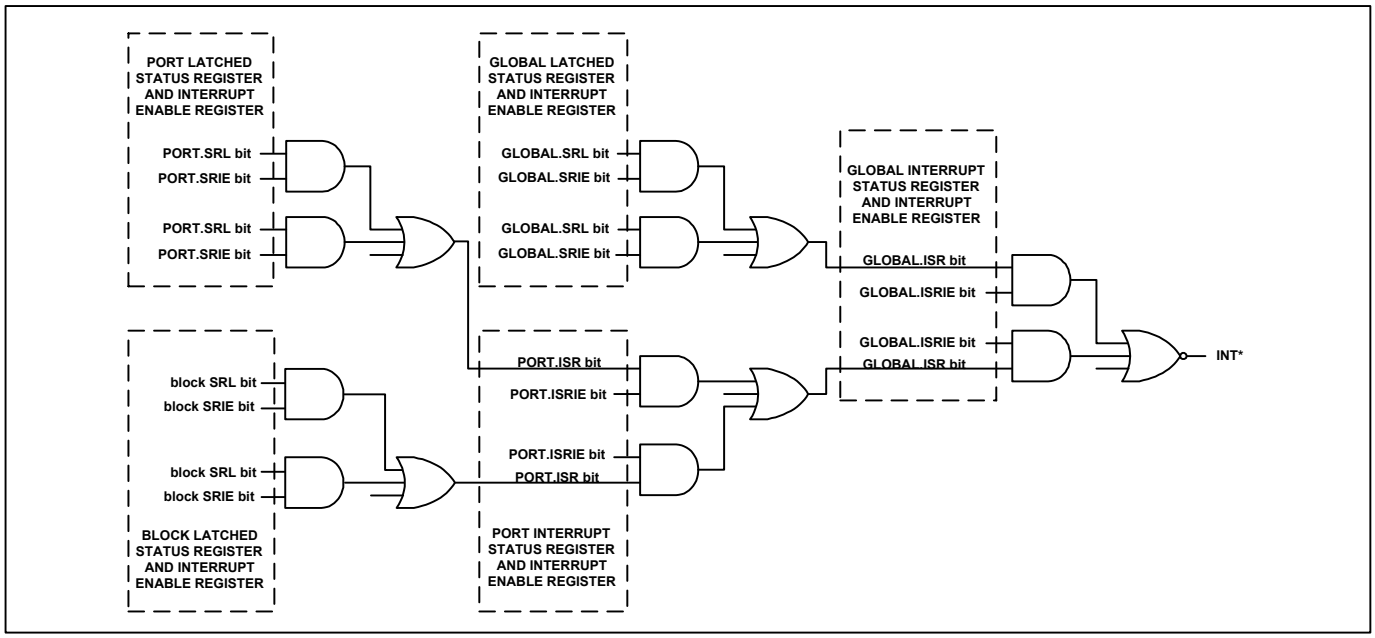


8.10 Interrupt Structure

The interrupt structure is designed to efficiently guide the user to the source of an interrupt. The status bits in the global interrupt status register (GLOBAL.ISR) are read to determine if the interrupt source comes from a global event, such as a one-second timer interrupt, or one of the ports. If the interrupt source is a global event, the global status register is read (GLOBAL.SRL) to determine the source. If the interrupt source is a port, the port interrupt status register (PORT.ISR) is read to determine if the interrupt source comes from a port event, such as a performance monitor update interrupt, or one of the functional blocks inside the port. If the interrupt source is a port event, the port status register is read (PORT.SRL) to determine the source. If the interrupt source is from a functional block inside the port, the associated block's status register is read to determine the source. The source of an interrupt can be determined by reading no more than three 16-bit registers.

Once the interrupt source has been determined, the interrupt can be cleared by either reading or writing the latched status register (see Section 8.8.5). An alternate method for clearing an interrupt is to disable the interrupt at the bit, block, port, or global level by writing a zero to the associated interrupt enable bit. Note: Disabling the interrupt at the block, port, or global level disables *all* interrupts sources at or below that level.

Figure 8-12. Interrupt Signal Flow



8.11 Reset and Power-Down

When only the hardware interface is enabled (IFSEL = 000 and HW = 1), the device is can be reset via the $\overline{\text{RST}}$ pin. The transmitters of all ports can be powered down using the TPD pin, while the receivers of all ports can be powered down using the RPD pin.

When a microprocessor interface is enabled (IFSEL ≠ 000), the device presents a number of reset and power down options. The device can be reset at a global level via the GLOBAL.CR1:RST bit or the RST pin, and at the port level via the PORT.CR1:RST bit. Each port can be powered down via the PORT.CR1:TPD and RPD bits. The JTAG logic is reset by the $\overline{\text{JTRST}}$ pin.

The external RST pin and the global reset bit (GLOBAL.CR1:RST) are combined to create an internal global reset signal. The global reset signal resets all the status and control registers on the chip (except the GLOBAL.CR1:RST bit), to their default values. It also resets all flip-flops in the global logic (including the CLAD block) and port logic to their reset values. The GLOBAL.CR1:RST bit stays set after a one is written to it. It is reset to zero when a zero is written to it or when the external RST pin is active.

At the port level, the global reset signal combines with the port reset bit (PORT.CR1:RST) to create a port reset signal. The port reset signal resets all the status and control registers in the port (except PORT.CR1:RST bit) to their default values. It also resets all flip-flops in the port logic to their reset values. The port reset bit (PORT.CR1:RST) stays set after a one is written to it. It is reset to zero when a zero is written to it or when the global reset signal is active.

The data path reset (RSTDP) resets all of the same registers and flip-flops as the “general” reset (RST), except for the control registers. This allows the device to be programmed while the data path logic is in reset. It is recommended that a port be placed in data path reset during configuration changes.

The global data path reset bit (GLOBAL.CR1:RSTDP) is set to one when the global reset signal is active. This bit is cleared when a zero is written to it while the global reset signal is inactive. The global data path reset resets all of the data path registers and flip-flops on the chip.

The port data path reset bit (PORT.CR1:RSTDP) is set to one when the port reset signal is active. It is cleared when a zero is written to it while the port reset signal is inactive. The port data path reset resets all of the port logic data path registers and flip-flops.

Table 8-16. Reset and Power-Down Sources

PIN	REGISTER BITS						INTERNAL SIGNALS					
	GLOBAL.CR1		PORT.CR1									
$\overline{RST}$	RST	RSTDP	RST	TPD	RPD	RSTDP	Global Reset	Global Data Path Reset	Port Reset	Tx Port Power-Down	Rx Port Power-Down	Port Data Path Reset
0	F0	F1	F0	F1	F1	F1	1	1	1	1	1	1
1	1	F1	F0	F1	F1	F1	1	1	1	1	1	1
1	0	1	0	0	0	0	0	1	0	0	0	1
1	0	0	1	F1	F1	F1	0	0	1	1	1	1
1	0	0	0	1	1	0	0	0	0	1	1	1
1	0	0	0	1	0	0	0	0	0	1	0	0
1	0	0	0	0	1	0	0	0	0	0	1	0
1	0	0	0	0	0	1	0	0	0	0	0	1
1	0	0	0	0	0	0	0	0	0	0	0	0

Register bit states: F0 = forced to 0, F1 = forced to 1, 0 = set to 0, 1 = set to 1

The reset signals in the device are asserted asynchronously and do not require a clock to put the logic into the reset state. The control registers do not require a clock to come out of the reset state, but all other logic does require a clock to come out of the reset state.

The port transmit power-down function (PORT.CR1:TPD) disables all the transmit clocks and powers down the transmit LIU to minimize power consumption. The port receive power-down function (PORT.CR1:RPD) disables all of the receive clocks and powers down the receive LIU to minimize power consumption. The one-second timer circuit can be powered down by disabling its reference clock. The CLAD can be powered down by disabling it (setting GLOBAL.CR2:CLAD[6:0] = 0). The global logic cannot be powered down.

After a global reset, all of the control and status registers in all ports are set to their default values and all the other flip-flops are reset to their reset values. The global data path reset (GLOBAL.CR1:RSTDP), all the port data path resets (PORT.CR1:RSTDP), and all the port power-down (PORT.CR1:TPD and RPD) bits are set after the global reset. A valid initialization sequence is to clear the port power-down bits in the ports that are to be active, write to all of the configuration registers to set them in the desired modes, then clear the GLOBAL.CR1:RSTDP and PORT.CR1:RSTDP bits. This causes all the logic to start up in a predictable manner. The device can also be initialized by clearing the GLOBAL.CR1:RSTDP, PORT.CR1:RSTDP, and PORT.CR1:TPD and RPD bits, then writing to all of the configuration registers to set them in the desired modes, and then clearing all of the latched status bits. This second initialization scheme can cause the device to operate unpredictably for a brief period of time.

Some of the I/O pins are put into a known state at reset. At the global level, the microprocessor interface output and I/O pins (D[15:0]) are forced into the high impedance state when the $\overline{RST}$ pin is active, but not when the GLOBAL.CR1:RST bit is active. The CLAD clock pins CLKA, CLKB, and CLKC are forced to be the LIU reference clock inputs. The general-purpose I/O pins (GPIOAn and GPIOBn) are forced to be inputs until after the $\overline{RST}$ pin is deasserted. At the port level, the LIU transmitter outputs TXP and TXN are forced into a high-impedance state.

Note: Setting any of the reset (RST), data path reset (RSTDP), or power-down (TPD, RPD) bits for less than 100 ns may result in the associated circuits coming up in a random state. When a power-down bit is cleared, it takes approximately 1ms for all of the associated circuits to power-up.

9. REGISTER MAPS AND DESCRIPTIONS

9.1 Overview

When a microprocessor interface is enabled (IFSEL[2:0] ≠ 000), the registers described in this section are accessible. The overall memory map is shown in Table 9-1. The DS32512 register map covers the address range of 000 to 7FFh. On the DS32508, writes in the address space for LIUs 9 through 12 are ignored, and reads from these addresses return 00h. On the DS32506, address line A[10] is not present, and writes into the address space for LIU 7 are ignored, and reads from these addresses return 00h. The address LSB A[0] is used to address the upper and lower bytes of a register in 8-bit mode, and to swap the upper and lower bytes in 16-bit mode.

In each register, bit 15 is the MSB and bit 0 is the LSB. Register addresses not listed and bits marked "—" are reserved and must be written with 0 and ignored when read. Writing other values to these registers may put the device in a factory test mode resulting in undefined operation. Bits labeled "0" or "1" must be written with that value for proper operation. Register fields with underlined names are read-only fields; writes to these fields have no effect. All other fields are read-write. Register fields are described in detail in the register descriptions in Sections 9.3 to 9.8.

9.1.1 Status Bits

The device has two types of status bits. Real-time status bits are read-only and indicate the state of a signal at the time it is read. Latched status bit are set when the associated event occurs and remain set until cleared. Once cleared, a latched status bit is not set again until the associated event recurs (goes away and comes back). A latched-on-change bit is a latched status bit that is set when the event occurs and when it goes away. A latched status bit can be cleared using either a clear-on-read or clear-on-write method (see Section 8.8.5). For clear-on-read, all latched status bits in a latched status register are cleared when the register is read. In 16-bit mode, all 16 latched status bits are cleared. In 8-bit mode, only the eight bits read are cleared. For clear-on-write, a latched bit in a latched status register is cleared when a logic 1 is written to that bit. For example, writing FFFFh to a 16-bit latched status register clears all latched status bits in the register, whereas writing 0001h only clears bit 0 of the register. When set, some latched status bits can cause an interrupt request if enabled to do so by corresponding interrupt enable bits.

9.1.2 Configuration Fields

Configuration fields are read-write. During reset, each configuration field reverts to the default value shown in the register definition. Configuration register bits marked "—" are reserved and must be written with 0. Configuration registers and bits can be written to and read from during a data path reset, however, all changes to these bits are ignored during the data path reset. As a result, all bits requiring a zero-to-one transition to initiate an action must have the transition occur after the data path reset has been removed. See Section 8.11 for more information about resets and data path resets.

9.1.3 Counters

All counters stop counting at their maximum count. A counter register is updated by asserting (low to high transition) the performance monitoring update signal (PMU). During a counter register update, the performance monitoring status signal (PMS) is deasserted. A counter register update consists of loading the counter register with the current count, resetting the counter, resetting the zero count status indication, and then asserting PMS. No events are missed during an update. See Section 8.7.4 for more information about performance monitor register updates.

9.2 Overall Register Map

Table 9-1. Overall Register Map

BASE ADDRESS	BLOCK
000h	Global Registers
080h	Port Registers for Port 1
100h	Port Registers for Port 2
180h	Port Registers for Port 3
200h	Port Registers for Port 4
280h	Port Registers for Port 5
300h	Port Registers for Port 6
380h	Port Registers for Port 7
400h	Port Registers for Port 8
480h	Port Registers for Port 9
500h	Port Registers for Port 10
580h	Port Registers for Port 11
600h	Port Registers for Port 12
680h	Unused

Table 9-2. Port Registers

ADDRESS OFFSET	DESCRIPTION	BLOCK
00h–1Fh	Port Common Registers	PORT
20h–2Fh	LIU Registers	LIU
30h–3Fh	B3ZS/HDB3 Encoder Registers	LINE Tx
40h–4Fh	B3ZS/HDB3 Decoder Registers	LINE Rx
50h–6Fh	BERT Registers	BERT
70h–7Fh	Unused	—

Note: *The address offsets given in this table are offsets from port base addresses shown in Table 9-1.*

9.3 Global Registers

Table 9-3. Global Register Map

ADDRESS OFFSET	REGISTER	REGISTER DESCRIPTION
000h	GLOBAL.IDR	ID Register
002h	GLOBAL.CR1	Global Control Register 1
004h	GLOBAL.CR2	Global Control Register 2
006h–00Eh	—	Unused
010h	GLOBAL.GIOACR1	General-Purpose I/O A Control Register 1
012h	GLOBAL.GIOACR2	General-Purpose I/O A Control Register 2
014h	GLOBAL.GIOBCR1	General-Purpose I/O B Control Register 1
016h	GLOBAL.GIOBCR2	General-Purpose I/O B Control Register 2
018h–01Eh	—	Unused
020h	GLOBAL.ISR	Global Interrupt Status Register
022h	GLOBAL.ISRIE	Global Interrupt Enable Register
024h–026h	—	Unused
028h	GLOBAL.SR	Global Status Register
02Ah	GLOBAL.SRL	Global Status Register Latched
02Ch	GLOBAL.SRIE	Global Status Register Interrupt Enable
02Eh–036h	—	Unused
038h	GLOBAL.GIOARR	General-Purpose I/O A Read Register
03Ah	GLOBAL.GIOBRR	General-Purpose I/O B Read Register
03Ch–07Eh	—	Unused

Register Name: **GLOBAL.IDR**
Register Description: **ID Register**
Register Address: **000h**

Bit #	15	14	13	12	11	10	9	8
Name	ID15	ID14	ID13	ID12	ID11	ID10	ID9	ID8

Bit #	7	6	5	4	3	2	1	0
Name	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

Bits 15 to 12: Device REV ID (ID[15:12]). These bits of the device ID register have the same information as the four bits of the JTAG REV ID portion of the JTAG ID register, JTAG ID[31:28]. See Section 10.

Bits 11 to 0: Device CODE ID (ID[11:0]). These bits of the device ID register have the same information as the 12 bits of the JTAG CODE ID portion of the JTAG ID register, JTAG ID[23:12]. See Section 10.

Register Name: **GLOBAL.CR1**
Register Description: **Global Control Register #1**
Register Address: **002h**

Bit #	15	14	13	12	11	10	9	8
Name	—	—	—	G1SRS[3:0]				G1SROE
Default	—	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	TMEI	MEIMS	GPM[1:0]		GPMU	—	RSTDP	RST
Default	0	0	0	0	0	0	1	0

Bits 12 to 9: Global One-Second Reference Source (G1SRS[3:0]). These bits determine the source for the internally generated one second reference. The source is selected from one of the CLAD clocks or from one of the port transmit clocks. See Section 8.7.2.

0000 = Disabled
0001 = DS3 reference clock
0010 = E3 reference clock
0011 = STS-1 reference clock
0100 = Port 1 TCLK
0101 = Port 2 TCLK
0110 = Port 3 TCLK
0111 = Port 4 TCLK
1000 = Port 5 TCLK
1001 = Port 6 TCLK
1010 = Port 7 TCLK
1011 = Port 8 TCLK
1100 = Port 9 TCLK
1101 = Port 10 TCLK
1110 = Port 11 TCLK
1111 = Port 12 TCLK

Bit 8: Global One-Second Reference Output Enable (G1SROE). This bit determines whether the GPIOB3 pin is used to output the global one second reference signal. See Section 8.7.2.

0 = GPIOB3 pin mode selected by GLOBAL.GIOBCR1:GIOB3S[1:0].
1 = GPIOB3 outputs the global one second reference signal specified by GLOBAL.CR1:G1SRS[3:0]

Bit 7: Transmit Manual Error Insert (TMEI). When GLOBAL.CR1:MEIMS = 0, this bit is used to insert errors in all blocks in all ports where block-level MEIMS = 1 and PORT.CR1:MEIMS = 1. Error(s) are inserted at the next opportunity after this bit transitions from low to high. See Section 8.7.5. Note: This bit should be set low immediately after each error insertion.

Bit 6: Manual Error Insert Mode Select (MEIMS). This bit specifies the source of the manual error insertion signal for all block-level error generators that have block-level MEIMS = 1 and PORT.CR1:MEIMS = 1. See Section 8.7.5.

0 = Global error insertion using GLOBAL.CR1:TMEI bit
1 = Global error insertion using the GPIOB2 pin

Bits 5 and 4: Global Performance Monitor Update Mode (GPM[1:0]). These bits specify the source of the performance monitoring update signal for all blocks that have block-level PMUM = 1 and PORT.CR1:PMUM = 1. See Section 8.7.4.

00 = Global PM update using the GLOBAL.CR1:GPMU bit
01 = Global PM update using the GPIOB1 pin
1X = One-second PM update using the internal one-second counter (see Section 8.7.2)

Bit 3: Global Performance Monitor Register Update (GPMU). When GLOBAL.CR1:GPM[1:0] = 00, this bit is used to update all of the performance monitor registers where block-level PMUM = 1 and PORT.CR1:PMUM = 1. When this bit transitions from low to high, all configured performance monitoring registers are updated with the latest counter value, and all associated counters are reset. This bit should remain high until the performance monitor update status bit (GLOBAL.SR:GPMS) goes high, and then it should be brought back low, which clears the GPMS status bit. If a counter increment occurs at the exact same time as the counter reset, the counter is loaded with a value of one, and the "counter is non-zero" latched status bit is set. See Section 8.7.4.

Bit 1: Reset Data Path (RSTDP). When this bit is set, it forces all of the internal data path and status registers in all ports to their default state. This bit must be set high for a minimum of 100ns. See Section 8.11.

0 = Normal operation
1 = Force all data path registers to their default values

Bit 0: Reset (RST). When this bit is set, all of the internal data path and status and control registers (except this RST bit), on all of the ports, are reset to their default state. This bit must be set high for a minimum of 100ns. This bit is logically ORed with the inverted hardware signal $\overline{\text{RST}}$. See Section 8.11.

0 = Normal operation
1 = Force all internal registers to their default values

Register Name: **GLOBAL.CR2**
Register Description: **Global Control Register #2**
Register Address: **004h**

Bit #	15	14	13	12	11	10	9	8
Name	—	CLAD[6:0]						
Default	—	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	—	—	CLKD19	INTM	RAS	RAD	LSBCRE	GWRM
Default	0	0	0	0	0	0	0	0

Bits 14 to 8: CLAD I/O Mode (CLAD[6:0]). These bits control the CLAD clock I/O pins REFCLK, CLKA, CLKB, CLKC and CLKD. See Table 8-11 and Table 8-12 in Section 8.7.1.

Bit 5: CLKD Frequency is 19.44MHz (CLKD19). This bit specifies the frequency to be output on CLKD when the CLAD[3] configuration bit is high.

0 = 77.76MHz
1 = 19.44MHz

Bit 4: INT Pin Mode (INTM). This bit determines the inactive mode of the $\overline{\text{INT}}$ pin. The $\overline{\text{INT}}$ pin always drives low when an enabled interrupt source is active. See Section 8.10.

0 = Pin is high impedance when no enabled interrupts are active
1 = Pin drives high when no enabled interrupts are active

Bit 3: RDY/$\overline{\text{ACK}}$ Select (RAS). This bit controls the microprocessor interface output pin RDY/ACK in Intel mode (IFSEL = 100 or 110) and Motorola mode (IFSEL = 101 or 111).

0 = Normal operation: RDY in Intel mode and $\overline{\text{ACK}}$ in Motorola mode
1 = Reverse operation: $\overline{\text{ACK}}$ in Intel mode and RDY in Motorola mode

Bit 2: RDY/$\overline{\text{ACK}}$ Disable (RAD). This bit disables the microprocessor interface output pin RDY/ACK.

0 = Enable, normal operation
1 = Disable, tri-state

Bit 1: Latched Status Bit Clear-on-Read Enable (LSBCRE). This bit determines when the latched status register bits are cleared. See Section 8.8.5.

0 = Latched status register bits are cleared on a write
1 = Latched status register bits are cleared on a read

Bit 0: Global Write Mode (GWRM). This bit enables the global write mode. When this bit is set, a write to a register of any port causes a write to the same register in all the ports. In this mode register reads are not supported and result in undefined data. See Section 8.8.6.

0 = Normal write mode
1 = Global write mode

Register Name: **GLOBAL.GIOACR1**
Register Description: **General-Purpose I/O A Control Register #1**
Register Address: **010h**

Bit #	15	14	13	12	11	10	9	8
Name	GIOA8S[1:0]		GIOA7S[1:0]		GIOA6S[1:0]		GIOA5S[1:0]	
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	GIOA4S[1:0]		GIOA3S[1:0]		GIOA2S[1:0]		GIOA1S[1:0]	
Default	0	0	0	0	0	0	0	0

Note: *See Section 8.7.3 for more information.*

Bits 15, 14: General-Purpose I/O A 8 Select (GIOA8S[1:0]). These bits specify the function of the GPIOA8 pin.
00 = Input
01 = Output LOS status for port 8
10 = Output logic 0
11 = Output logic 1

Bits 13, 12: General-Purpose I/O A 7 Select (GIOA7S[1:0]). These bits specify the function of the GPIOA7 pin.
00 = Input
01 = Output LOS status for port 7
10 = Output logic 0
11 = Output logic 1

Bits 11, 10: General-Purpose I/O A 6 Select (GIOA6S[1:0]). These bits specify the function of the GPIOA6 pin.
00 = Input
01 = Output LOS status for port 6
10 = Output logic 0
11 = Output logic 1

Bits 9, 8: General-Purpose I/O A 5 Select (GIOA5S[1:0]). These bits specify the function of the GPIOA5 pin.
00 = Input
01 = Output LOS status for port 5
10 = Output logic 0
11 = Output logic 1

Bits 7, 6: General-Purpose I/O A 4 Select (GIOA4S[1:0]). These bits specify the function of the GPIOA4 pin.
00 = Input
01 = Output LOS status for port 4
10 = Output logic 0
11 = Output logic 1

Bits 5, 4: General-Purpose I/O A 3 Select (GIOA3S[1:0]). These bits specify the function of the GPIOA3 pin
00 = Input
01 = Output LOS status for port 3
10 = Output logic 0
11 = Output logic 1

Bits 3, 2: General-Purpose I/O A 2 Select (GIOA2S[1:0]). These bits specify the function of the GPIOA2 pin.
00 = Input
01 = Output LOS status for port 2
10 = Output logic 0
11 = Output logic 1

Bits 1, 0: General-Purpose I/O A 1 Select (GIOA1S[1:0]). These bits specify the function of the GPIOA1 pin.
00 = Input
01 = Output LOS status for port 1
10 = Output logic 0
11 = Output logic 1

Register Name: **GLOBAL.GIOACR2**
Register Description: **General-Purpose I/O A Control Register #2**
Register Address: **012h**

Bit #	15	14	13	12	11	10	9	8
Name	—	—	—	—	—	—	—	—
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	GIOA12S[1:0]		GIOA11S[1:0]		GIOA10S[1:0]		GIOA9S[1:0]	
Default	0	0	0	0	0	0	0	0

Note: *See Section 8.7.3 for more information.*

Bits 7, 6: General-Purpose I/O A 12 Select (GIOA12S[1:0]). These bits specify the function of the GPIOA12 pin.

00 = Input
01 = Output LOS status for port 12
10 = Output logic 0
11 = Output logic 1

Bits 5, 4: General-Purpose I/O A 11 Select (GIOA11S[1:0]). These bits specify the function of the GPIOA11 pin

00 = Input
01 = Output LOS status for port 11
10 = Output logic 0
11 = Output logic 1

Bits 3, 2: General-Purpose I/O A 10 Select (GIOA10S[1:0]). These bits specify the function of the GPIOA10 pin.

00 = Input
01 = Output LOS status for port 10
10 = Output logic 0
11 = Output logic 1

Bits 1, 0: General-Purpose I/O A 9 Select (GIOA9S[1:0]). These bits specify the function of the GPIOA9 pin.

00 = Input
01 = Output LOS status for port 9
10 = Output logic 0
11 = Output logic 1

Register Name: **GLOBAL.GIOBCR1**
Register Description: **General-Purpose I/O B Control Register #1**
Register Address: **014h**

Bit #	15	14	13	12	11	10	9	8
Name	GIOB8S[1:0]		GIOB7S[1:0]		GIOB6S[1:0]		GIOB5S[1:0]	
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	GIOB4S[1:0]		GIOB3S[1:0]		GIOB2S[1:0]		GIOB1S[1:0]	
Default	0	0	0	0	0	0	0	0

Note: *See Section 8.7.3 for more information.*

Bits 15, 14: General-Purpose I/O B 8 Select (GIOB8S[1:0]). These bits specify the function of the GPIOB8 pin.

00 = Input
01 = Output LOS status for port 8
10 = Output logic 0
11 = Output logic 1

Bits 13, 12: General-Purpose I/O B 7 Select (GIOB7S[1:0]). These bits specify the function of the GPIOB7 pin.

00 = Input
01 = Output LOS status for port 7
10 = Output logic 0
11 = Output logic 1

Bits 11, 10: General-Purpose I/O B 6 Select (GIOB6S[1:0]). These bits specify the function of the GPIOB6 pin.

00 = Input
01 = Output LOS status for port 6
10 = Output logic 0
11 = Output logic 1

Bits 9, 8: General-Purpose I/O B 5 Select (GIOB5S[1:0]). These bits specify the function of the GPIOB5 pin.

00 = Input
01 = Output LOS status for port 5
10 = Output logic 0
11 = Output logic 1

Bits 7, 6: General-Purpose I/O B 4 Select (GIOB4S[1:0]). These bits specify the function of the GPIOB4 pin.

00 = Input
01 = Output LOS status for port 4
10 = Output logic 0
11 = Output logic 1

Bits 5, 4: General-Purpose I/O B 3 Select (GIOB3S[1:0]). These bits specify the function of the GPIOB3 pin. Note: If GLOBAL.CR1:G1SROE is set to 1, GPIOB3 is the global one second reference output signal.

00 = Input
01 = Output LOS status for port 3
10 = Output logic 0
11 = Output logic 1

Bits 3, 2: General-Purpose I/O B 2 Select (GIOB2S[1:0]). These bits specify the function of the GPIOB2 pin. Note: If GLOBAL.CR1:MEIMS is set to 1, GPIOB2 is the global transmit manual error insertion (TMEI) input signal.

00 = Input
01 = Output LOS status for port 2
10 = Output logic 0
11 = Output logic 1

Bits 1, 0: General-Purpose I/O B 1 Select (GIOB1S[1:0]). These bits specify the function of the GPIOB1 pin. Note: If GLOBAL.CR1:GPM[1:0] is set to 01, GPIOB1 is the global performance monitoring update input signal.

00 = Input
01 = Output LOS status for port 1
10 = Output logic 0
11 = Output logic 1

Register Name: **GLOBAL.GIOBCR2**
Register Description: **General-Purpose I/O B Control Register #2**
Register Address: **016h**

Bit #	15	14	13	12	11	10	9	8
Name	—	—	—	—	—	—	—	—
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	GIOB12S[1:0]		GIOB11S[1:0]		GIOB10S[1:0]		GIOB9S[1:0]	
Default	0	0	0	0	0	0	0	0

Note: *See Section 8.7.3 for more information.*

Bits 7, 6: General-Purpose I/O 12 Select (GIOB12S[1:0]). These bits specify the function of the GPIOB12 pin.

00 = Input
01 = Output LOS status for port 12
10 = Output logic 0
11 = Output logic 1

Bits 5, 4: General-Purpose I/O 11 Select (GIOB11S[1:0]). These bits specify the function of the GPIOB11 pin

00 = Input
01 = Output LOS status for port 11
10 = Output logic 0
11 = Output logic 1

Bits 3, 2: General-Purpose I/O 10 Select (GIOB10S[1:0]). These bits specify the function of the GPIOB10 pin.

00 = Input
01 = Output LOS status for port 10
10 = Output logic 0
11 = Output logic 1

Bits 1, 0: General-Purpose I/O 9 Select (GIOB9S[1:0]). These bits specify the function of the GPIOB9 pin.

00 = Input
01 = Output LOS status for port 9
10 = Output logic 0
11 = Output logic 1

Register Name: **GLOBAL.ISR**
Register Description: **Global Interrupt Status Register**
Register Address: **020h**

Bit #	15	14	13	12	11	10	9	8
Name	—	—	—	P12ISR	P11ISR	P10ISR	P9ISR	P8ISR

Bit #	7	6	5	4	3	2	1	0
Name	P7ISR	P6ISR	P5ISR	P4ISR	P3ISR	P2ISR	P1ISR	GSR

Bits 12 to 1: Port n Interrupt Status Register (PnISR). This bit is set when any of the bits in the port n interrupt status register (PORT.ISR) are set and enabled for interrupt. When set, this bit causes an interrupt if GLOBAL.ISRIE:PnISRIE is set. See Section 8.10.

Bit 0: Global Status Register (GSR). This bit is set when any of the latched status register bits in the global latched status register (GLOBAL.SRL) are set and enabled for interrupt. When set, this bit causes an interrupt if GLOBAL.ISRIE:GSRIE is set. See Section 8.10.

Register Name: **GLOBAL.ISRIE**
Register Description: **Global Interrupt Status Register Interrupt Enable**
Register Address: **022h**

Bit #	15	14	13	12	11	10	9	8
Name	—	—	—	P12ISRIE	P11ISRIE	P10ISRIE	P9ISRIE	P8ISRIE
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	P7ISRIE	P6ISRIE	P5ISRIE	P4ISRIE	P3ISRIE	P2ISRIE	P1ISRIE	GSRIE
Default	0	0	0	0	0	0	0	0

Bits 12 to 1: Port n Interrupt Status Register Interrupt Enable (PnISRIE). This bit is the interrupt enable for the GLOBAL.ISR:PnISR status bit. See Section 8.10.

0 = mask the interrupt
1 = enable the interrupt

Bit 0: Global Status Register Interrupt Enable (GSRIE). This bit is the interrupt enable for the GLOBAL.ISR:GSR status bit. See Section 8.10.

0 = mask the interrupt
1 = enable the interrupt

Register Name: **GLOBAL.SR**
Register Description: **Global Status Register**
Register Address: **028h**

Bit #	15	14	13	12	11	10	9	8
Name	—	—	—	—	—	—	—	—
Default	—	—	—	—	—	—	—	—

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	CLOL	—	GPMS
Default	—	—	—	—	—	0	—	0

Bit 2: CLAD Loss of Lock (CLOL). This bit is set when the CLAD is not locked to the reference frequency.

Bit 0: Global Performance Monitoring Update Status (GPMS). This bit is set when the PORT.SR:PMS status bits are set in all of the ports that are enabled for global update control (i.e., all ports that have PORT.CR1:PMUM = 1). Ports that have PORT.CR1:PMUM = 0 have no effect on this bit. In global software update mode, the global update request bit (GLOBAL.CR1:GPMU) should be held high until this status bit goes high. See Section 8.7.4.

0 = The associated update request signal is low or not all register updates are completed.
1 = The requested performance register updates are all completed.

Register Name: **GLOBAL.SRL**
Register Description: **Global Status Register Latched**
Register Address: **02Ah**

Bit #	15	14	13	12	11	10	9	8
Name	—	—	—	—	—	—	—	—

Bit #	7	6	5	4	3	2	1	0
Name	—	CLKCL	CLKBL	CLKAL	CLADL	CLOLL	G1SREFL	GPMSL

Bit 6: CLAD C Clock Activity Latched (CLKCL). This bit is set when the signal on the CLKC pin is active. Note: This bit should always be low when GLOBAL.CR2:CLAD[6:4] ≠ 000. See Section 8.7.1.

Bit 5: CLAD B Clock Activity Latched (CLKBL). This bit is set when the signal on the CLKB pin is active. Note: This bit should always be low when GLOBAL.CR2:CLAD[6:4] ≠ 000. See Section 8.7.1.

Bit 4: CLAD A Clock Activity Latched (CLKAL). This bit is set when the signal on the CLKA pin is active. Note: This bit should always be low when GLOBAL.CR2:CLAD[6:4] ≠ 000. See Section 8.7.1.

Bit 3: CLAD Reference Clock Activity Status Latched (CLADL). This bit is set when the CLAD PLL reference clock signal on the REFCLK pin is active. Note: When GLOBAL.CR2:CLAD[6:4] = 000, the REFCLK pin is unused. See Section 8.7.1.

Bit 2: CLAD Loss of Lock Latched (CLOLL). This bit is set when the GLOBAL.SR:CLOL status bit transitions from low to high.

Bit 1: Global One-Second Status Latched (G1SREFL). This bit is set once each second when the internal global one-second timer signal transitions low to high. When set, this bit causes an interrupt if interrupt enables GLOBAL.SRIE:G1SREFIE and GLOBAL.ISRIE:GSRIE are both set. See Section 8.7.1.

Bit 0: Global Performance Monitoring Update Status Latched (GPMSL). This bit is set when the GLOBAL.SR:GPMS status bit changes from low to high. When set, this bit causes an interrupt if interrupt enables GLOBAL.SRIE:GPMSIE and GLOBAL.ISRIE:GSRIE are both set. See Section 8.7.1.

Register Name: **GLOBAL.SRIE**
Register Description: **Global Status Register Interrupt Enable**
Register Address: **02Ch**

Bit #	15	14	13	12	11	10	9	8
Name	—	—	—	—	—	—	—	—
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	CLOLIE	G1SREFIE	GPMSIE
Default	0	0	0	0	0	0	0	0

Bit 2: CLAD Loss of Lock Interrupt Enable (CLOLIE). This bit is the interrupt enable for the GLOBAL.SRL:CLOLL bit.

0 = mask the interrupt
1 = enable the interrupt

Bit 1: Global One-Second Interrupt Enable (G1SREFIE). This bit is the interrupt enable for the GLOBAL.SRL:G1SREFL bit.

0 = mask the interrupt
1 = enable the interrupt

Bit 0: Global Performance Monitoring Update Status Interrupt Enable (GPMSIE). This bit is the interrupt enable for the GLOBAL.SRL: GPMSL bit.

0 = mask the interrupt
1 = enable the interrupt

Register Name: **GLOBAL.GIOARR**
Register Description: **General-Purpose I/O A Read Register**
Register Address: **038h**

Bit #	15	14	13	12	11	10	9	8
Name	—	—	—	—	GPIOA12	GPIOA11	GPIOA10	GPIOA9

Bit #	7	6	5	4	3	2	1	0
Name	GPIOA8	GPIOA7	GPIOA6	GPIOA5	GPIOA4	GPIOA3	GPIOA2	GPIOA1

Bits 11 to 0: General-Purpose I/O A n Status (GPIOAn). Bit n indicates the status of general-purpose I/O A pin n (GPIOAn). See Section 8.7.3.

Register Name: **GLOBAL.GIOBRR**
Register Description: **General-Purpose I/O B Read Register**
Register Address: **03Ah**

Bit #	15	14	13	12	11	10	9	8
Name	—	—	—	—	GPIOB12	GPIOB11	GPIOB10	GPIOB9

Bit #	7	6	5	4	3	2	1	0
Name	GPIOB8	GPIOB7	GPIOB6	GPIOB5	GPIOB4	GPIOB3	GPIOB2	GPIOB1

Bits 11 to 0: General-Purpose I/O B n Status (GPIOBn). Bit n indicates the status of general-purpose I/O B pin n (GPIOBn). See Section 8.7.3.

9.4 Port Common Registers

Table 9-4. Port Common Register Map

ADDRESS OFFSET	REGISTER	REGISTER DESCRIPTION
00h	PORT.CR1	Port Control Register 1
02h	PORT.CR2	Port Control Register 2
04h	PORT.CR3	Port Control Register 3
06h	—	Unused
08h	—	Unused
0Ah	PORT.INV	Port I/O Invert Control Register
0Ch	—	Unused
0Eh	—	Unused
10h	PORT.ISR	Port Interrupt Status Register
12h	—	Unused
14h	PORT.ISRIE	Port Interrupt Status Register Interrupt Enable
16h	—	Unused
18h	PORT.SR	Port Status Register
1Ah	PORT.SRL	Port Status Register Latched
1Ch	PORT.SRIE	Port Status Register Interrupt Enable
1Eh	—	Unused

Register Name: **PORT.CR1**
Register Description: **Port Control Register 1**
Register Address: **n * 80h + 00h**

Bit #	15	14	13	12	11	10	9	8
Name	—	—	—	—	—	—	—	—
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	TMEI	MEIMS	PMUM	PMU	TPD	RPD	RSTDP	RST
Default	0	0	0	0	1	1	1	0

Bit 7: Transmit Manual Error Insert (TMEI). When PORT.CR1:MEIMS = 0, this bit is used to insert errors in all blocks where block-level MEIMS = 1. Error(s) are inserted at the next opportunity after this bit transitions from low to high. See Section 8.7.5. Note: This bit should be set low immediately after each error insertion.

Bit 6: Transmit Manual Error Insert Mode Select (MEIMS). This bit specifies the source of the error insertion signal for all block-level error generators that have block-level MEIMS = 1. See Section 8.7.5.

0 = Port-level error insertion via PORT.CR1:TMEI
1 = Global error insertion as specified by GLOBAL.CR1:MEIMS

Bit 5: Port Performance Monitor Update Mode (PMUM). This bit specifies the source of the performance monitoring update signal for all blocks that have block-level PMUM = 1. See Section 8.7.4.

0 = Port-level PM update via PORT.CR1:PMU
1 = Global PM update as specified by GLOBAL.CR1:GPM[1:0]

Bit 4: Port Performance Monitor Register Update (PMU). When PORT.CR1:PMUM = 0, this bit is used to update all of the performance monitor registers where block-level PMUM = 1. When this bit transitions from low to high, all configured performance monitoring registers are updated with the latest counter values, and all associated counters are reset. This bit should remain high until the performance monitor update status bit (PORT.SR:PMS) goes high, and then it should be brought back low, which clears the PMS status bit. If a counter increment occurs at the exact same time as the counter reset, the counter is loaded with a value of one, and the “counter is non-zero” latched status bit is set. See Section 8.7.4.

Bit 3: Transmit Power-Down (TPD). When this bit is set, the transmit path of the port is powered down and considered “out of service”. The digital logic is powered down by stopping the clocks. See Section 8.11.

0 = Normal operation
1 = Power down the port transmit path (TXP and TXN become high impedance)

Bit 2: Receive Power-Down (RPD). When this bit is set, the receive path of the port is powered down and considered “out of service”. The digital logic is powered down by stopping the clocks. See Section 8.11.

0 = Normal operation
1 = Power down the port receive path (RPOS/RDAT, RNEG/RLCV, and RCLK become high impedance)

Bit 1: Reset Data Path (RSTDP). When this bit is set, it forces all of the port’s internal data path and status registers to their default state. This bit must be set high for a minimum of 100ns and then set back low. See Section 8.11.

0 = Normal operation
1 = Force all data path registers to their default values

Bit 0: Reset (RST). When this bit is set, all of the internal data path and status and control registers (except this RST bit) of this port are reset to their default state. This bit must be set high for a minimum of 100ns. This bit is logically ORed with the inverted hardware signal $\overline{\text{RST}}$ and the GLOBAL.CR1:RST bit. See Section 8.11.

0 = Normal operation
1 = Force all internal registers to their default values

Register Name: **PORT.CR2**
Register Description: **Port Control Register 2**
Register Address: **n * 80h + 02h**

Bit #	15	14	13	12	11	10	9	8
Name	—	—	—	—	—	—	—	—
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	LM[1:0]		—	ROD	TBIN	RBIN	TCC	—
Default	0	0	0	0	0	0	0	0

Bits 7 and 6: LIU Mode (LM[1:0]). These bits select the operating mode of the port. See Section 8.1.

00 = DS3
01 = E3
10 = STS-1
11 = reserved

Bit 4: Receive Output Disable (ROD). See Section 8.3.6.4.

0 = enable the receiver outputs
1 = disable the receiver outputs (RCLK, RPOS/RDAT, and RNEG/RLCV)

Bit 3: Transmit Binary Interface Enable (TBIN). See Section 8.2.2.

0 = Transmitter framer interface is bipolar on the TPOS and TNEG pins. The B3ZS/HDB3 encoder is disabled.
1 = Transmitter framer interface is binary on the TDAT pin. The B3ZS/HDB3 encoder is enabled.

Bit 2: Receive Binary Interface Enable (RBIN). See Section 8.3.6.

0 = Receiver framer interface is bipolar on the RPOS and RNEG pins. The B3ZS/HDB3 decoder is disabled.
1 = Receiver framer interface is binary on the RDAT pin with the RLCV pin indicating line-code violations. The B3ZS/HDB3 encoder is enabled.

Bit 1: Transmit Common Clock Mode (TCC). See Section 8.2.1.1.

0 = Source transmit clock for port n from TCLKn
1 = Source transmit clock for port n from TCLK1

Register Name: **PORT.CR3**
Register Description: **Port Control Register 3**
Register Address: **n * 80h + 04h**

Bit #	15	14	13	12	11	10	9	8
Name	—	—	—	—	—	—	BERTE	BERTD
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	SCRD	—	—	AIST	TAIS	LBS	LB[1:0]	
Default	0	0	0	0	0	0	0	0

Bit 9: BERT Enable (BERTE). See Section 8.5.

0 = disable the BERT pattern generator (the pattern detector is always enabled)
1 = enable the BERT pattern generator (the pattern detector is always enabled)

Bit 8: BERT Direction (BERTD). See Section 8.5.

0 = line direction (transmit to receive)
1 = system direction (receive to transmit)

Bit 7: STS-1 Scrambling Disable (SCRD). This bit controls STS-1 scrambling when AIS-L is generated in STS-1 mode. See Section 8.2.3.

0 = Perform scrambling
1 = Do not perform scrambling

Bit 4: AIS Type (AIST). See Section 8.2.4.

0 = Unframed all ones
1 = Framed DS3 AIS (DS3 mode), unframed all ones (E3 mode), or AIS-L (STS-1 mode)

Bit 3: Transmit AIS (TAIS). The type of AIS signal depends on the LIU mode (DS3, E3, or STS-1) and the configured AIS type. See Section 8.2.4.

0 = transmit normal data
1 = transmit AIS signal

Bit 2: Loopback Select (LBS). This bit affects the function of the loopback mode (LBM[1:0]) bits.

Bits 1 and 0: Loopback Mode (LB[1:0]). These bits enable loopbacks. The effect of the LB = 11 decode is controlled by the LBS configuration bit. See Section 8.6.

00 = No loopback
01 = Diagnostic loopback (DLB)
10 = Line loopback (LLB)
11 (LBS = 0) = Line loopback (LLB) and diagnostic loopback (DLB) simultaneously
11 (LBS = 1) = Analog loopback (ALB)

Register Name: **PORT.INV**
Register Description: **Port I/O Invert Control Register**
Register Address: **n * 80h + 0Ah**

Bit #	15	14	13	12	11	10	9	8
Name	—	—	—	—	—	—	—	—
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	—	TNEGI	TPOSI	TCLKI	—	RNEGI	RPOSI	RCLKI
Default	0	0	0	0	0	0	0	0

Bit 6: TNEG Invert (TNEGI). This bit inverts the TNEG input pin when set.

0 = Noninverted
1 = Inverted

Bit 5: TPOS/TDAT Invert (TPOSI). This bit inverts the TPOS/TDAT input pin when set.

0 = Noninverted
1 = Inverted

Bit 4: TCLK Invert (TCLKI). This bit inverts the TCLK pin input pin when set. See Section 8.2.1.

0 = Noninverted; TPOS/TDAT and TNEG are sampled on the rising edge of TCLK.
1 = Inverted; TPOS/TDAT and TNEG are sampled on the falling edge of TCLK.

Bit 2: RNEG/RLCV Invert (RNEGI). This bit inverts the RNEG/RLCV output pin when set.

0 = Noninverted
1 = Inverted

Bit 1: RPOS/RDAT Invert (RPOSI). This bit inverts the RPOS/RDAT output pin when set.

0 = Noninverted
1 = Inverted

Bit 0: RCLK Invert (RCLKI). This bit inverts the RCLKn output pin when set. See Section 8.3.6.3.

0 = Noninverted; RPOS/RDAT and RNEG/RLCV are updated on the falling edge of RCLK.
1 = Inverted; RPOS/RDAT and RNEG/RLCV are updated on the rising edge of RCLK.

Register Name: **PORT.ISR**
Register Description: **Port Interrupt Status Register**
Register Address: **n * 80h + 10h**

Bit #	15	14	13	12	11	10	9	8
Name	—	—	—	—	—	—	—	—

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	LDSR	LIUSR	BSR	PSR

Bit 3: Line Decoder Status Register Interrupt Status (LDSR). This bit is set when any of the latched status register bits in the B3ZS/HDB3 Line Decoder block are set and enabled for interrupt. When set, this bit causes an interrupt if PORT.ISRIE:LDSRIE and GLOBAL.ISRIE:PnISRIE are both set. See Section 8.10.

Bit 2: LIU Status Register Interrupt Status (LIUSR). This bit is set when any of the latched status register bits in the LIU block are set and enabled for interrupt. When set, this bit causes an interrupt if PORT.ISRIE:LIUSRIE and GLOBAL.ISRIE: PnISRIE are both set. See Section 8.10.

Bit 1: BERT Status Register Interrupt Status (BSR). This bit is set when any of the latched status register bits in the BERT block are set and enabled for interrupt. When set, this bit causes an interrupt if PORT.ISRIE:BSRIE and GLOBAL.ISRIE: PnISRIE are both set. See Section 8.10.

Bit 0: Port Status Register Interrupt Status (PSR). This bit is set when any of the latched status register bits in the port latched status register (PORT.SRL) are set and enabled for interrupt. When set, this bit causes an interrupt if PORT.ISRIE:PSRIE and GLOBAL.ISRIE: PnISRIE are both set. See Section 8.10.

Register Name: **PORT.ISRIE**
Register Description: **Port Interrupt Status Register Interrupt Enable**
Register Address: **n * 80h + 14h**

Bit #	15	14	13	12	11	10	9	8
Name	—	—	—	—	—	—	—	—
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	LDSRIE	LIUSRIE	BSRIE	PSRIE
Default	0	0	0	0	0	0	0	0

Bit 3: Line Decoder Status Register Interrupt Enable (LDSRIE). This bit is the interrupt enable for the PORT.ISR:LDSR status bit.

0 = mask the interrupt
1 = enable the interrupt

Bit 2: LIU Status Register Interrupt Enable (LIUSRIE). This bit is the interrupt enable for the PORT.ISR:LIUSR status bit.

0 = mask the interrupt
1 = enable the interrupt

Bit 1: BERT Status Register Interrupt Enable (BSRIE). This bit is the interrupt enable for the PORT.ISR:BSR status bit.

0 = mask the interrupt
1 = enable the interrupt

Bit 0: Port Status Register Interrupt Enable (PSRIE). This bit is the interrupt enable for the PORT.ISR:PSR status bit.

0 = mask the interrupt
1 = enable the interrupt

Register Name: **PORT.SR**
Register Description: **Port Status Register**
Register Address: **n * 80h + 18h**

Bit #	15	14	13	12	11	10	9	8
Name	—	—	—	—	—	—	—	—
Default	—	—	—	—	—	—	—	—

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	—	PMS
Default	—	—	—	—	—	—	—	0

Bit 0: Performance Monitoring Update Status (PMS). This bit is set when the PMS bits are set in all of the port functional blocks that are configured for port-level update control (i.e., all blocks that have PMUM = 1). Blocks that have PMUM = 0 have no effect on this bit. In port-level software update mode, the port update request bit (PORT.CR1:PMU) should be held high until this status bit goes high. See Section 8.7.4.

0 = The associated update request signal is low or not all register updates are completed.
1 = The requested performance register updates are all completed.

Register Name: **PORT.SRL**
Register Description: **Port Status Register Latched**
Register Address: **n * 80h + 1Ah**

Bit #	15	14	13	12	11	10	9	8
Name	—	—	—	—	—	—	—	TCLKL

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	—	PMSL

Bit 8: Transmit Clock Activity Status Latched (TCLKL). This bit is set when the signal on the TCLK pin used by this port (TCLK*n* when TCC = 0, TCLK1 when TCC = 1) is active. When set, this bit causes an interrupt if interrupt enables PORT.SRIE:TCLKIE, PORT.ISRIE:PSRIE, and GLOBAL.ISRIE: PnISRIE are all set.

Bit 0: Performance Monitoring Update Status Latched (PMSL). This bit is set when the PORT.SR:PMS status bit changes from low to high. When set, this bit causes an interrupt if interrupt enables PORT.SRIE:PMSIE, PORT.ISRIE:PSRIE and GLOBAL.ISRIE:PnISRIE are all set. See Section 8.7.4.

Register Name: **PORT.SRIE**
Register Description: **Port Status Register Interrupt Enable**
Register Address: **n * 80h + 1Ch**

Bit #	15	14	13	12	11	10	9	8
Name	—	—	—	—	—	—	—	TCLKIE
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	—	PMSIE
Default	0	0	0	0	0	0	0	0

Bit 8: Transmit Clock Activity Latched Status Interrupt Enable (TCLKIE). This bit is the interrupt enable for the PORT.SRL:TCLKL bit.

0 = mask the interrupt
1 = enable the interrupt

Bit 0: Performance Monitoring Update Latched Status Interrupt Enable (PMSIE). This bit is the interrupt enable for the PORT.SRL:PMSL bit.

0 = mask the interrupt
1 = enable the interrupt

9.5 LIU Registers

ADDRESS OFFSET	REGISTER	REGISTER DESCRIPTION
20h	LIU.CR1	Control Register 1
22h	LIU.CR2	Control Register 2
24h	LIU.TWSCR1	Transmit Waveshaping Control Register 1
26h	LIU.TWSCR2	Transmit Waveshaping Control Register 2
28h	LIU.SR	Status Register
2Ah	LIU.SRL	Status Register Latched
2Ch	LIU.SRIE	Status Register Interrupt Enable
2Eh	LIU.RGLR	Receive Gain Level Register

Register Name: **LIU.CR1**
Register Description: **LIU Control Register 1**
Register Address: **n * 80h + 20h**

Bit #	15	14	13	12	11	10	9	8
Name	—	—	—	—	JAD[1:0]		JAS[1:0]	
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	—	—	TLBO	TOE	TTRE	TRESADJ[2:0]		
Default	0	0	0	0	0	0	0	0

Bits 11, 10: Jitter Attenuator Depth (JAD[1:0]). These bits select the jitter attenuator buffer depth. See Section 8.4.

00 = 16 bits
01 = 32 bits
10 = 64 bits
11 = 128 bits

Bit 9, 8: Jitter Attenuator Select (JAS[1:0]). These bits select the location of the jitter attenuator. See Section 8.4.

00 = Disabled
01 = Receive Path
10 = Transmit Path
11 = Transmit Path

Bit 5: Transmit LIU LBO (TLBO). This bit is used to enable the transmit LBO circuit which causes the transmit signal to be preattenuated to mimic the attenuation of approximately approximates about 225 feet of cable. This is used to reduce near-end crosstalk when the cable lengths are short. This signal is only valid in DS3 and STS-1 modes. See Section 8.2.6.

0 = Disabled
1 = Enabled

Bit 4: Transmit Output Enable (TOE). This bit enables the transmitter outputs (TXP and TXN). The transmitter continues to operate internally when the transmitter is tri-stated. Only the line driver and driver monitor are disabled. See Section 8.2.7. Note: This bit is ORed with the associated TOE input pin.

0 = TXP and TXN are high impedance
1 = TXP and TXN are driven

Bit 3: Transmit Termination Resistor Enable (TTRE). This bit indicates when the transmitter internal termination is enabled. See Section 8.2.8.

0 = Disabled, the transmitter is terminated externally
1 = Enabled, the transmitter is terminated internally

Bits 2, 0: Transmit Resistor Adjustment (TRESADJ[2:0]). These bits are used to adjust the internal termination resistance of the transmitter. See Section 8.2.8.

000 = 75Ω
001 = 82Ω
010 = 90Ω
011 = 100Ω
100 = 68Ω
101 = 62Ω
110 = 56Ω
111 = 50Ω

Register Name: **LIU.CR2**
Register Description: **LIU Control Register 2**
Register Address: **n * 80h + 22h**

Bit #	15	14	13	12	11	10	9	8
Name	—	—	—	—	—	—	—	—
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	—	—	RFL2E	RMON	RTRE	RRESADJ[2:0]		
Default	0	0	0	0	0	0	0	0

Bit 5: Receive Fail 2 Enable (RFL2E). This bit is used to enable the receive failure type 2 detection. See Section 8.3.8.

0 = Disable receive failure type 2 detection
1 = Enable receive failure type 2 detection

Bit 4: Receive LIU Monitor Mode (RMON). This bit is used to enable the receive LIU monitor mode preamplifier. Enabling the preamplifier adds about 14dB of linear amplification for use in monitor applications where the signal has been reduced 20dB using resistive attenuator circuits. Note: When enabled, the preamp is turned on or off automatically depending upon the input signal level. See Section 8.3.2.

0 = Disable the preamp
1 = Enable the preamp

Bit 3: Receive Termination Resistor Enable (RTRE). This bit indicates when the receiver internal termination is enabled. See Section 8.3.1.

0 = Disabled, the receiver is terminated externally
1 = Enabled, the receiver is terminated internally

Bits 2 to 0: Receive Resistor Adjustment (RRESADJ[2:0]). These bits are used to adjust the internal termination resistance of the receiver. See Section 8.3.1.

000 = 75Ω
001 = 82Ω
010 = 90Ω
011 = 100Ω
100 = 68Ω
101 = 62Ω
110 = 56Ω
111 = 50Ω

Register Name: **LIU.TWSCR1**
Register Description: **LIU Transmit Waveshaping Control Register 1**
Register Address: **n * 80h + 24h**

Bit #	15	14	13	12	11	10	9	8
Name	TWSC[15:8]							
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	TWSC[7:0]							
Default	0	0	0	0	0	0	0	0

See Figure 8-1, Figure 8-2, and Figure 8-3 for illustrations of the first and second rise/fall time segments of the DS3 and STS-1 waveforms and the overshoot, one level, undershoot, and zero level segments for the E3 waveform.

Bits 15, 14: Transmit Waveshaping Control (TWSC[15:14]). In DS3 and STS-1 modes, this field adjusts the width of the first of two rising-edge segments. In E3 mode this field adjusts the width of the leading edge overshoot.

	DS3/STS-1 Behavior	E3 Behavior
00 -	normal first rise time	normal overshoot width
01 -	increase first rise time by 0.1ns	increase overshoot width
10 -	decrease first rise time by 0.1ns	decrease overshoot width
11 -	decrease first rise time by 0.2ns	decrease overshoot width

Bits 13, 12: Transmit Waveshaping Control (TWSC[13:12]). In DS3 and STS-1 modes, this field adjusts the width of the second of two rising-edge segments. In E3 mode this field adjusts the width of the pulse plateau.

	DS3/STS-1 Behavior	E3 Behavior
00 -	normal second rise time	normal “one level” time
01 -	increase second rise time by 0.1ns	increase “one level” time by 0.15ns
10 -	decrease second rise time by 0.1ns	decrease “one level” time by 0.15ns
11 -	decrease second rise time by 0.1ns	decrease “one level” time by 0.3ns

Bits 11, 10: Transmit Waveshaping Control (TWSC[11:10]). In DS3 and STS-1 modes, this field adjusts the width of the first of two falling-edge segments. In E3 mode this field adjusts the width of the trailing edge undershoot.

	DS3/STS-1 Behavior	E3 Behavior
00 -	normal first fall time	normal undershoot width
01 -	increase first fall time by 0.1ns	increase undershoot width by 0.15ns
10 -	decrease first fall time by 0.1ns	decrease undershoot width by 0.15ns
11 -	decrease first fall time by 0.1ns	decrease undershoot width by 0.3ns

Bits 9, 8: Transmit Waveshaping Control (TWSC[9:8]). In DS3 and STS-1 modes, this field adjusts the width of the second of two falling-edge segments. In E3 mode this field adjusts the width of the zero after the trailing edge.

	DS3/STS-1 Behavior	E3 Behavior
00 -	normal second fall time	normal “zero level” width
01 -	increase second fall time by 0.1ns	increase “zero level” width by 0.15ns
10 -	decrease second fall time by 0.1ns	decrease “zero level” width by 0.15ns
11 -	decrease second fall time by 0.2ns	decrease “zero level” width by 0.3ns

Bits 7, 6: Transmit Waveshaping Control (TWSC[7:6]). In DS3 and STS-1 modes, this field adjusts the amplitude of the first of two rising-edge segments. In E3 mode this field adjusts the amplitude of the leading edge overshoot. The 11 value is a special case in which the entire pulse is made narrower.

	DS3/STS-1 Behavior	E3 Behavior
00 -	normal first rise amplitude	normal overshoot
01 -	decrease first rise amplitude 15%	decrease overshoot amplitude 2%
10 -	increase first rise amplitude 15%	increase overshoot amplitude 2%
11 -	decrease pulse width by 0.15ns	decrease pulse width by 0.15ns

Bits 5, 4: Transmit Waveshaping Control (TWSC[5:4]). In DS3 and STS-1 modes, this field adjusts the amplitude of the second of two rising-edge segments. In E3 mode this field has no effect, except for the 11 value, which is a special case in which the entire pulse is made wider.

	DS3/STS-1 Behavior	E3 Behavior
00 -	normal rise amplitude	normal pulse
01 -	decrease second rise amplitude 15%	normal pulse
10 -	increase second rise amplitude 15%	normal pulse
11 -	increase pulse width by 0.15ns	increase pulse width by 0.15ns

Bits 3, 2: Transmit Waveshaping Control (TWSC[3:2]). In DS3 and STS-1 modes, this field adjusts the amplitude of the first of two falling-edge segments. In E3 mode this field adjusts the amplitude of the trailing edge overshoot. The 11 value is a special case in which the entire pulse is made wider.

	DS3/STS-1 Behavior	E3 Behavior
00 -	normal first fall time	normal undershoot
01 -	decrease first fall time amplitude 15%	decrease undershoot 2%
10 -	increase first fall time amplitude 15%	increase undershoot 2%
11 -	increase pulse width by 0.15ns	increase pulse width by 0.15ns

Bits 1, 0: Transmit Waveshaping Control (TWSC[1:0]). In DS3 and STS-1 modes, this field adjusts the fall time of the second of two falling-edge segments. In E3 mode this field has no effect, except for the 11 value, which is a special case in which the entire pulse is made narrower.

	DS3/STS-1 Behavior	E3 Behavior
00 -	normal second fall time	normal pulse
01 -	decrease second fall time amplitude 15%	normal pulse
10 -	increase second fall time amplitude 15%	normal pulse
11 -	decrease pulse width by 0.15ns	decrease pulse width by 0.15ns

Register Name: **LIU.TWSCR2**
Register Description: **LIU Transmit Waveshaping Control Register 2**
Register Address: **n * 80h + 26h**

Bit #	15	14	13	12	11	10	9	8
Name	—	—	—	—	—	—	—	—
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	TWSC[19:16]			
Default	0	0	0	0	0	0	0	0

Bits 3 to 0: Transmit Waveshaping Control (TWSC[19:16]). This field adjusts overall amplitude of the transmit output pulse.

0000 - nominal amplitude (see Table 11-6 and Table 11-7)
0001 - increase amplitude by 3.75%
0010 - increase amplitude by 7.5%
0011 - increase amplitude by 11.25%
0100 - increase amplitude by 15%
0101 - increase amplitude by 20%
0110 - increase amplitude by 25%
0111 - increase amplitude by 30%
1000 - decrease amplitude by 12.5%
1001 - decrease amplitude by 9.375%
1010 - decrease amplitude by 6.25%
1011 - decrease amplitude by 3.125%
110X - increase amplitude to internal current limit
111X - increase amplitude to maximum, current limiting disabled

Register Name: **LIU.SR**
Register Description: **LIU Status Register**
Register Address: **n * 80h + 28h**

Bit #	15	14	13	12	11	10	9	8
Name	—	—	—	—	—	TDM	TFAIL	LOMC
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	RPAS	RFAIL1	RFAIL2	RLOL	ALOS
Default	1	1	0	0	0	0	0	0

Bit 10: Transmit Driver Monitor (TDM). This bit indicates when the transmit driver is faulty. See Section 8.2.9.

0 = the transmit line driver is operating properly
1 = the transmit line driver is faulty

Bit 9: Transmit Output Failure (TFAIL). This bit indicates when there is a failure on the transmit differential outputs (TXP/TXN). See Section 8.2.9.

0 = an open or short has not been detected on TXP or TXN
1 = an open or short has been detected on TXP or TXN

Bit 8: Loss of Master Clock (LOMC). This bit indicates whether or not the master reference clock (DS3, E3, or STS-1, depending on PORT.CR2:LM[1:0] setting) is available from the CLAD block. See Section 8.7.1.

0 = the master reference clock is present
1 = that master reference clock is not present

Bit 4: Receive Preamp Status (RPAS). See Section 8.3.2.

0 = the receiver preamp is off
1 = the receiver preamp is on

Bit 3: Receive Failure Type 1 (RFAIL1). See Section 8.3.8.

0 = a receive failure type 1 has not been detected on RXP or RXN
1 = a receive failure type 1 has been detected on RXP or RXN.

Bit 2: Receive Failure Type 2 (RFAIL2). See Section 8.3.8.

0 = a receive failure type 2 has not been detected on RXP or RXN
1 = a receive failure type 2 has been detected on RXP or RXN.

Bit 1: Receive Loss of Lock (RLOL). See Section 8.3.4.

0 = the incoming clock frequency on RXP/RXN is within ±7700ppm of the master reference clock
1 = the incoming clock frequency on RXP/RXN is more than ±7900ppm away from the master reference clock

Bit 0: Analog Loss of Signal (ALOS). See Section 8.3.5.

0 = an analog LOS (ALOS) condition has not been detected
1 = an ALOS condition has been detected

Register Name: **LIU.SRL**
Register Description: **LIU Status Register Latched**
Register Address: **n * 80h + 2Ah**

Bit #	15	14	13	12	11	10	9	8
Name	—	—	—	JAFL	JAEL	TDML	TFAILL	LOMCL
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	—	—	RGLCL	RPASL	RFAIL1L	RFAIL2L	RLOLL	ALOSL
Default	0	0	0	0	0	0	0	0

Bit 12: Jitter Attenuator Full Latched (JAFL). This bit is set when the jitter attenuator buffer is full, or when data has been lost due to a jitter attenuator buffer underflow or overflow. When set, this bit causes an interrupt if interrupt enables LIU.SRIE:JAFIE, PORT.ISRIE:LDSRIE and GLOBAL.ISRIE:PnISRIE are all set. See Section 8.4.

Bit 11: Jitter Attenuator Empty Latched (JAEL). This bit is set when the jitter attenuator buffer is empty, or when data has been lost due to a jitter attenuator buffer underflow or overflow. When set, this bit causes an interrupt if interrupt enables LIU.SRIE:JAEIE, PORT.ISRIE:LDSRIE and GLOBAL.ISRIE:PnISRIE are all set. See Section 8.4.

Bit 10: Transmit Driver Monitor Change Latched (TDML). This bit is set when the LIU.SR:TDM bit changes state. When set, this bit causes an interrupt if interrupt enables LIU.SRIE:TDMIE, PORT.ISRIE:LDSRIE and GLOBAL.ISRIE:PnISRIE are all set.

Bit 9: Transmit Output Failure Change Latched (TFAILL). This bit is set when the LIU.SR:TFAIL bit changes state. When set, this bit causes an interrupt if interrupt enables LIU.SRIE:TFAILIE, PORT.ISRIE:LDSRIE and GLOBAL.ISRIE:PnISRIE are all set.

Bit 8: Loss of Master Clock Latched (LOMCL). This bit is set when the LIU.SR:LOMC bit is set. When set, this bit causes an interrupt if interrupt enables LIU.SRIE:LOMCIE, PORT.ISRIE:LDSRIE and GLOBAL.ISRIE:PnISRIE are all set.

Bit 5: Receive Gain Level Change Latched (RGLCL). This bit is set when the receive gain level (LIU.RGLR: RGL[7:0]) changes. When set, this bit causes an interrupt if interrupt enables LIU.SRIE:RGLCIE, PORT.ISRIE:LDSRIE and GLOBAL.ISRIE:PnISRIE are all set.

Bit 4: Receive Preamp Status Change Latched (RPASL). This bit is set when the LIU.SR:RPAS bit changes state. When set, this bit causes an interrupt if interrupt enables LIU.SRIE:RPASIE, PORT.ISRIE:LDSRIE and GLOBAL.ISRIE:PnISRIE are all set.

Bit 3: Receive Failure Type 1 Change Latched (RFAIL1L). This bit is set when the LIU.SR:RFAIL1 bit changes state. When set, this bit causes an interrupt if interrupt enables LIU.SRIE:RFAIL1IE, PORT.ISRIE:LDSRIE and GLOBAL.ISRIE:PnISRIE are all set.

Bit 2: Receive Failure Type 2 Change Latched (RFAIL2L). This bit is set when the LIU.SR:RFAIL2 bit changes state. When set, this bit causes an interrupt if interrupt enables LIU.SRIE:RFAIL2IE, PORT.ISRIE:LDSRIE and GLOBAL.ISRIE:PnISRIE are all set.

Bit 1: Receive Loss of Lock Change Latched (RLOLL). This bit is set when the LIU.SR:RLOL bit changes state. When set, this bit causes an interrupt if interrupt enables LIU.SRIE:RLOLIE, PORT.ISRIE:LDSRIE and GLOBAL.ISRIE:PnISRIE are all set.

Bit 0: Analog Loss of Signal Change Latched (ALOSL). This bit is set when the LIU.SR:ALOS bit changes state. When set, this bit causes an interrupt if interrupt enables LIU.SRIE:ALOSIE, PORT.ISRIE:LDSRIE and GLOBAL.ISRIE:PnISRIE are all set.

Register Name: **LIU.SRIE**
Register Description: **LIU Status Register Interrupt Enable**
Register Address: **n * 80h + 2Ch**

Bit #	15	14	13	12	11	10	9	8
Name	—	—	—	JAFIE	JAEIE	TDMIE	TFAILIE	LOMCIE
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	—	—	RGLCIE	RPASIE	RFAIL1IE	RFAIL2IE	RLOLIE	ALOSIE
Default	0	0	0	0	0	0	0	0

Bit 12: Jitter Attenuator Full Interrupt Enable (JAFIE). This bit is the interrupt enable for the LIU.SRL:JAFL bit.

0 = interrupt disabled
1 = interrupt enabled

Bit 11: Jitter Attenuator Empty Interrupt Enable (JAEIE). This bit is the interrupt enable for the LIU.SRL:JAEL bit.

0 = interrupt disabled
1 = interrupt enabled

Bit 10: Transmit Driver Monitor Interrupt Enable (TDMIE). This bit is the interrupt enable for the LIU.SRL:TDML bit.

0 = interrupt disabled
1 = interrupt enabled

Bit 9: Transmit Output Failure Interrupt Enable (TFAILIE). This bit is the interrupt enable for the LIU.SRL:TFAILL bit.

0 = interrupt disabled
1 = interrupt enabled

Bit 8: Loss of Master Clock Interrupt Enable (LOMCIE). This bit is the interrupt enable for the LIU.SRL:LOMCL bit.

0 = interrupt disabled
1 = interrupt enabled

Bit 5: Receive Gain Level Change Interrupt Enable (RGLCIE). This bit is the interrupt enable for the LIU.SRL:RGLCL bit.

0 = interrupt disabled
1 = interrupt enabled

Bit 4: Receive Preamp Status Interrupt Enable (RPASIE). This bit is the interrupt enable for the LIU.SRL:RPASL bit.

0 = interrupt disabled
1 = interrupt enabled

Bit 3: Receive Failure Type 1 Interrupt Enable (RFAIL1IE). This bit is the interrupt enable for the LIU.SRL:RFAIL1L bit.

0 = interrupt disabled
1 = interrupt enabled

Bit 2: Receive Failure Type 2 Interrupt Enable (RFAIL2IE). This bit is the interrupt enable for the LIU.SRL:RFAIL2L bit.

0 = interrupt disabled
1 = interrupt enabled

Bit 1: Receive Loss of Lock Interrupt Enable (RLOLIE). This bit is the interrupt enable for the LIU.SRL:RLOLL bit.

0 = interrupt disabled
1 = interrupt enabled

Bit 0: Analog Loss Of Signal Interrupt Enable (ALOSIE). This bit is the interrupt enable for the LIU.SRL:ALOSL bit.

0 = interrupt disabled
1 = interrupt enabled

Register Name: **LIU.RGLR**
Register Description: **LIU Receive Gain Level Register**
Register Address: **n * 80h + 2Eh**

Bit #	15	14	13	12	11	10	9	8
Name	—	—	—	—	—	—	—	—
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	RGL7	RGL6	RGL5	RGL4	RGL3	RGL2	RGL1	RGL0
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: Receive Gain Level (RGL[7:0]). This field reports the real-time receiver gain level in 0.25 dB increments. Values of 00–60h indicate receiver gain of 0dB to +24dB in 0.25dB increments. Values of F4–Fifth indicate receiver gain of -3dB to -0.25dB in 0.25dB increments. See Section 8.3.3.

9.6 B3ZS/HDB3 Encoder Registers

ADDRESS OFFSET	REGISTER	REGISTER DESCRIPTION
30h	LINE.TCR	B3ZS/HDB3 Transmit Control Register
32h–3Eh	—	Unused

Register Name: **LINE.TCR**
Register Description: **B3ZS/HDB3 Transmit Control Register**
Register Address: **n * 80h + 30h**

Bit #	15	14	13	12	11	10	9	8
Name	—	—	—	—	—	—	—	—
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	TZSD	EXZI	BPVI	TSEI	MEIMS
Default	0	0	0	0	0	0	0	0

Bit 4: Transmit Zero Suppression Encoding Disable (TZSD)

0 = zero suppression (B3ZS or HDB3) encoding is enabled
1 = zero suppression (B3ZS or HDB3) encoding is disabled, and only AMI encoding is performed

Bit 3: Excessive Zero Insert Enable (EXZI). See Section 8.2.3.

0 = excessive zero event (EXZ) insertion is disabled
1 = excessive zero event insertion is enabled

Bit 2: Bipolar Violation Insert Enable (BPVI). See Section 8.2.3.

0 = bipolar violation (BPV) insertion is disabled
1 = bipolar violation insertion is enabled.

Bit 1: Transmit Single Error Insert (TSEI). When LINE.TCR:MEIMS = 0, this bit is used to insert errors of the type(s) specified by EXZI and BPVI in the transmit data stream. A zero-to-one transition causes a single error to be inserted. For a second error to be inserted, this bit must be set to 0, and then back to 1. Note: If LINE.TCR:MEIMS is low, and this bit transitions more than once between error insertion opportunities, only one error is inserted. See Section 8.7.5.

Bit 0: Manual Error Insert Mode Select (MEIMS). This bit specifies the source of the error insertion signal for the transmit encoder/decoder block. Note: If the TMEI pin or TSEI bit is one, changing the state of this bit may cause an error to be inserted. See Section 8.7.5.

0 = Block-level error insertion using the LINE.TCR:TSEI control bit
1 = Port-level or global-level error insertion as specified by PORT.CR1:MEIMS

9.7 B3ZS/HDB3 Decoder Registers

ADDRESS OFFSET	REGISTER	REGISTER DESCRIPTION
40h	LINE.RCR	B3ZS/HDB3 Receive Control Register
42h	—	Unused
44h	LINE.RSR	B3ZS/HDB3 Receive Status Register
46h	LINE.RSRL	B3ZS/HDB3 Receive Status Register Latched
48h	LINE.RSRIE	B3ZS/HDB3 Receive Status Register Interrupt Enable
4Ah	—	Unused
4Ch	LINE.RBPVCR	B3ZS/HDB3 Receive Bipolar Violation Count Register
4Eh	LINE.REXZCR	B3ZS/HDB3 Receive Excessive Zero Count Register

Register Name: **LINE.RCR**
Register Description: **B3ZS/HDB3 Receive Control Register**
Register Address: **n * 80h + 40h**

Bit #	15	14	13	12	11	10	9	8
Name	—	—	—	—	—	—	—	—
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	E3CVE	REZSF	RDZSF	RZSD
Default	0	0	0	0	0	0	0	0

Bit 3: E3 Code Violation Enable (E3CVE). In E3 mode (PORT.CR2:LM[1:0] = 01), this bit specifies whether the LINE.RBPVCR register counts bipolar violations or E3 coding violations. Note: E3 line coding violations are defined in ITU O.161 as consecutive bipolar violations of the same polarity. This bit is ignored in B3ZS mode. See Section 8.3.6.2.

0 = bipolar violations.
1 = E3 line coding violations

Bit 2: Receive BPV Error Detection Zero Suppression Code Format (REZSF). When REZSF = 0, BPV error detection detects a B3ZS signature if a zero is followed by a bipolar violation (BPV), and an HDB3 signature if two zeros are followed by a BPV. When REZSF = 1, BPV error detection detects a B3ZS signature if a zero is followed by a BPV that has the opposite polarity of the BPV in the previous B3ZS signature, and an HDB3 signature if two zeros are followed by a BPV that has the opposite polarity of the BPV in the previous HDB3 signature. Note: Immediately after a reset (RST or DPRST bit high), this bit is ignored. The first B3ZS signature is defined as a zero followed by a BPV, and the first HDB3 signature is defined as two zeros followed by a BPV. All subsequent B3ZS/HDB3 signatures are determined by the setting of this bit. *Note: The default setting (REZSF = 0) conforms to ITU O.162. The default setting may falsely ignore actual BPVs that are not codewords. It is recommended that REZSF be set to one for most applications. This setting is more robust to accurately detect codewords.* See Section 8.3.6.2.

Bit 1: Receive Zero Suppression Decoding Zero Suppression Code Format (RDZSF). When RDZSF = 0, zero suppression decoding detects a B3ZS signature if a zero is followed by a bipolar violation (BPV), and an HDB3 signature if two zeros are followed by a BPV. When RDZSF = 1, zero suppression decoding detects a B3ZS signature if a zero is followed by a BPV that has the opposite polarity of the BPV in the previous B3ZS signature, and an HDB3 signature if two zeros are followed by a BPV that has the opposite polarity of the BPV in the previous HDB3 signature. Note: Immediately after a reset (RST or DPRST bit high), this bit is ignored. The first B3ZS signature is defined as a zero followed by a BPV, and the first HDB3 signature is defined as two zeros followed by a BPV. All subsequent B3ZS/HDB3 signatures are determined by the setting of this bit. *Note: The default setting (RDZSF = 0) may falsely decode actual BPVs that are not codewords. It is recommended that RDZSF be set to one for most applications. This setting is more robust to accurately detect codewords.* See Section 8.3.6.2.

Bit 0: Receive Zero Suppression Decoding Disable (RZSD)

0 = zero suppression (B3ZS or HDB3) decoding is enabled
1 = zero suppression (B3ZS or HDB3) decoding is disabled, and only AMI decoding is performed

Register Name: **LINE.RSR**
Register Description: **B3ZS/HDB3 Receive Status Register**
Register Address: **n * 80h + 44h**

Bit #	15	14	13	12	11	10	9	8
Name	—	—	—	—	—	—	—	—
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	EXZC	—	BPVC	LOS
Default	0	0	0	0	0	0	0	0

Bit 3: Excessive Zero Count (EXZC). See Section 8.3.6.

0 = the Receive Excessive Zero Count Register (**LINE.REXZCR**) is zero
1 = the Receive Excessive Zero Count Register (**LINE.REXZCR**) is one or more

Bit 1: Bipolar Violation Count (BPVC). See Section 8.3.6.

0 = the Receive Bipolar Violation Count Register (**LINE.RBPVCR**) is zero
1 = the Receive Bipolar Violation Count Register (**LINE.RBPVCR**) is one or more

Bit 0: Loss of Signal (LOS). See Section 8.3.5.

0 = receive line interface is not in a LOS condition
1 = receive line interface is in an LOS condition

Register Name: **LINE.RSRL**
Register Description: **B3ZS/HDB3 Receive Status Register Latched**
Register Address: **n * 80h + 46h**

Bit #	15	14	13	12	11	10	9	8
Name	—	—	—	—	—	—	—	—
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	—	—	ZSCDL	EXZL	EXZCL	BPVL	BPVCL	LOSL
Default	0	0	0	0	0	0	0	0

Bit 5: Zero Suppression Code Detect Latched (ZSCDL). This bit is set when a B3ZS or HDB3 signature is detected. When set, this bit causes an interrupt if interrupt enables LINE.RSRIE:ZSCDIE, PORT.ISRIE:LDSRIE and GLOBAL.ISRIE:PnISRIE are all set. See Section 8.3.6.

Bit 4: Excessive Zero Latched (EXZL). This bit is set when an excessive zero event is detected on the incoming bipolar data stream. When set, this bit causes an interrupt if interrupt enables LINE.RSRIE:EXZIE, PORT.ISRIE:LDSRIE and GLOBAL.ISRIE:PnISRIE are all set. See Section 8.3.6.

Bit 3: Excessive Zero Count Latched (EXZCL). This bit is set when LINE.RSR:EXZC transitions from zero to one. When set, this bit causes an interrupt if interrupt enables LINE.RSRIE:EXZCIE, PORT.ISRIE:LDSRIE and GLOBAL.ISRIE:PnISRIE are all set. See Section 8.3.6.

Bit 2: Bipolar Violation Latched (BPVL). This bit is set when a bipolar violation (or E3 LCV if enabled) is detected on the incoming bipolar data stream. When set, this bit causes an interrupt if interrupt enables LINE.RSRIE:BPVIE, PORT.ISRIE:LDSRIE and GLOBAL.ISRIE:PnISRIE are all set. See Section 8.3.6.

Bit 1: Bipolar Violation Count Latched (BPVCL). This bit is set when LINE.RSR:BPVC transitions from zero to one. When set, this bit causes an interrupt if interrupt enables LINE.RSRIE:BPVCIE, PORT.ISRIE:LDSRIE and GLOBAL.ISRIE:PnISRIE are all set. See Section 8.3.6.

Bit 0: Loss of Signal Change Latched (LOSL). This bit is set when LINE.RSR:LOS changes state. When set, this bit causes an interrupt if interrupt enables LINE.RSRIE:LOSIE, PORT.ISRIE:LDSRIE and GLOBAL.ISRIE:PnISRIE are all set. See Section 8.3.5.

Register Name: **LINE.RSRIE**
Register Description: **B3ZS/HDB3 Receive Status Register Interrupt Enable**
Register Address: **n * 80h + 48h**

Bit #	15	14	13	12	11	10	9	8
Name	—	—	—	—	—	—	—	—
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	—	—	ZSCDIE	EXZIE	EXZCIE	BPVIE	BPVCIE	LOSIE
Default	0	0	0	0	0	0	0	0

Bit 5: Zero Suppression Code Detect Interrupt Enable (ZSCDIE). This bit is the interrupt enable for the LINE.RSRL:ZSCDL status bit.

0 = mask the interrupt
1 = enable the interrupt

Bit 4: Excessive Zero Interrupt Enable (EXZIE). This bit is the interrupt enable for the LINE.RSRL:EXZL status bit.

0 = mask the interrupt
1 = enable the interrupt

Bit 3: Excessive Zero Count Interrupt Enable (EXZCIE). This bit is the interrupt enable for the LINE.RSRL:EXZCL status bit.

0 = mask the interrupt
1 = enable the interrupt

Bit 2: Bipolar Violation Interrupt Enable (BPVIE). This bit is the interrupt enable for the LINE.RSRL:BPVL status bit.

0 = mask the interrupt
1 = enable the interrupt

Bit 1: Bipolar Violation Count Interrupt Enable (BPVCIE). This bit is the interrupt enable for the LINE.RSRL:BPVCL status bit.

0 = mask the interrupt
1 = enable the interrupt

Bit 0: Loss-of-Signal Interrupt Enable (LOSIE). This bit is the interrupt enable for the LINE.RSRL:LOSL status bit.

0 = mask the interrupt
1 = enable the interrupt

Register Name: **LINE.RBPVCR**
Register Description: **B3ZS/HDB3 Receive Bipolar Violation Count Register**
Register Address: **n * 80h + 4Ch**

Bit #	15	14	13	12	11	10	9	8
Name	BPV[15:8]							
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	BPV[7:0]							
Default	0	0	0	0	0	0	0	0

Bits 15 to 0: Bipolar Violation Count (BPV[15:0]). These 16 bits indicate the number of bipolar violations detected on the incoming bipolar data stream. See Section 8.3.6.

Register Name: **LINE.REXZCR**
Register Description: **B3ZS/HDB3 Receive Excessive Zero Count Register**
Register Address: **n * 80h + 4Eh**

Bit #	15	14	13	12	11	10	9	8
Name	EXZ[15:8]							
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	EXZ[7:0]							
Default	0	0	0	0	0	0	0	0

Bit 15 to 0: Excessive Zero Count (EXZ[15:0]). These 16 bits indicate the number of excessive zero conditions detected on the incoming bipolar data stream. See Section 8.3.6.

9.8 BERT Registers

ADDRESS OFFSET	REGISTER	REGISTER DESCRIPTION
50h	BERT.CR	BERT Control Register
52h	BERT.PCR	BERT Pattern Configuration Register
54h	BERT.SPR1	BERT Seed/Pattern Register 1
56h	BERT.SPR2	BERT Seed/Pattern Register 2
58h	BERT.TEICR	Transmit Error Insertion Control Register
5Ah	—	Unused
5Ch	BERT.SR	BERT Status Register
5Eh	BERT.SRL	BERT Status Register Latched
60h	BERT.SRIE	BERT Status Register Interrupt Enable
62h	—	Unused
64h	BERT.RBECR1	Receive Bit Error Count Register 1
66h	BERT.RBECR2	Receive Bit Error Count Register 2
68h	BERT.RBCR1	Receive Bit Count Register 1
6Ah	BERT.RBCR2	Receive Bit Count Register 2
6Ch	—	Unused
6Eh	—	Unused

Register Name: **BERT.CR**
Register Description: **BERT Control Register**
Register Address: **n * 80h + 50h**

Bit #	15	14	13	12	11	10	9	8
Name	—	—	—	—	—	—	—	—
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	PMUM	LPMU	RNPL	RPIC	MPR	APRD	TNPL	TPIC
Default	0	0	0	0	0	0	0	0

Bit 7: Performance Monitoring Update Mode (PMUM). This bit specifies the source of the performance monitoring update signal for the BERT block. See Section 8.7.4. Note: If RPMU or LPMU is one, changing the state of this bit may cause a performance monitoring update to occur.

0 = Block-level update via BERT.CR:LPMU
1 = Port-level or global update as specified by PORT.CR1:PMUM

Bit 6: Local Performance Monitoring Update (LPMU). When BERT.CR:PMUM = 0, this bit updates the performance monitoring registers in the BERT block. When this bit transitions from low to high, the BERT.RBECR and BERT.RBCR registers are updated with the latest counter values and the counters are reset. This bit should remain high until the performance monitor update status bit (BERT.SR:PMS) goes high, and then it should be brought back low, which clears the PMS status bit. If a counter increment occurs at the exact same time as the counter reset, the counter is loaded with a value of one, and the “counter is non-zero” latched status bit is set. See Section 8.7.4.

Bit 5: Receive New Pattern Load (RNPL). A zero-to-one transition of this bit causes the programmed test pattern (QRSS, PTS, PLF[4:0], PTF[4:0] in the BERT.PCR register, and BSP[31:0] in the BERT.SPR registers) to be loaded into the receive pattern generator. This bit must be changed to zero and back to one for another pattern to be loaded. Loading a new pattern forces the receive pattern generator out of the “Sync” state which causes a resynchronization to be initiated. Note: The test pattern fields mentioned above must not change for four RCLK cycles after this bit transitions from zero to one. See Section 8.5.1.

Bit 4: Receive Pattern Inversion Control (RPIC). See Section 8.5.1.

0 = do not invert the incoming data stream
1 = invert the incoming data stream

Bit 3: Manual Pattern Resynchronization (MPR). A zero-to-one transition of this bit causes the receive pattern generator to resynchronize to the incoming pattern. This bit must be changed to zero and back to one for another resynchronization to be initiated. Note: A manual resynchronization forces the pattern detector out of the "Sync" state. See Section 8.5.2.

Bit 2: Automatic Pattern Resynchronization Disable (APRD). When APRD = 0, the receive pattern generator automatically resynchronizes to the incoming pattern if six or more times during the current 64-bit window the incoming data stream bit and the receive pattern generator output bit did not match. When APRD = 1, the receive pattern generator does not automatically resynchronize to the incoming pattern. Note: Automatic synchronization is prevented by not allowing the receive pattern generator to automatically exit the "Sync" state. See Section 8.5.2.

Bit 1: Transmit New Pattern Load (TNPL). A zero-to-one transition of this bit causes the programmed test pattern (QRSS, PTS, PLF[4:0], PTF[4:0] in the BERT.PCR register, and BSP[31:0] in the BERT.SPR registers) to be loaded into the transmit pattern generator. This bit must be changed to zero and back to one for another pattern to be loaded. Note: The test pattern fields mentioned above must not change for four TCLK cycles after this bit transitions from zero to one. See Section 8.5.1.

Bit 0: Transmit Pattern Inversion Control (TPIC). See Section 8.5.1.

0 = do not invert the outgoing data stream
1 = invert the outgoing data stream

Register Name: **BERT.PCR**
Register Description: **BERT Pattern Configuration Register**
Register Address: **n * 80h + 52h**

Bit #	15	14	13	12	11	10	9	8
Name	—	—	—	PTF[4:0]				
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	—	QRSS	PTS	PLF[4:0]				
Default	0	0	0	0	0	0	0	0

Bits 12 to 8: Pattern Tap Feedback (PTF[4:0]). These five bits control the PRBS "tap" feedback of the pattern generator. The "tap" feedback is from bit y of the pattern generator (y = PTF[4:0] + 1). These bits are ignored when the BERT block is programmed for a repetitive pattern (PTS = 1). For a PRBS signal, the feedback is an XOR of bit n and bit y. See Section 8.5.1.

Bit 6: QRSS Enable (QRSS). See Section 8.5.1.

0 = Disabled: the pattern generator configuration is controlled by PTS, PLF[4:0], PTF[4:0], and BSP[31:0]
1 = Enabled: the pattern generator configuration is forced to a PRBS pattern with a generating polynomial of $x^{20} + x^{17} + 1$, and the output of the pattern generator is forced to one if the next 14 output bits are all zero.

Bit 5: Pattern Type Select (PTS). See Section 8.5.1.

0 = PRBS pattern
1 = repetitive pattern.

Bits 4 to 0: Pattern Length Feedback (PLF[4:0]). This field controls the "length" feedback of the pattern generator. The "length" feedback is from bit n of the pattern generator (n = PLF[4:0] + 1). For a PRBS signal, the feedback is an XOR of bit n and bit y. For a repetitive pattern the feedback is bit n. See Section 8.5.1.

Register Name: **BERT.SPR1**
Register Description: **BERT Seed/Pattern Register #1**
Register Address: **n * 80h + 54h**

Bit #	15	14	13	12	11	10	9	8
Name	BSP[15:8]							
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	BSP[7:0]							
Default	0	0	0	0	0	0	0	0

Bits 15 to 0: BERT Seed/Pattern (BSP[15:0])

Register Name: **BERT.SPR2**
Register Description: **BERT Seed/Pattern Register #2**
Register Address: **n * 80h + 56h**

Bit #	15	14	13	12	11	10	9	8
Name	BSP[31:24]							
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	BSP[23:16]							
Default	0	0	0	0	0	0	0	0

Bits 15 to 0: BERT Seed/Pattern (BSP[31:16])

BERT Seed/Pattern (BSP[31:0]). This 32-bit field is the programmable seed for a transmit PRBS pattern, or the programmable pattern for a transmit or receive repetitive pattern. BSP[31] is the first bit output on the transmit side for a 32-bit repetitive pattern or 32-bit PRBS. BSP[31] is the first bit input on the receive side for a 32-bit repetitive pattern. See Section 8.5.1.

Register Name: **BERT.TEICR**
Register Description: **BERT Transmit Error Insertion Control Register**
Register Address: **n * 80h + 58h**

Bit #	15	14	13	12	11	10	9	8
Name	—	—	—	—	—	—	—	—
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	—	—	TEIR[2:0]			BEI	TSEI	MEIMS
Default	0	0	0	0	0	0	0	0

Bits 5 to 3: Transmit Error Insertion Rate (TEIR[2:0]). This field indicates the rate at which errors are automatically inserted in the output data stream. One out of every 10^n bits is inverted, where n = TEIR[2:0]. A value of 0 disables error insertion. A value of 1 results in every 10th bit being inverted. A value of 2 result in every 100th bit being inverted. Error insertion starts when this field is written with a non-zero value. If this field is written during an error insertion, the new error rate is used after the next error is inserted. See Section 8.5.3.1.

Bit 2: Bit Error Insertion Enable (BEI). See Section 8.5.3.1.

0 = single-bit error insertion is disabled
1 = single-bit error insertion is enabled

Bit 1: Transmit Single Error Insert (TSEI). When BERT.TEICR:MEIMS = 0 and BEI = 1, this bit is used to insert single-bit errors in the outgoing BERT data stream. A zero-to-one transition causes a single bit error to be inserted. For a second bit error to be inserted, this bit must be set to 0, and back to 1. Note: If MEIMS is low, and this bit transitions more than once between error insertion opportunities, only one error is inserted. See Section 8.7.5.

Bit 0: Manual Error Insert Mode Select (MEIMS). This bit specifies the source of the error insertion signal for the BERT block. Note: If TMEI or TSEI is one, changing the state of this bit may cause a bit error to be inserted. See Section 8.7.5.

0 = error insertion is initiated by the BERT.TEICR:TSEI register bit
1 = error insertion is initiated by the transmit manual error insertion signal (TMEI) specified by the PORT.CR1:MEIMS register bit.

Register Name: **BERT.SR**
Register Description: **BERT Status Register**
Register Address: **n * 80h + 5Ch**

Bit #	15	14	13	12	11	10	9	8
Name	—	—	—	—	—	—	—	—
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	PMS	—	BEC	OOS
Default	0	0	0	0	1	0	0	0

Bit 3: Performance Monitoring Update Status (PMS). This bit is set when the performance monitoring registers (BERT.RBCR and BERT.RBECR) have been updated. PMS is asynchronously forced low when the BERT.CR:LPMU bit (BERT.CR:PMUM = 0) or RPMU signal (BERT.CR:PMUM = 1) goes low. See Section 8.7.4.

0 = The associated update request signal is low or not all register updates are completed
1 = The requested performance register updates are all completed

Bit 1: Bit Error Count (BEC). See Section 8.5.1.

0 = the bit error count is zero
1 = the bit error count is one or more

Bit 0: Out of Synchronization (OOS). See Section 8.5.1.

0 = the receive pattern generator is synchronized to the incoming pattern
1 = the receive pattern generator is not synchronized to the incoming pattern

Register Name: **BERT.SRL**
Register Description: **BERT Status Register Latched**
Register Address: **n * 80h + 5Eh**

Bit #	15	14	13	12	11	10	9	8
Name	—	—	—	—	—	—	—	—
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	PMSL	BEL	BECL	OOSL
Default	0	0	0	0	0	0	0	0

Bit 3: Performance Monitoring Update Status Latched (PMSL). This bit is set when the BERT.SR:PMS bit transitions from zero to one. When set, this bit causes an interrupt if interrupt enables BERT.SRIE:PMSIE, PORT.ISRIE:BSRIE and GLOBAL.ISRIE:PnISRIE are all set.

Bit 2: Bit Error Latched (BEL). This bit is set when a bit error is detected in the received pattern. When set, this bit causes an interrupt if interrupt enables BERT.SRIE:BEIE, PORT.ISRIE:BSRIE and GLOBAL.ISRIE:PnISRIE are all set.

Bit 1: Bit Error Count Latched (BECL). This bit is set when the BERT.SR:BEC bit transitions from zero to one. When set, this bit causes an interrupt if interrupt enables BERT.SRIE:BECIE, PORT.ISRIE:BSRIE and GLOBAL.ISRIE:PnISRIE are all set.

Bit 0: Out of Synchronization Latched (OOSL). This bit is set when the BERT.SR:OOS bit changes state. When set, this bit causes an interrupt if interrupt enables BERT.SRIE:OOSIE, PORT.ISRIE:BSRIE and GLOBAL.ISRIE:PnISRIE are all set.

Register Name: **BERT.SRIE**
Register Description: **BERT Status Register Interrupt Enable**
Register Address: **n * 80h + 60h**

Bit #	15	14	13	12	11	10	9	8
Name	—	—	—	—	—	—	—	—
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	PMSIE	BEIE	BECIE	OOSIE
Default	0	0	0	0	0	0	0	0

Bit 3: Performance Monitoring Update Status Interrupt Enable (PMSIE). This bit is the interrupt enable for the BERT.SRL:PMSL status bit.

0 = mask the interrupt
1 = enable the interrupt

Bit 2: Bit Error Interrupt Enable (BEIE). This bit is the interrupt enable for the BERT.SRL:BEL status bit.

0 = mask the interrupt
1 = enable the interrupt

Bit 1: Bit Error Count Interrupt Enable (BECIE). This bit is the interrupt enable for the BERT.SRL:BECL status bit.

0 = mask the interrupt
1 = enable the interrupt

Bit 0: Out of Synchronization Interrupt Enable (OOSIE). This bit is the interrupt enable for the BERT.SRL:OOSL status bit.

0 = mask the interrupt
1 = enable the interrupt

Register Name: **BERT.RBECR1**
Register Description: **BERT Receive Bit Error Count Register #1**
Register Address: **n * 80h + 64h**

Bit #	15	14	13	12	11	10	9	8
Name	BEC[15:8]							
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	BEC[7:0]							
Default	0	0	0	0	0	0	0	0

Bits 15 to 0: Bit Error Count (BEC[15:0])

Register Name: **BERT.RBECR2**
Register Description: **BERT Receive Bit Error Count Register #2**
Register Address: **n * 80h + 66h**

Bit #	15	14	13	12	11	10	9	8
Name	—	—	—	—	—	—	—	—
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	BEC[23:16]							
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: Bit Error Count (BEC[23:16])

Bit Error Count (BEC[23:0]). This field is the holding register for an internal BERT bit error counter that tracks the number of bit errors detected in the incoming data stream since the last performance monitoring update. The internal counter stops incrementing when it reaches a count of FF FFFFh and does not increment when an OOS condition exists. This register is updated when a performance monitoring update is performed. See Section 8.7.4. The source for the performance monitoring update signal is specified by the BERT.CR:PMUM bit.

Register Name: **BERT.RBCR1**
Register Description: **BERT Receive Bit Count Register #1**
Register Address: **n * 80h + 68h**

Bit #	15	14	13	12	11	10	9	8
Name	BC[15:8]							
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	BC[7:0]							
Default	0	0	0	0	0	0	0	0

Bits 15 to 0: Bit Count (BC[15:0])

Register Name: **BERT.RBCR2**
Register Description: **BERT Receive Bit Count Register #2**
Register Address: **n * 80h + 6Ah**

Bit #	15	14	13	12	11	10	9	8
Name	BC[31:24]							
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	BC[23:16]							
Default	0	0	0	0	0	0	0	0

Bits 15 to 0: Bit Count (BC[31:16])

Bit Count (BC[31:0]). This field is the holding register for an internal BERT bit counter that tracks the total number of bit received in the incoming data stream since the last performance monitoring update. The internal counter stops incrementing when it reaches a count of FFFF FFFFh and does not increment when an OOS condition exists. This register is updated when a performance monitoring update is performed. See Section 8.7.4. The source for the performance monitoring update signal is specified by the BERT.CR:PMUM bit.

10. JTAG INFORMATION

The DS325xx LIUs support the standard instruction codes SAMPLE/PRELOAD, BYPASS, and EXTEST. Optional public instructions included are HIGHZ, CLAMP, and IDCODE. The devices contain the following items, which meet the requirements set by the IEEE 1149.1 Standard Test Access Port and Boundary Scan Architecture:

- Test Access Port (TAP)
- TAP Controller
- Instruction Register
- Bypass Register
- Boundary Scan Register
- Device Identification Register

The TAP has the necessary interface pins, namely JTCLK, $\overline{\text{JTRST}}$, JTDI, JTDO, and JTMS. Details on these pins can be found in Table 7-9. Details about the boundary scan architecture and the TAP can be found in IEEE 1149.1-1990, IEEE 1149.1a-1993, and IEEE 1149.1b-1994.

IEEE 1149.1 requires a minimum of two test registers—the bypass register and the boundary scan register. The bypass register is a 1-bit shift register used with the BYPASS, CLAMP, and HIGHZ instructions to provide a short path between JTDI and JTDO. The boundary scan register contains a shift register path and a latched parallel output for control cells and digital I/O cells. DS325xx BSDL files are available at www.maxim-ic.com/TechSupport/telecom/bsdl.htm. An optional test register, the identification register, has also been included in the device design. The identification register contains a 32-bit shift register and a 32-bit latched parallel output. Table 10-1 shows the identification register contents for the DS32506, DS32508, and DS32512 devices.

Table 10-1. JTAG ID Code

PART	REVISION	DEVICE CODE	MANUFACTURER CODE	REQUIRED
DS32506	Consult factory	0000 0000 0111 1000	00010100001	1
DS32508	Consult factory	0000 0000 0111 1001	00010100001	1
DS32512	Consult factory	0000 0000 0111 1010	00010100001	1

11. ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Input or Output Lead with Respect to V_{SS}……-0.3V to +5.5V
Supply Voltage Range with Respect to V_{SS}
VDD33……...-0.3V to +3.63V
VDD18 ……..-0.1V to +1.89V
Ambient Operating Temperature Range*……..-40°C to +85°C
Junction Operating Temperature Range……-40°C to +125°C
Storage Temperature Range……...-55°C to +125°C
Soldering Temperature…….See IPC/JEDEC J-STD-020 Specification

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

**Ambient operating temperature range when device is mounted on a four-layer JEDEC test board with no airflow.*

Note: The typical values listed in the following tables and operation at -40°C are not production tested, but are guaranteed by design (GBD).

Table 11-1. Recommended DC Operating Conditions

(T_A = -40°C to +85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Digital Supply Voltage	VDD18		1.71	1.8	1.89	V
	VDD33		3.135	3.300	3.465	
Analog Supply Voltage	AVDD	CVDD, JVDD, RVDD, and TVDD	1.71	1.80	1.89	V
Logic 1, All Other Input Pins	V_{IH}		2.0		3.6	V
Logic 0, All Other Input Pins	V_{IL}		-0.3		+0.8	V

Table 11-2. DC Characteristics

(VDD18 = 1.8V ±5%, VDD33 = 3.3V ±5%, AVDD = 1.8V ±5%, T_A = -40°C to +85°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current, VDD18 (Note 1)	I_{DD18}	DS32506		248	320	mA
		DS32508		324	420	
		DS32512		476	620	
Supply Current, VDD33 (Note 1)	I_{DD33}	DS32506		90	165	mA
		DS32508		120	220	
		DS32512		180	330	
Supply Current, Transmitters Disabled (All TOE = 0), VDD18 (Note 2)	$I_{DDTTS18}$	DS32506		170	200	mA
		DS32508		220	260	
		DS32512		320	380	
Supply Current, Transmitters Disabled (All TOE = 0), VDD33 (Note 2)	$I_{DDTTS33}$	DS32506		90	165	mA
		DS32508		120	220	
		DS32512		180	330	
Supply Current, Power-Down (All TPD = RPD = 1), VDD18 (Notes 2, 3)	I_{DDPD18}	DS32506, DS32508, DS32512		16	40	mA
Supply Current, Power-Down (All TPD = RPD = 1), VDD33 (Notes 2, 3)	I_{DDPD33}	DS32506, DS32508, DS32512		5.3	10	mA
Lead Capacitance	C_{IO}			7	10	pF
Input Leakage, Input Pins with Pullup	I_{IL}	(Note 4)	-300		+10	µA
Input Leakage, All Other Input Pins	I_{IL}	(Note 4)	-50		+10	µA
Output Leakage (when High-Z)	I_{LO}	(Note 4)	-10		+10	µA
Output Voltage (I_O = -4.0mA)	V_{OH}		2.4		VDD33	V
Output Voltage (I_O = +4.0mA)	V_{OL}		0		0.4	V

Note 1: TCLKn = CLKC = 51.84MHz; LMn[1:0] = 10 (STS-1 mode); TXPn/TXNn driving all ones into 75Ω resistive loads; analog loopback enabled; all other inputs at VDD33 or grounded; all other outputs open.

Note 2: TCLKn = CLKC = 51.84MHz; LMn[1:0] = 10 (STS-1 mode); other inputs at VDD33 or grounded; digital outputs left open circuited.

Note 3: HW = 0, CLAD[6:0] = 0000000 (disabled), G1SRS[3:0] = 0000 (disable), $\overline{CS}$ = 1 (inactive).

Note 4: 0V < V_{IN} < VDD18 for all other digital inputs.

Table 11-3. Framer Interface Timing

(VDD18 = 1.8V ±5%, VDD33 = 3.3V ±5%, AVDD = 1.8V ±5%, T_A = -40°C to +85°C.) (See Figure 11-1 and Figure 11-2.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
RCLK/TCLK Clock Period	t1	(Notes 1, 2)		22.4		ns
		(Notes 2, 3)		29.1		
		(Notes 2, 4)		19.3		
RCLK Duty Cycle	t2/t, t3/t1	(Notes 5, 6)	45	50	55	%
TCLK Duty Cycle	t2/t, t3/t1	(Note 6)	30		70	%
LIU Reference Clock Duty Cycle	t2/t, t3/t1	(Notes 6, 7)	30		70	%
TPOS/TDAT, TNEG to TCLK Setup Time	t4	(Notes 6, 8)	3			ns
TPOS/TDAT, TNEG Hold Time	t5	(Notes 6, 8)	1			ns
RCLK to RPOS/RDAT, RNEG/RLCV Value Change	t6	(Notes 5, 6, 9)	1		7	ns
RCLK Rise and Fall Time	t7	(Notes 6, 10)		1	2	ns
TCLK Rise and Fall Time	t8	(Notes 5, 11)			2	ns

Note 1: DS3 mode.

Note 2: 78MHz is the maximum instantaneous frequency for a gapped clock. The maximum average frequency is 45.094MHz for DS3, 34.643MHz for E3, and 52.255MHz for STS-1.

Note 3: E3 mode.

Note 4: STS-1 mode.

Note 5: Outputs loaded with 25pF, measured at 50% threshold.

Note 6: Not tested during production test.

Note 7: The LIU reference clock must be a ±20ppm low-jitter clock. See Section 8.7.1 for more information on reference clocks.

Note 8: When TCLKI = 0, TPOS/TDAT and TNEG are sampled on the rising edge of TCLK. When TCLKI = 1, TPOS/TDAT and TNEG are sampled on the falling edge of TCLK.

Note 9: When RCLKI = 0, RPOS/RDAT and RNEG/RLCV are updated on the falling edge of RCLK. When RCLKI = 1, RPOS/RDAT and RNEG/RLCV are updated on the rising edge of RCLK.

Note 10: Outputs loaded with 25pF, measured between $V_{OL(MAX)}$ and $V_{OH(MIN)}$.

Note 11: Measured between $V_{IL(MAX)}$ and $V_{IH(MIN)}$.

Figure 11-1. Transmitter Framer Interface Timing Diagram

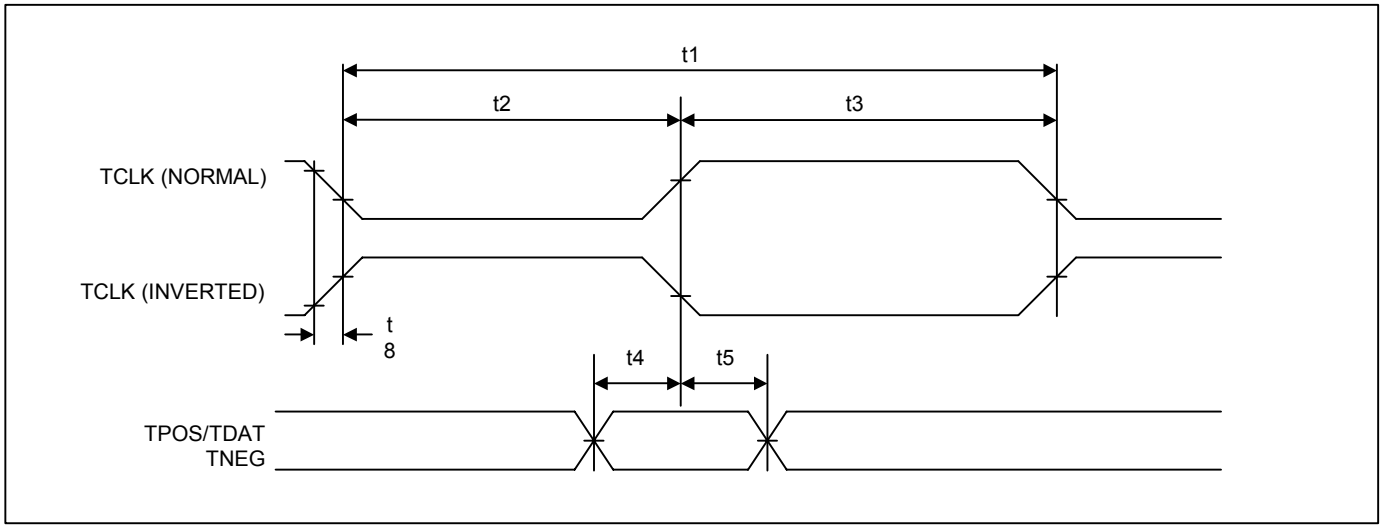


Figure 11-2. Receiver Framer Interface Timing Diagram

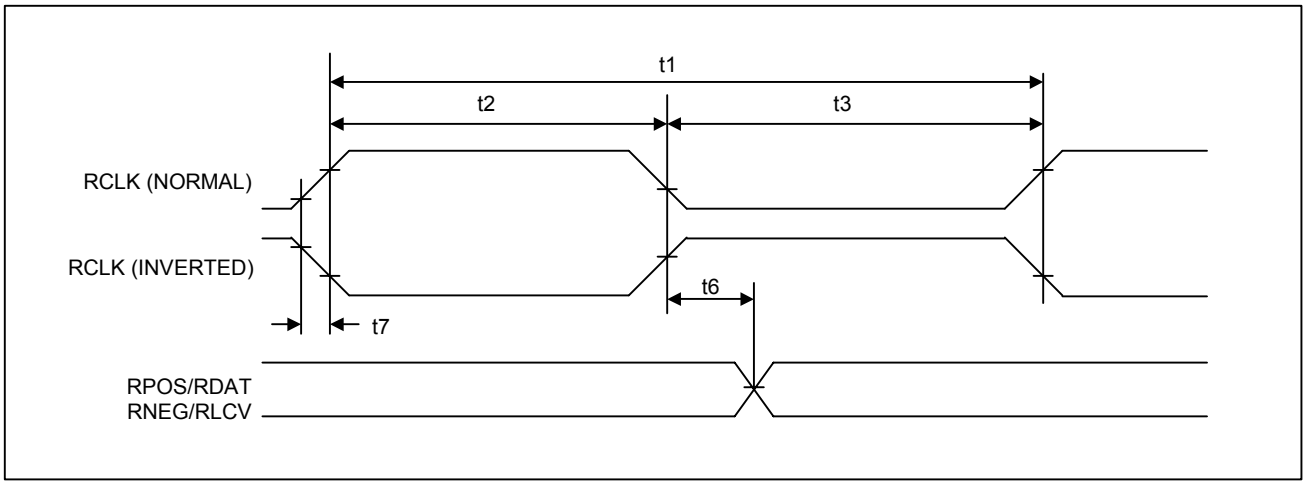


Table 11-4. Receiver Input Characteristics—DS3 and STS-1 Modes

(VDD18 = 1.8V ±5%, VDD33 = 3.3V ±5%, AVDD = 1.8V ±5%, T_A = -40°C to +85°C.)

PARAMETER	MIN	TYP	MAX	UNITS
Receive Sensitivity (Length of Cable)		1500		ft
Signal-to-Noise Ratio, Interfering Signal Test (Notes 1, 2)		10		
Input Pulse Amplitude, RMON = 0 (Notes 2, 3)			1000	mVpk
Input Pulse Amplitude, RMON = 1 (Note 2, 3)			200	mVpk
Analog LOS Declare, RMON = 0 (Note 4)		-23	-25	dB
Analog LOS Clear, RMON = 0 (Note 4)	-20	-22		dB
Analog LOS Declare, RMON = 1 (Note 4)		-37	-39	dB
Analog LOS Clear, RMON = 1 (Note 4)	-34	-36		dB
Intrinsic Jitter Generation (Note 2)		0.02		UI_{P-P}

Note 1: An interfering signal (2^{15} - 1 PRBS, B3ZS encoded, compliant waveshape, nominal bit rate) is added to the input signal. The combined signal is passed through 0 to 900 feet of coaxial cable and presented to the DS325xx receiver. This spec indicates the lowest signal-to-noise ratio that results in a bit error ratio $\leq 10^{-9}$.

Note 2: Not tested during production test.

Note 3: Measured on the line side (i.e., the BNC connector side) of the 1:1 receive transformer (See Figure 4-1). During measurement, incoming data traffic is unframed 2^{15} - 1 PRBS.

Note 4: With respect to nominal 800mVpk signal.

Table 11-5. Receiver Input Characteristics—E3 Mode

(VDD18 = 1.8V ±5%, VDD33 = 3.3V ±5%, AVDD = 1.8V ±5%, T_A = -40°C to +85°C.)

PARAMETER	MIN	TYP	MAX	UNITS
Receive Sensitivity (Length of Cable)	900	1200	1500	ft
Signal-to-Noise Ratio, Interfering Signal Test (Notes 1, 2)		12		
Input Pulse Amplitude, RMON = 0 (Notes 2, 3)			1300	mVpk
Input Pulse Amplitude, RMON = 1 (Notes 2, 3)			260	mVpk
Analog LOS Declare, RMON = 0 (Note 4)			-24	dB
Analog LOS Clear, RMON = 0 (Note 4)	-18			dB
Analog LOS Declare, RMON = 1 (Note 4)			-44	dB
Analog LOS Clear, RMON = 1 (Note 4)	-38			dB
Intrinsic Jitter Generation (Note 2)		0.03		UI_{P-P}

Note 1: An interfering signal (2^{23} - 1 PRBS, HDB3 encoded, compliant waveshape, nominal bit rate) is added to the input signal. The combined signal is passed through 0 to 900 feet of coaxial cable and presented to the DS325xx receiver. This spec indicates the lowest signal-to-noise ratio that results in a bit error ratio $\leq 10^{-9}$.

Note 2: Not tested during production test.

Note 3: Measured on the line side (i.e., the BNC connector side) of the 1:1 receive transformer (See Figure 4-1). During measurement, incoming data traffic is unframed 2^{23} - 1 PRBS.

Note 4: With respect to nominal 1000mVpk signal.

Table 11-6. Transmitter Output Characteristics—DS3 and STS-1 Modes

(VDD18 = 1.8V ±5%, VDD33 = 3.3V ±5%, AVDD = 1.8V ±5%, T_A = -40°C to +85°C.)

PARAMETER	MIN	TYP	MAX	UNITS
DS3 Output Pulse Amplitude, TLBO = 0 (Note 1)	700	800	900	mVpk
DS3 Output Pulse Amplitude, TLBO = 1 (Note 1)	500	600	700	mVpk
STS-1 Output Pulse Amplitude, TLBO = 0 (Note 1)	700	800	900	mVpk
STS-1 Output Pulse Amplitude, TLBO = 1 (Note 1)	500	600	700	mVpk
Ratio of Positive and Negative Pulse-Peak Amplitudes	0.9	1.0	1.1	
DS3 Power Level at 22.368MHz (Note 2)	-1.8		+5.7	dBm
DS3 Power Level at 44.736MHz vs. Power Level at 22.368MHz (Note 2)			-20	dB
Transmit Driver Monitor Minimum Threshold (V_{TXMIN}), TLBO = 0		680		mVpk
Transmit Driver Monitor Minimum Threshold (V_{TXMIN}), TLBO = 1		480		mVpk
Transmit Driver Monitor Maximum Threshold (V_{TXMAX}), TLBO = 0		920		mVpk
Transmit Driver Monitor Maximum Threshold (V_{TXMAX}), TLBO = 1		720		mVpk

Note 1: Measured on the line side (i.e., the BNC connector side) of the 1:1 transmit transformer (Figure 4-1).

Note 2: Unframed all-ones output signal, 3kHz bandwidth.

Table 11-7. Transmitter Output Characteristics—E3 Mode

(VDD18 = 1.8V ±5%, VDD33 = 3.3V ±5%, AVDD = 1.8V ±5%, T_A = -40°C to +85°C.)

PARAMETER	MIN	TYP	MAX	UNITS
Output Pulse Amplitude (Note 1)	900	1000	1100	mVpk
Pulse Width (Note 1)		14.55		ns
Positive/Negative Pulse Amplitude Ratio (at Centers of Pulses) (Note 1)	0.95	1.00	1.05	
Positive/Negative Pulse Width Ratio (at Nominal Half Amplitude)	0.95	1.00	1.05	
Transmit Driver Monitor Minimum Threshold (V_{TXMIN})		880		mVpk
Transmit Driver Monitor Maximum Threshold (V_{TXMAX})		1120		mVpk

Note 1: Measured on the line side (i.e., the BNC connector side) of the 1:1 transmit transformer (Figure 4-1).

Table 11-8. Parallel CPU Interface Timing

(VDD18 = 1.8V ±5%, VDD33 = 3.3V ±5%, AVDD = 1.8V ±5%, T_A = -40°C to +85°C.)
(See Figure 11-3, Figure 11-4, Figure 11-5, Figure 11-6, Figure 11-7, Figure 11-8, Figure 11-9, and Figure 11-10.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Setup Time for A[10:0] Valid to $\overline{RD}$, $\overline{WR}$, or $\overline{DS}$ Active (Notes 1, 2)	t1	0			ns
Setup Time for $\overline{CS}$ Active to $\overline{RD}$, $\overline{WR}$, or $\overline{DS}$ Active	t2	0			ns
Delay Time from $\overline{RD}$ or $\overline{DS}$ Active to D[15:0] Valid Without RDY/$\overline{ACK}$ Handshake	t3a			65	ns
Delay Time from RDY or ACK Active to D[15:0] Valid	t3b			20	ns
Hold Time from $\overline{RD}$, $\overline{WR}$, or $\overline{DS}$ Inactive to $\overline{CS}$ Inactive	t4	0			ns
Delay from $\overline{CS}$, $\overline{RD}$, or $\overline{DS}$ Inactive to D[15:0] Invalid (Note 3)	t5	2			ns
Wait Time from $\overline{WR}$ or $\overline{DS}$ Active to Latch D[15:0] Without RDY/$\overline{ACK}$ Handshake	t6a	65			ns
Wait Time from RDY or ACK Active to Latch D[15:0]	t6b	20			ns
D[15:0] Setup Time to $\overline{WR}$ or $\overline{DS}$ Inactive	t7	10			ns
D[15:0] Hold Time from $\overline{WR}$ or $\overline{DS}$ Inactive	t8	2			ns
A[10:0] Hold Time from $\overline{WR}$, $\overline{RD}$, or $\overline{DS}$ Inactive	t9a	5			ns
Delay from $\overline{WR}$, $\overline{RD}$, or $\overline{DS}$ Inactive to ALE Active	t9b	20			ns
$\overline{RD}$, $\overline{WR}$, or $\overline{DS}$ Inactive Time	t10	75			ns
Muxed Address Valid to ALE Inactive (Note 4)	t11	10			ns
Muxed Address Hold Time from ALE Inactive (Note 4)	t12	10			ns
ALE Pulse Width (Note 4)	t13	20			ns
Setup Time for ALE High or Muxed Address Valid to $\overline{CS}$ Active (Notes 4, 5, 6)	t14	0			ns
Delay from $\overline{CS}$ Inactive to D[15:0] Disable	t15			15	ns
Delay from $\overline{CS}$ Active to RDY/$\overline{ACK}$ Enable	t16			15	ns
Delay from $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, or $\overline{DS}$ Inactive to RDY/$\overline{ACK}$ Inactive (Note 7)	t17	2			ns
Delay from $\overline{CS}$ Inactive to RDY/$\overline{ACK}$ Disable	t18			15	ns

Note 1: D[15:0] loaded with 50pF when tested as outputs.

Note 2: If a gapped clock is applied on TCLK and local loopback is enabled, read cycle time must be extended by the length of the largest TCLK gap.

Note 3: Not tested during production test.

Note 4: In nonmultiplexed bus applications (Figure 11-3 to Figure 11-6), ALE should be wired high. In multiplexed bus applications (Figure 11-7 to Figure 11-10), A[10:0] should be wired to D[15:0] and the falling edge of ALE latches the address.

Note 5: t14 starts at the occurrence of the rising edge of ALE or A[10:0] valid whichever occurs later.

Note 6: In order to avoid bus contention, during a read cycle A[10:0] should be disabled prior to $\overline{RD}$ or $\overline{DS}$ being active.

Note 7: RDY/ACK may be disabled (t18) before going inactive (t17).

Figure 11-3. Parallel CPU Interface Intel Read Timing Diagram (Nonmultiplexed)

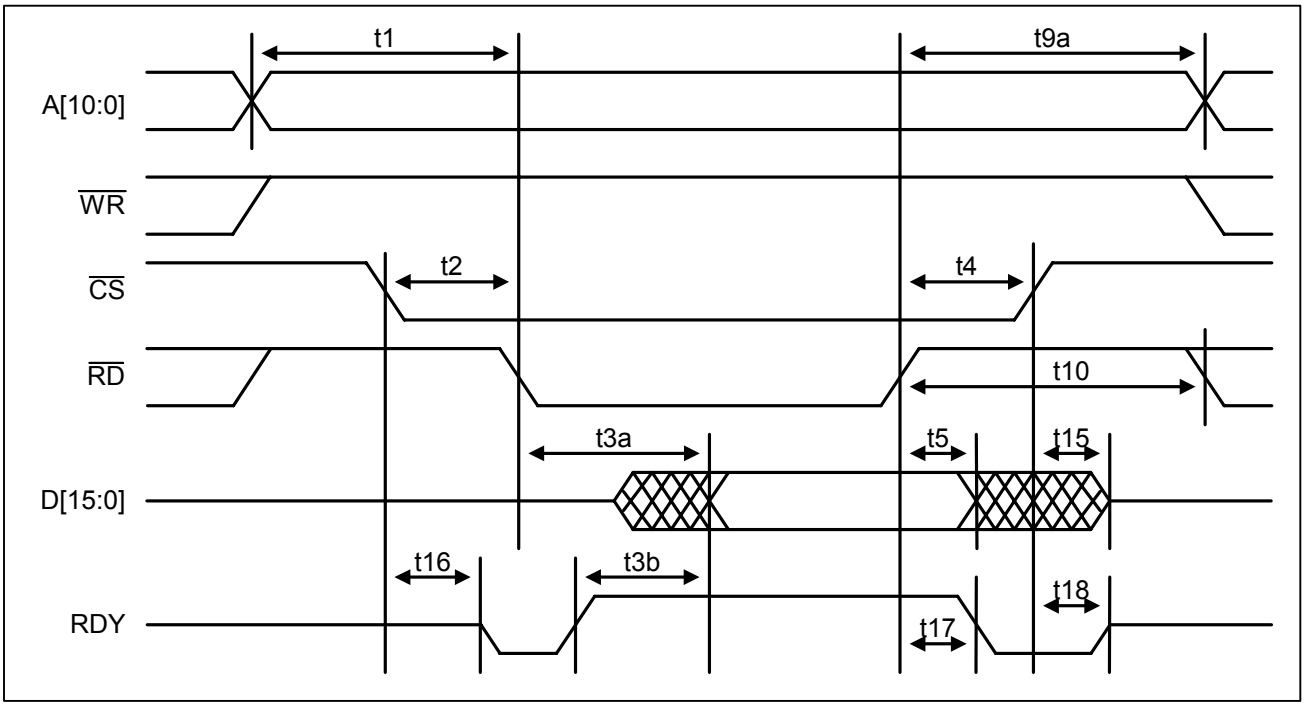


Figure 11-4. Parallel CPU Interface Intel Write Timing Diagram (Nonmultiplexed)

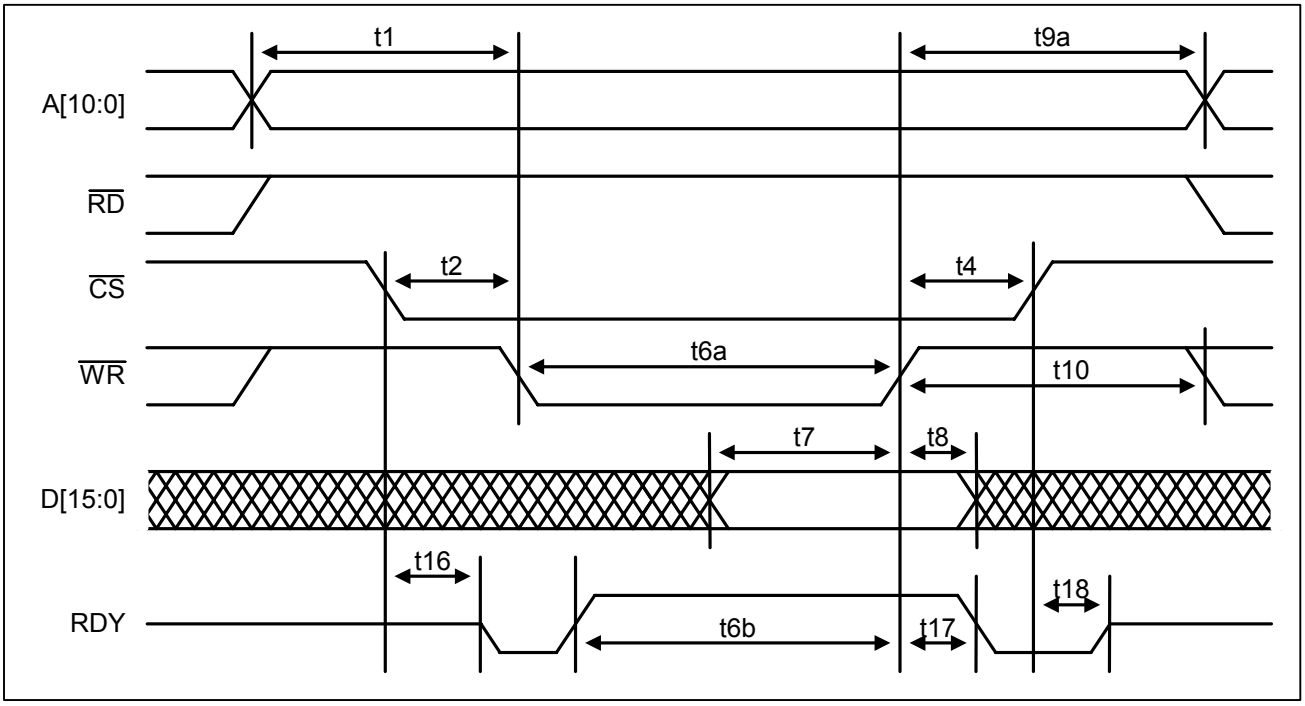


Figure 11-5. Parallel CPU Interface Motorola Read Timing Diagram (Nonmultiplexed)

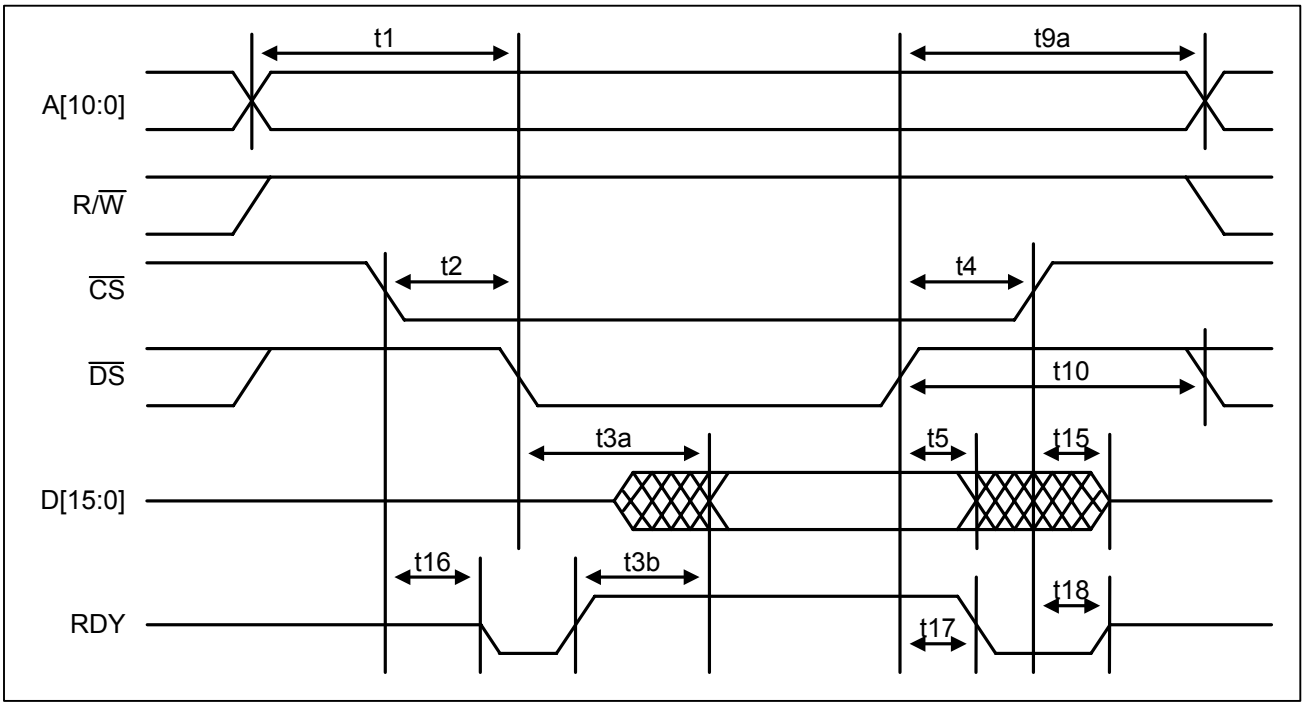


Figure 11-6. Parallel CPU Interface Motorola Write Timing Diagram (Nonmultiplexed)

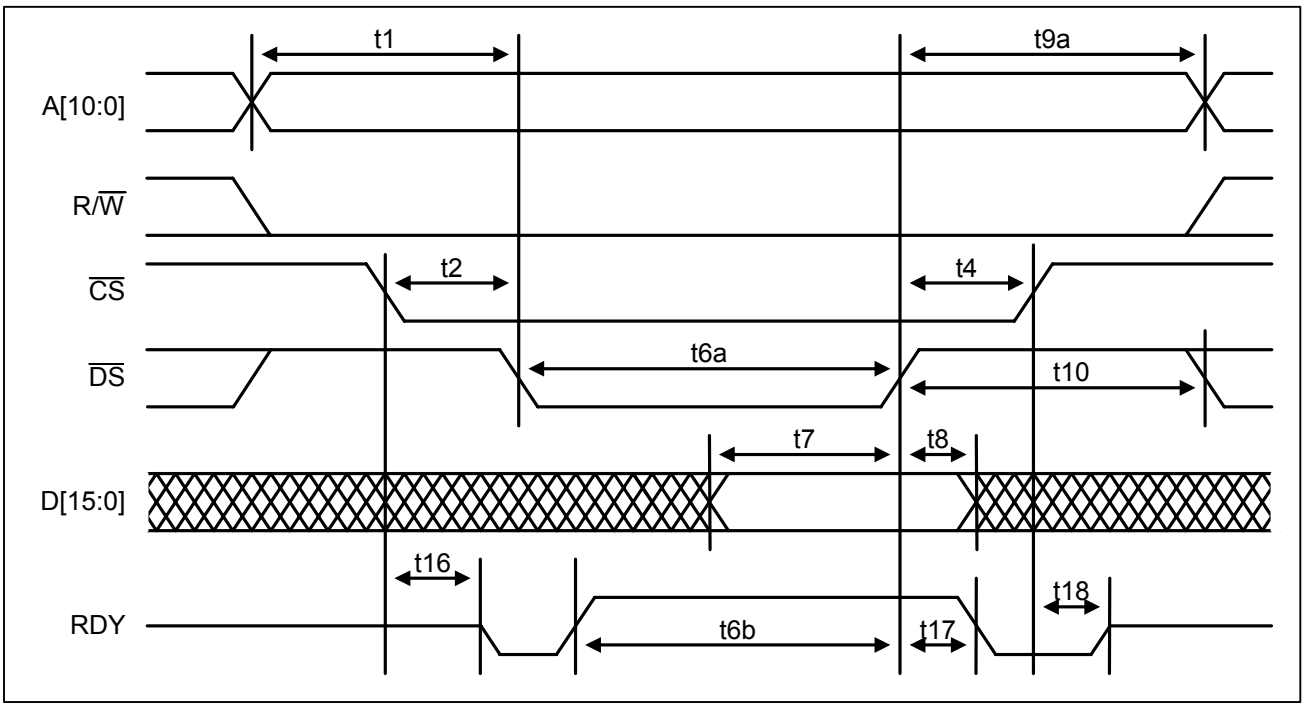


Figure 11-7. Parallel CPU Interface Intel Read Timing Diagram (Multiplexed)

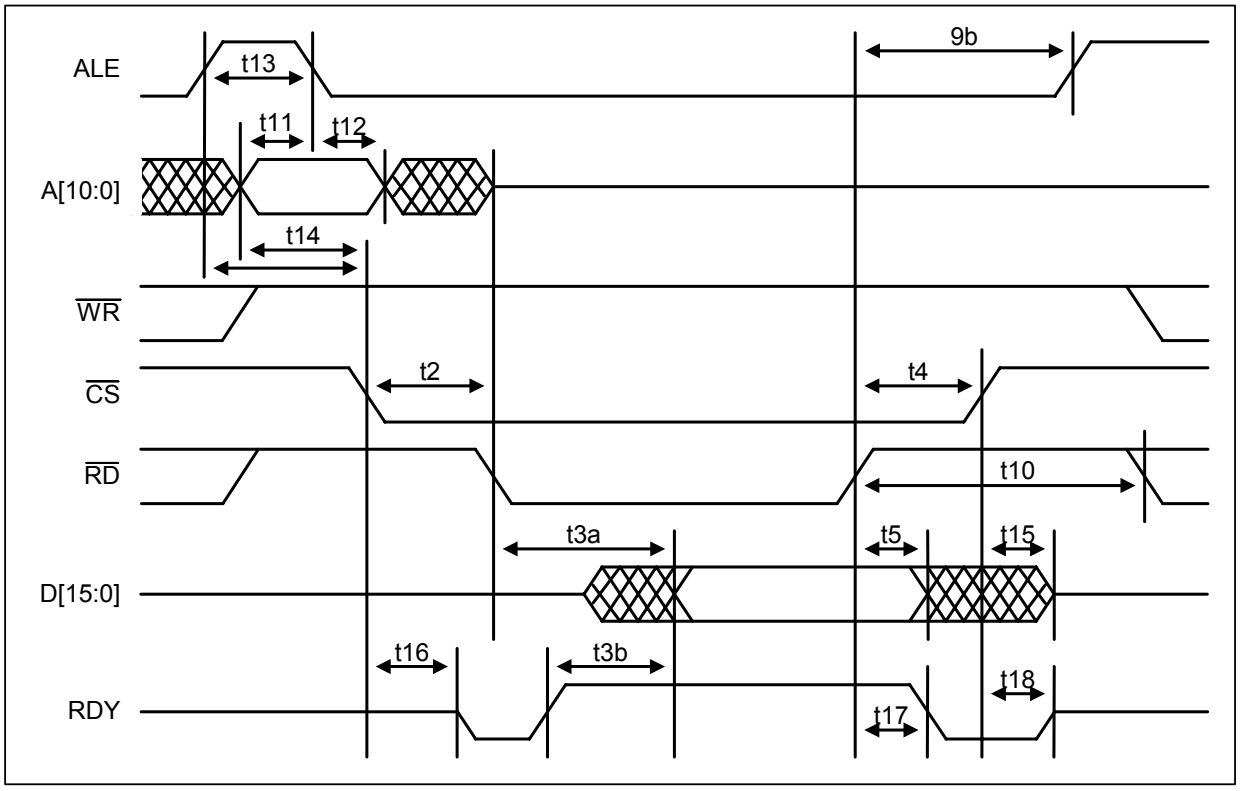


Figure 11-8. Parallel CPU Interface Intel Write Timing Diagram (Multiplexed)

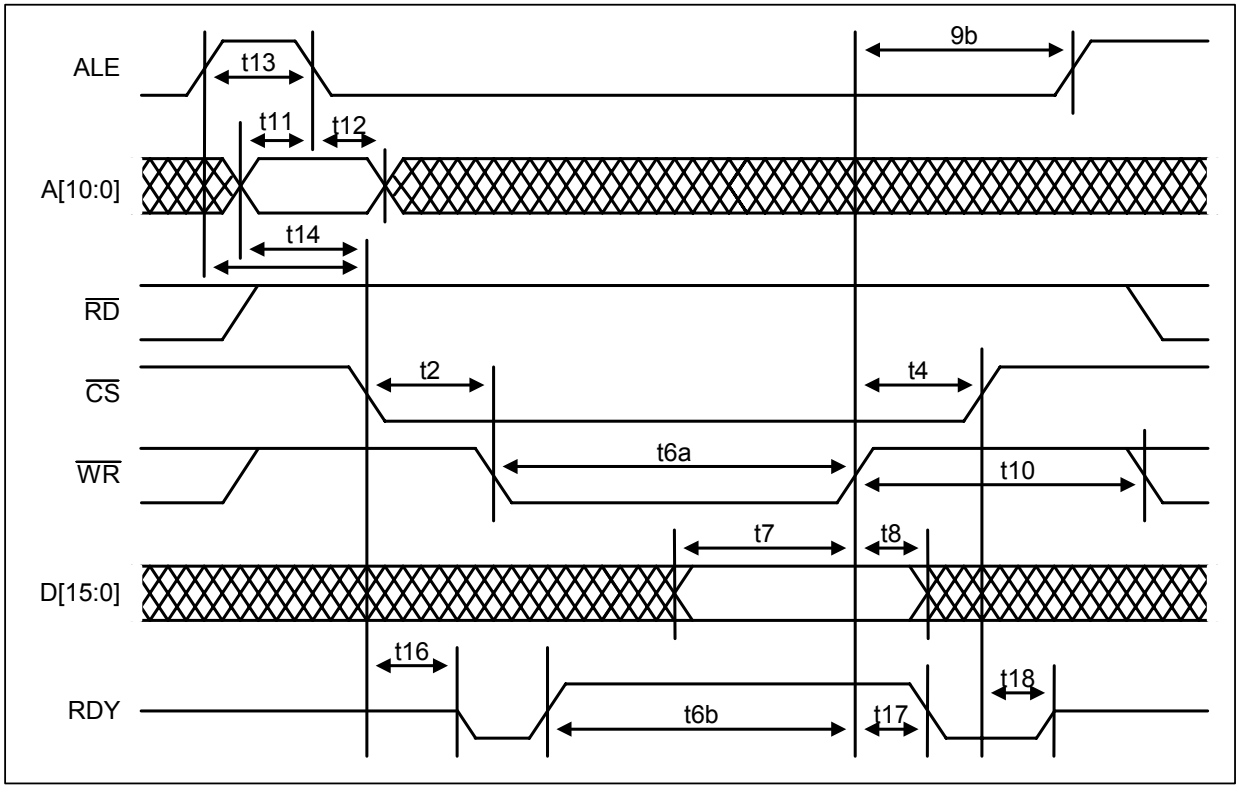


Figure 11-9. Parallel CPU Interface Motorola Read Timing Diagram (Multiplexed)

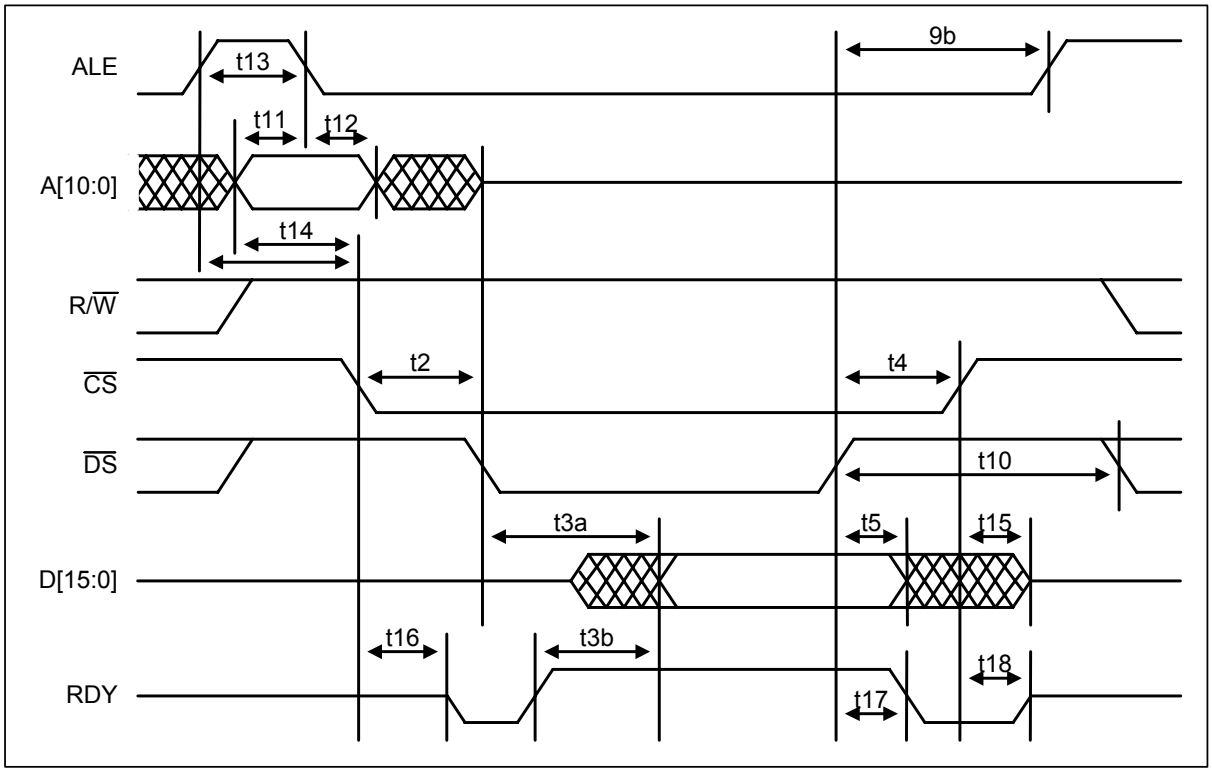


Figure 11-10. Parallel CPU Interface Motorola Write Timing Diagram (Multiplexed)

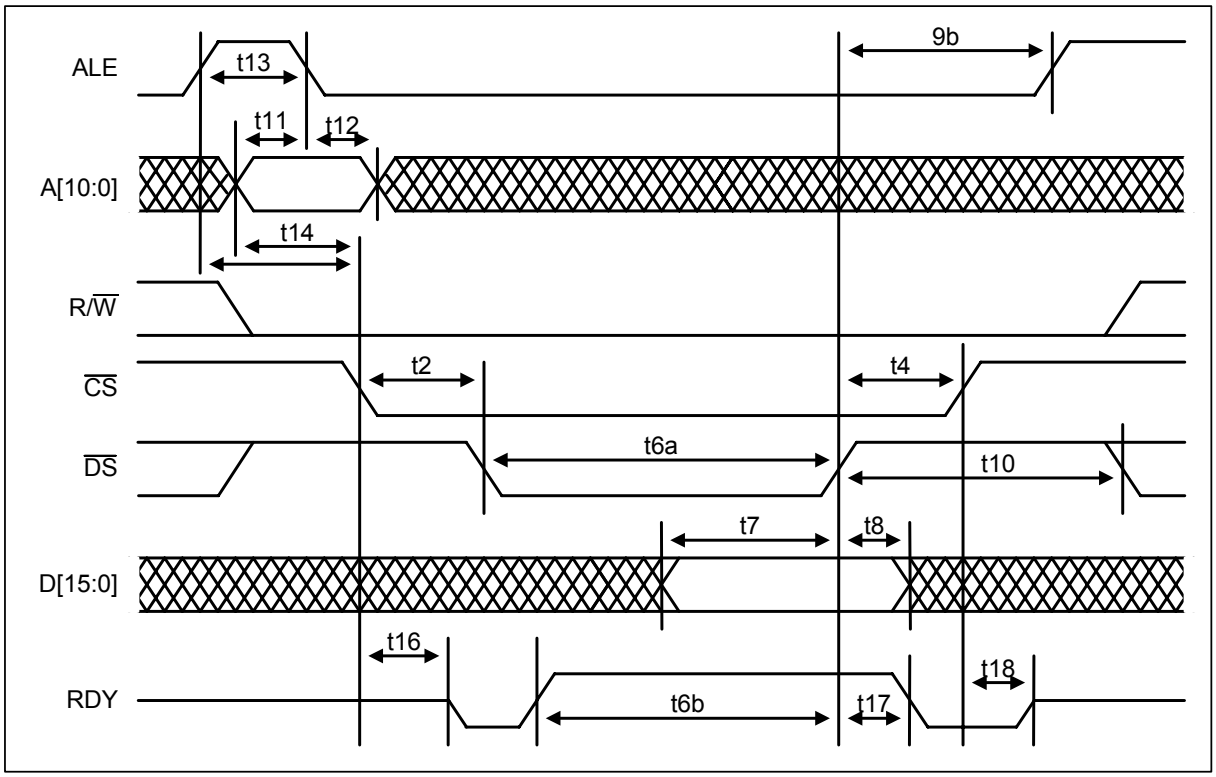


Table 11-9. SPI Interface Timing

(VDD18 = 1.8V ±5%, VDD33 = 3.3V ±5%, AVDD = 1.8V ±5%, T_A = -40°C to +85°C.)
(See Figure 11-11.) (Note 1)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
SCLK Frequency	f_{BUS}			10	MHz
SCLK Cycle Time	t_{CYC}	100			ns
$\overline{CS}$ Setup to First SCLK Edge	t_{SUC}	15			ns
$\overline{CS}$ Hold Time After Last SCLK Edge	t_{HDC}	15			ns
SCLK High Time	t_{CLKH}	50			ns
SCLK Low Time	t_{CLKL}	50			ns
SDI Data Setup Time	t_{SUI}	5			ns
SDI Data Hold Time	t_{HDI}	15			ns
SDO Enable Time (High Impedance to Output Active)	t_{EN}	0			ns
SDO Disable Time (Output Active to High Impedance)	t_{DIS}			25	ns
SDO Data Valid Time	t_{DV}			40	ns
SDO Data Hold Time After Update SCLK Edge	t_{HDO}	5			ns

Note 1: All timing is specified with 100 pF load on all SPI pins.

Figure 11-11. SPI Interface Timing Diagram

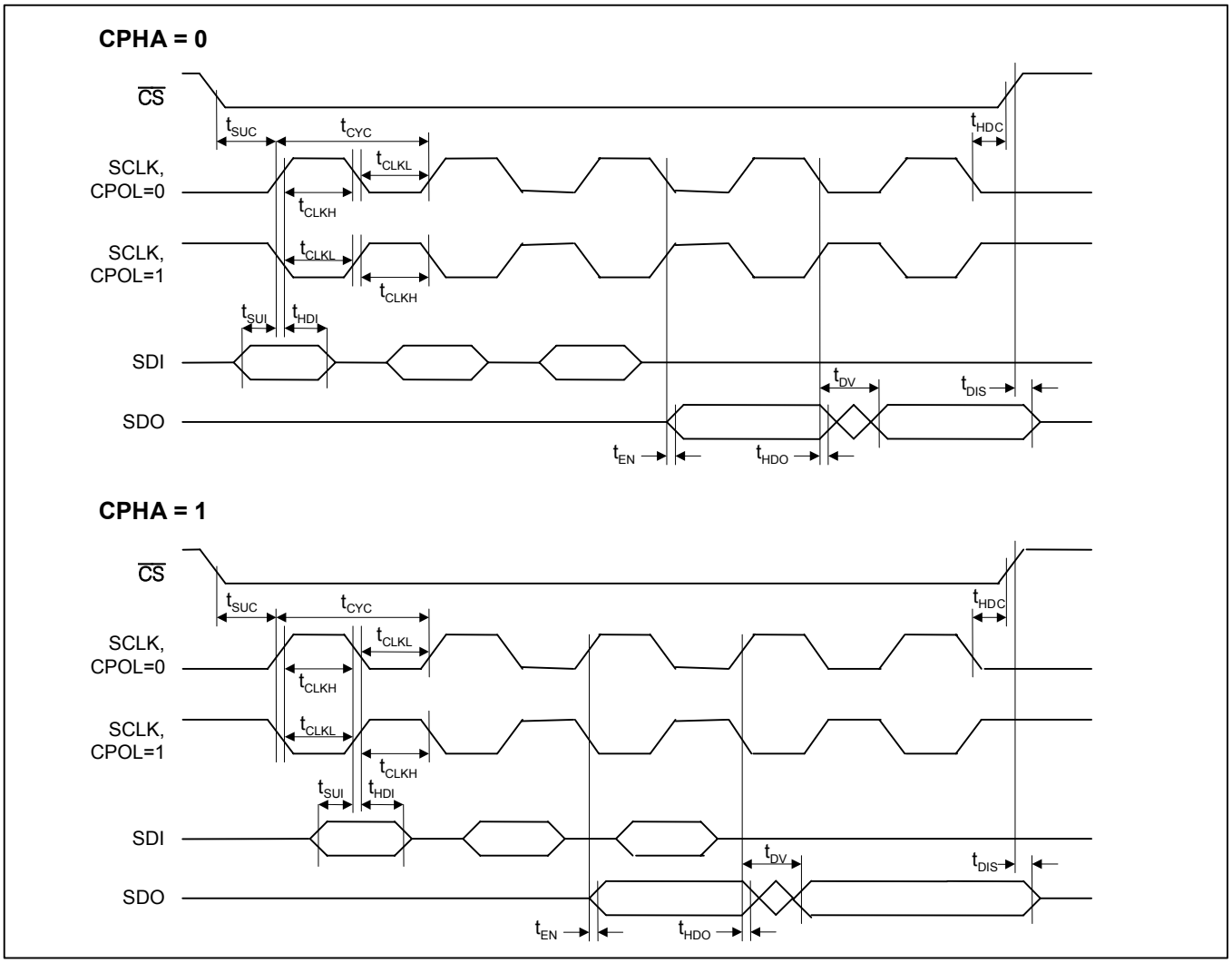


Table 11-10. JTAG Interface Timing

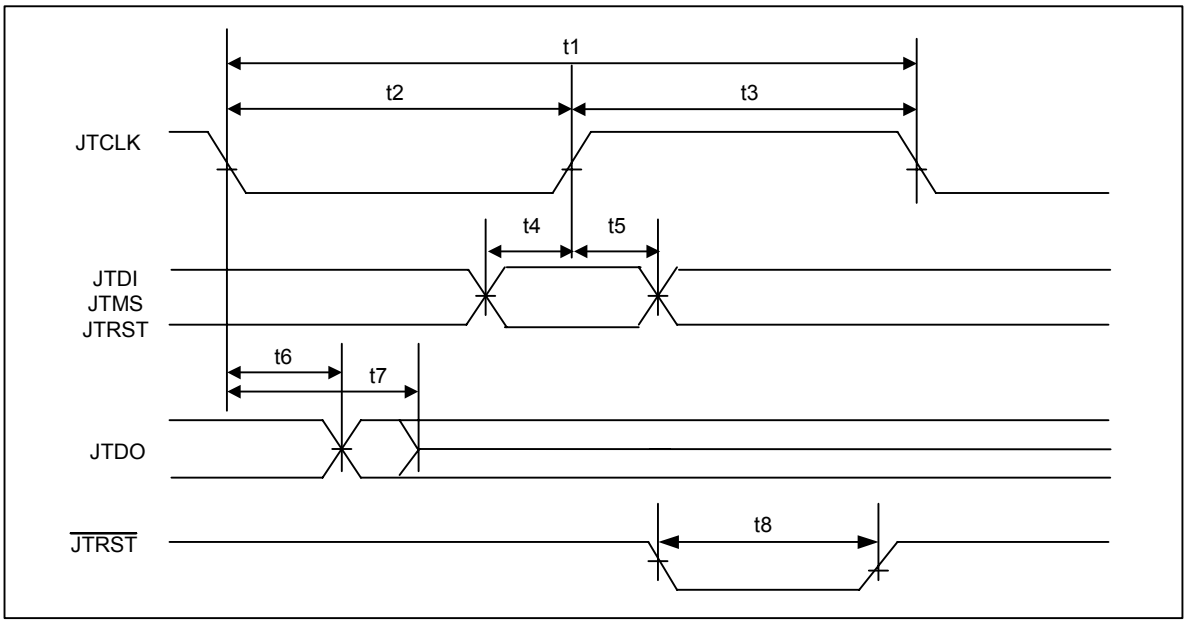
(VDD18 = 1.8V ±5%, VDD33 = 3.3V ±5%, AVDD = 1.8V ±5%, T_A = -40°C to +85°C.)
(See Figure 11-12.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
JTCLK Clock Period	t1		1000		ns
JTCLK Clock High/Low Time (Note 1)	t2/t3	50	500		ns
JTCLK to JTDI, JTMS Setup Time	t4	50			ns
JTCLK to JTDI, JTMS Hold Time	t5	50			ns
JTCLK to JTDO Delay	t6	2		50	ns
JTCLK to JTDO High-Z Delay (Note 2)	t7	2		50	ns
$\overline{\text{JTRST}}$ Width Low Time	t8	100			ns

Note 1: Clock can be stopped high or low.

Note 2: Not tested during production test.

Figure 11-12. JTAG Timing Diagram



12. PIN ASSIGNMENTS

Table 12-1. Pin Assignments Sorted by Signal Name for DS32506/DS32508/DS32512

SIGNAL	BALL	SIGNAL	BALL	SIGNAL	BALL	SIGNAL	BALL
A0	V5	RCLK8	N16	TCC	C6	TVSS4	P6
A1/LB5[1]	T8	RCLK9	H11	TCLK1	L16	TVSS4	U3
A2/LB6[1]	W5	RCLK10	T20	TCLK2	R22	TVSS4	V1
A3/LB7[1]	R9	RCLK11	G18	TCLK3	K18	TVSS5	C9
A4/LB8[1]	Y4	RCLK12	R18	TCLK4	M17	TVSS5	E9
A5/LB9[1]	P9	RCLKI	A3	TCLK5	J18	TVSS5	F10
A6/LB10[1]	AA3	$\overline{RD}/\overline{DS}$	R11	TCLK6	T21	TVSS6	U10
A7/LB11[1]	T9	RDY/$\overline{ACK}$	U8	TCLK7	G21	TVSS6	V8
A8/LB12[1]	AB2	REFCLK	L22	TCLK8	P17	TVSS6	V9
A9/ITRE	R10	RESREF	L2	TCLK9	H15	TVSS7	C12
A10	W6	RLOS1	K19	TCLK10	U20	TVSS7	D11
AIST	E7	RLOS2	P22	TCLK11	E20	TVSS7	F12
ALE	T10	RLOS3	F22	TCLK12	T17	TVSS8	T12
CLADBYP	G7	RLOS4	V22	TCLKI	C5	TVSS8	V12
CLKA	M21	RLOS5	H19	TDM1	K21	TVSS8	Y12
CLKB	M22	RLOS6	M14	TDM2	P21	TVSS9	D14
CLKC	M19	RLOS7	H16	TDM3	K15	TVSS9	E15
CLKD	M20	RLOS8	W21	TDM4	P19	TVSS9	F14
$\overline{CS}$	Y5	RLOS9	D20	TDM5	J20	TVSS10	U14
CVDD	L18	RLOS10	P14	TDM6	N17	TVSS10	V15
CVDD	L19	RLOS11	H9	TDM7	H14	TVSS10	Y16
CVSS	L20	RLOS12	R13	TDM8	Y21	TVSS11	C18
D0/LB1[0]/SDO	T5	RMON1	L6	TDM9	B22	TVSS11	C19
D1/LB2[0]/SDI	T6	RMON2	R4	TDM10	U19	TVSS11	F16
D2/LB3[0]/SCLK	R5	RMON3	F2	TDM11	H10	TVSS12	U16
D3/LB4[0]	R6	RMON4	AA1	TDM12	T16	TVSS12	V18
D4/LB5[0]	T7	RMON5	D8	$\overline{TEST}$	E4	TVSS12	Y20
D5/LB6[0]	R7	RMON6	V10	TLBO1	L7	TXN1	J1
D6/LB7[0]/CPHA	V4	RMON7	A10	TLBO2	M9	TXN1	J2
D7/LB8[0]/CPOL	P7	RMON8	V13	TLBO3	K8	TXN2	P1
D8/LB9[0]	U5	RMON9	B14	TLBO4	N5	TXN2	P2
D9/LB10[0]	W4	RMON10	W16	TLBO5	D10	TXN3	D1
D10/LB11[0]	Y3	RMON11	A18	TLBO6	Y7	TXN3	D2
D11/LB12[0]	N8	RMON12	W19	TLBO7	E13	TXN4	W1
D12/LB1[1]	AA2	RNEG1	K17	TLBO8	AB10	TXN4	W2
D13/LB1[2]	P8	RNEG2	N21	TLBO9	D16	TXN5	A7
D14/LB1[3]	AB1	RNEG3	E22	TLBO10	AA14	TXN5	B7
D15/LB1[4]	R8	RNEG4	L14	TLBO11	F17	TXN6	AA8
GPIOA1/LM1[1]	J5	RNEG5	J17	TLBO12	T14	TXN6	AB8
GPIOA2/LM2[1]	M7	RNEG6	Y22	TNEG1	J22	TXN7	A12

SIGNAL	BALL	SIGNAL	BALL	SIGNAL	BALL	SIGNAL	BALL
GPIOA3/LM3[1]	J7	RNEG7	H18	TNEG2	M18	TXN7	B12
GPIOA4/LM4[1]	N6	RNEG8	N15	TNEG3	K20	TXN8	AA12
GPIOA5/LM5[1]	F8	RNEG9	H12	TNEG4	W22	TXN8	AB12
GPIOA6/LM6[1]	U11	RNEG10	W20	TNEG5	J19	TXN9	A16
GPIOA7/LM7[1]	F11	RNEG11	G17	TNEG6	V21	TXN9	B16
GPIOA8/LM8[1]	U13	RNEG12	R17	TNEG7	E21	TXN10	AA16
GPIOA9/LM9[1]	F13	RPD	B3	TNEG8	AA22	TXN10	AB16
GPIOA10/LM10[1]	Y14	RPOS1	J21	TNEG9	C21	TXN11	A20
GPIOA11/LM11[1]	F15	RPOS2	L17	TNEG10	R15	TXN11	B20
GPIOA12/LM12[1]	Y18	RPOS3	J15	TNEG11	F19	TXN12	AA20
GPIOB1/LM1[0]	G2	RPOS4	U22	TNEG12	T18	TXN12	AB20
GPIOB2/LM2[0]	M4	RPOS5	H20	TOE1	K22	TXP1	H1
GPIOB3/LM3[0]	G5	RPOS6	P20	TOE2	T22	TXP1	H2
GPIOB4/LM4[0]	T1	RPOS7	H17	TOE3	G22	TXP2	N1
GPIOB5/LM5[0]	E8	RPOS8	R20	TOE4	M16	TXP2	N2
GPIOB6/LM6[0]	Y10	RPOS9	F18	TOE5	C22	TXP3	C1
GPIOB7/LM7[0]	B10	RPOS10	T19	TOE6	R19	TXP3	C2
GPIOB8/LM8[0]	AB14	RPOS11	G16	TOE7	F21	TXP4	U1
GPIOB9/LM9[0]	A14	RPOS12	R16	TOE8	P16	TXP4	U2
GPIOB10/LM10[0]	R12	$\overline{\text{RST}}$	C3	TOE9	D21	TXP5	A8
GPIOB11/LM11[0]	B18	RVDD1	L4	TOE10	V19	TXP5	B8
GPIOB12/LM12[0]	U15	RVDD2	P3	TOE11	F20	TXP6	AA7
$\overline{\text{HIZ}}$	J8	RVDD3	G4	TOE12	U17	TXP6	AB7
HW	B1	RVDD4	V3	TPD	D6	TXP7	A13
IFSEL0	U9	RVDD5	C8	TPOS1	L15	TXP7	B13
IFSEL1	Y6	RVDD6	Y9	TPOS2	N19	TXP8	AA11
IFSEL2	W7	RVDD7	C11	TPOS3	H21	TXP8	AB11
$\overline{\text{INT}}$	AB3	RVDD8	Y13	TPOS4	M15	TXP9	A17
JAD0	G8	RVDD9	E14	TPOS5	J16	TXP9	B17
JAD1	C4	RVDD10	V16	TPOS6	U21	TXP10	AA15
JAS0	F7	RVDD11	D17	TPOS7	G20	TXP10	AB15
JAS1	E5	RVDD12	U18	TPOS8	P15	TXP11	A21
JTCLK	D4	RVSS1	L1	TPOS9	H13	TXP11	B21
JTDI	D3	RVSS2	P5	TPOS10	V20	TXP12	AA19
JTDO	F6	RVSS3	F5	TPOS11	E19	TXP12	AB19
JTMS	H7	RVSS4	W3	TPOS12	R14	VDD18	C10
$\overline{\text{JTRST}}$	E3	RVSS5	C7	TVDD1	J3	VDD18	C17
JVDD1	H3	RVSS6	W10	TVDD1	K4	VDD18	G1
JVDD2	M1	RVSS7	E11	TVDD1	K5	VDD18	H22
JVDD3	A1	RVSS8	W13	TVDD2	M3	VDD18	N20
JVDD4	T4	RVSS9	C14	TVDD2	M6	VDD18	T2
JVDD5	E10	RVSS10	Y17	TVDD2	N3	VDD18	AA10
JVDD6	AA6	RVSS11	E17	TVDD3	A2	VDD18	AA18
JVDD7	D13	RVSS12	AB22	TVDD3	F4	VDD33	J10

SIGNAL	BALL	SIGNAL	BALL	SIGNAL	BALL	SIGNAL	BALL
JVDD8	W11	RXN1	K1	TVDD3	K6	VDD33	J13
JVDD9	E16	RXN2	R2	TVDD4	N7	VDD33	K9
JVDD10	W14	RXN3	E1	TVDD4	U4	VDD33	K14
JVDD11	E18	RXN4	Y2	TVDD4	V2	VDD33	N9
JVDD12	V17	RXN5	B6	TVDD5	B9	VDD33	N14
JVSS1	H4	RXN6	AB9	TVDD5	D9	VDD33	P10
JVSS2	M2	RXN7	A11	TVDD5	F9	VDD33	P13
JVSS3	B2	RXN8	AB13	TVDD6	P11	VSS	A22
JVSS4	T3	RXN9	A15	TVDD6	V7	VSS	J6
JVSS5	A9	RXN10	AA17	TVDD6	Y8	VSS	J9
JVSS6	AB6	RXN11	A19	TVDD7	D12	VSS	J11
JVSS7	C13	RXN12	AA21	TVDD7	E12	VSS	J12
JVSS8	V11	RXP1	K2	TVDD7	G10	VSS	K7
JVSS9	C16	RXP2	R1	TVDD8	U12	VSS	K10
JVSS10	V14	RXP3	E2	TVDD8	W12	VSS	K11
JVSS11	D19	RXP4	Y1	TVDD8	Y11	VSS	K12
JVSS12	W17	RXP5	A6	TVDD9	C15	VSS	K13
LBS	H8	RXP6	AA9	TVDD9	D15	VSS	L5
MT0	L21	RXP7	B11	TVDD9	G12	VSS	L8
MT1	D5	RXP8	AA13	TVDD10	T13	VSS	L9
MT2	G6	RXP9	B15	TVDD10	W15	VSS	L10
MT3	AA4	RXP10	AB17	TVDD10	Y15	VSS	L11
MT4	AB4	RXP11	B19	TVDD11	C20	VSS	L12
MT5	A4	RXP12	AB21	TVDD11	D18	VSS	L13
MT6	B4	TAIS1	F1	TVDD11	G14	VSS	M10
MT7	AA5	TAIS2	L3	TVDD12	T15	VSS	M11
MT8	AB5	TAIS3	H6	TVDD12	W18	VSS	M12
MT9	A5	TAIS4	R3	TVDD12	Y19	VSS	M13
MT10	B5	TAIS5	G9	TVSS1	J4	VSS	N10
RBIN	E6	TAIS6	W8	TVSS1	K3	VSS	N11
RCLK1	K16	TAIS7	G11	TVSS1	M8	VSS	N12
RCLK2	N22	TAIS8	T11	TVSS2	M5	VSS	N13
RCLK3	D22	TAIS9	G13	TVSS2	N4	VSS	P18
RCLK4	N18	TAIS10	P12	TVSS2	P4	VSS	U6
RCLK5	J14	TAIS11	G15	TVSS3	F3	VSS	U7
RCLK6	R21	TAIS12	AB18	TVSS3	G3	VSS	W9
RCLK7	G19	TBIN	D7	TVSS3	H5	$\overline{WR}$/R/$\overline{W}$	V6

Note: *There are two TXP leads and two TXN leads for each LIU port. For best performance, the two TXP leads must be wired together and the two TXN leads must be wired together on each port.*

Figure 12-1. DS32512 Pin Assignment, Hardware and Microprocessor Interfaces

Left Half

	1	2	3	4	5	6	7	8	9	10	11
A	JVDD3	TVDD3	RCLKI	MT5	MT9	RXP5	TXN5	TXP5	JVSS5	RMON7	RXN7
B	HW	JVSS3	RPD	MT6	MT10	RXN5	TXN5	TXP5	TVDD5	GPIOB7	RXP7
C	TXP3	TXP3	$\overline{\text{RST}}$	JAD1	TCLKI	TCC	RVSS5	RVDD5	TVSS5	VDD18	RVDD7
D	TXN3	TXN3	JTDI	JTCLK	MT1	TPD	TBIN	RMON5	TVDD5	TLBO5	TVSS7
E	RXN3	RXP3	$\overline{\text{JTRST}}$	$\overline{\text{TEST}}$	JAS1	RBIN	AIST	GPIOB5	TVSS5	JVDD5	RVSS7
F	TAIS1	RMON3	TVSS3	TVDD3	RVSS3	JTDO	JAS0	GPIOA5	TVDD5	TVSS5	GPIOA7
G	VDD18	GPIOB1	TVSS3	RVDD3	GPIOB3	MT2	CLADBYP	JAD0	TAIS5	TVDD7	TAIS7
H	TXP1	TXP1	JVDD1	JVSS1	TVSS3	TAIS3	JTMS	LBS	RLOS11	TDM11	RCLK9
J	TXN1	TXN1	TVDD1	TVSS1	GPIOA1	VSS	GPIOA3	$\overline{\text{HIZ}}$	VSS	VDD33	VSS
K	RXN1	RXP1	TVSS1	TVDD1	TVDD1	TVDD3	VSS	TLBO3	VDD33	VSS	VSS
L	RVSS1	RESREF	TAIS2	RVDD1	VSS	RMON1	TLBO1	VSS	VSS	VSS	VSS
M	JVDD2	JVSS2	TVDD2	GPIOB2	TVSS2	TVDD2	GPIOA2	TVSS1	TLBO2	VSS	VSS
N	TXP2	TXP2	TVDD2	TVSS2	TLBO4	GPIOA4	TVDD4	D11	VDD33	VSS	VSS
P	TXN2	TXN2	RVDD2	TVSS2	RVSS2	TVSS4	D7/CPOL	D13	A5	VDD33	TVDD6
R	RXP2	RXN2	TAIS4	RMON2	D2/SCLK	D3	D5	D15	A3	A9	$\overline{\text{RD}}$/$\overline{\text{DS}}$
T	GPIOB4	VDD18	JVSS4	JVDD4	D0/SDO	D1/SDI	D4	A1	A7	ALE	TAIS8
U	TXP4	TXP4	TVSS4	TVDD4	D8	VSS	VSS	RDY/$\overline{\text{ACK}}$	IFSEL0	TVSS6	GPIOA6
V	TVSS4	TVDD4	RVDD4	D6/CPHA	A0	$\overline{\text{WR}}$/R/$\overline{\text{W}}$	TVDD6	TVSS6	TVSS6	RMON6	JVSS8
W	TXN4	TXN4	RVSS4	D9	A2	A10	IFSEL2	TAIS6	VSS	RVSS6	JVDD8
Y	RXP4	RXN4	D10	A4	$\overline{\text{CS}}$	IFSEL1	TLBO6	TVDD6	RVDD6	GPIOB6	TVDD8
AA	RMON4	D12	A6	MT3	MT7	JVDD6	TXP6	TXN6	RXP6	VDD18	TXP8
AB	D14	A8	$\overline{\text{INT}}$	MT4	MT8	JVSS6	TXP6	TXN6	RXN6	TLBO8	TXP8
	1	2	3	4	5	6	7	8	9	10	11

	High-Speed Analog		Low-Speed Analog
	High-Speed Digital		Low-Speed Digital
	N.C. and Manufacturing Test		VDD 1.8V
	VDDIO 3.3V		Analog VSS
	Analog VDD 1.8V		VSS

Right Half

12	13	14	15	16	17	18	19	20	21	22	
TXN7	TXP7	GPIOB9	RXN9	TXN9	TXP9	RMON11	RXN11	TXN11	TXP11	VSS	A
TXN7	TXP7	RMON9	RXP9	TXN9	TXP9	GPIOB11	RXP11	TXN11	TXP11	TDM9	B
TVSS7	JVSS7	RVSS9	TVDD9	JVSS9	VDD18	TVSS11	TVSS11	TVDD11	TNEG9	TOE5	C
TVDD7	JVDD7	TVSS9	TVDD9	TLBO9	RVDD11	TVDD11	JVSS11	RLOS9	TOE9	RCLK3	D
TVDD7	TLBO7	RVDD9	TVSS9	JVDD9	RVSS11	JVDD11	TPOS11	TCLK11	TNEG7	RNEG3	E
TVSS7	GPIOA9	TVSS9	GPIOA11	TVSS11	TLBO11	RPOS9	TNEG11	TOE11	TOE7	RLOS3	F
TVDD9	TAIS9	TVDD11	TAIS11	RPOS11	RNEG11	RCLK11	RCLK7	TPOS7	TCLK7	TOE3	G
RNEG9	TPOS9	TDM7	TCLK9	RLOS7	RPOS7	RNEG7	RLOS5	RPOS5	TPOS3	VDD18	H
VSS	VDD33	RCLK5	RPOS3	TPOS5	RNEG5	TCLK5	TNEG5	TDM5	RPOS1	TNEG1	J
VSS	VSS	VDD33	TDM3	RCLK1	RNEG1	TCLK3	RLOS1	TNEG3	TDM1	TOE1	K
VSS	VSS	RNEG4	TPOS1	TCLK1	RPOS2	CVDD	CVDD	CVSS	MT0	REFCLK	L
VSS	VSS	RLOS6	TPOS4	TOE4	TCLK4	TNEG2	CLKC	CLKD	CLKA	CLKB	M
VSS	VSS	VDD33	RNEG8	RCLK8	TDM6	RCLK4	TPOS2	VDD18	RNEG2	RCLK2	N
TAIS10	VDD33	RLOS10	TPOS8	TOE8	TCLK8	VSS	TDM4	RPOS6	TDM2	RLOS2	P
GPIOB10	RLOS12	TPOS12	TNEG10	RPOS12	RNEG12	RCLK12	TOE6	RPOS8	RCLK6	TCLK2	R
TVSS8	TVDD10	TLBO12	TVDD12	TDM12	TCLK12	TNEG12	RPOS10	RCLK10	TCLK6	TOE2	T
TVDD8	GPIOA8	TVSS10	GPIOB12	TVSS12	TOE12	RVDD12	TDM10	TCLK10	TPOS6	RPOS4	U
TVSS8	RMON8	JVSS10	TVSS10	RVDD10	JVDD12	TVSS12	TOE10	TPOS10	TNEG6	RLOS4	V
TVDD8	RVSS8	JVDD10	TVDD10	RMON10	JVSS12	TVDD12	RMON12	RNEG10	RLOS8	TNEG4	W
TVSS8	RVDD8	GPIOA10	TVDD10	TVSS10	RVSS10	GPIOA12	TVDD12	TVSS12	TDM8	RNEG6	Y
TXN8	RXP8	TLBO10	TXP10	TXN10	RXN10	VDD18	TXP12	TXN12	RXN12	TNEG8	AA
TXN8	RXN8	GPIOB8	TXP10	TXN10	RXP10	TAIS12	TXP12	TXN12	RXP12	RVSS12	AB
12	13	14	15	16	17	18	19	20	21	22	

	High-Speed Analog		Low-Speed Analog
	High-Speed Digital		Low-Speed Digital
	N.C. and Manufacturing Test		VDD 1.8V
	VDDIO 3.3V		Analog VSS
	Analog VDD 1.8V		VSS

Figure 12-2. DS32512 Pin Assignment, Hardware Interface Only

Left Half

	1	2	3	4	5	6	7	8	9	10	11
A	JVDD3	TVDD3	RCLKI	MT5	MT9	RXP5	TXN5	TXP5	JVSS5	RMON7	RXN7
B	HW	JVSS3	RPD	MT6	MT10	RXN5	TXN5	TXP5	TVDD5	LM7[0]	RXP7
C	TXP3	TXP3	$\overline{\text{RST}}$	JAD1	TCLKI	TCC	RVSS5	RVDD5	TVSS5	VDD18	RVDD7
D	TXN3	TXN3	JTDI	JTCLK	MT1	TPD	TBIN	RMON5	TVDD5	TLBO5	TVSS7
E	RXN3	RXP3	$\overline{\text{JTRST}}$	$\overline{\text{TEST}}$	JAS1	RBIN	AIST	LM5[0]	TVSS5	JVDD5	RVSS7
F	TAIS1	RMON3	TVSS3	TVDD3	RVSS3	JTDO	JAS0	LM5[1]	TVDD5	TVSS5	LM7[1]
G	VDD18	LM1[0]	TVSS3	RVDD3	LM3[0]	MT2	CLADBYP	JAD0	TAIS5	TVDD7	TAIS7
H	TXP1	TXP1	JVDD1	JVSS1	TVSS3	TAIS3	JTMS	LBS	RLOS11	TDM11	RCLK9
J	TXN1	TXN1	TVDD1	TVSS1	LM1[1]	VSS	LM3[1]	$\overline{\text{HIZ}}$	VSS	VDD33	VSS
K	RXN1	RXP1	TVSS1	TVDD1	TVDD1	TVDD3	VSS	TLBO3	VDD33	VSS	VSS
L	RVSS1	RESREF	TAIS2	RVDD1	VSS	RMON1	TLBO1	VSS	VSS	VSS	VSS
M	JVDD2	JVSS2	TVDD2	LM2[0]	TVSS2	TVDD2	LM2[1]	TVSS1	TLBO2	VSS	VSS
N	TXP2	TXP2	TVDD2	TVSS2	TLBO4	LM4[1]	TVDD4	LB12[0]	VDD33	VSS	VSS
P	TXN2	TXN2	RVDD2	TVSS2	RVSS2	TVSS4	LB8[0]	LB2[1]	LB9[1]	VDD33	TVDD6
R	RXP2	RXN2	TAIS4	RMON2	LB3[0]	LB4[0]	LB6[0]	LB4[1]	LB7[1]	ITRE	N.C.
T	LM4[0]	VDD18	JVSS4	JVDD4	LB1[0]	LB2[0]	LB5[0]	LB5[1]	LB11[1]	N.C.	TAIS8
U	TXP4	TXP4	TVSS4	TVDD4	LB9[0]	VSS	VSS	N.C.	IFSEL0	TVSS6	LM6[1]
V	TVSS4	TVDD4	RVDD4	LB7[0]	N.C.	N.C.	TVDD6	TVSS6	TVSS6	RMON6	JVSS8
W	TXN4	TXN4	RVSS4	LB10[0]	LB6[1]	N.C.	IFSEL2	TAIS6	VSS	RVSS6	JVDD8
Y	RXP4	RXN4	LB11[0]	LB8[1]	N.C.	IFSEL1	TLBO6	TVDD6	RVDD6	LM6[0]	TVDD8
AA	RMON4	LB1[1]	LB10[1]	MT3	MT7	JVDD6	TXP6	TXN6	RXP6	VDD18	TXP8
AB	LB3[1]	LB12[1]	N.C.	MT4	MT8	JVSS6	TXP6	TXN6	RXN6	TLBO8	TXP8
	1	2	3	4	5	6	7	8	9	10	11

	High-Speed Analog		Low-Speed Analog
	High-Speed Digital		Low-Speed Digital
	N.C. and Manufacturing Test		VDD 1.8V
	VDDIO 3.3V		Analog VSS
	Analog VDD 1.8V		VSS

Right Half

12	13	14	15	16	17	18	19	20	21	22	
TXN7	TXP7	LM9[0]	RXN9	TXN9	TXP9	RMON11	RXN11	TXN11	TXP11	VSS	A
TXN7	TXP7	RMON9	RXP9	TXN9	TXP9	LM11[0]	RXP11	TXN11	TXP11	TDM9	B
TVSS7	JVSS7	RVSS9	TVDD9	JVSS9	VDD18	TVSS11	TVSS11	TVDD11	TNEG9	TOE5	C
TVDD7	JVDD7	TVSS9	TVDD9	TLBO9	RVDD11	TVDD11	JVSS11	RLOS9	TOE9	RCLK3	D
TVDD7	TLBO7	RVDD9	TVSS9	JVDD9	RVSS11	JVDD11	TPOS11	TCLK11	TNEG7	RNEG3	E
TVSS7	LM9[1]	TVSS9	LM11[1]	TVSS11	TLBO11	RPOS9	TNEG11	TOE11	TOE7	RLOS3	F
TVDD9	TAIS9	TVDD11	TAIS11	RPOS11	RNEG11	RCLK11	RCLK7	TPOS7	TCLK7	TOE3	G
RNEG9	TPOS9	TDM7	TCLK9	RLOS7	RPOS7	RNEG7	RLOS5	RPOS5	TPOS3	VDD18	H
VSS	VDD33	RCLK5	RPOS3	TPOS5	RNEG5	TCLK5	TNEG5	TDM5	RPOS1	TNEG1	J
VSS	VSS	VDD33	TDM3	RCLK1	RNEG1	TCLK3	RLOS1	TNEG3	TDM1	TOE1	K
VSS	VSS	RNEG4	TPOS1	TCLK1	RPOS2	CVDD	CVDD	CVSS	MT0	REFCLK	L
VSS	VSS	RLOS6	TPOS4	TOE4	TCLK4	TNEG2	CLKC	CLKD	CLKA	CLKB	M
VSS	VSS	VDD33	RNEG8	RCLK8	TDM6	RCLK4	TPOS2	VDD18	RNEG2	RCLK2	N
TAIS10	VDD33	RLOS10	TPOS8	TOE8	TCLK8	VSS	TDM4	RPOS6	TDM2	RLOS2	P
LM10[0]	RLOS12	TPOS12	TNEG10	RPOS12	RNEG12	RCLK12	TOE6	RPOS8	RCLK6	TCLK2	R
TVSS8	TVDD10	TLBO12	TVDD12	TDM12	TCLK12	TNEG12	RPOS10	RCLK10	TCLK6	TOE2	T
TVDD8	LM8[1]	TVSS10	LM12[0]	TVSS12	TOE12	RVDD12	TDM10	TCLK10	TPOS6	RPOS4	U
TVSS8	RMON8	JVSS10	TVSS10	RVDD10	JVDD12	TVSS12	TOE10	TPOS10	TNEG6	RLOS4	V
TVDD8	RVSS8	JVDD10	TVDD10	RMON10	JVSS12	TVDD12	RMON12	RNEG10	RLOS8	TNEG4	W
TVSS8	RVDD8	LM10[1]	TVDD10	TVSS10	RVSS10	LM12[1]	TVDD12	TVSS12	TDM8	RNEG6	Y
TXN8	RXP8	TLBO10	TXP10	TXN10	RXN10	VDD18	TXP12	TXN12	RXN12	TNEG8	AA
TXN8	RXN8	LM8[0]	TXP10	TXN10	RXP10	TAIS12	TXP12	TXN12	RXP12	RVSS12	AB
12	13	14	15	16	17	18	19	20	21	22	

	High-Speed Analog		Low-Speed Analog
	High-Speed Digital		Low-Speed Digital
	N.C. and Manufacturing Test		VDD 1.8V
	VDDIO 3.3V		Analog VSS
	Analog VDD 1.8V		VSS

Figure 12-3. DS32512 Pin Assignment, Microprocessor Interface Only

Left Half

	1	2	3	4	5	6	7	8	9	10	11
A	JVDD3	TVDD3	N.C.	MT5	MT9	RXP5	TXN5	TXP5	JVSS5	N.C.	RXN7
B	HW	JVSS3	N.C.	MT6	MT10	RXN5	TXN5	TXP5	TVDD5	GPIOB7	RXP7
C	TXP3	TXP3	$\overline{\text{RST}}$	N.C.	N.C.	N.C.	RVSS5	RVDD5	TVSS5	VDD18	RVDD7
D	TXN3	TXN3	JTDI	JTCLK	MT1	N.C.	N.C.	N.C.	TVDD5	N.C.	TVSS7
E	RXN3	RXP3	$\overline{\text{JTRST}}$	$\overline{\text{TEST}}$	N.C.	N.C.	N.C.	GPIOB5	TVSS5	JVDD5	RVSS7
F	N.C.	N.C.	TVSS3	TVDD3	RVSS3	JTDO	N.C.	GPIOA5	TVDD5	TVSS5	GPIOA7
G	VDD18	GPIOB1	TVSS3	RVDD3	GPIOB3	MT2	CLADBYP	N.C.	N.C.	TVDD7	N.C.
H	TXP1	TXP1	JVDD1	JVSS1	TVSS3	N.C.	JTMS	N.C.	N.C.	N.C.	RCLK9
J	TXN1	TXN1	TVDD1	TVSS1	GPIOA1	VSS	GPIOA3	$\overline{\text{HIZ}}$	VSS	VDD33	VSS
K	RXN1	RXP1	TVSS1	TVDD1	TVDD1	TVDD3	VSS	N.C.	VDD33	VSS	VSS
L	RVSS1	RESREF	N.C.	RVDD1	VSS	N.C.	N.C.	VSS	VSS	VSS	VSS
M	JVDD2	JVSS2	TVDD2	GPIOB2	TVSS2	TVDD2	GPIOA2	TVSS1	N.C.	VSS	VSS
N	TXP2	TXP2	TVDD2	TVSS2	N.C.	GPIOA4	TVDD4	D11	VDD33	VSS	VSS
P	TXN2	TXN2	RVDD2	TVSS2	RVSS2	TVSS4	D7/CPOL	D13	A5	VDD33	TVDD6
R	RXP2	RXN2	N.C.	N.C.	D2/SCLK	D3	D5	D15	A3	A9	$\overline{\text{RD}}/\overline{\text{DS}}$
T	GPIOB4	VDD18	JVSS4	JVDD4	D0/SDO	D1/SDI	D4	A1	A7	ALE	N.C.
U	TXP4	TXP4	TVSS4	TVDD4	D8	VSS	VSS	RDY/$\overline{\text{ACK}}$	IFSEL0	TVSS6	GPIOA6
V	TVSS4	TVDD4	RVDD4	D6/CPHA	A0	$\overline{\text{WR}}$/R/$\overline{\text{W}}$	TVDD6	TVSS6	TVSS6	N.C.	JVSS8
W	TXN4	TXN4	RVSS4	D9	A2	A10	IFSEL2	N.C.	VSS	RVSS6	JVDD8
Y	RXP4	RXN4	D10	A4	$\overline{\text{CS}}$	IFSEL1	N.C.	TVDD6	RVDD6	GPIOB6	TVDD8
AA	N.C.	D12	A6	MT3	MT7	JVDD6	TXP6	TXN6	RXP6	VDD18	TXP8
AB	D14	A8	$\overline{\text{INT}}$	MT4	MT8	JVSS6	TXP6	TXN6	RXN6	N.C.	TXP8
	1	2	3	4	5	6	7	8	9	10	11

	High-Speed Analog		Low-Speed Analog
	High-Speed Digital		Low-Speed Digital
	N.C. and Manufacturing Test		VDD 1.8V
	VDDIO 3.3V		Analog VSS
	Analog VDD 1.8V		VSS

Right Half

12	13	14	15	16	17	18	19	20	21	22	
TXN7	TXP7	GPIOB9	RXN9	TXN9	TXP9	N.C.	RXN11	TXN11	TXP11	VSS	A
TXN7	TXP7	N.C.	RXP9	TXN9	TXP9	GPIOB11	RXP11	TXN11	TXP11	N.C.	B
TVSS7	JVSS7	RVSS9	TVDD9	JVSS9	VDD18	TVSS11	TVSS11	TVDD11	TNEG9	N.C.	C
TVDD7	JVDD7	TVSS9	TVDD9	N.C.	RVDD11	TVDD11	JVSS11	N.C.	N.C.	RCLK3	D
TVDD7	N.C.	RVDD9	TVSS9	JVDD9	RVSS11	JVDD11	TPOS11	TCLK11	TNEG7	RNEG3	E
TVSS7	GPIOA9	TVSS9	GPIOA11	TVSS11	N.C.	RPOS9	TNEG11	N.C.	N.C.	N.C.	F
TVDD9	N.C.	TVDD11	N.C.	RPOS11	RNEG11	RCLK11	RCLK7	TPOS7	TCLK7	N.C.	G
RNEG9	TPOS9	N.C.	TCLK9	N.C.	RPOS7	RNEG7	N.C.	RPOS5	TPOS3	VDD18	H
VSS	VDD33	RCLK5	RPOS3	TPOS5	RNEG5	TCLK5	TNEG5	N.C.	RPOS1	TNEG1	J
VSS	VSS	VDD33	N.C.	RCLK1	RNEG1	TCLK3	N.C.	TNEG3	N.C.	N.C.	K
VSS	VSS	RNEG4	TPOS1	TCLK1	RPOS2	CVDD	CVDD	CVSS	MT0	REFCLK	L
VSS	VSS	N.C.	TPOS4	N.C.	TCLK4	TNEG2	CLKC	CLKD	CLKA	CLKB	M
VSS	VSS	VDD33	RNEG8	RCLK8	N.C.	RCLK4	TPOS2	VDD18	RNEG2	RCLK2	N
N.C.	VDD33	N.C.	TPOS8	N.C.	TCLK8	VSS	N.C.	RPOS6	N.C.	N.C.	P
GPIOB10	N.C.	TPOS12	TNEG10	RPOS12	RNEG12	RCLK12	N.C.	RPOS8	RCLK6	TCLK2	R
TVSS8	TVDD10	N.C.	TVDD12	N.C.	TCLK12	TNEG12	RPOS10	RCLK10	TCLK6	N.C.	T
TVDD8	GPIOA8	TVSS10	GPIOB12	TVSS12	N.C.	RVDD12	N.C.	TCLK10	TPOS6	RPOS4	U
TVSS8	N.C.	JVSS10	TVSS10	RVDD10	JVDD12	TVSS12	N.C.	TPOS10	TNEG6	N.C.	V
TVDD8	RVSS8	JVDD10	TVDD10	N.C.	JVSS12	TVDD12	N.C.	RNEG10	N.C.	TNEG4	W
TVSS8	RVDD8	GPIOA10	TVDD10	TVSS10	RVSS10	GPIOA12	TVDD12	TVSS12	N.C.	RNEG6	Y
TXN8	RXP8	N.C.	TXP10	TXN10	RXN10	VDD18	TXP12	TXN12	RXN12	TNEG8	AA
TXN8	RXN8	GPIOB8	TXP10	TXN10	RXP10	N.C.	TXP12	TXN12	RXP12	RVSS12	AB
12	13	14	15	16	17	18	19	20	21	22	

	High-Speed Analog		Low-Speed Analog
	High-Speed Digital		Low-Speed Digital
	N.C. and Manufacturing Test		VDD 1.8V
	VDDIO 3.3V		Analog VSS
	Analog VDD 1.8V		VSS

Figure 12-4. DS32508 Pin Assignment, Hardware and Microprocessor Interfaces

Left Half

	1	2	3	4	5	6	7	8	9	10	11
A	JVDD3	TVDD3	RCLKI	MT5	N.C.	RXP5	TXN5	TXP5	JVSS5	RMON7	RXN7
B	HW	JVSS3	RPD	MT6	N.C.	RXN5	TXN5	TXP5	TVDD5	GPIOB7	RXP7
C	TXP3	TXP3	$\overline{\text{RST}}$	JAD1	TCLKI	TCC	RVSS5	RVDD5	TVSS5	VDD18	RVDD7
D	TXN3	TXN3	JTDI	JTCLK	MT1	TPD	TBIN	RMON5	TVDD5	TLBO5	TVSS7
E	RXN3	RXP3	$\overline{\text{JTRST}}$	$\overline{\text{TEST}}$	JAS1	RBIN	AIST	GPIOB5	TVSS5	JVDD5	RVSS7
F	TAIS1	RMON3	TVSS3	TVDD3	RVSS3	JTDO	JAS0	GPIOA5	TVDD5	TVSS5	GPIOA7
G	VDD18	GPIOB1	TVSS3	RVDD3	GPIOB3	MT2	CLADBYP	JAD0	TAIS5	TVDD7	TAIS7
H	TXP1	TXP1	JVDD1	JVSS1	TVSS3	TAIS3	JTMS	LBS	N.C.	N.C.	N.C.
J	TXN1	TXN1	TVDD1	TVSS1	GPIOA1	VSS	GPIOA3	$\overline{\text{HIZ}}$	VSS	VDD33	VSS
K	RXN1	RXP1	TVSS1	TVDD1	TVDD1	TVDD3	VSS	TLBO3	VDD33	VSS	VSS
L	RVSS1	RESREF	TAIS2	RVDD1	VSS	RMON1	TLBO1	VSS	VSS	VSS	VSS
M	JVDD2	JVSS2	TVDD2	GPIOB2	TVSS2	TVDD2	GPIOA2	TVSS1	TLBO2	VSS	VSS
N	TXP2	TXP2	TVDD2	TVSS2	TLBO4	GPIOA4	TVDD4	D11	VDD33	VSS	VSS
P	TXN2	TXN2	RVDD2	TVSS2	RVSS2	TVSS4	D7/CPOL	D13	A5	VDD33	TVDD6
R	RXP2	RXN2	TAIS4	RMON2	D2/SCLK	D3	D5	D15	A3	A9	$\overline{\text{RD}}/\overline{\text{DS}}$
T	GPIOB4	VDD18	JVSS4	JVDD4	D0/SDO	D1/SDI	D4	A1	A7	ALE	TAIS8
U	TXP4	TXP4	TVSS4	TVDD4	D8	VSS	VSS	RDY/$\overline{\text{ACK}}$	IFSEL0	TVSS6	GPIOA6
V	TVSS4	TVDD4	RVDD4	D6/CPHA	A0	$\overline{\text{WR}}$/R/$\overline{\text{W}}$	TVDD6	TVSS6	TVSS6	RMON6	JVSS8
W	TXN4	TXN4	RVSS4	D9	A2	A10	IFSEL2	TAIS6	VSS	RVSS6	JVDD8
Y	RXP4	RXN4	D10	A4	$\overline{\text{CS}}$	IFSEL1	TLBO6	TVDD6	RVDD6	GPIOB6	TVDD8
AA	RMON4	D12	A6	MT3	MT7	JVDD6	TXP6	TXN6	RXP6	VDD18	TXP8
AB	D14	A8	$\overline{\text{INT}}$	MT4	MT8	JVSS6	TXP6	TXN6	RXN6	TLBO8	TXP8
	1	2	3	4	5	6	7	8	9	10	11

	High-Speed Analog		Low-Speed Analog
	High-Speed Digital		Low-Speed Digital
	N.C. and Manufacturing Test		VDD 1.8V
	VDDIO 3.3V		Analog VSS
	Analog VDD 1.8V		VSS

Right Half

12	13	14	15	16	17	18	19	20	21	22	
TXN7	TXP7	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	VSS	A
TXN7	TXP7	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	B
TVSS7	JVSS7	VSS	VSS	VSS	VDD18	VSS	VSS	VSS	N.C.	TOE5	C
TVDD7	JVDD7	VSS	VSS	N.C.	VSS	VSS	VSS	N.C.	N.C.	RCLK3	D
TVDD7	TLBO7	VSS	VSS	VSS	VSS	VSS	N.C.	N.C.	TNEG7	RNEG3	E
TVSS7	N.C.	VSS	N.C.	VSS	N.C.	N.C.	N.C.	N.C.	TOE7	RLOS3	F
VSS	N.C.	VSS	N.C.	N.C.	N.C.	N.C.	RCLK7	TPOS7	TCLK7	TOE3	G
N.C.	N.C.	TDM7	N.C.	RLOS7	RPOS7	RNEG7	RLOS5	RPOS5	TPOS3	VDD18	H
VSS	VDD33	RCLK5	RPOS3	TPOS5	RNEG5	TCLK5	TNEG5	TDM5	RPOS1	TNEG1	J
VSS	VSS	VDD33	TDM3	RCLK1	RNEG1	TCLK3	RLOS1	TNEG3	TDM1	TOE1	K
VSS	VSS	RNEG4	TPOS1	TCLK1	RPOS2	CVDD	CVDD	CVSS	MT0	REFCLK	L
VSS	VSS	RLOS6	TPOS4	TOE4	TCLK4	TNEG2	CLKC	CLKD	CLKA	CLKB	M
VSS	VSS	VDD33	RNEG8	RCLK8	TDM6	RCLK4	TPOS2	VDD18	RNEG2	RCLK2	N
N.C.	VDD33	N.C.	TPOS8	TOE8	TCLK8	VSS	TDM4	RPOS6	TDM2	RLOS2	P
N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	TOE6	RPOS8	RCLK6	TCLK2	R
TVSS8	VSS	N.C.	VSS	N.C.	N.C.	N.C.	N.C.	N.C.	TCLK6	TOE2	T
TVDD8	GPIOA8	VSS	N.C.	VSS	N.C.	VSS	N.C.	N.C.	TPOS6	RPOS4	U
TVSS8	RMON8	VSS	VSS	VSS	VSS	VSS	N.C.	N.C.	TNEG6	RLOS4	V
TVDD8	RVSS8	VSS	VSS	N.C.	VSS	VSS	N.C.	N.C.	RLOS8	TNEG4	W
TVSS8	RVDD8	N.C.	VSS	VSS	VSS	N.C.	VSS	VSS	TDM8	RNEG6	Y
TXN8	RXP8	N.C.	N.C.	N.C.	N.C.	VDD18	N.C.	N.C.	N.C.	TNEG8	AA
TXN8	RXN8	GPIOB8	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	VSS	AB
12	13	14	15	16	17	18	19	20	21	22	

	High-Speed Analog		Low-Speed Analog
	High-Speed Digital		Low-Speed Digital
	N.C. and Manufacturing Test		VDD 1.8V
	VDDIO 3.3V		Analog VSS
	Analog VDD 1.8V		VSS

Figure 12-5. DS32508 Pin Assignment, Hardware Interface Only

Left Half

	1	2	3	4	5	6	7	8	9	10	11
A	JVDD3	TVDD3	RCLKI	MT5	N.C.	RXP5	TXN5	TXP5	JVSS5	RMON7	RXN7
B	HW	JVSS3	RPD	MT6	N.C.	RXN5	TXN5	TXP5	TVDD5	LM7[0]	RXP7
C	TXP3	TXP3	$\overline{\text{RST}}$	JAD1	TCLKI	TCC	RVSS5	RVDD5	TVSS5	VDD18	RVDD7
D	TXN3	TXN3	JTDI	JTCLK	MT1	TPD	TBIN	RMON5	TVDD5	TLBO5	TVSS7
E	RXN3	RXP3	$\overline{\text{JTRST}}$	$\overline{\text{TEST}}$	JAS1	RBIN	AIST	LM5[0]	TVSS5	JVDD5	RVSS7
F	TAIS1	RMON3	TVSS3	TVDD3	RVSS3	JTDO	JAS0	LM5[1]	TVDD5	TVSS5	LM7[1]
G	VDD18	LM1[0]	TVSS3	RVDD3	LM3[0]	MT2	CLADBYP	JAD0	TAIS5	TVDD7	TAIS7
H	TXP1	TXP1	JVDD1	JVSS1	TVSS3	TAIS3	JTMS	LBS	N.C.	N.C.	N.C.
J	TXN1	TXN1	TVDD1	TVSS1	LM1[1]	VSS	LM3[1]	$\overline{\text{HIZ}}$	VSS	VDD33	VSS
K	RXN1	RXP1	TVSS1	TVDD1	TVDD1	TVDD3	VSS	TLBO3	VDD33	VSS	VSS
L	RVSS1	RESREF	TAIS2	RVDD1	VSS	RMON1	TLBO1	VSS	VSS	VSS	VSS
M	JVDD2	JVSS2	TVDD2	LM2[0]	TVSS2	TVDD2	LM2[1]	TVSS1	TLBO2	VSS	VSS
N	TXP2	TXP2	TVDD2	TVSS2	TLBO4	LM4[1]	TVDD4	N.C.	VDD33	VSS	VSS
P	TXN2	TXN2	RVDD2	TVSS2	RVSS2	TVSS4	LB8[0]	LB2[1]	N.C.	VDD33	TVDD6
R	RXP2	RXN2	TAIS4	RMON2	LB3[0]	LB4[0]	LB6[0]	LB4[1]	LB7[1]	ITRE	N.C.
T	LM4[0]	VDD18	JVSS4	JVDD4	LB1[0]	LB2[0]	LB5[0]	LB5[1]	N.C.	N.C.	TAIS8
U	TXP4	TXP4	TVSS4	TVDD4	N.C.	VSS	VSS	N.C.	IFSEL0	TVSS6	LM6[1]
V	TVSS4	TVDD4	RVDD4	LB7[0]	N.C.	N.C.	TVDD6	TVSS6	TVSS6	RMON6	JVSS8
W	TXN4	TXN4	RVSS4	N.C.	LB6[1]	N.C.	IFSEL2	TAIS6	VSS	RVSS6	JVDD8
Y	RXP4	RXN4	N.C.	LB8[1]	N.C.	IFSEL1	TLBO6	TVDD6	RVDD6	LM6[0]	TVDD8
AA	RMON4	LB1[1]	N.C.	MT3	MT7	JVDD6	TXP6	TXN6	RXP6	VDD18	TXP8
AB	LB3[1]	N.C.	N.C.	MT4	MT8	JVSS6	TXP6	TXN6	RXN6	TLBO8	TXP8
	1	2	3	4	5	6	7	8	9	10	11

	High-Speed Analog		Low-Speed Analog
	High-Speed Digital		Low-Speed Digital
	N.C. and Manufacturing Test		VDD 1.8V
	VDDIO 3.3V		Analog VSS
	Analog VDD 1.8V		VSS

Right Half

12	13	14	15	16	17	18	19	20	21	22	
TXN7	TXP7	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	VSS	A
TXN7	TXP7	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	B
TVSS7	JVSS7	VSS	VSS	VSS	VDD18	VSS	VSS	VSS	N.C.	TOE5	C
TVDD7	JVDD7	VSS	VSS	N.C.	VSS	VSS	VSS	N.C.	N.C.	RCLK3	D
TVDD7	TLBO7	VSS	VSS	VSS	VSS	VSS	N.C.	N.C.	TNEG7	RNEG3	E
TVSS7	N.C.	VSS	N.C.	VSS	N.C.	N.C.	N.C.	N.C.	TOE7	RLOS3	F
VSS	N.C.	VSS	N.C.	N.C.	N.C.	N.C.	RCLK7	TPOS7	TCLK7	TOE3	G
N.C.	N.C.	TDM7	N.C.	RLOS7	RPOS7	RNEG7	RLOS5	RPOS5	TPOS3	VDD18	H
VSS	VDD33	RCLK5	RPOS3	TPOS5	RNEG5	TCLK5	TNEG5	TDM5	RPOS1	TNEG1	J
VSS	VSS	VDD33	TDM3	RCLK1	RNEG1	TCLK3	RLOS1	TNEG3	TDM1	TOE1	K
VSS	VSS	RNEG4	TPOS1	TCLK1	RPOS2	CVDD	CVDD	CVSS	MT0	REFCLK	L
VSS	VSS	RLOS6	TPOS4	TOE4	TCLK4	TNEG2	CLKC	CLKD	CLKA	CLKB	M
VSS	VSS	VDD33	RNEG8	RCLK8	TDM6	RCLK4	TPOS2	VDD18	RNEG2	RCLK2	N
N.C.	VDD33	N.C.	TPOS8	TOE8	TCLK8	VSS	TDM4	RPOS6	TDM2	RLOS2	P
N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	TOE6	RPOS8	RCLK6	TCLK2	R
TVSS8	VSS	N.C.	VSS	N.C.	N.C.	N.C.	N.C.	N.C.	TCLK6	TOE2	T
TVDD8	LM8[1]	VSS	N.C.	VSS	N.C.	VSS	N.C.	N.C.	TPOS6	RPOS4	U
TVSS8	RMON8	VSS	VSS	VSS	VSS	VSS	N.C.	N.C.	TNEG6	RLOS4	V
TVDD8	RVSS8	VSS	VSS	N.C.	VSS	VSS	N.C.	N.C.	RLOS8	TNEG4	W
TVSS8	RVDD8	N.C.	VSS	VSS	VSS	N.C.	VSS	VSS	TDM8	RNEG6	Y
TXN8	RXP8	N.C.	N.C.	N.C.	N.C.	VDD18	N.C.	N.C.	N.C.	TNEG8	AA
TXN8	RXN8	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	VSS	AB
12	13	14	15	16	17	18	19	20	21	22	

	High-Speed Analog		Low-Speed Analog
	High-Speed Digital		Low-Speed Digital
	N.C. and Manufacturing Test		VDD 1.8V
	VDDIO 3.3V		Analog VSS
	Analog VDD 1.8V		VSS

Figure 12-6. DS32508 Pin Assignment, Microprocessor Interface Only

Left Half

	1	2	3	4	5	6	7	8	9	10	11
A	JVDD3	TVDD3	N.C.	MT5	N.C.	RXP5	TXN5	TXP5	JVSS5	N.C.	RXN7
B	HW	JVSS3	N.C.	MT6	N.C.	RXN5	TXN5	TXP5	TVDD5	GPIOB7	RXP7
C	TXP3	TXP3	$\overline{\text{RST}}$	N.C.	N.C.	N.C.	RVSS5	RVDD5	TVSS5	VDD18	RVDD7
D	TXN3	TXN3	JTDI	JTCLK	MT1	N.C.	N.C.	N.C.	TVDD5	N.C.	TVSS7
E	RXN3	RXP3	$\overline{\text{JTRST}}$	$\overline{\text{TEST}}$	N.C.	N.C.	N.C.	GPIOB5	TVSS5	JVDD5	RVSS7
F	N.C.	N.C.	TVSS3	TVDD3	RVSS3	JTDO	N.C.	GPIOA5	TVDD5	TVSS5	GPIOA7
G	VDD18	GPIOB1	TVSS3	RVDD3	GPIOB3	MT2	CLADBYP	N.C.	N.C.	TVDD7	N.C.
H	TXP1	TXP1	JVDD1	JVSS1	TVSS3	N.C.	JTMS	N.C.	N.C.	N.C.	N.C.
J	TXN1	TXN1	TVDD1	TVSS1	GPIOA1	VSS	GPIOA3	$\overline{\text{HIZ}}$	VSS	VDD33	VSS
K	RXN1	RXP1	TVSS1	TVDD1	TVDD1	TVDD3	VSS	N.C.	VDD33	VSS	VSS
L	RVSS1	RESREF	N.C.	RVDD1	VSS	N.C.	N.C.	VSS	VSS	VSS	VSS
M	JVDD2	JVSS2	TVDD2	GPIOB2	TVSS2	TVDD2	GPIOA2	TVSS1	N.C.	VSS	VSS
N	TXP2	TXP2	TVDD2	TVSS2	N.C.	GPIOA4	TVDD4	D11	VDD33	VSS	VSS
P	TXN2	TXN2	RVDD2	TVSS2	RVSS2	TVSS4	D7/CPOL	D13	A5	VDD33	TVDD6
R	RXP2	RXN2	N.C.	N.C.	D2/SCLK	D3	D5	D15	A3	A9	$\overline{\text{RD}}/\overline{\text{DS}}$
T	GPIOB4	VDD18	JVSS4	JVDD4	D0/SDO	D1/SDI	D4	A1	A7	ALE	N.C.
U	TXP4	TXP4	TVSS4	TVDD4	D8	VSS	VSS	RDY/$\overline{\text{ACK}}$	IFSEL0	TVSS6	GPIOA6
V	TVSS4	TVDD4	RVDD4	D6/CPHA	A0	$\overline{\text{WR}}$/R/$\overline{\text{W}}$	TVDD6	TVSS6	TVSS6	N.C.	JVSS8
W	TXN4	TXN4	RVSS4	D9	A2	A10	IFSEL2	N.C.	VSS	RVSS6	JVDD8
Y	RXP4	RXN4	D10	A4	$\overline{\text{CS}}$	IFSEL1	N.C.	TVDD6	RVDD6	GPIOB6	TVDD8
AA	N.C.	D12	A6	MT3	MT7	JVDD6	TXP6	TXN6	RXP6	VDD18	TXP8
AB	D14	A8	$\overline{\text{INT}}$	MT4	MT8	JVSS6	TXP6	TXN6	RXN6	N.C.	TXP8
	1	2	3	4	5	6	7	8	9	10	11

	High-Speed Analog		Low-Speed Analog
	High-Speed Digital		Low-Speed Digital
	N.C. and Manufacturing Test		VDD 1.8V
	VDDIO 3.3V		Analog VSS
	Analog VDD 1.8V		VSS

Right Half

12	13	14	15	16	17	18	19	20	21	22	
TXN7	TXP7	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	VSS	A
TXN7	TXP7	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	B
TVSS7	JVSS7	VSS	VSS	VSS	VDD18	VSS	VSS	VSS	N.C.	N.C.	C
TVDD7	JVDD7	VSS	VSS	N.C.	VSS	VSS	VSS	N.C.	N.C.	RCLK3	D
TVDD7	N.C.	VSS	VSS	VSS	VSS	VSS	N.C.	N.C.	TNEG7	RNEG3	E
TVSS7	N.C.	VSS	N.C.	VSS	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	F
VSS	N.C.	VSS	N.C.	N.C.	N.C.	N.C.	RCLK7	TPOS7	TCLK7	N.C.	G
N.C.	N.C.	N.C.	N.C.	N.C.	RPOS7	RNEG7	N.C.	RPOS5	TPOS3	VDD18	H
VSS	VDD33	RCLK5	RPOS3	TPOS5	RNEG5	TCLK5	TNEG5	N.C.	RPOS1	TNEG1	J
VSS	VSS	VDD33	N.C.	RCLK1	RNEG1	TCLK3	N.C.	TNEG3	N.C.	N.C.	K
VSS	VSS	RNEG4	TPOS1	TCLK1	RPOS2	CVDD	CVDD	CVSS	MT0	REFCLK	L
VSS	VSS	N.C.	TPOS4	N.C.	TCLK4	TNEG2	CLKC	CLKD	CLKA	CLKB	M
VSS	VSS	VDD33	RNEG8	RCLK8	N.C.	RCLK4	TPOS2	VDD18	RNEG2	RCLK2	N
N.C.	VDD33	N.C.	TPOS8	N.C.	TCLK8	VSS	N.C.	RPOS6	N.C.	N.C.	P
N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	RPOS8	RCLK6	TCLK2	R
TVSS8	VSS	N.C.	VSS	N.C.	N.C.	N.C.	N.C.	N.C.	TCLK6	N.C.	T
TVDD8	GPIOA8	VSS	N.C.	VSS	N.C.	VSS	N.C.	N.C.	TPOS6	RPOS4	U
TVSS8	N.C.	VSS	VSS	VSS	VSS	VSS	N.C.	N.C.	TNEG6	N.C.	V
TVDD8	RVSS8	VSS	VSS	N.C.	VSS	VSS	N.C.	N.C.	N.C.	TNEG4	W
TVSS8	RVDD8	N.C.	VSS	VSS	VSS	N.C.	VSS	VSS	N.C.	RNEG6	Y
TXN8	RXP8	N.C.	N.C.	N.C.	N.C.	VDD18	N.C.	N.C.	N.C.	TNEG8	AA
TXN8	RXN8	GPIOB8	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	VSS	AB
12	13	14	15	16	17	18	19	20	21	22	

	High-Speed Analog		Low-Speed Analog
	High-Speed Digital		Low-Speed Digital
	N.C. and Manufacturing Test		VDD 1.8V
	VDDIO 3.3V		Analog VSS
	Analog VDD 1.8V		VSS

Figure 12-7. DS32506 Pin Assignment, Hardware and Microprocessor Interfaces

Left Half

	1	2	3	4	5	6	7	8	9	10	11
A	JVDD3	TVDD3	RCLKI	MT5	N.C.	RXP5	TXN5	TXP5	JVSS5	N.C.	N.C.
B	HW	JVSS3	RPD	MT6	N.C.	RXN5	TXN5	TXP5	TVDD5	N.C.	N.C.
C	TXP3	TXP3	$\overline{\text{RST}}$	JAD1	TCLKI	TCC	RVSS5	RVDD5	TVSS5	VDD18	VSS
D	TXN3	TXN3	JTDI	JTCLK	MT1	TPD	TBIN	RMON5	TVDD5	TLBO5	VSS
E	RXN3	RXP3	$\overline{\text{JTRST}}$	$\overline{\text{TEST}}$	JAS1	RBIN	AIST	GPIOB5	TVSS5	JVDD5	VSS
F	TAIS1	RMON3	TVSS3	TVDD3	RVSS3	JTDO	JAS0	GPIOA5	TVDD5	TVSS5	N.C.
G	VDD18	GPIOB1	TVSS3	RVDD3	GPIOB3	MT2	CLADBYP	JAD0	TAIS5	VSS	N.C.
H	TXP1	TXP1	JVDD1	JVSS1	TVSS3	TAIS3	JTMS	LBS	N.C.	N.C.	N.C.
J	TXN1	TXN1	TVDD1	TVSS1	GPIOA1	VSS	GPIOA3	$\overline{\text{HIZ}}$	VSS	VDD33	VSS
K	RXN1	RXP1	TVSS1	TVDD1	TVDD1	TVDD3	VSS	TLBO3	VDD33	VSS	VSS
L	RVSS1	RESREF	TAIS2	RVDD1	VSS	RMON1	TLBO1	VSS	VSS	VSS	VSS
M	JVDD2	JVSS2	TVDD2	GPIOB2	TVSS2	TVDD2	GPIOA2	TVSS1	TLBO2	VSS	VSS
N	TXP2	TXP2	TVDD2	TVSS2	TLBO4	GPIOA4	TVDD4	D11	VDD33	VSS	VSS
P	TXN2	TXN2	RVDD2	TVSS2	RVSS2	TVSS4	D7/CPOL	D13	A5	VDD33	TVDD6
R	RXP2	RXN2	TAIS4	RMON2	D2/SCLK	D3	D5	D15	A3	A9	$\overline{\text{RD}}/\overline{\text{DS}}$
T	GPIOB4	VDD18	JVSS4	JVDD4	D0/SDO	D1/SDI	D4	A1	A7	ALE	N.C.
U	TXP4	TXP4	TVSS4	TVDD4	D8	VSS	VSS	RDY/$\overline{\text{ACK}}$	IFSEL0	TVSS6	GPIOA6
V	TVSS4	TVDD4	RVDD4	D6/CPHA	A0	$\overline{\text{WR}}$/R/$\overline{\text{W}}$	TVDD6	TVSS6	TVSS6	RMON6	VSS
W	TXN4	TXN4	RVSS4	D9	A2	N.C.	IFSEL2	TAIS6	VSS	RVSS6	VSS
Y	RXP4	RXN4	D10	A4	$\overline{\text{CS}}$	IFSEL1	TLBO6	TVDD6	RVDD6	GPIOB6	VSS
AA	RMON4	D12	A6	MT3	N.C.	JVDD6	TXP6	TXN6	RXP6	VDD18	N.C.
AB	D14	A8	$\overline{\text{INT}}$	MT4	N.C.	JVSS6	TXP6	TXN6	RXN6	N.C.	N.C.
	1	2	3	4	5	6	7	8	9	10	11

	High-Speed Analog		Low-Speed Analog
	High-Speed Digital		Low-Speed Digital
	N.C. and Manufacturing Test		VDD 1.8V
	VDDIO 3.3V		Analog VSS
	Analog VDD 1.8V		VSS

Right Half

12	13	14	15	16	17	18	19	20	21	22	
N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	VSS	A
N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	B
VSS	VSS	VSS	VSS	VSS	VDD18	VSS	VSS	VSS	N.C.	TOE5	C
VSS	VSS	VSS	VSS	N.C.	VSS	VSS	VSS	N.C.	N.C.	RCLK3	D
VSS	N.C.	VSS	VSS	VSS	VSS	VSS	N.C.	N.C.	N.C.	RNEG3	E
VSS	N.C.	VSS	N.C.	VSS	N.C.	N.C.	N.C.	N.C.	N.C.	RLOS3	F
VSS	N.C.	VSS	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	TOE3	G
N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	RLOS5	RPOS5	TPOS3	VDD18	H
VSS	VDD33	RCLK5	RPOS3	TPOS5	RNEG5	TCLK5	TNEG5	TDM5	RPOS1	TNEG1	J
VSS	VSS	VDD33	TDM3	RCLK1	RNEG1	TCLK3	RLOS1	TNEG3	TDM1	TOE1	K
VSS	VSS	RNEG4	TPOS1	TCLK1	RPOS2	CVDD	CVDD	CVSS	MT0	REFCLK	L
VSS	VSS	RLOS6	TPOS4	TOE4	TCLK4	TNEG2	CLKC	CLKD	CLKA	CLKB	M
VSS	VSS	VDD33	N.C.	N.C.	TDM6	RCLK4	TPOS2	VDD18	RNEG2	RCLK2	N
N.C.	VDD33	N.C.	N.C.	N.C.	N.C.	VSS	TDM4	RPOS6	TDM2	RLOS2	P
N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	TOE6	N.C.	RCLK6	TCLK2	R
VSS	VSS	N.C.	VSS	N.C.	N.C.	N.C.	N.C.	N.C.	TCLK6	TOE2	T
VSS	N.C.	VSS	N.C.	VSS	N.C.	VSS	N.C.	N.C.	TPOS6	RPOS4	U
VSS	N.C.	VSS	VSS	VSS	VSS	VSS	N.C.	N.C.	TNEG6	RLOS4	V
VSS	VSS	VSS	VSS	N.C.	VSS	VSS	N.C.	N.C.	N.C.	TNEG4	W
VSS	VSS	N.C.	VSS	VSS	VSS	N.C.	VSS	VSS	N.C.	RNEG6	Y
N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	VDD18	N.C.	N.C.	N.C.	N.C.	AA
N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	VSS	AB
12	13	14	15	16	17	18	19	20	21	22	

	High-Speed Analog		Low-Speed Analog
	High-Speed Digital		Low-Speed Digital
	N.C. and Manufacturing Test		VDD 1.8V
	VDDIO 3.3V		Analog VSS
	Analog VDD 1.8V		VSS

Figure 12-8. DS32506 Pin Assignment, Hardware Interface Only

Left Half

	1	2	3	4	5	6	7	8	9	10	11
A	JVDD3	TVDD3	RCLKI	MT5	N.C.	RXP5	TXN5	TXP5	JVSS5	N.C.	N.C.
B	HW	JVSS3	RPD	MT6	N.C.	RXN5	TXN5	TXP5	TVDD5	N.C.	N.C.
C	TXP3	TXP3	$\overline{\text{RST}}$	JAD1	TCLKI	TCC	RVSS5	RVDD5	TVSS5	VDD18	VSS
D	TXN3	TXN3	JTDI	JTCLK	MT1	TPD	TBIN	RMON5	TVDD5	TLBO5	VSS
E	RXN3	RXP3	$\overline{\text{JTRST}}$	$\overline{\text{TEST}}$	JAS1	RBIN	AIST	LM5[0]	TVSS5	JVDD5	VSS
F	TAIS1	RMON3	TVSS3	TVDD3	RVSS3	JTDO	JAS0	LM5[1]	TVDD5	TVSS5	N.C.
G	VDD18	LM1[0]	TVSS3	RVDD3	LM3[0]	MT2	CLADBYP	JAD0	TAIS5	VSS	N.C.
H	TXP1	TXP1	JVDD1	JVSS1	TVSS3	TAIS3	JTMS	LBS	N.C.	N.C.	N.C.
J	TXN1	TXN1	TVDD1	TVSS1	LM1[1]	VSS	LM3[1]	$\overline{\text{HIZ}}$	VSS	VDD33	VSS
K	RXN1	RXP1	TVSS1	TVDD1	TVDD1	TVDD3	VSS	TLBO3	VDD33	VSS	VSS
L	RVSS1	RESREF	TAIS2	RVDD1	VSS	RMON1	TLBO1	VSS	VSS	VSS	VSS
M	JVDD2	JVSS2	TVDD2	LM2[0]	TVSS2	TVDD2	LM2[1]	TVSS1	TLBO2	VSS	VSS
N	TXP2	TXP2	TVDD2	TVSS2	TLBO4	LM4[1]	TVDD4	N.C.	VDD33	VSS	VSS
P	TXN2	TXN2	RVDD2	TVSS2	RVSS2	TVSS4	N.C.	LB2[1]	N.C.	VDD33	TVDD6
R	RXP2	RXN2	TAIS4	RMON2	LB3[0]	LB4[0]	LB6[0]	LB4[1]	VSS	ITRE	N.C.
T	LM4[0]	VDD18	JVSS4	JVDD4	LB1[0]	LB2[0]	LB5[0]	LB5[1]	N.C.	N.C.	N.C.
U	TXP4	TXP4	TVSS4	TVDD4	N.C.	VSS	VSS	N.C.	IFSEL0	TVSS6	LM6[1]
V	TVSS4	TVDD4	RVDD4	VSS	N.C.	N.C.	TVDD6	TVSS6	TVSS6	RMON6	VSS
W	TXN4	TXN4	RVSS4	N.C.	LB6[1]	N.C.	IFSEL2	TAIS6	VSS	VSS	VSS
Y	RXP4	RXN4	N.C.	N.C.	N.C.	IFSEL1	TLBO6	TVDD6	RVDD6	LM6[0]	VSS
AA	RMON4	LB1[1]	N.C.	MT3	N.C.	JVDD6	TXP6	TXN6	RXP6	VDD18	N.C.
AB	LB3[1]	N.C.	N.C.	MT4	N.C.	JVSS6	TXP6	TXN6	RXN6	N.C.	N.C.
	1	2	3	4	5	6	7	8	9	10	11

	High-Speed Analog		Low-Speed Analog
	High-Speed Digital		Low-Speed Digital
	N.C. and Manufacturing Test		VDD 1.8V
	VDDIO 3.3V		Analog VSS
	Analog VDD 1.8V		VSS

Right Half

12	13	14	15	16	17	18	19	20	21	22	
N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	VSS	A
N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	B
VSS	VSS	VSS	VSS	VSS	VDD18	VSS	VSS	VSS	N.C.	TOE5	C
VSS	VSS	VSS	VSS	N.C.	VSS	VSS	VSS	N.C.	N.C.	RCLK3	D
VSS	N.C.	VSS	VSS	VSS	VSS	VSS	N.C.	N.C.	N.C.	RNEG3	E
VSS	N.C.	VSS	N.C.	VSS	N.C.	N.C.	N.C.	N.C.	N.C.	RLOS3	F
VSS	N.C.	VSS	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	TOE3	G
N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	RLOS5	RPOS5	TPOS3	VDD18	H
VSS	VDD33	RCLK5	RPOS3	TPOS5	RNEG5	TCLK5	TNEG5	TDM5	RPOS1	TNEG1	J
VSS	VSS	VDD33	TDM3	RCLK1	RNEG1	TCLK3	RLOS1	TNEG3	TDM1	TOE1	K
VSS	VSS	RNEG4	TPOS1	TCLK1	RPOS2	CVDD	CVDD	CVSS	MT0	REFCLK	L
VSS	VSS	RLOS6	TPOS4	TOE4	TCLK4	TNEG2	CLKC	CLKD	CLKA	CLKB	M
VSS	VSS	VDD33	N.C.	N.C.	TDM6	RCLK4	TPOS2	VDD18	RNEG2	RCLK2	N
N.C.	VDD33	N.C.	N.C.	N.C.	N.C.	VSS	TDM4	RPOS6	TDM2	RLOS2	P
N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	TOE6	N.C.	RCLK6	TCLK2	R
VSS	VSS	N.C.	VSS	N.C.	N.C.	N.C.	N.C.	N.C.	TCLK6	TOE2	T
VSS	N.C.	VSS	N.C.	VSS	N.C.	VSS	N.C.	N.C.	TPOS6	RPOS4	U
VSS	N.C.	VSS	VSS	VSS	VSS	VSS	N.C.	N.C.	TNEG6	RLOS4	V
VSS	VSS	VSS	VSS	N.C.	VSS	VSS	N.C.	N.C.	N.C.	TNEG4	W
VSS	VSS	N.C.	VSS	VSS	VSS	N.C.	VSS	VSS	N.C.	RNEG6	Y
N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	VDD18	N.C.	N.C.	N.C.	N.C.	AA
N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	VSS	AB
12	13	14	15	16	17	18	19	20	21	22	

	High-Speed Analog		Low-Speed Analog
	High-Speed Digital		Low-Speed Digital
	N.C. and Manufacturing Test		VDD 1.8V
	VDDIO 3.3V		Analog VSS
	Analog VDD 1.8V		VSS

Figure 12-9. DS32506 Pin Assignment, Microprocessor Interface Only

Left Half

	1	2	3	4	5	6	7	8	9	10	11
A	JVDD3	TVDD3	N.C.	MT5	N.C.	RXP5	TXN5	TXP5	JVSS5	N.C.	N.C.
B	HW	JVSS3	N.C.	MT6	N.C.	RXN5	TXN5	TXP5	TVDD5	N.C.	N.C.
C	TXP3	TXP3	$\overline{RST}$	N.C.	N.C.	N.C.	RVSS5	RVDD5	TVSS5	VDD18	VSS
D	TXN3	TXN3	JTDI	JTCLK	MT1	N.C.	N.C.	N.C.	TVDD5	N.C.	VSS
E	RXN3	RXP3	$\overline{JTRST}$	$\overline{TEST}$	N.C.	N.C.	N.C.	GPIOB5	TVSS5	JVDD5	VSS
F	N.C.	N.C.	TVSS3	TVDD3	RVSS3	JTDO	N.C.	GPIOA5	TVDD5	TVSS5	N.C.
G	VDD18	GPIOB1	TVSS3	RVDD3	GPIOB3	MT2	CLADBYP	N.C.	N.C.	VSS	N.C.
H	TXP1	TXP1	JVDD1	JVSS1	TVSS3	N.C.	JTMS	N.C.	N.C.	N.C.	N.C.
J	TXN1	TXN1	TVDD1	TVSS1	GPIOA1	VSS	GPIOA3	$\overline{HIZ}$	VSS	VDD33	VSS
K	RXN1	RXP1	TVSS1	TVDD1	TVDD1	TVDD3	VSS	N.C.	VDD33	VSS	VSS
L	RVSS1	RESREF	N.C.	RVDD1	VSS	N.C.	N.C.	VSS	VSS	VSS	VSS
M	JVDD2	JVSS2	TVDD2	GPIOB2	TVSS2	TVDD2	GPIOA2	TVSS1	N.C.	VSS	VSS
N	TXP2	TXP2	TVDD2	TVSS2	N.C.	GPIOA4	TVDD4	D11	VDD33	VSS	VSS
P	TXN2	TXN2	RVDD2	TVSS2	RVSS2	TVSS4	D7/CPOL	D13	A5	VDD33	TVDD6
R	RXP2	RXN2	N.C.	N.C.	D2/SCLK	D3	D5	D15	A3	A9	$\overline{RD}/\overline{DS}$
T	GPIOB4	VDD18	JVSS4	JVDD4	D0/SDO	D1/SDI	D4	A1	A7	ALE	N.C.
U	TXP4	TXP4	TVSS4	TVDD4	D8	VSS	VSS	RDY/$\overline{ACK}$	IFSEL0	TVSS6	GPIOA6
V	TVSS4	TVDD4	RVDD4	D6/CPHA	A0	$\overline{WR}$/R/$\overline{W}$	TVDD6	TVSS6	TVSS6	N.C.	VSS
W	TXN4	TXN4	RVSS4	D9	A2	N.C.	IFSEL2	N.C.	VSS	RVSS6	VSS
Y	RXP4	RXN4	D10	A4	$\overline{CS}$	IFSEL1	N.C.	TVDD6	RVDD6	GPIOB6	VSS
AA	N.C.	D12	A6	MT3	N.C.	JVDD6	TXP6	TXN6	RXP6	VDD18	N.C.
AB	D14	A8	$\overline{INT}$	MT4	N.C.	JVSS6	TXP6	TXN6	RXN6	N.C.	N.C.
	1	2	3	4	5	6	7	8	9	10	11

	High-Speed Analog		Low-Speed Analog
	High-Speed Digital		Low-Speed Digital
	N.C. and Manufacturing Test		VDD 1.8V
	VDDIO 3.3V		Analog VSS
	Analog VDD 1.8V		VSS

Right Half

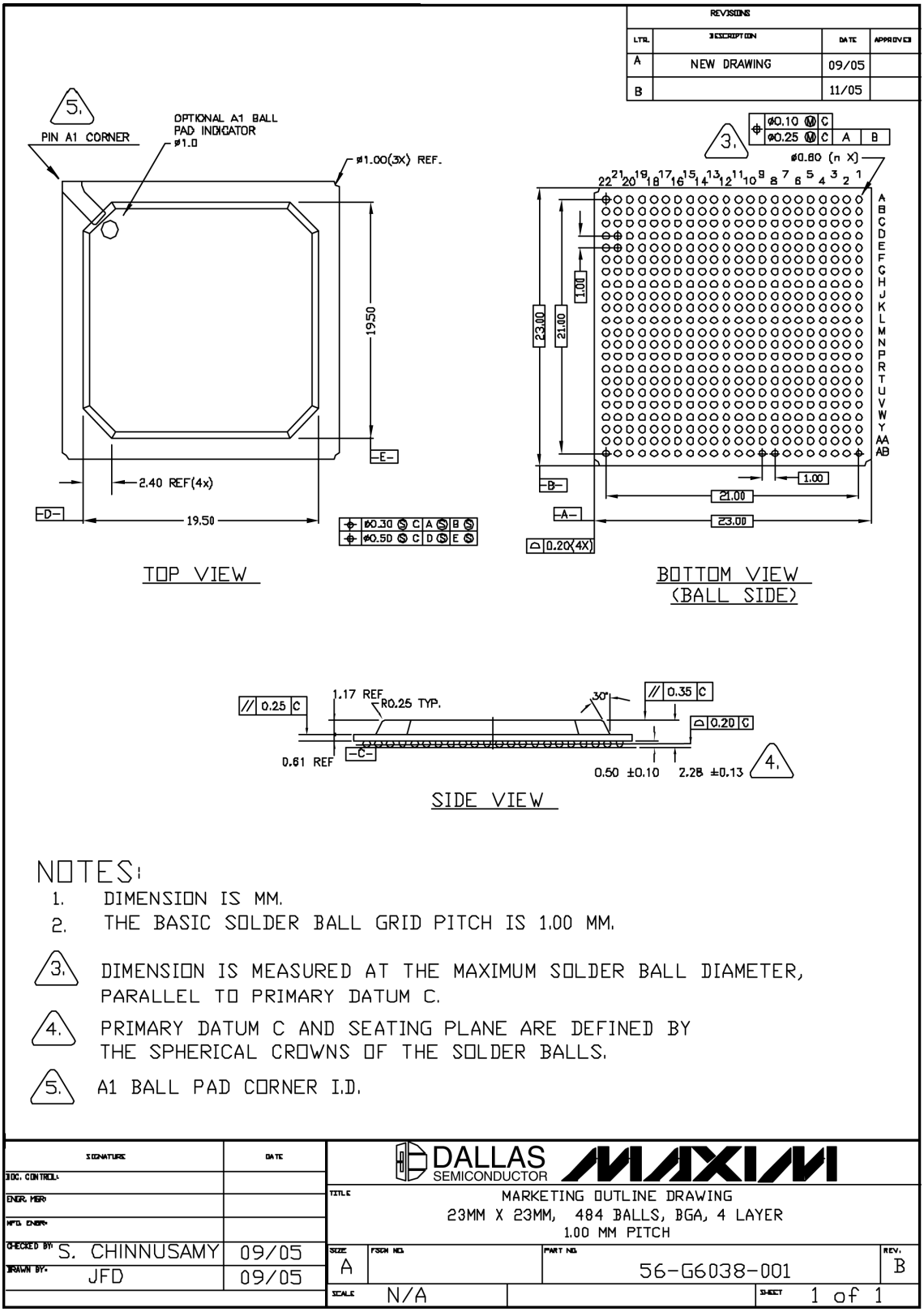
12	13	14	15	16	17	18	19	20	21	22	
N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	VSS	A
N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	B
VSS	VSS	VSS	VSS	VSS	VDD18	VSS	VSS	VSS	N.C.	N.C.	C
VSS	VSS	VSS	VSS	N.C.	VSS	VSS	VSS	N.C.	N.C.	RCLK3	D
VSS	N.C.	VSS	VSS	VSS	VSS	VSS	N.C.	N.C.	N.C.	RNEG3	E
VSS	N.C.	VSS	N.C.	VSS	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	F
VSS	N.C.	VSS	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	G
N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	RPOS5	TPOS3	VDD18	H
VSS	VDD33	RCLK5	RPOS3	TPOS5	RNEG5	TCLK5	TNEG5	N.C.	RPOS1	TNEG1	J
VSS	VSS	VDD33	N.C.	RCLK1	RNEG1	TCLK3	N.C.	TNEG3	N.C.	N.C.	K
VSS	VSS	RNEG4	TPOS1	TCLK1	RPOS2	CVDD	CVDD	CVSS	MT0	REFCLK	L
VSS	VSS	N.C.	TPOS4	N.C.	TCLK4	TNEG2	CLKC	CLKD	CLKA	CLKB	M
VSS	VSS	VDD33	N.C.	N.C.	N.C.	RCLK4	TPOS2	VDD18	RNEG2	RCLK2	N
N.C.	VDD33	N.C.	N.C.	N.C.	N.C.	VSS	N.C.	RPOS6	N.C.	N.C.	P
N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	RCLK6	TCLK2	R
VSS	VSS	N.C.	VSS	N.C.	N.C.	N.C.	N.C.	N.C.	TCLK6	N.C.	T
VSS	N.C.	VSS	N.C.	VSS	N.C.	VSS	N.C.	N.C.	TPOS6	RPOS4	U
VSS	N.C.	VSS	VSS	VSS	VSS	VSS	N.C.	N.C.	TNEG6	N.C.	V
VSS	VSS	VSS	VSS	N.C.	VSS	VSS	N.C.	N.C.	N.C.	TNEG4	W
VSS	VSS	N.C.	VSS	VSS	VSS	N.C.	VSS	VSS	N.C.	RNEG6	Y
N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	VDD18	N.C.	N.C.	N.C.	N.C.	AA
N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	VSS	AB
12	13	14	15	16	17	18	19	20	21	22	

	High-Speed Analog		Low-Speed Analog
	High-Speed Digital		Low-Speed Digital
	N.C. and Manufacturing Test		VDD 1.8V
	VDDIO 3.3V		Analog VSS
	Analog VDD 1.8V		VSS

13. PACKAGE INFORMATION

(The package drawing(s) in this data sheet may not reflect the most current specifications. The package number provided for each package is a link to the latest package outline information.)

13.1 484-Lead BGA (23mm x 23mm) (56-G60038-001)



14. THERMAL INFORMATION

Table 14-1. Thermal Properties, Natural Convection

PARAMETER	MIN	TYP	MAX	UNITS
Ambient Temperature (Note 1)	-40		+85	°C
Junction Temperature	-40		+125	°C
Theta-JA (θ_{JA}), Still Air (Note 1)		16.0		°C/W
Theta-JC (θ_{JC})		5.4		°C/W
Psi-JB		7.7		°C/W
Psi-JT		0.4		°C/W

Note 1: The package is mounted on a four-layer JEDEC standard test board with no airflow and dissipating maximum power.

Table 14-2. Theta-JA (θ_{JA}) vs. Airflow

FORCED AIR (METERS PER SECOND)	THETA-JA (θ_{JA})
0	16.0 °C/W
1	13.8 °C/W
2	12.8 °C/W

15. ACRONYMS AND ABBREVIATIONS

AIS	Alarm Indication Signal
AMI	Alternate Mark Inversion
B3ZS	Bipolar with Three-Zero Substitution
BER	Bit-Error Rate, Bit-Error Ratio
BPV	Bipolar Violation
CV	Code Violation
DS3	Digital Signal, Level 3
EXZ	Excessive Zeros
HDB3	High-Density Bipolar of Order 3
IO, I/O	Input/Output
LIU	Line Interface Unit
LOL	Loss of Lock
LOS	Loss of Signal
LSB	Least Significant Bit
MSB	Most Significant Bit
PDH	Plesiochronous Digital Hierarchy
PRBS	Pseudo-Random Bit Sequence
Rx, RX	Receive
SONET	Synchronous Optical Network
SDH	Synchronous Digital Hierarchy
STS	Synchronous Transmission Signal
STS-1	Synchronous Transmission Signal at Level 1
Tx, TX	Transmit
UI	Unit Interval
UI_{P-P}	Unit Interval Peak-to-Peak
UI_{RMS}	Unit Intervals Root Mean Square

16. TRADEMARK ACKNOWLEDGEMENTS

ACCUNET is a registered trademark of AT&T.
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17. DATA SHEET REVISION HISTORY

REVISION DATE	DESCRIPTION	PAGES CHANGED
062906	Initial data sheet release.	—
091307	Added Internal Receive Enable (ITRE) pin to Table 7-1. Short Pin Descriptions.	14
	Changed VDD18 tolerance from ±10% to ±5% (Table 7-1. Short Pin Descriptions).	15
	Added Internal Receive Enable (ITRE) pin description to Table 7-5. Hardware Interface Pin Description.	20
	Changed VDD18 tolerance from ±10% to ±5% (Table 7-10. Power-Supply Pin Descriptions).	23
	In Section 8.2.8, removed “Note that internal termination is only available when a microprocessor interface is enabled.”	25
	Changed RXP to TXN in the third paragraph of *Section 8.2.9: Driver Monitor and Output Failure Detection*.	26
	In Section 8.3.1, removed “Note that internal termination is only available when a microprocessor interface is enabled.”	30
	Removed *Section 8.12: Initialization*.	48
	In the *Absolute Maximum Ratings* section, changed the VDD18 supply range from ”-0.1V to +1.98V” to “-0.1V to +1.89V”.	92
	In Table 11-1, changed VDD18 from 1.62V (min) to 1.71V (min) and 1.98V (max) to 1.89V (max).	
	In Table 11-2, changed all I_{DD18}, I_{DD33}, $I_{DDTTS18}$, and $I_{DDTTS33}$ typ and max values.	93
	In Table 11-2 to Table 11-10, changed VDD18 tolerance from ±10% to ±5%.	93, 94, 96, 97, 98, 103, 105
	In Table 12-1, added ITRE to ball R10.	106
	In Figure 12-2, Figure 12-5, and Figure 12-8, changed ball R10 from N.C. to ITRE for DS32512, DS32508, and DS32506 hardware-interface-only pin assignments.	111, 117, 123
040808	In Figure 12-8 (left half), corrected typos where some pins for port 7 were listed (do not exist on the DS32506). Changed pins A10, A11, B10, B11, F11, and G11 to N.C. Changed pins C11, D11, E11, G10, R9, and V4 to VSS.	123
103008	In Section 9.7, clarified register bit text descriptions for LINE.RSR:BPVC and LINE.RSR:EXCZ.	83