BLP8G10S-45P; BLP8G10S-45PG

Power LDMOS transistor

Rev. 1 — 25 July 2013 Product data sheet

1. Product profile

1.1 General description

The BLP8G10S-45P and BLP8G10S-45PG are dual path, 45 W LDMOS power transistors for base station applications at frequencies from 700 MHz to 1000 MHz.

Table 1. Application performance

Typical RF performance at T_{case} = 25 °C; I_{Dq} = 224 mA in common source class-AB production circuit.

Test signal	f	V_{DS}	$P_{L(AV)}$	G_p	η_D	ACPR
	(MHz)	(V)	(W)	(dB)	(%)	(dBc)
2-carrier W-CDMA	960	28	2.5	20.8	19.8	–49 [1]

[1] Test signal: 3GPP; test model 1; 64 DPCH; PAR = 8.4 dB at 0.01% probability on CCDF; carrier spacing = 5 MHz; per section unless otherwise specified.

1.2 Features and benefits

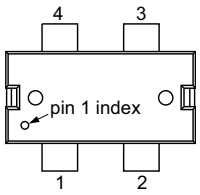
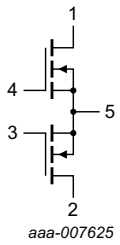
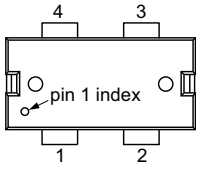
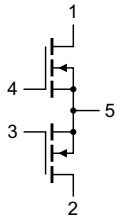
- High efficiency
- Excellent ruggedness
- Designed for broadband operation (700 MHz to 1000 MHz)
- Excellent thermal stability
- High power gain
- Integrated ESD protection
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

- W-CDMA
- LTE
- GSM

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
BLP8G10S-45P (SOT1223-1)			
1	drain 1		 aaa-007625
2	drain 2		
3	gate 2		
4	gate 1		
5	source [1]		
BLP8G10S-45PG (SOT1224-1)			
1	drain 1		 aaa-007625
2	drain 2		
3	gate 2		
4	gate 1		
5	source [1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLP8G10S-45P	HSOP4F	plastic, heatsink small outline package; 4 leads (flat)	SOT1223-1
BLP8G10S-45PG	HSOP4	plastic, heatsink small outline package; 4 leads	SOT1224-1

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter		Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		–0.5	+13	V
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature	[1]	-	225	°C
T_{case}	case temperature	[1]	-	150	°C

[1] Continuous use at maximum temperature will affect the reliability.

5. Thermal characteristics

Table 5. Thermal characteristics

Values specified for entire device.

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j\text{-}case)}$	thermal resistance from junction to case	T_{case} = 85 °C; P_L = 5 W	0.85	K/W

6. Characteristics

Table 6. DC characteristics

T_{case} = 25 °C; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.4 mA	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 40 mA	1.5	1.9	2.3	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 28 V	-	-	1.4	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	-	7.3	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	140	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 2 A	-	3.0	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{DS} = 10 V; I_D = 1.4 A V_{GS} = $V_{GS(th)}$ + 3.75 V	-	500	-	mΩ

Table 7. RF characteristics

Test signal: 2-carrier W-CDMA; PAR 8.4 dB at 0.01 % probability on CCDF; 3GPP test model 1; 1-64 DPCH; f_1 = 952.5 MHz; f_2 = 957.5 MHz; RF performance at V_{DS} = 28 V; I_{Dq} = 224 mA; T_{case} = 25 °C; per section in a class-AB production circuit unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	P_L = 2.5 W	20	20.8	-	dB
RL_{in}	input return loss	P_L = 2.5 W	-	–18	–9	dB
η_D	drain efficiency	P_L = 2.5 W	18	19.8	-	%
ACPR	adjacent channel power ratio	P_L = 2.5 W	-	–49	–43	dBc

7. Test information

7.1 Ruggedness in class-AB operation

The BLP8G10S-45P and BLP8G10S-45PG are capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 28 V; I_{Dq} = 224 mA; P_L = 25 W; f = 728 MHz.

7.2 Impedance information

Table 8. Typical impedance BLP8G10S-45P

Measured load-pull data. Typical values per section unless otherwise specified.

f (MHz)	Z_S [1] (Ω)	Z_L [1][2] (Ω)
BLP8G10S-45P		
720	11.6 – j12.9	5.44 + j6.34
746	14.8 – j9.2	4.51 + j6.03
757	15.3 – j4.6	4.23 + j6.15
791	13.3 – j1.6	3.99 + j5.62
820	6.5 – j1.1	3.87 + j5.37
869	5.2 – j2.4	4.25 + j4.49
894	4.4 – j3.0	3.69 + j4.89
925	3.8 – j3.9	3.49 + j4.72
942	3.6 – j4.2	3.06 + j4.46
960	3.6 – j4.7	3.29 + j4.04
BLP8G10S-45PG		
720	13.2 – j7.7	4.34 + j5.10
746	11.8 – j4.6	4.58 + j4.94
757	10.4 – j3.7	4.50 + j5.34
791	9.8 – j2.5	4.19 + j4.87
869	5.0 – j4.0	4.27 + j3.42
881	4.6 – j4.2	3.62 + j3.45
894	4.2 – j4.7	3.77 + j3.29
925	3.8 – j5.6	3.60 + j3.15
942	3.7 – j5.8	3.29 + j2.89
961	3.6 – j6.4	3.36 + j2.47

[1] Z_S and Z_L defined in Figure 1.

[2] Z_L is selected for maximum efficiency.

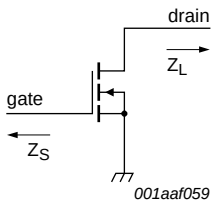
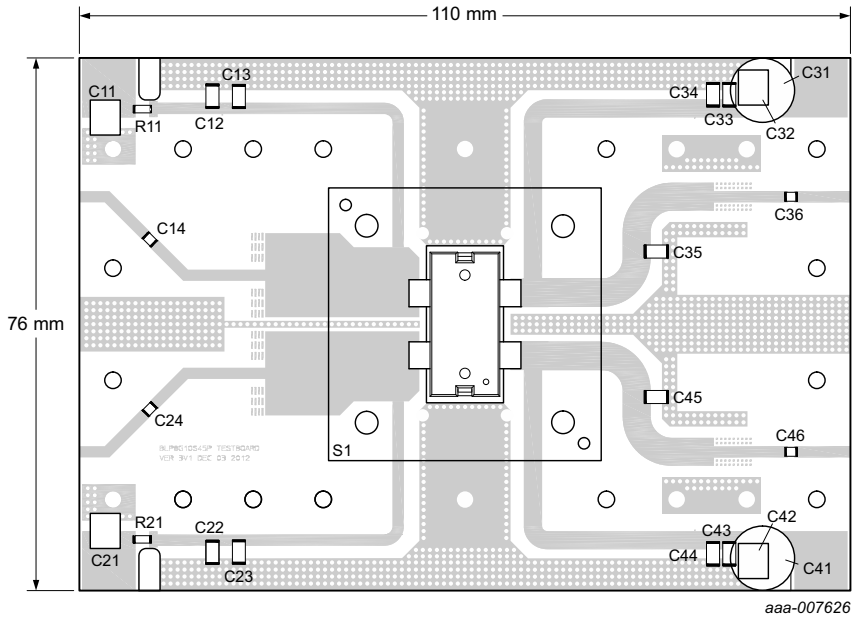


Fig 1. Definition of transistor impedance

7.3 Test circuit



See Table 9 for a list of components.

Fig 2. Component layout for class-AB production test circuit

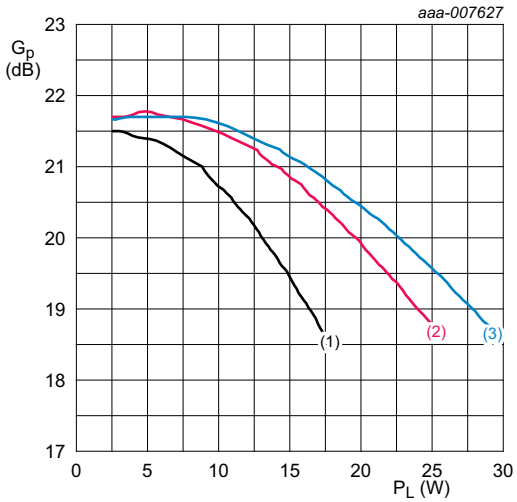
Table 9. List of components

For test circuit see Figure 2.

Component	Description	Value	Remarks
C11, C21, C32, C42	multilayer ceramic chip capacitor	10 μF, 50 V	
C12, C22, C33, C43	multilayer ceramic chip capacitor	1 μF, 50 V	
C13, C23, C34, C44	multilayer ceramic chip capacitor	43 pF	ATC100B
C14, C24, C36, C46	multilayer ceramic chip capacitor	43 pF	ATC100A
C31, C41	electrolytic capacitor	220 μF, 63 V	
C35, C45	multilayer ceramic chip capacitor	3.3 pF	ATC100B
R11, R21	chip resistor	10 Ω	Multi Comp SMD 1206
S1	socket	-	Johnstech

7.4 Graphical data

7.4.1 2-Carrier W-CDMA



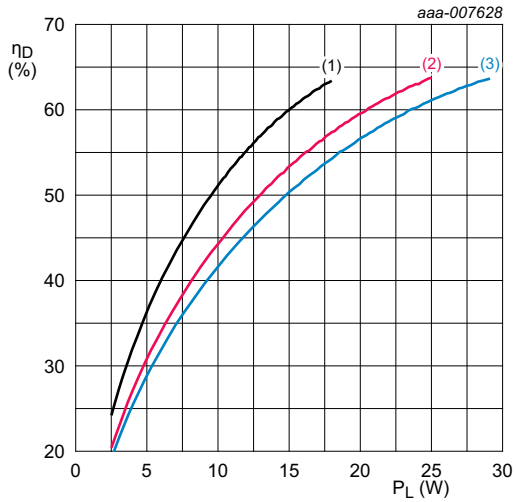
V_{DS} = 28 V; I_{Dq} = 224 mA; carrier spacing = 5 MHz; f_c = 960 MHz

(1) V_{DS} = 24 V

(2) V_{DS} = 28 V

(3) V_{DS} = 32 V

Fig 3. Power gain as a function of output power per section; typical values



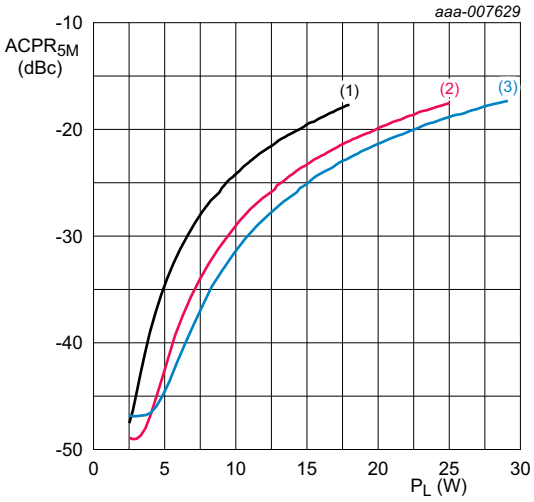
V_{DS} = 28 V; I_{Dq} = 224 mA; carrier spacing = 5 MHz; f_c = 960 MHz

(1) V_{DS} = 24 V

(2) V_{DS} = 28 V

(3) V_{DS} = 32 V

Fig 4. Drain efficiency as a function of output power per section; typical values



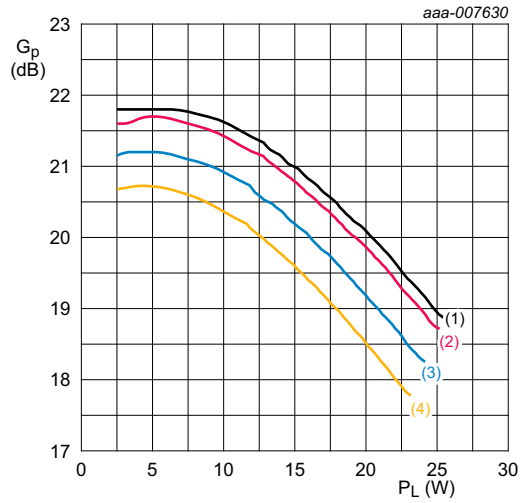
V_{DS} = 28 V; I_{Dq} = 224 mA; carrier spacing = 5 MHz; f_c = 960 MHz

(1) V_{DS} = 24 V

(2) V_{DS} = 28 V

(3) V_{DS} = 32 V

Fig 5. Adjacent channel power ratio (5 MHz) as a function of output power per section; typical values



V_{DS} = 28 V; I_{Dq} = 224 mA; carrier spacing = 5 MHz; f_c = 960 MHz

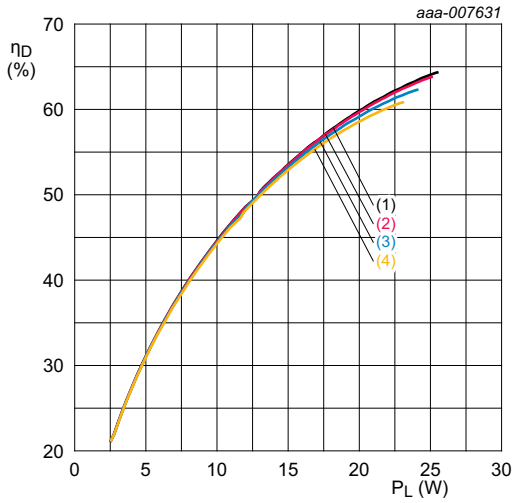
(1) T_{case} = 15 °C

(2) T_{case} = 25 °C

(3) T_{case} = 55 °C

(4) T_{case} = 85 °C

Fig 6. Power gain as a function of output power per section; typical values



V_{DS} = 28 V; I_{Dq} = 224 mA; carrier spacing = 5 MHz; f_c = 960 MHz

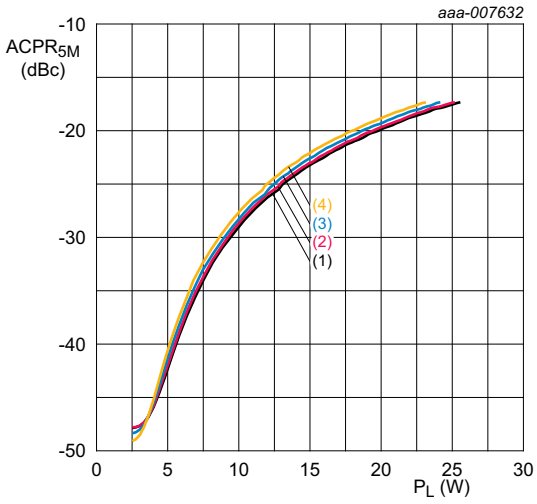
(1) T_{case} = 15 °C

(2) T_{case} = 25 °C

(3) T_{case} = 55 °C

(4) T_{case} = 85 °C

Fig 7. Drain efficiency as a function of output power per section; typical values



V_{DS} = 28 V; I_{Dq} = 224 mA; carrier spacing = 5 MHz; f_c = 960 MHz

(1) T_{case} = 15 °C

(2) T_{case} = 25 °C

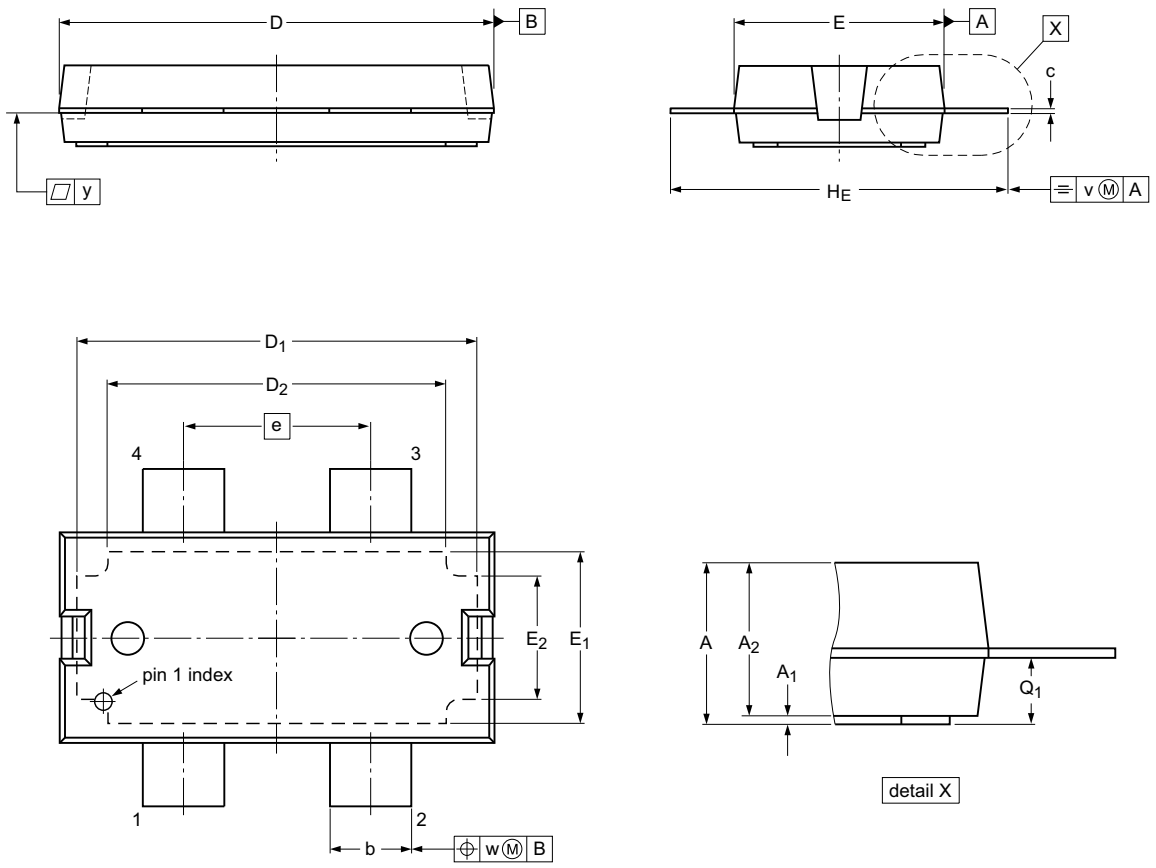
(3) T_{case} = 55 °C

(4) T_{case} = 85 °C

Fig 8. Adjacent channel power ratio (5 MHz) as a function of output power per section; typical values

8. Package outline

HSOP4F: plastic, heatsink small outline package; 4 leads(flat) **SOT1223-1**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	b	c	$D^{(1)}$	D_1	D_2	$E^{(1)}$	E_1	E_2	e	H_E	Q_1	v	w	y
	max	3.9	0.2	3.65	3.90	0.27	20.62	19.00	16.05	10.01	8.18	5.89		16.16	1.62			
mm	nom		0.1	3.60	3.85	0.22	20.57	18.95	16.00	9.96	8.13	5.84	8.85	15.96	1.57	0.25	0.25	0.1
	min		0	3.55	3.80	0.17	20.52	18.90	15.95	9.91	8.08	5.79		15.76	1.52			

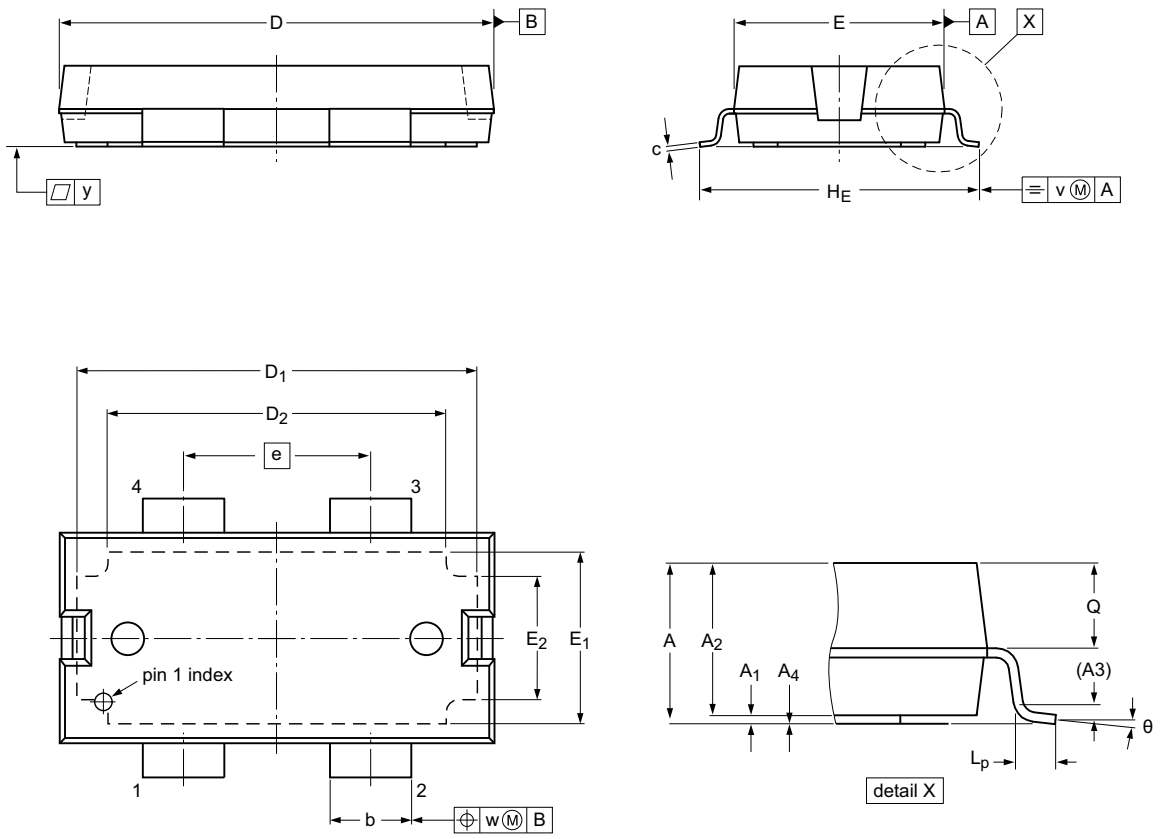
Note
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

sot1223-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1223-1						~~12-03-06~~ 12-04-25

Fig 9. Package outline SOT1223-1 (HSOP4F)

HSOP4: plastic, heatsink small outline package; 4 leads **SOT1224-1**



0 10 mm

scale

Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	A_3	A_4	b	c	$D^{(1)}$	D_1	D_2	$E^{(1)}$	E_1	E_2	e	H_E	L_p	Q	v	w	y	θ
	max	3.9	0.2	3.65		0.06	3.90	0.27	20.62	19.00	16.05	10.01	8.18	5.89		13.5	1.10	2.07				7°
mm	nom		0.1	3.60	0.35	0	3.85	0.22	20.57	18.95	16.00	9.96	8.13	5.84	8.85	13.2	0.95	2.02	0.25	0.25	0.1	3°
	min		0	3.55		-0.02	3.80	0.17	20.52	18.90	15.95	9.91	8.08	5.79		12.9	0.80	1.97				0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

sot1224-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1224-1						~~12-03-12~~ 12-04-25

Fig 10. Package outline SOT1224-1 (HSOP4)

9. Handling information

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

10. Abbreviations

Table 10. Abbreviations

Acronym	Description
3GPP	3rd Generation Partnership Project
CCDF	Complementary Cumulative Distribution Function
DPCH	Dedicated Physical CHannel
ESD	ElectroStatic Discharge
GSM	Global System for Mobile Communications
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
LTE	Long Term Evolution
PAR	Peak-to-Average Ratio
SMD	Surface Mounted Device
VSWR	Voltage Standing-Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

11. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLP8G10S-45P_8G10S-45PG v.1	20130725	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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14. Contents

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