PRELIMINARY

CY7S1061G, CY7S1061GE

16-Mbit (1 M words × 16 bit) Static RAM with Deep-Sleep Feature and Error-Correcting Code (ECC)

Features

- High speed
  - t_{AA} = 10 ns
- Ultra-low power Deep Sleep (DS) current
  - I_{DS} = 22-µA maximum
- Low active and standby currents
  - I_{CC} = 90-mA typical
  - I_{SB2} = 20-mA typical
- Wide operating voltage range: 1.65 V to 2.2 V, 2.2 V to 3.6 V, and 4.5 V to 5.5 V
- Embedded error-correcting code (ECC) for single-bit error correction
- 1.0-V data retention
- Transistor-transistor logic (TTL) compatible inputs and outputs
- Error indication (ERR) pin to indicate 1-bit error detection and correction
- Available in Pb-free 48-pin TSOP I, 54-pin TSOP II, and 48-ball VFBGA packages

Functional Description

The CY7S1061G is a high-performance CMOS fast static RAM organized as 1,048,576 words by 16 bits. This device features fast access times (10 ns) and a unique ultra-low power Deep Sleep mode. With Sleep mode currents as low as 22 µA, the CY7S1061G device combines the best features of fast and low-power SRAM in industry-standard package options. The device also features embedded ECC[1]. ECC logic can detect and correct single-bit error in the accessed location. The CY7S1061GE device includes an ERR pin that signals an error-detection and correction event during a read cycle

To access devices with a single-chip enable input, assert the chip enable input ($\overline{CE}$) LOW. To access dual chip enable devices, assert both chip enable inputs – $\overline{CE}_1$ as LOW and CE_2 as HIGH.

To perform data writes, assert the Write Enable ($\overline{WE}$) input LOW, and provide the data and address on device data pins (I/O_0 through I/O_{15}) and address pins (A_0 through A_{19}) respectively. The Byte High Enable ($\overline{BHE}$) and Byte Low Enable ($\overline{BLE}$) inputs control byte writes, and write data on the corresponding I/O lines to the memory location specified. $\overline{BHE}$ controls I/O_8 through I/O_{15} and $\overline{BLE}$ controls I/O_0 through I/O_7.

To perform data reads, assert the Output Enable ($\overline{OE}$) input and provide the required address on the address lines. Read data is accessible on the I/O lines (I/O_0 through I/O_{15}). You can perform byte accesses by asserting the required byte enable signal ($\overline{BHE}$ or $\overline{BLE}$) to read either the upper byte or the lower byte of data from the specified address location.

All I/Os (I/O_0 through I/O_{15}) are placed in a high-impedance state when the device is deselected ($\overline{CE}$ HIGH for single chip enable devices and $\overline{CE}_1$ HIGH and CE_2 LOW for dual chip enable devices), or the control signals ($\overline{OE}$, $\overline{BLE}$, $\overline{BHE}$) are de-asserted.

The device is placed in a low power Deep Sleep mode when the Deep Sleep pin ($\overline{DS}$) is LOW. In this state, the device is disabled for normal operation and is placed in a data retention mode. The device can be activated by de-asserting the Deep Sleep pin ($\overline{DS}$ HIGH).

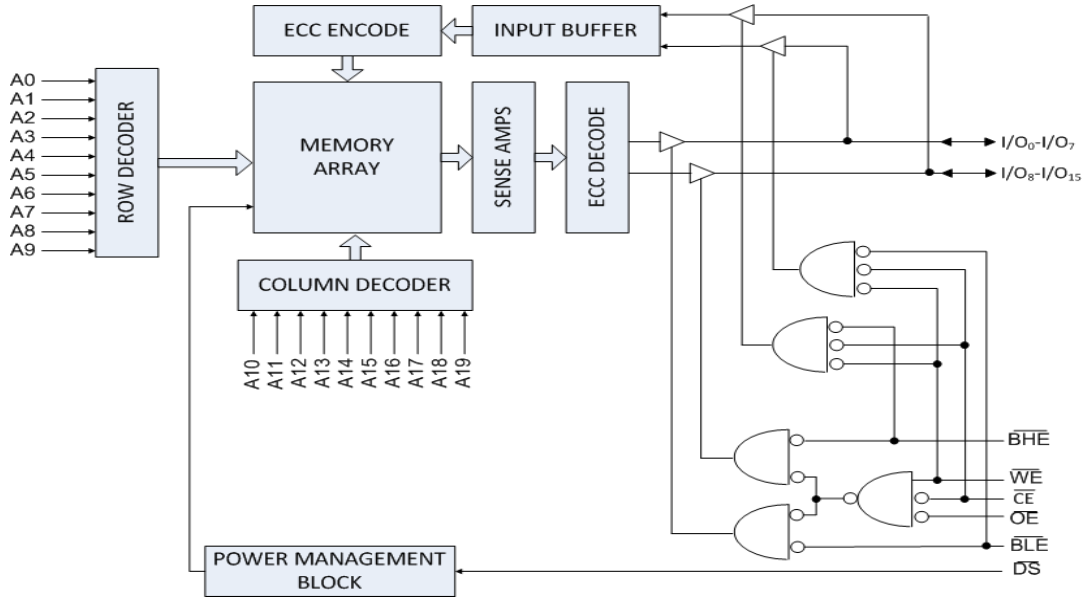
The CY7S1061G is available in 48-pin TSOP I, 54-pin TSOP II, and 48-ball VFBGA packages.

Product Portfolio

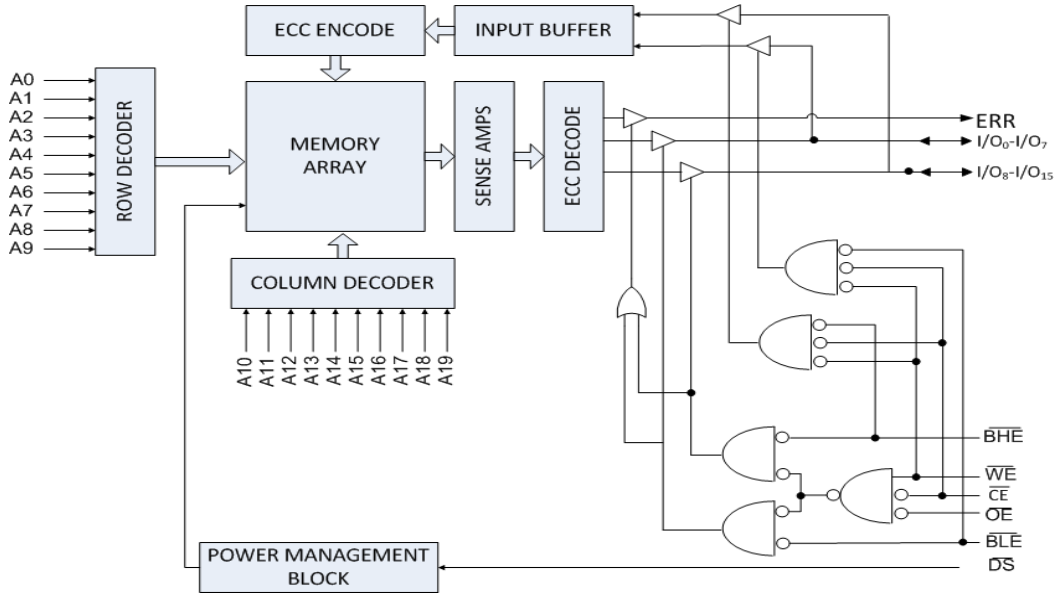
Product	Range	V_{CC} Range (V)	Speed (ns)	Current Consumption					
				Operating I_{CC} (mA) f = f_{max}		Standby, I_{SB2} (mA)		Deep-Sleep Current (µA)	
				Typ [2]	Max	Typ [2]	Max	Typ [1]	Max
CY7S1061G18	Industrial	1.65 V–2.2 V	15	70	80	20	30	8	22
CY7S1061G(E)30		2.2 V–3.6 V	10	90	110				
CY7S1061G		4.5–5.5 V	10	90	110				

Notes
1. This device does not support automatic write-back on error detection.
2. Typical values are included only for reference and are not guaranteed or tested. Typical values are measured at V_{CC} = 1.8 V (for a V_{CC} range of 1.65 V–2.2 V), V_{CC} = 3 V (for a V_{CC} range of 2.2 V–3.6 V), and V_{CC} = 5 V (for a V_{CC} range of 4.5 V–5.5 V), T_A = 25 °C.

Logic Block Diagram - CY7S1061G



Logic Block Diagram - CY7S1061GE



Contents

Pin Configurations

Figure 1. 48-ball VFBGA (6 × 8 × 1.0 mm) pinout (Top View) [3]

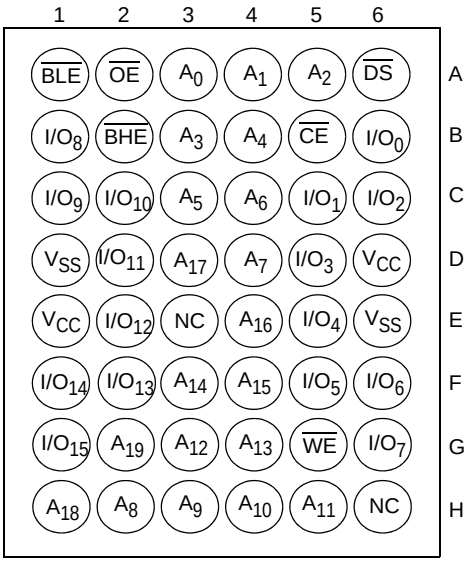
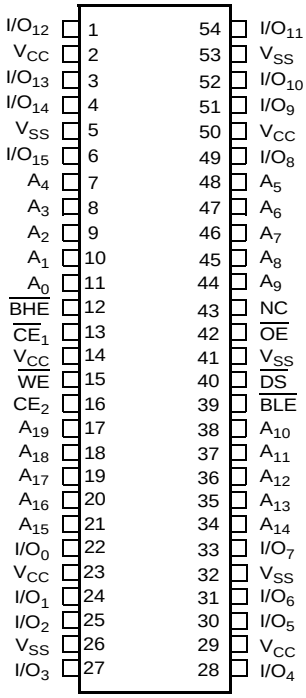


Figure 2. 54-pin TSOP II (22.4 × 11.84 × 1.0 mm) pinout [3]



Note
3. NC pins are not connected internally to the die.

Pin Configurations (continued)

Figure 3. 48-pin TSOP I (12 × 18.4 × 1 mm) pinout (Top View) [4]

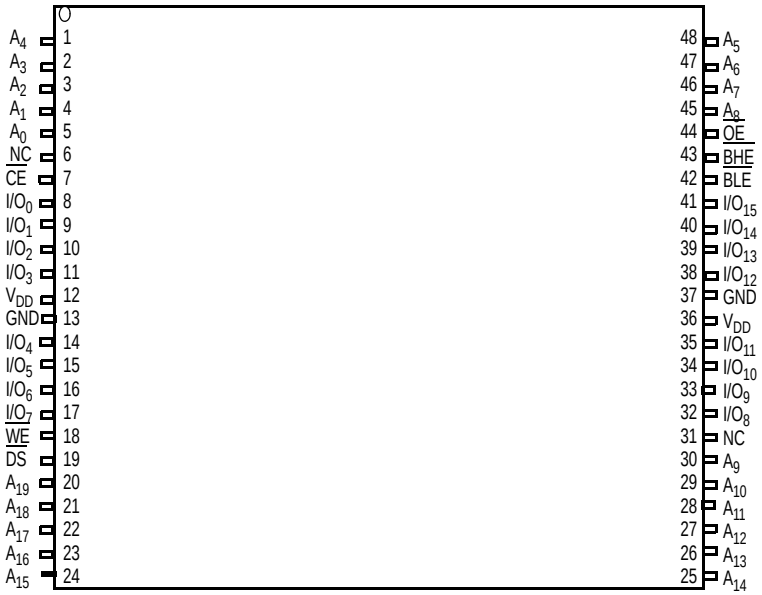
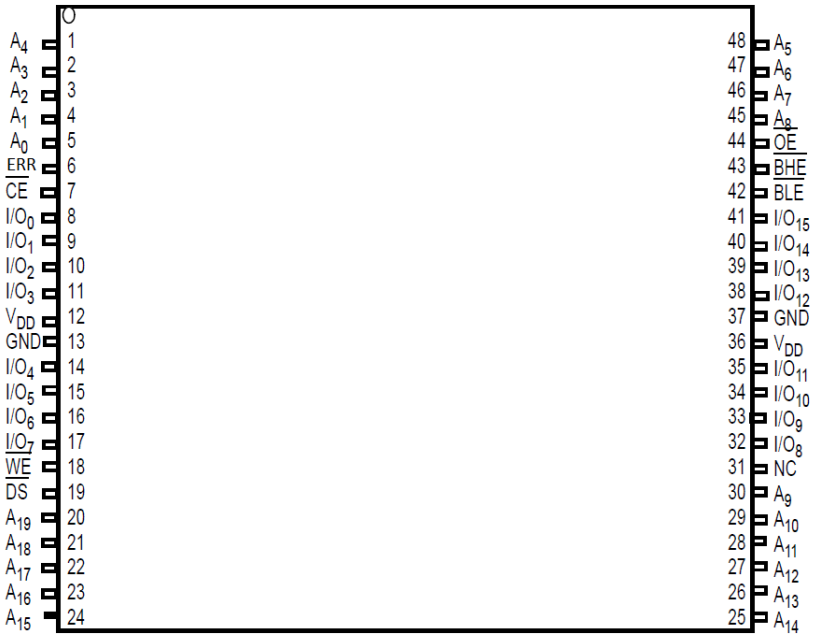


Figure 4. 48-pin TSOP I (12 × 18.4 × 1 mm) pinout, ERR output at pin 6 (Top View)



Note
4. NC pins are not connected internally to the die.

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature ..... –65 °C to +150 °C

Ambient temperature with power applied ..... –55 °C to +125 °C

Supply voltage on V_{CC} relative to GND[5] .....–0.5 V to +6.0 V

DC voltage applied to outputs in High Z State[5] .....–0.5 V to V_{CC} + 0.5 V

DC input voltage[5] .....–0.5 V to V_{CC} + 0.5 V

Current into outputs (LOW) ..... 20 mA

Static discharge voltage (MIL-STD-883, Method 3015) ..... > 2001 V

Latch-up current ..... > 140 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Industrial	–40 °C to +85 °C	1.65 V to 2.2 V, 2.2 V to 3.6 V, 4.5 V to 5.5 V

DC Electrical Characteristics

Over the operating range of –40 °C to +85 °C

Parameter	Description		Test Conditions		10 ns / 15 ns			Unit
					Min	Typ[8]	Max	
V_{OH}	Output HIGH voltage	1.65 V to 2.2 V	V_{CC} = Min, I_{OH} = –0.1 mA		1.4	–	–	V
		2.2 V to 2.7 V	V_{CC} = Min, I_{OH} = –1.0 mA		2.0	–	–	
		2.7 V to 3.6 V	V_{CC} = Min, I_{OH} = –4.0 mA		2.2	–	–	
		4.5 V to 5.5 V	V_{CC} = Min, I_{OH} = –4.0 mA		2.4	–	–	
V_{OL}	Output LOW voltage	1.65 V to 2.2 V	V_{CC} = Min, I_{OL} = 0.1 mA		–	–	0.2	V
		2.2 V to 2.7 V	V_{CC} = Min, I_{OL} = 2 mA		–	–	0.4	
		2.7 V to 3.6 V	V_{CC} = Min, I_{OL} = 8 mA		–	–	0.4	
		4.5 V to 5.5 V	V_{CC} = Min, I_{OL} = 8 mA		–	–	0.4	
V_{IH}[5, 6]	Input HIGH voltage	1.65 V to 2.2 V	–		1.4	–	V_{CC} + 0.2	V
		2.2 V to 2.7 V	–		2.0	–	V_{CC} + 0.3	
		2.7 V to 3.6 V	–		2.0	–	V_{CC} + 0.3	
		4.5 V to 5.5 V	–		2.2	–	V_{CC} + 0.5	
V_{IL}[5, 6]	Input LOW voltage	1.65 V to 2.2 V	–		–0.2	–	0.4	V
		2.2 V to 2.7 V	–		–0.3	–	0.6	
		2.7 V to 3.6 V	–		–0.3	–	0.8	
		4.5 V to 5.5 V	–		–0.5	–	0.8	
I_{IX}	Input leakage current		GND ≤ V_{IN} ≤ V_{CC}		–1.0	–	+1.0	µA
I_{OZ}	Output leakage current		GND ≤ V_{OUT} ≤ V_{CC}, Output disabled		–1.0	–	+1.0	µA
I_{CC}	V_{CC} operating supply current		V_{CC} = Max, I_{OUT} = 0 mA, CMOS levels	f = 100 MHz	–	90.0	110.0	mA
				f = 66.7 MHz	–	70.0	80.0	
I_{SB1}	Standby current – TTL inputs		Max V_{CC}, $\overline{CE}$[7] ≥ V_{IH}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}		–	–	40.0	mA
I_{SB2}	Standby current – CMOS inputs		Max V_{CC}, $\overline{CE}$[7] ≥ V_{CC} – 0.2 V, $\overline{DS}$ ≥ V_{CC} – 0.2 V, V_{IN} ≥ V_{CC} – 0.2 V or V_{IN} ≤ 0.2 V, f = 0		–	20.0	30.0	mA
I_{DS}	Deep-Sleep current		Max V_{CC}, $\overline{CE}$[7] ≥ V_{CC} – 0.2 V, $\overline{DS}$ ≤ 0.2 V, V_{IN} ≥ V_{CC} – 0.2 V or V_{IN} ≤ 0.2 V, f = 0		–	8.0	22.0	µA

Notes

5. V_{IL} (min) = –2.0 V and V_{IH} (max) = V_{CC} + 2 V for pulse durations of less than 2 ns.
6. For $\overline{DS}$ pin, V_{IH} (min) is V_{CC} – 0.2 V and V_{IL} (max) is 0.2 V.
7. For all dual chip enable devices, $\overline{CE}$ is the logical combination of $\overline{CE_1}$ and CE_2. When $\overline{CE_1}$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE_1}$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.
8. Typical values are included only for reference and are not guaranteed or tested. Typical values are measured at V_{CC} = 1.8 V (for a V_{CC} range of 1.65 V–2.2 V), V_{CC} = 3 V (for a V_{CC} range of 2.2 V–3.6 V), and V_{CC} = 5 V (for a V_{CC} range of 4.5 V–5.5 V), T_A = 25 °C.

Capacitance

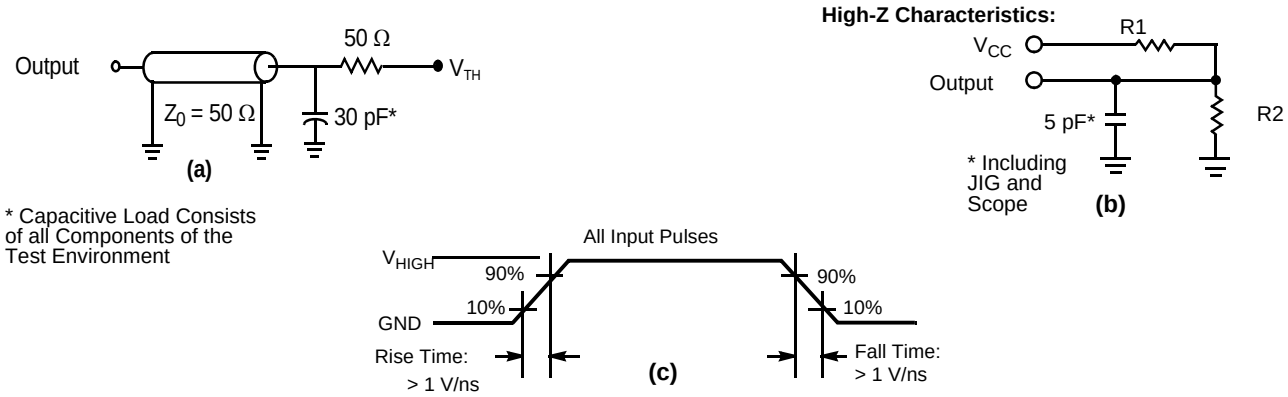
Parameter [9]	Description	Test Conditions	All packages	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, $V_{CC(typ)}$	10	pF
C_{OUT}	I/O capacitance		10	pF

Thermal Resistance

Parameter [9]	Description	Test Conditions	48-ball VFBGA	54-pin TSOP II	48-pin TSOP I	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four layer printed circuit board	31.50	93.63	57.99	°C/W
Θ_{JC}	Thermal resistance (junction to case)		15.75	21.58	13.42	°C/W

AC Test Loads and Waveforms

Figure 5. AC Test Loads and Waveforms[10]



Parameters	1.8 V	3.0 V	5.0 V	Unit
R1	1667	317	317	Ω
R2	1538	351	351	Ω
V_{TH}	V_{CC}/2	1.5	1.5	V
V_{HIGH}	1.8	3.0	3.0	V

Notes
9. Tested initially and after any design or process changes that may affect these parameters.
10. Full-device AC operation assumes a 100-µs ramp time from 0 to V_{CC} (min) and100-µs wait time after V_{CC} stabilizes to its operational value.

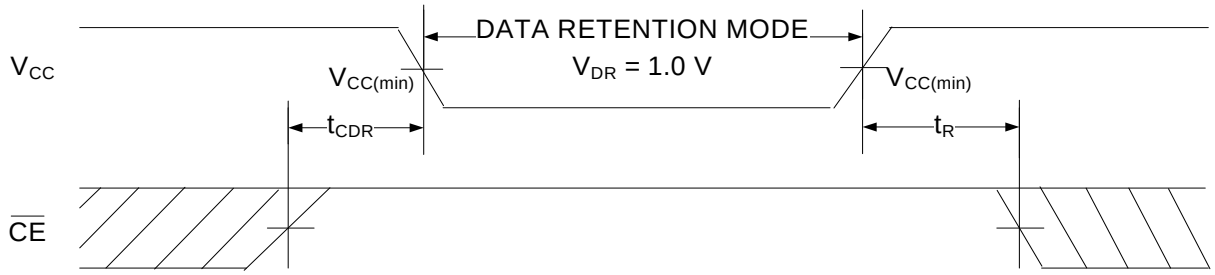
Data Retention Characteristics

Over the Operating Range of –40 °C to +85 °C

Parameter	Description	Conditions	Min	Max	Unit
V_{DR}	V_{CC} for data retention		1.0	–	V
I_{CCDR}	Data retention current	$V_{CC} = V_{DR}$, $\overline{CE} \geq V_{CC} - 0.2$ V, $\overline{DS} \geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V	–	30.0	mA
t_{CDR} [11]	Chip deselect to data retention time		0	–	ns
t_R[11]	Operation recovery time	2.2 V < $V_{CC} \leq$ 5.5 V	10.0	–	ns
		$V_{CC} \leq$ 2.2 V	15.0	–	ns

Data Retention Waveform

Figure 6. Data Retention Waveform[12, 13]



Notes

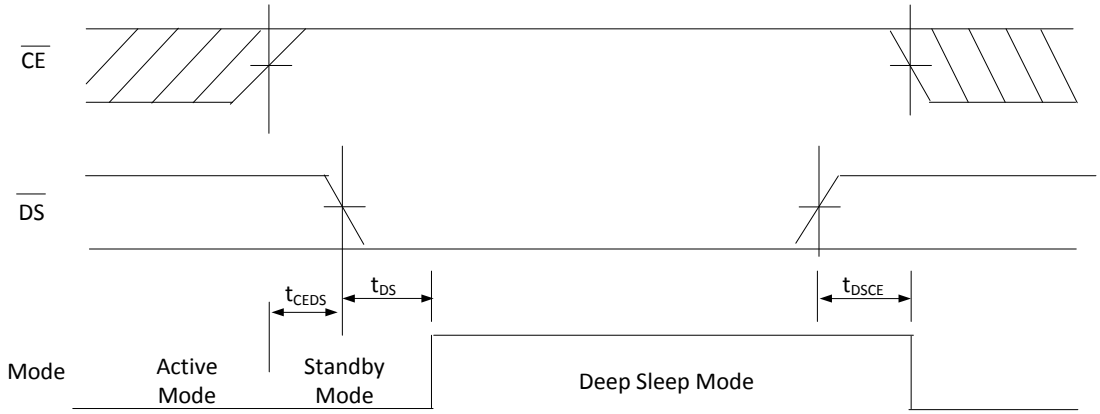
11. Tested initially and after any design or process changes that may affect these parameters.
12. Full device operation requires linear V_{CC} ramp from V_{DR} to V_{CC} (min) ≥ 100 µs or stable at V_{CC} (min) ≥ 100 µs.
13. For all dual chip enable devices, $\overline{CE}$ is the logical combination of $\overline{CE}_1$ and CE_2. When $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE}_1$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.

Deep-Sleep Mode Characteristics

Over the Operating Range of –40 °C to +85 °C

Parameter	Description	Conditions	Min	Max	Unit
I_{DS}	Deep Sleep Mode current	$V_{CC} = V_{CC}$ (max), $\overline{CE}$[14] $\geq V_{CC} - 0.2$ V, $\overline{DS} \leq 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V	–	22	µA
t_{CEDS} [14]	Time between de-assertion of $\overline{CE}$[14] and assertion of $\overline{DS}$		100	–	ns
t_{DS} [14]	$\overline{DS}$ assertion to Deep-Sleep mode transition time		–	1	ms
t_{DSCE} [14]	Time between de-assertion of $\overline{DS}$ and assertion of $\overline{CE}$[14]		1	–	ms

Figure 7. Active, Standby, and Deep-Sleep Operation Modes [15]



Notes
14. Address, data, and control lines should not toggle within t_{DS}. They should be fixed to one of the logic levels- V_{IH} or V_{IL}.
15. For all dual chip enable devices, $\overline{CE}$ is the logical combination of $\overline{CE}_1$ and CE_2. When $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE}_1$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.

AC Switching Characteristics

Over the operating range of –40 °C to +85 °C

Parameter [16]	Description	10 ns		15 ns		Unit
		Min	Max	Min	Max	
Read Cycle						
t_{power}	V_{CC} (stable) to the first access[17]	100.0	-	100.0	-	µs
t_{RC}	Read cycle time	10.0	–	15.0	–	ns
t_{AA}	Address to data valid / ERR valid	–	10.0	–	15.0	ns
t_{OHA}	Data / ERR hold from address change	3.0	–	3.0	–	ns
t_{ACE}	$\overline{CE}$ LOW to data valid / ERR valid	–	10.0	–	15.0	ns
t_{DOE}	$\overline{OE}$ LOW to data valid / ERR valid	–	5.0	–	8.0	ns
t_{LZOE}	$\overline{OE}$ LOW to low-Z[18 , 19]	0	–	1.0	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to high-Z[18 , 19]	–	5.0	–	8.0	ns
t_{LZCE}	$\overline{CE}$ LOW to low-Z[18, 19, 20]	3.0	–	3.0	–	ns
t_{HZCE}	$\overline{CE}$ HIGH to high-Z[18, 19, 20]	–	5.0	–	8.0	ns
t_{PU}	$\overline{CE}$ LOW to power-up[21]	0	–	0	–	ns
t_{PD}	$\overline{CE}$ HIGH to power-down[21]	–	10.0	–	15.0	ns
t_{DBE}	Byte enable to data valid	–	5.0	–	8.0	ns
t_{LZBE}	Byte enable to low-Z[18, 19]	0	–	1.0	–	ns
t_{HZBE}	Byte disable to high-Z[18, 19]	–	5.0	–	8.0	ns
Write Cycle[22, 23]						
t_{WC}	Write cycle time	10.0	–	15.0	–	ns
t_{SCE}	$\overline{CE}$ LOW to write end [20]	7.0	–	12.0	–	ns
t_{AW}	Address setup to write end	7.0	–	12.0	–	ns
t_{HA}	Address hold from write end	0	–	0	–	ns
t_{SA}	Address setup to write start	0	–	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	7.0	–	12.0	–	ns
t_{SD}	Data setup to write end	5.0	–	8.0	–	ns
t_{HD}	Data hold from write end	0	–	0	–	ns
t_{LZWE}	$\overline{WE}$ HIGH to low-Z [18, 19]	3.0	–	3.0	–	ns
t_{HZWE}	$\overline{WE}$ LOW to high-Z[18, 19]	–	5.0	–	8.0	ns
t_{BW}	Byte Enable to End of Write	7.0	–	12.0	–	ns

Notes

16. Test conditions assume signal transition time (rise/fall) of 3 ns or less, timing reference levels of 1.5 V (for $V_{CC} \geq 3$ V) and $V_{CC}/2$ (for $V_{CC} < 3$ V), and input pulse levels of 0 to 3 V (for $V_{CC} \geq 3$ V), and 0 to V_{CC} (for $V_{CC} < 3$V). Test conditions for the read cycle use the output loading shown in part (a) of Figure 5 on page 7, unless specified otherwise
17. t_{POWER} gives the minimum amount of time that the power supply is at stable V_{CC} until the first memory access is performed
18. t_{HZOE}, t_{HZCE}, t_{HZWE}, t_{HZBE}, t_{LZOE}, t_{LZCE}, t_{LZWE}, and t_{LZBE} are specified with a load capacitance of 5 pF, as shown in part (b) of Figure 5 on page 7. Transition is measured ±200 mV from steady state voltage.
19. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any device.
20. For all dual chip enable devices, $\overline{CE}$ is the logical combination of CE_1 and CE_2. When CE_1 is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when CE_1 is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.
21. These parameters are guaranteed by design and are not tested.
22. The internal write time of the memory is defined by the overlap of $\overline{WE} = V_{IL}$, $\overline{CE} = V_{IL}$, and $\overline{BHE}$ or $\overline{BLE} = V_{IL}$. These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
23. The minimum write pulse width for Write Cycle No. 2 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) should be the sum of t_{HZWE} and t_{SD}.

Switching Waveforms

Figure 8. Read Cycle No. 1 of CY7S1061G(Address Transition Controlled) [24, 25]

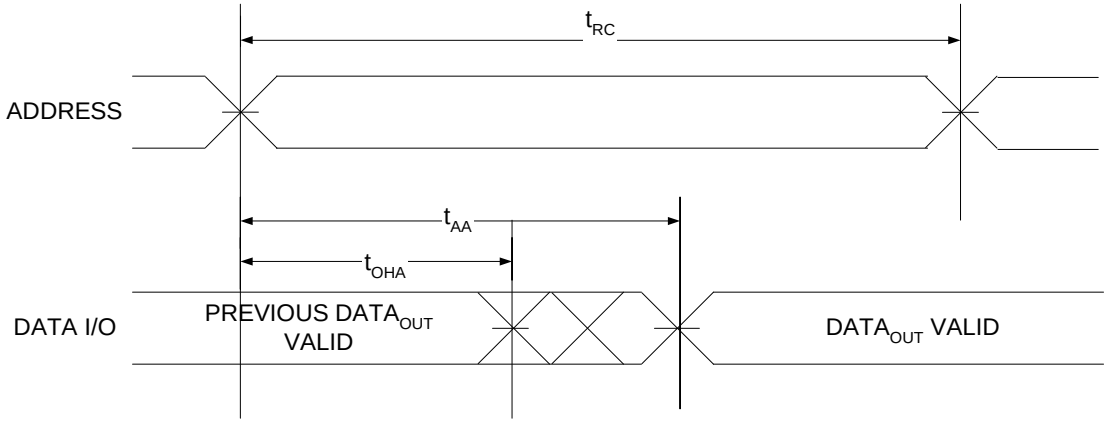
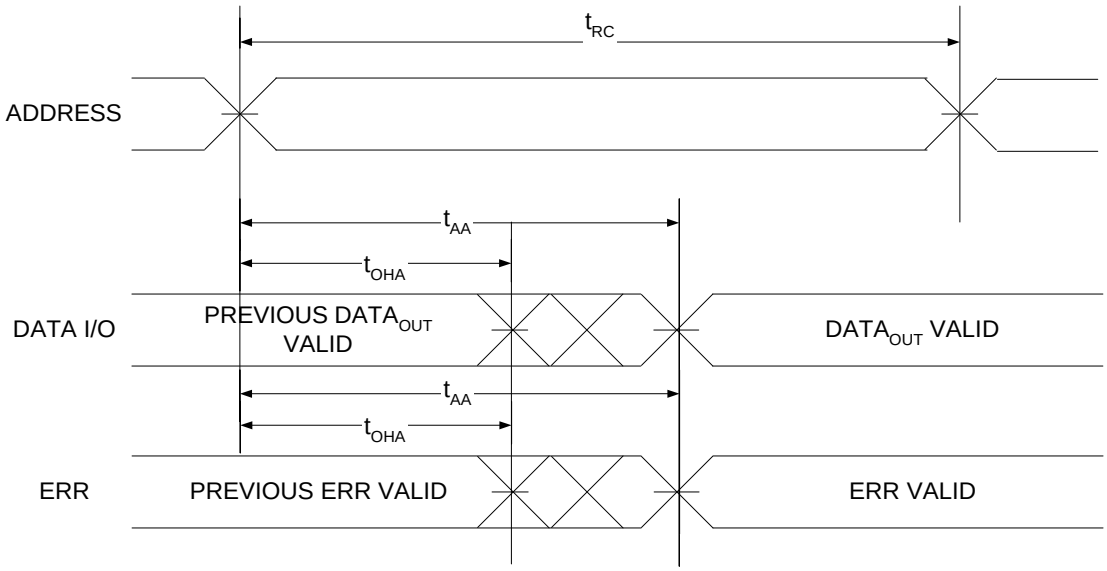


Figure 9. Read Cycle No. 2 of CY7S1061GE (Address Transition Controlled) [24, 25]



Notes
24. The device is continuously selected. $\overline{OE}$= V_{IL}, $\overline{CE}$ = V_{IL}, $\overline{BHE}$ or $\overline{BLE}$ or both = V_{IL}.
25. $\overline{WE}$ is HIGH for read cycle.

Switching Waveforms (continued)

Figure 10. Read Cycle No. 3 ($\overline{OE}$ Controlled) [26, 27, 28]

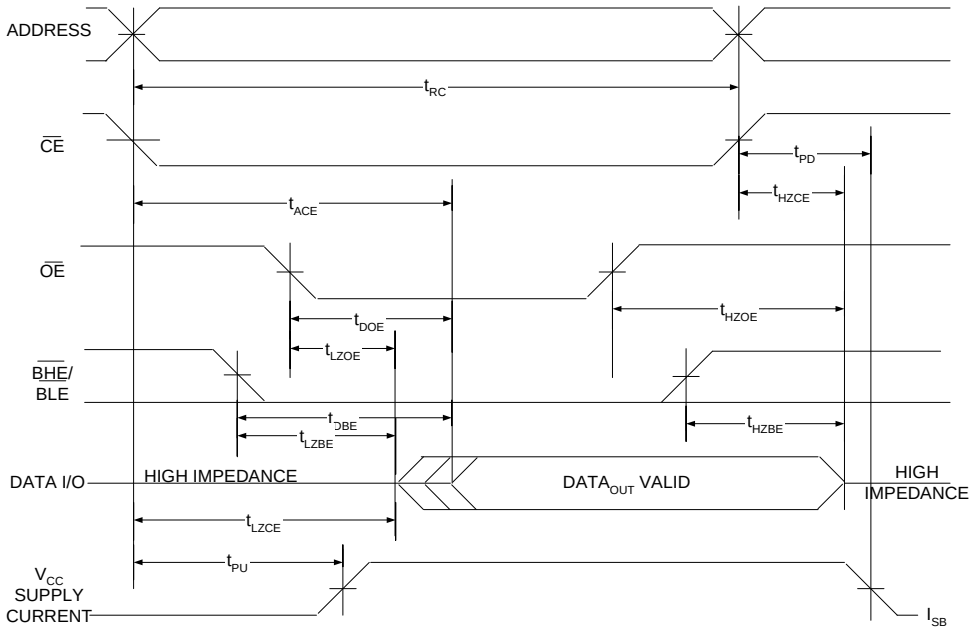
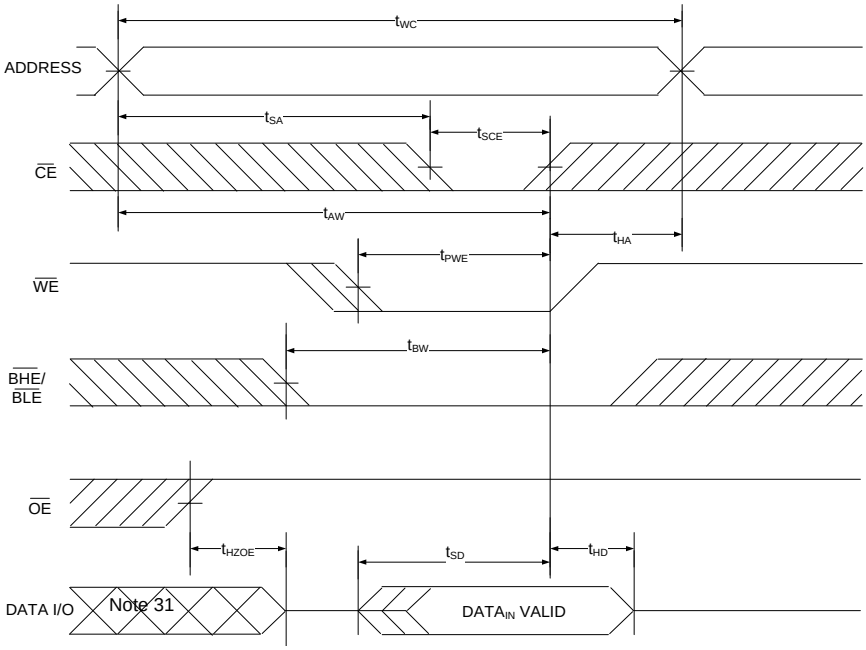


Figure 11. Write Cycle No. 1 ($\overline{CE}$ Controlled) [27, 29, 30]



Notes

26. $\overline{WE}$ is HIGH for read cycle.
27. For all dual chip enable devices, $\overline{CE}$ is the logical combination of $\overline{CE}_1$ and CE_2. When $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE}_1$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.
28. Address valid prior to or coincident with $\overline{CE}$ LOW transition.
29. The internal write time of the memory is defined by the overlap of $\overline{WE}$ = V_{IL}, $\overline{CE}$ = V_{IL} and $\overline{BHE}$ or $\overline{BLE}$ = V_{IL}. These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
30. Data I/O is in high-impedance state if $\overline{CE}$ = V_{IH}, or $\overline{OE}$ = V_{IH} or $\overline{BHE}$, and/or $\overline{BLE}$ = V_{IH}.
31. During this period, the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 12. Write Cycle No. 2 (WE Controlled, OE LOW) [32, 33, 34, 35]

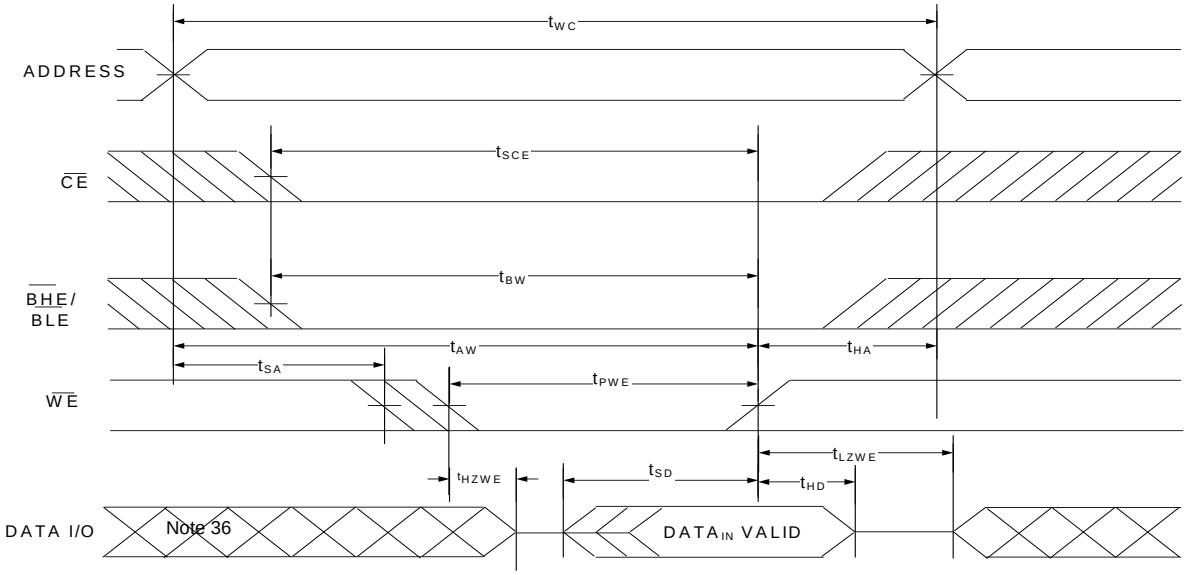
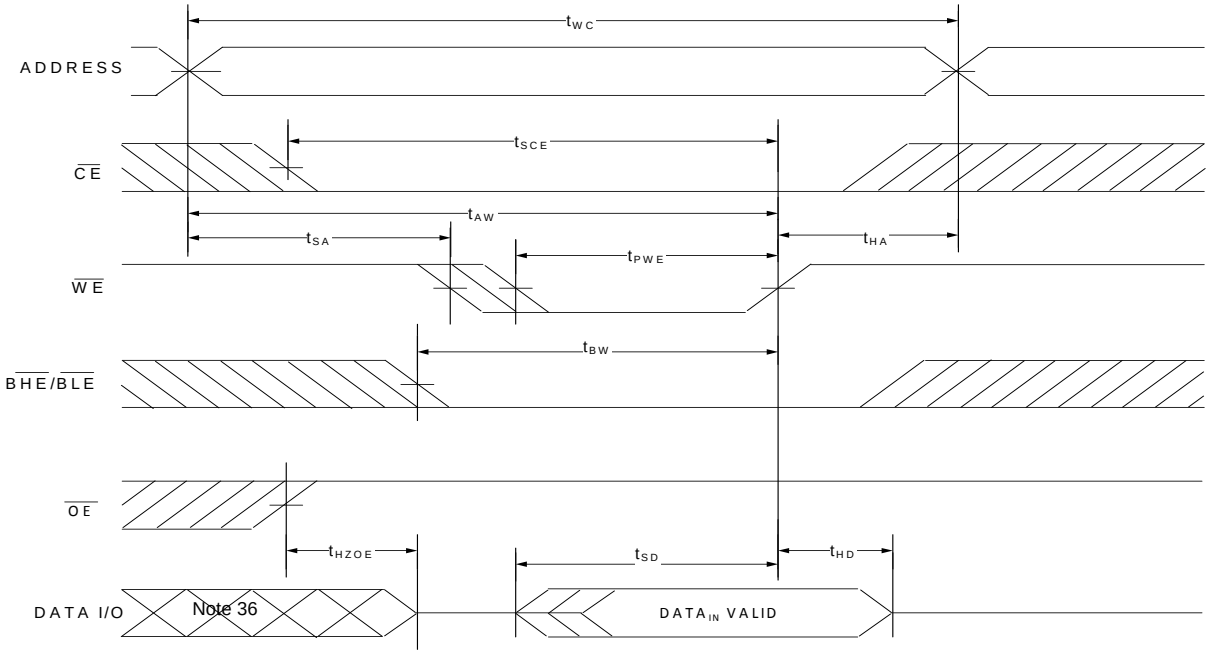


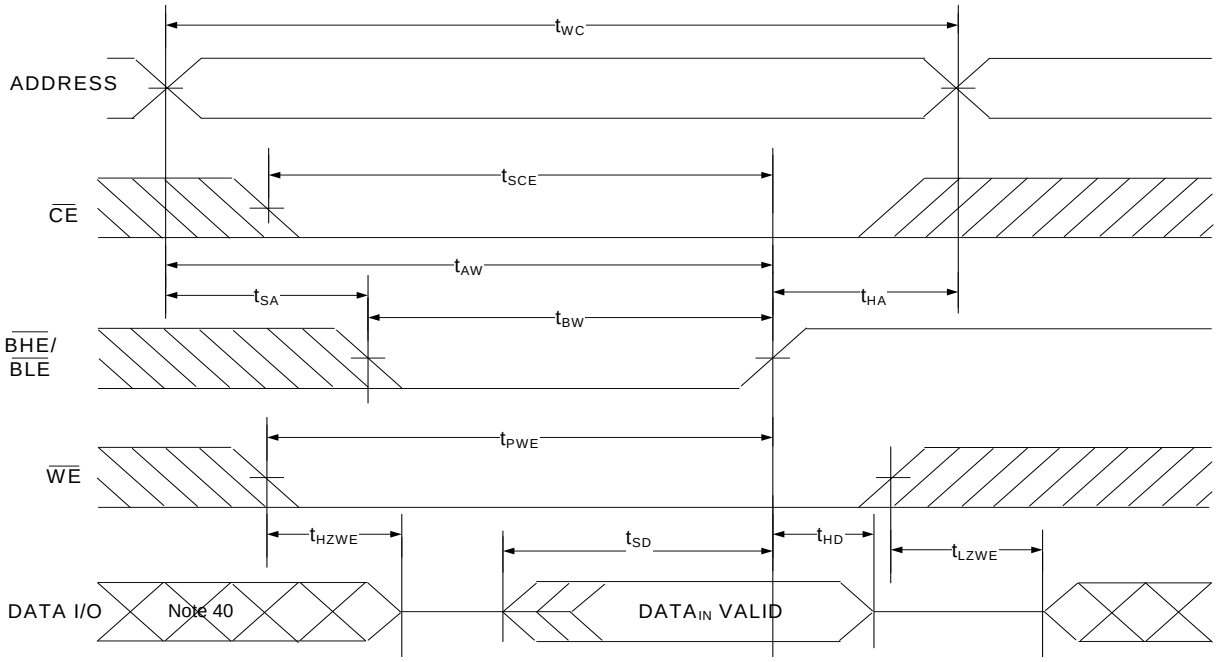
Figure 13. Write Cycle No. 3 (WE controlled) [32, 34, 35]



32. For all dual chip enable devices, $\overline{CE}$ is the logical combination of $\overline{CE}_1$ and CE_2. When $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE}_1$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.
33. The minimum write pulse width for Write Cycle No. 2 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) should be sum of t_{HZWE} and t_{SD}.
34. The internal write time of the memory is defined by the overlap of $\overline{WE} = V_{IL}$, $\overline{CE} = V_{IL}$ and $\overline{BHE}$ or $\overline{BLE} = V_{IL}$. These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
35. Data I/O is in high-impedance state if $\overline{CE} = V_{IH}$, or $\overline{OE} = V_{IH}$ or $\overline{BHE}$, and/or $\overline{BLE} = V_{IH}$.
36. During this period, the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 14. Write Cycle No. 3 ($\overline{BLE}$ or $\overline{BHE}$ Controlled) [37, 38, 39]



Notes

37. For all dual chip enable devices, $\overline{CE}$ is the logical combination of $\overline{CE}_1$ and CE_2. When $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE}_1$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.
38. The internal write time of the memory is defined by the overlap of $\overline{WE}$ = V_{IL}, $\overline{CE}$ = V_{IL} and $\overline{BHE}$ or $\overline{BLE}$ = V_{IL}. These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
39. Data I/O is in high-impedance state if $\overline{CE}$ = V_{IH}, or $\overline{OE}$ = V_{IH}, or $\overline{BHE}$, and/or $\overline{BLE}$ = V_{IH}.
40. During this period, the I/Os are in output state. Do not apply input signals.

Truth Table

$\overline{DS}$	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	I/O_0–I/O_7	I/O_8–I/O_{15}	Mode	Power
H	H	X[41]	X[41]	X[41]	X[41]	High-Z	High-Z	Standby	Standby (I_{SB})
H	L	L	H	L	L	Data out	Data out	Read all bits	Active (I_{CC})
H	L	L	H	L	H	Data out	High-Z	Read lower bits only	Active (I_{CC})
H	L	L	H	H	L	High-Z	Data out	Read upper bits only	Active (I_{CC})
H	L	X	L	L	L	Data in	Data in	Write all bits	Active (I_{CC})
H	L	X	L	L	H	Data in	High-Z	Write lower bits only	Active (I_{CC})
H	L	X	L	H	L	High-Z	Data in	Write upper bits only	Active (I_{CC})
H	L	H	H	X	X	High-Z	High-Z	Selected, outputs disabled	Active (I_{CC})
L[42]	H	X	X	X	X	High-Z	High-Z	Deep Sleep	Deep-Sleep Ultra Low Power (I_{DS})
L	L	X	X	X	X	–	–	Invalid mode[43]	–
H	L	X	X	H	H	High-Z	High-Z	Selected, outputs disabled	Active (I_{CC})

ERR Output – CY7S1061GE

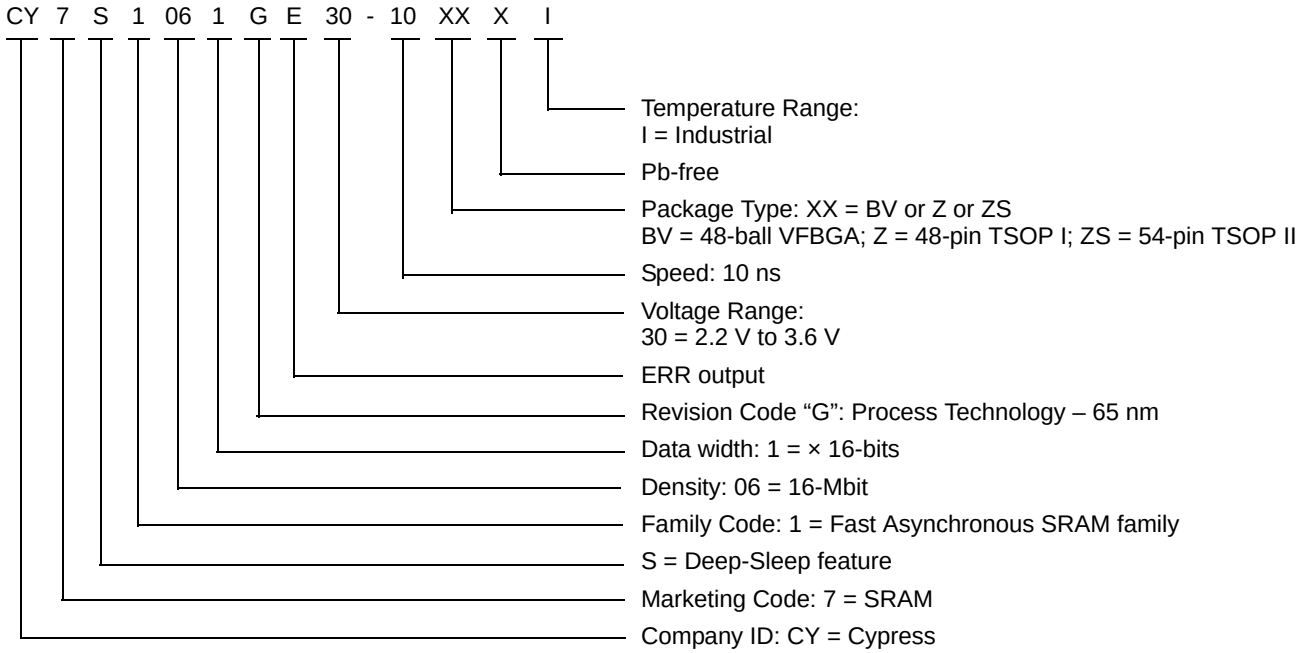
Output	Mode
0	Read operation, no single-bit error in the stored data.
1	Read operation, single-bit error detected and corrected.
High-Z	Device deselected or outputs disabled or Write operation

Notes
41. The input voltage levels on these pins should be either at V_{IH} or V_{IL}.
42. V_{IL} on $\overline{DS}$ must be $\leq$ 0.2 V.
43. This mode does not guarantee data retention. Power cycling needs to be performed for the device to return to normal operation.

Ordering Information

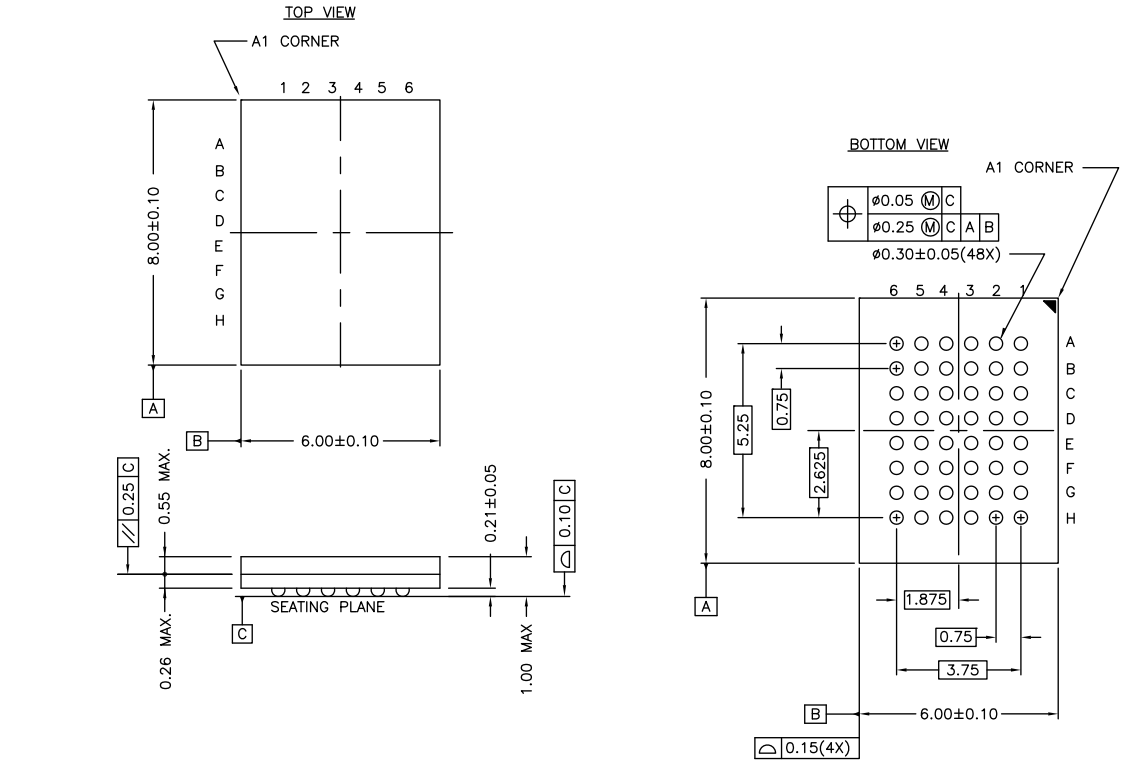
Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
10	CY7S1061G30-10BVXI	51-85150	48-ball VFBGA (6 × 8 × 1.0 mm) (Pb-free)	Industrial
	CY7S1061G30-10ZXI	51-85183	48-pin TSOP I (12 × 18.4 × 1.0 mm) (Pb-free)	
	CY7S1061G30-10ZSXI	51-85160	54-pin TSOP II (22.4 × 11.84 × 1.0 mm) (Pb-free)	
	CY7S1061GE30-10ZXI	51-85183	48-pin TSOP I (12 × 18.4 × 1.0 mm) (Pb-free), ERR output at pin 6	

Ordering Code Definitions



Package Diagrams

Figure 15. 48-ball VFBGA (6 × 8 × 1.0 mm) BV48/BZ48 Package Outline, 51-85150

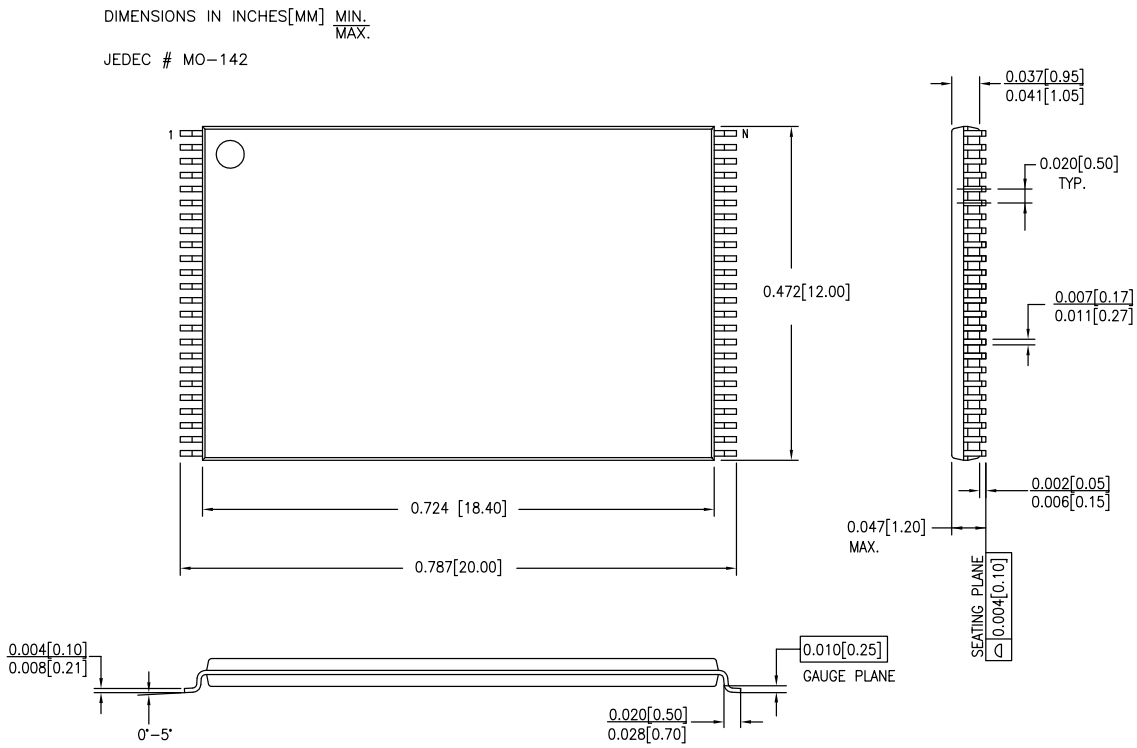


NOTE:
PACKAGE WEIGHT: See Cypress Package Material Declaration Datasheet (PMDD) posted on the Cypress web.

51-85150 *H

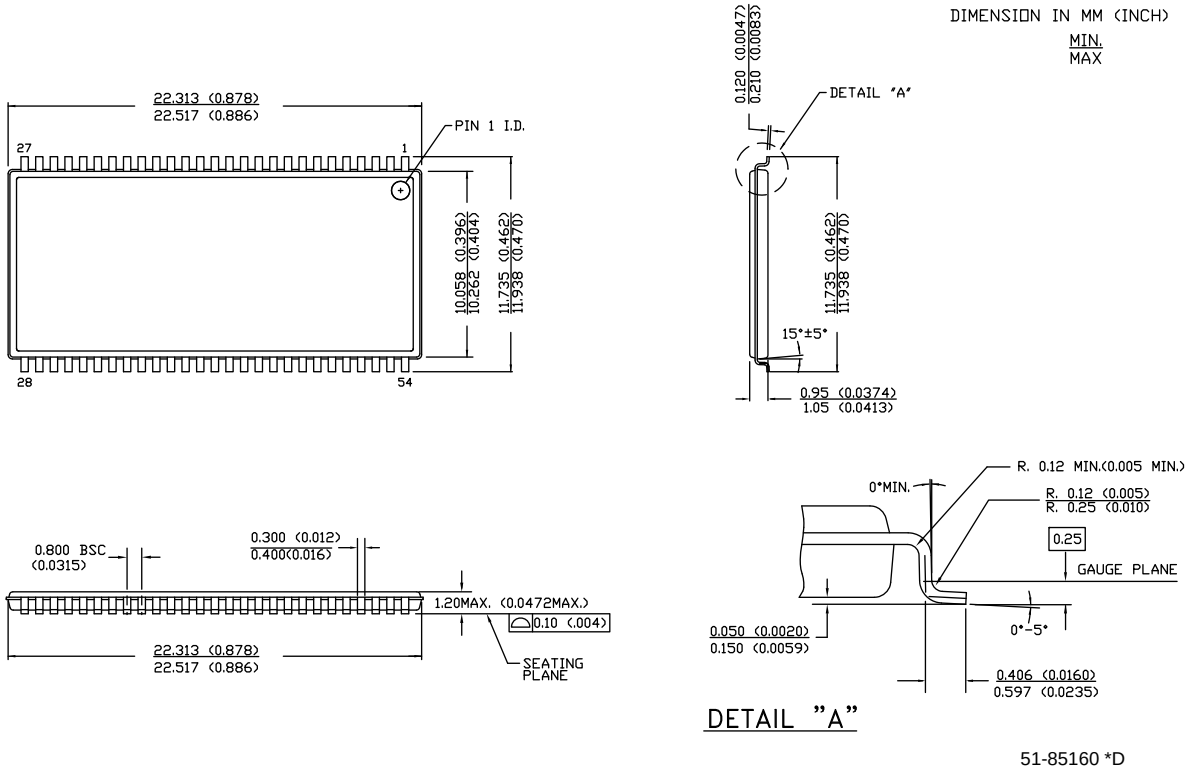
Package Diagrams (continued)

Figure 16. 48-pin TSOP I (12 × 18.4 × 1.0 mm) Z48A Package Outline, 51-85183



Package Diagrams (continued)

Figure 17. 54-pin TSOP II (22.4 × 11.84 × 1.0 mm) Z54-II Package Outline, 51-85160



Acronyms

Acronym	Description
$\overline{\text{BHE}}$	Byte High Enable
$\overline{\text{BLE}}$	Byte Low Enable
$\overline{\text{CE}}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/output
$\overline{\text{OE}}$	Output Enable
SRAM	Static random access memory
TTL	Transistor-transistor logic
VFBGA	Very fine-pitch ball grid array
$\overline{\text{WE}}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
µs	microsecond
mA	milliampere
mm	millimeter
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Errata

This section describes the errata for the 16-Mbit asynchronous FAST SRAM - CY7S1061G30 and CY7S1061GE30 - in 65-nm process technology. Details include errata trigger conditions, scope of impact, available workaround, and silicon revision applicability. Compare this document to the device's datasheet for a complete functional description.

If you have questions, contact your local Cypress Sales Representative or raise a technical support case at www.cypress.com/go/support.

Part Numbers Affected

Part Number	Device Characteristics
CY7S1061G30 (all packages and options)	16-Mbit FAST SRAM
CY7S1061GE30 (all packages and options)	16-Mbit FAST SRAM

FAST SRAM[44] Qualification Status

Product Status: All Engineering Samples (**Note:** Reliability qualification is not complete. These samples are recommended to be used only for engineering builds and evaluation, and not for production builds).

FAST SRAM[44] Errata Summary

This table defines the errata applicability to available 16-Mbit devices.

Items	Part Numbers	Silicon Rev	Fix Status
FAST SRAM [44] does not meet 10-ns speed-in AC switching parameters as specified in the datasheet specifications.	CY7S1061G30 CY7S1061GE30	*A	Fixed devices to be available from April 11, 2014.

■ Problem Definition

CY7S1061G30 and CY7S1061GE30 do not meet 10-ns speed in AC switching parameters as specified in Table 1.

■ Parameters Affected

AC switching parameters

■ Trigger Condition

Functionality is not guaranteed when the device is operated at speed of 10 ns.

■ Scope of Impact

This issue may not pose problems for most end systems because they may incorporate some margin to the datasheet specifications. The deviation from the datasheet specified limit of 10 ns is 2 ns.

■ Workaround

The RAM controller timing needs additional margin to accommodate the slower speed.

■ Fix Status

The fix for the above issue is in progress. Fixed devices will be available from April 11, 2014.

Note
44. This applies to all MPNs mentioned in Part Numbers Affected.

AC Switching Characteristics

Table 1. Comparison of AC Switching Parameters for 10 ns and 12 ns part

Parameter	Description	–10 ns		–12 ns		Unit
		Min	Max	Min	Max	
Read Cycle						
t_{RC}	Read cycle time	10	–	12	–	ns
t_{AA}	Address to data valid	–	10	–	12	ns
t_{OHA}	Data hold from address change	3	–	3	–	ns
t_{ACE}	$\overline{CE}$ Low to data valid	–	10	–	12	ns
t_{DOE}	$\overline{OE}$ Low to data valid	–	5	–	7	ns
t_{LZOE}	$\overline{OE}$ Low to low-Z	1	–	1	–	ns
t_{HZOE}	$\overline{OE}$ High to high-Z	–	5	–	7	ns
t_{LZCE}	$\overline{CE}$ Low to low-Z	3	–	3	–	ns
t_{HZCE}	$\overline{CE}$ High to high-Z	–	5	–	7	ns
t_{PU}	$\overline{CE}$ Low to power-up	0	–	0	–	ns
t_{PD}	$\overline{CE}$ High to power-down	–	10	–	12	ns
t_{DBE}	Byte Enable to data valid	–	5	–	7	ns
t_{LZBE}	Byte Enable to low-Z	1	–	1	–	ns
t_{HZBE}	Byte Disable to high-Z	–	6	–	7	ns
Write Cycle						
t_{WC}	Write cycle time	10	–	12	–	ns
t_{SCE}	$\overline{CE}$ Low to write end	7	–	9	–	ns
t_{AW}	Address setup to write end	7	–	9	–	ns
t_{HA}	Address hold from write end	0	–	0	–	ns
t_{SA}	Address setup to write start	0	–	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	7	–	9	–	ns
t_{SD}	Data setup to write end	5	–	7	–	ns
t_{HD}	Data hold from write end	0	–	0	–	ns
t_{LZWE}	$\overline{WE}$ High to low-Z	3	–	3	–	ns
t_{HZWE}	$\overline{WE}$ Low to high-Z	–	5	–	7	ns
t_{BW}	Byte Enable to end of write	7	–	9	–	ns

Document History Page

Document Title: CY7S1061G/CY7S1061GE, 16-Mbit (1 M words × 16 bit) Static RAM with Deep-Sleep Feature and Error Correcting Code (ECC) Document Number: 001-79707				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	3656657	TAVA	06/26/2012	New data sheet.
*A	3776318	AJU	10/30/2012	Updated Document Title to “16-Mbit (1 M words × 16 bit) Static RAM with Deep-Sleep Feature”. Updated Features: Highlighted typical and standby currents. Changed operating voltage range from “1.65 V to 5.5 V” to “1.65 V to 2.2 V, 2.2 V to 3.6 V, 4.5 V to 5.5 V”. Added 48-pin TSOP I and 54-pin TSOP II pinouts, packages, and all related parameters. Updated Functional Description (for better clarity). Removed Selection Guide. Updated Logic Block Diagram - CY7S1061G (for better clarity). Updated Pin Configurations: Updated Note 3 (for better clarity). Updated Product Portfolio to list all product options. Added typical values for I_{CC} and I_{SB2} parameters. Split V_{CC} range in the second row from “2.2 V–5.5 V” into two rows namely “2.2 V–3.6 V” and “4.5 V to 5.5 V”. Updated Note 1 for better clarity. Updated Operating Range: Changed V_{CC} from “1.65 V to 5.5 V” to “1.65 V to 2.2 V, 2.2 V to 3.6 V, 4.5 V to 5.5 V”. Changed latch up current limit from 200 to 140 mA (per JEDEC limits). Updated DC Electrical Characteristics: Changed maximum value of I_{CC} parameter from 100 mA to 110 mA for the Test Condition f = 100 MHz. Changed maximum value of I_{SB1} parameter from 30 mA to 40 mA. Changed maximum value of I_{SB2} parameter from 25 mA to 30 mA. Updated I_{SB2} and I_{DS} test conditions to reflect correct CMOS input levels. Added footnotes 6 and 7. Updated Capacitance (Changed C_{IN} and C_{OUT} values from 8 pF to 10 pF). Updated Thermal Resistance (Changed Thermal resistance values for 48-ball VFBGA from 28.37, 5.79 to 31.50, 13.75 °C/W). Updated AC Test Loads and Waveforms (Added values for V_{HIGH} parameter in the table). Updated Data Retention Characteristics: Changed maximum value of I_{CCDR} parameter from 25 mA to 30 mA. Added t_{CEDS} and t_{DSCE} parameters and their details. Updated Note 12 (for better clarity).

Document History Page (continued)

Document Title: CY7S1061G/CY7S1061GE, 16-Mbit (1 M words × 16 bit) Static RAM with Deep-Sleep Feature and Error Correcting Code (ECC) Document Number: 001-79707				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
*A (cont.)	3776318	AJU	10/30/2012	Updated AC Switching Characteristics: Removed t_{POWER} parameter and associated note "t_{POWER} gives the minimum amount of time that the power supply is at typical V_{CC} values until the first memory access" (spec captured in Note 7). Removed the note "The minimum write cycle time for Write Cycle No. 2 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}." and its references. Updated Note 13 to include difference in input levels for V_{CC} operation of less than 3 V. Updated Note 22 for better clarity. Updated Switching Waveforms: Updated Note 28 to correct typos. Updated Truth Table: Added Notes 41 and 42. Updated Ordering Information. Updated Package Diagrams.
*B	4003550	AJU	05/17/2013	No technical updates.
*C	4116197	MEMJ	09/06/2013	Updated Document Title to "16-Mbit (1 M words × 16 bit) Static RAM with Deep-Sleep Feature and Error Correcting Code (ECC)". Updated Features: Changed I_{SB2} from 30 mA Typical to 20mA Typical. Added "Embedded Error Correcting Code (ECC) for single-bit error correction" Updated V_{DR} from 1.5 V to 1 V. Updated Functional Description: Added ECC description. Updated Logic Block Diagram - CY7S1061G: Made CE_1 active low (Replaced CE_1 with $\overline{CE}_1$). Updated Data Retention Characteristics: Changed minimum value of V_{DR} from 1.5 V to 1.0 V. Updated Data Retention Waveform: Changed V_{DR} from 1.5 V to 1.0 V. Updated AC Switching Characteristics: Changed minimum value of t_{LZOE} parameter from 1 ns to 0 ns for 10 ns speed bin. Changed minimum value of t_{LZBE} parameter from 1 ns to 0 ns for 10 ns speed bin. Updated Ordering Information (Updated part numbers). Updated in new template.

Document History Page (continued)

Document Title: CY7S1061G/CY7S1061GE, 16-Mbit (1 M words × 16 bit) Static RAM with Deep-Sleep Feature and Error Correcting Code (ECC) Document Number: 001-79707				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
*D	4189510	MEMJ	11/12/2013	Updated Pin Configurations: Added Figure 4. Update DC Electrical Characteristics: Added minimum value of I_{SB2} parameter. Added Note 8 and referred the same note in minimum value of I_{SB2} parameter. Updated Deep-Sleep Mode Characteristics: Referred Note 15 in t_{CEDS} and t_{DSCE} parameters. Updated Ordering Information (Updated part numbers).
*E	4272659	MEMJ	02/06/2014	Updated Deep-Sleep Mode Characteristics: Renamed "I_{DSDR}" as "I_{DS}" in parameter column. Updated AC Switching Characteristics: Added Note 19 and referred the same note in description of t_{LZOE}, t_{HZOE}, t_{LZCE}, t_{HZCE}, t_{LZBE}, t_{HZBE}, t_{LZWE}, t_{HZWE} parameters.
*F	4292074	MEMJ/VINI	03/07/2014	Updated Features: Added logic block diagram for CY7S1061GE Specified I_{DS} value as 'maximum' Updated Product Portfolio Added I_{DS} typical of 8 µA. Update DC Electrical Characteristics: Added Column for Typical values in DC Electrical Characteristics Added I_{DS} typical of 8 µA Updated Note 10 to "Full device AC operation assumes a 100-µs ramp time from 0 to V_{CC} (min) and100-µs wait time after V_{CC} stabilization." Added Note 13 in Figure 6. Update AC Switching Characteristics Added t_{POWER} and associated Note 17 Added ERR timing information Updated t_{SD} from 5.5 ns to 5 ns. Added Note 23 and referred to write cycle timings Updated Switching Waveforms Changed title of Figure 8 from "Read Cycle No. 1" to "Read Cycle No. 1 of CY7S1061G" Added Figure 13 ($\overline{WE}$ controlled) Added Note 31 in Figure 11, Note 36 in Figure 12, and Note 40 in Figure 14 to indicate I/Os are in output state. Added condition to place outputs in the disable state by making both $\overline{BHE}$ and BLE HIGH in Truth Table. Added ERR output table Added Errata.
*G	4330547	AJU	04/02/2014	No content update.

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