

Small-sized Class-D Speaker Amplifiers

Filter-Less Class-D Monaural Speaker Amplifier

BD27400GUL

General Description

BD27400GUL is a low voltage drive class-D monaural speaker amplifier that was developed for cellular telephones, mobile audio products and the others.

The LC filter of the speaker output is unnecessary and the external part can compose a speaker amplifier at three.

Because the efficiency is high and is low consumption power with the class-D operation, it is the optimal for the application of the battery drive.

Also Current consumption of 0μ A when standby and fast transitions from standby to active with little pop noise make it is suitable for applications that switch repeatedly between suspended and active.

Features

- High output power
 2.5W typ.(VDD=5V, RL=4Ω, THD+N=10%, BTL)
- Very small package 9-Pin WL-CSP
- Gain selectable by external resistor
- LC Filter less
- Protection circuitry (Short protection, Thermal shutdown, Under voltage lockout)
- Analogue differential input / PWM digital output
- Pop noise suppression circuitry

Applications

■ Mobile phone, Smart phone, Digital video camera

Key Specifications

Operating voltage Range: 2.5V to 5.5V
 Circuit current(No signal): 2.9mA(Typ)
 Circuit current(Stand by): 0.1μA(Typ)
 Output Power(RL=8Ω): 0.85W(Typ)
 Output Power(RL=4Ω): 2.5W(Typ)
 Start-up time: 3.0msec(Typ)
 Operating Temperature Range: -40°C to +85°C

 Package(s)
 W(Typ) x D(Typ) x H(Max)

 VCSP50L1
 1.50mm x 1.50mm x 0.55mm



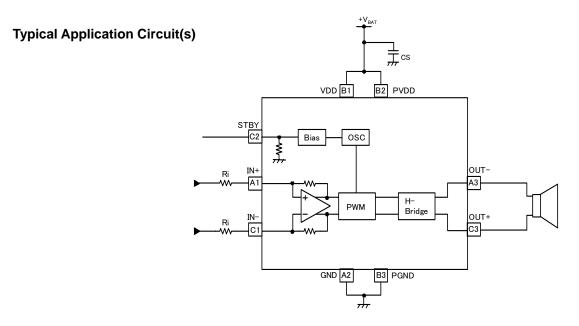


Figure 1. Application circuit

OProduct structure : Silicon monolithic integrated circuit OThis product has no designed protection against radioactive rays

Pin Configuration(s)

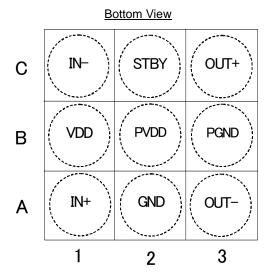


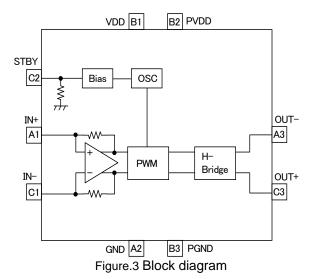
Figure.2 Pin configuration

Pin Description(s)

No.	Name	I/O	Function
A1	IN+	I	Positive input terminal
A2	GND	Р	GND terminal (Connect to PGND terminal)
А3	OUT-	0	Negative output terminal
B1	VDD	Р	Power supply terminal (Connect to PVDD terminal)
B2	PVDD	Р	Power supply terminal (Connect to VDD terminal)
В3	PGND	Р	Power GND terminal (Connect to GND terminal)
C1	IN-	I	Negative input terminal
C2	STBY	ı	Stand by control terminal
СЗ	OUT+	0	Positive output terminal

^{**}Connect VDD(B1) and PVDD(B2) on PCB board, and use a single power supply.

Block Diagram(s)



Absolute Maximum Ratings(Ta = 25°C)

Parameter	Symbol	Rating	Unit
Power Supply Voltage	VDDmax	7.0	V
Power Dissipation	Pd	0.69 ^(Note 1)	W
STBY Terminal Input Voltage Range	Vstby	-0.3 to VDD+0.3	V
IN+, IN- Terminal Voltage Range	Vin	-0.3 to VDD+0.3	V
Storage Temperature Range	Tstg	-55 to +150	°C
Maximum Junction Temperature	Tjmax	150	°C
Operating Temperature Range	Topr	-40 to +85	°C

⁽Note 1) Derating in done 5.52 mW/°C for operating above Ta≥25°C (Mount on 1-layer 50.0mm x 58.0mm x 1.6mm board)

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Conditions(Ta= -40°C to +85°C)

Parameter	Symbol	Min	Тур	Max	Unit
Power Supply Voltage	VDD	2.5	3.6	5.5	V
Common Mode Input Voltage Range	VIC	+0.5	-	VDD-0.8	V

Electrical Characteristics (Unless otherwise specified Ta=25°C, VDD=3.6V, R₁=80.BTL Connection)

Par	ameter	Symbol	Min	Тур	Max	Unit	Conditions
Circuit current (No signal)		I _{CC}	-	2.9	5.4	mA	Active mode, No load
Circuit current (S	tandby)	I _{STBY}	-	0.1	-	μΑ	Standby mode
Output power 1		P _{O1}	450	680	-	mW	8 Ω, f=1kHz, THD+N=1% *1
Output power 2		P _{O2}	550	850	-	mW	8 Ω, f=1kHz, THD+N=10% *1
Output power 3		P _{O3}	-	2.5	-	W	4 Ω, f=1kHz, THD+N=10% *1
Voltage gain		Gain	<u>285kΩ</u> Ri	<u>300kΩ</u> Ri	<u>315kΩ</u> Ri	V	BTL, RL=100kΩ
Total harmonic di	stortion	THD+N	-	0.18	-	%	8 Ω, f=1kHz,0.4W
Output noise volt	age	Vno	-	40	-	μVrms	A-weighting
Power supply ripp	ole rejection ratio	PSRR	-	64	-	dB	0.1Vp-p, f=217Hz
Common mode r	ejection ratio	CMRR	-	55	-	dB	0.1Vp-p, f=217Hz
Input impedance		Zin	-	150	-	kΩ	
Switching Frequency		fosc	200	250	300	kHz	_
Start-up time		Ton	1	3	5	msec	_
STBY	High level	V_{STBYH}	1.4	-	VDD	V	Active mode
threshold voltage	Low level	V _{STBYL}	0	-	0.4	V	Stand by mode
STBY input impe	R _{STBY}	210	300	390	kΩ		

^{*1:} Band-width = $400 \sim 30 \text{kHz}$, BTL=Bridge Tied Load (Voltage between A3-C3.)

≪Gain adjustment≫

Please use a gain adjustment below 26dB (Input Resistor Ri≥15kΩ)

Typical Performance Curves

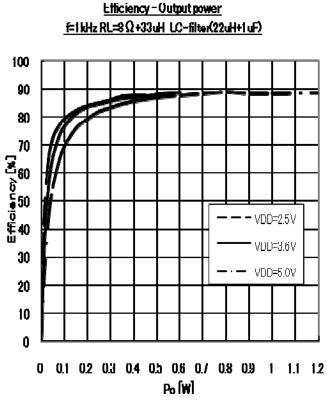


Figure.4

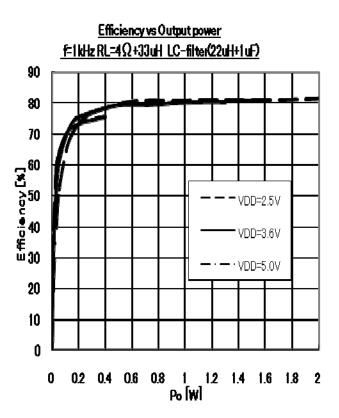


Figure.5

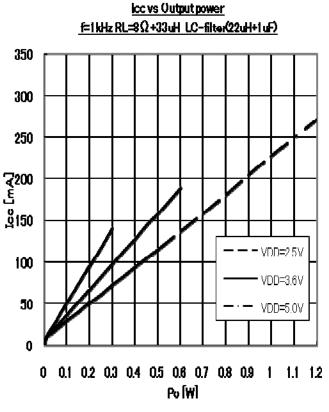


Figure.6

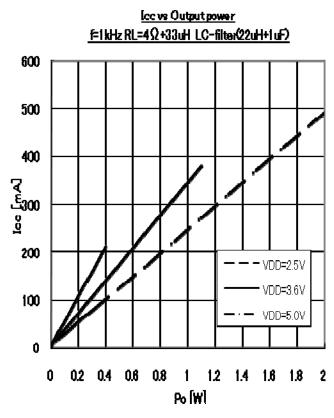
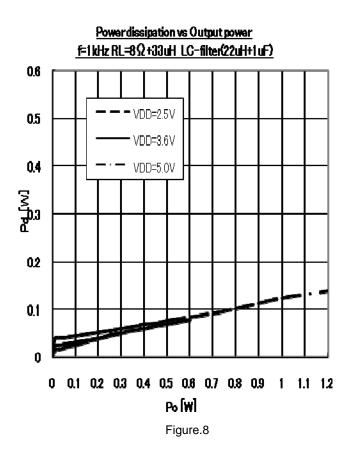
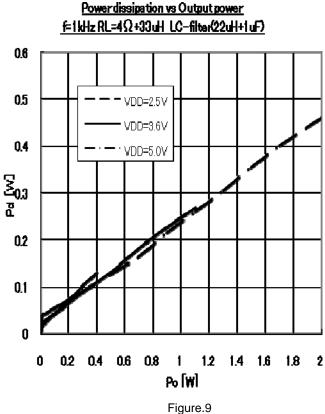
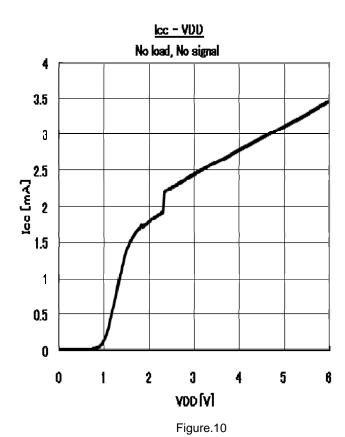
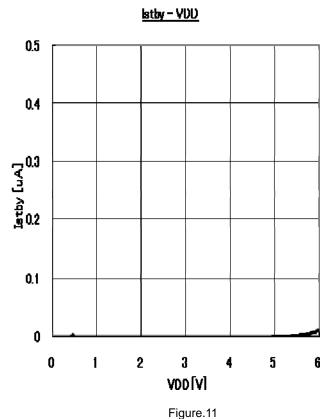


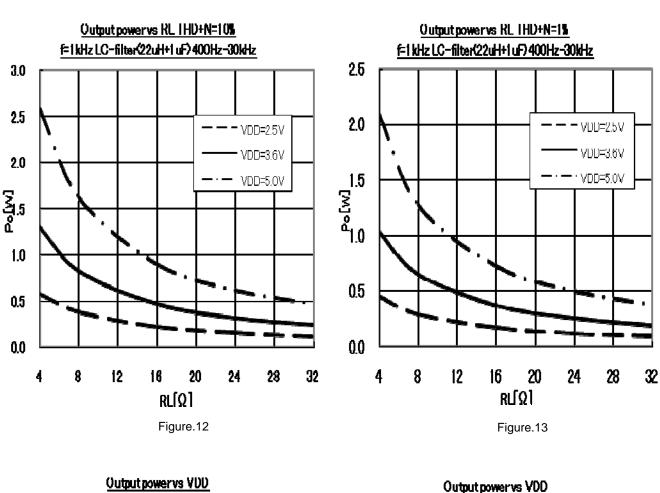
Figure.7

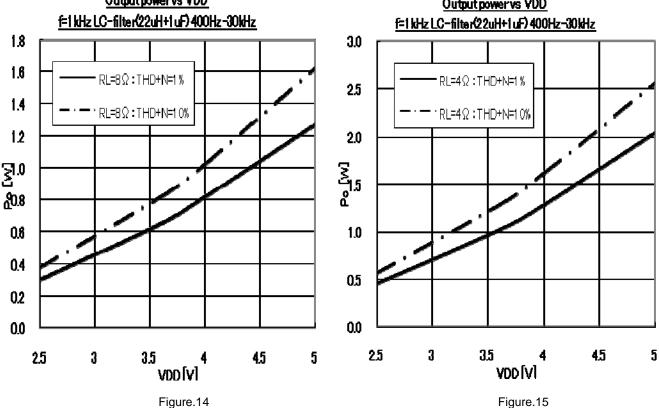


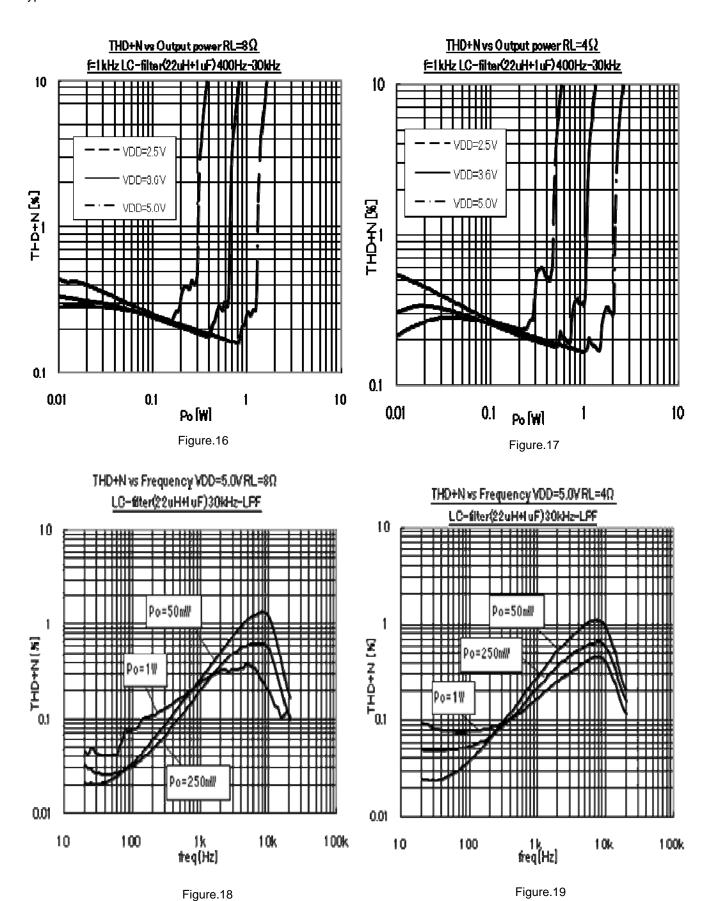


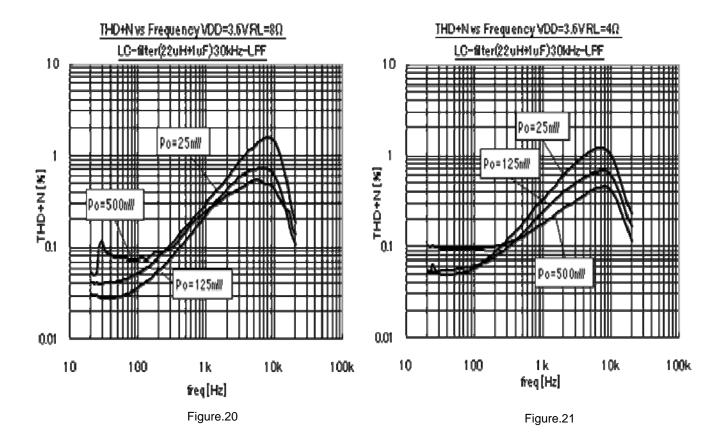


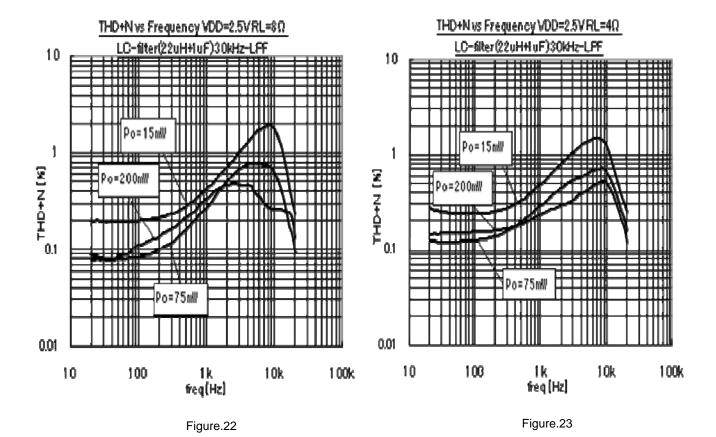


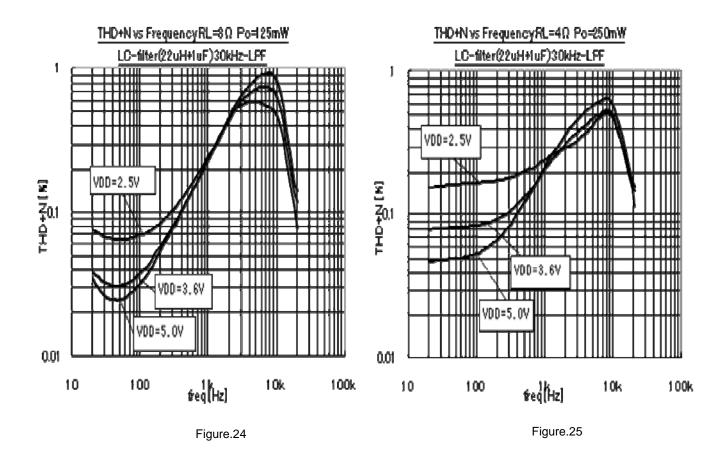


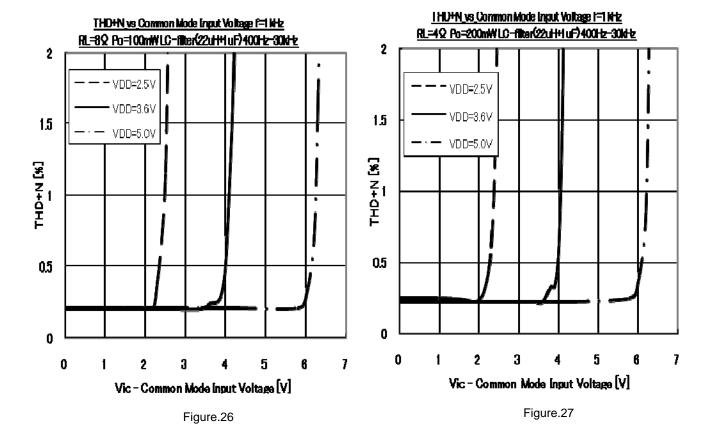




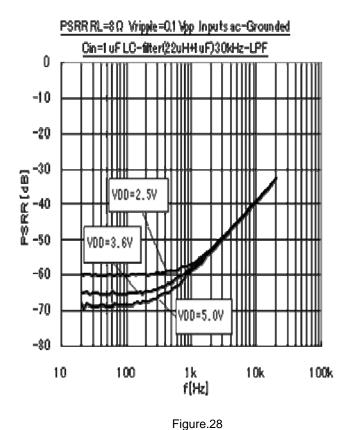








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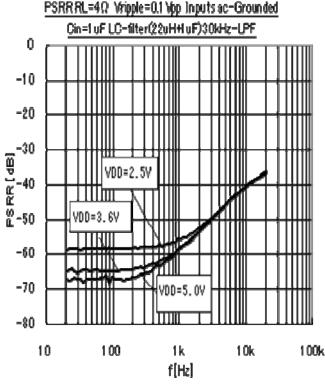
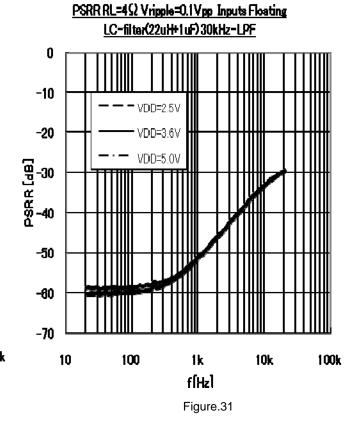
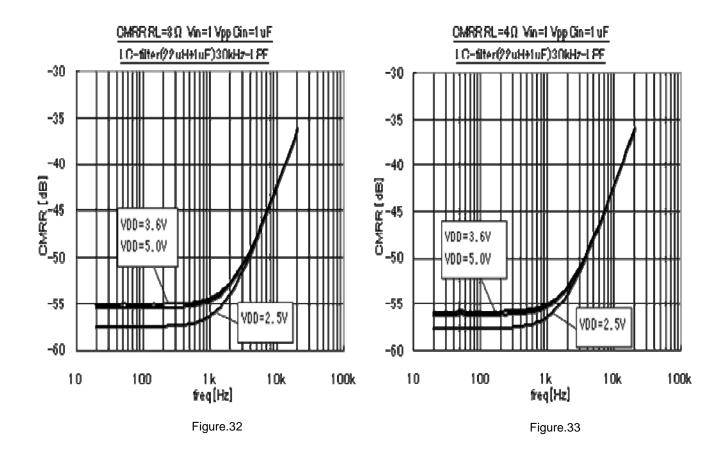


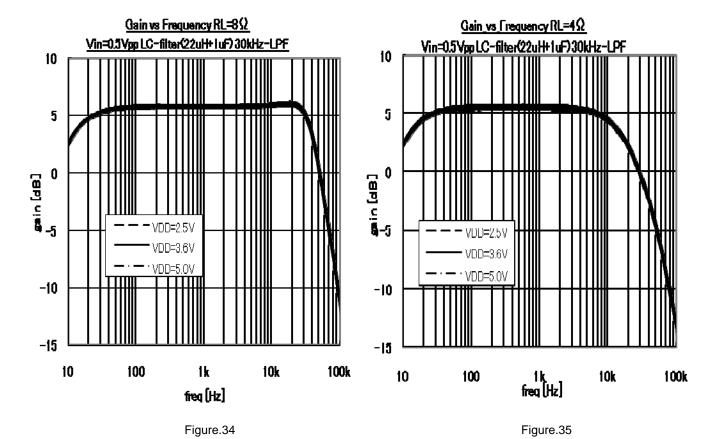
Figure.29

PSRR RL=8 Ω Vripple=0.1 Vpp Inputs Floating LC-filter(22uH+1uF)30kHz-LPF 0 -10 VDD=2.5V -20 VDD=3.6V PSRR [48] VDD=5.0V -50 -60 -70 10 100 1k 10k 100k f[Hz]

Figure.30







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Application Example(s)

Connect VDD(B1) and PVDD(B2) on PCB board, and use a single power supply.

(1)Differential input

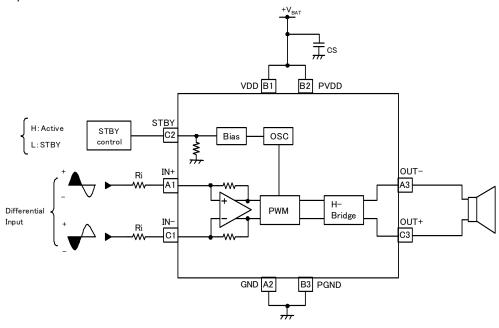


Figure.36 Differential input for mobile phone

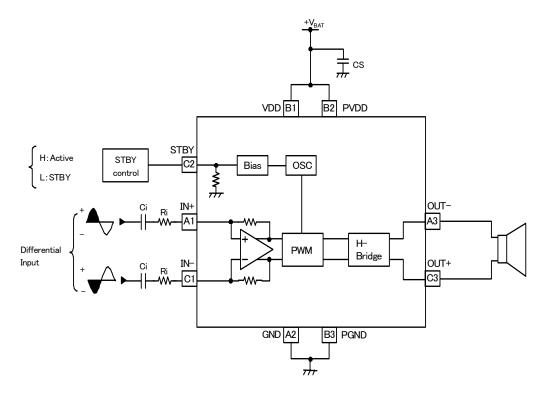


Figure.37 Differential input with coupling input capacitors

(2)Single-Ended input

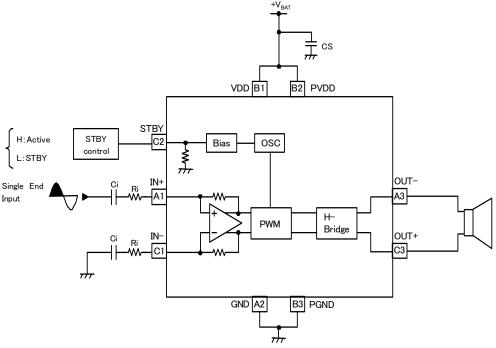


Figure.38 Single-Ended input

- It is possible to input audio signal from IN+ terminal, or IN- terminal when single-end mode.
- Don't make the input terminal (no input terminal, C1 terminal in above figure) open.

 Pop noise may be caused when the power supply starts up or the standby is released, if input terminal is opened.
- Connect non signal input side(C1 in above figure)to GND through Ci, and make the value of Ri, Ci of non signal input side same as the value of signal input side (A1 in above figure).

 Pop noise may be caused if each values of Ci, Ri are different, because the values of Ci, Ri decide the rise of Input terminal DC voltage when start-up. Difference of input terminal DC voltages may make pop noise.
- Make the value of Ri, Ci of non signal input side same as the value of signal input side when making LPF(Low Pass Filter) at previous stage of Ci.
- Put external input resistor Ri as close as possible to this IC.

Selection of Components Externally Connected

- Description of External components
 - ① Input coupling capacitor (Ci) and input resistor (Ri).

It makes an Input coupling capacitor 0.1uF. Input impedance is $150 k\,\Omega$.

It sets cutoff frequency fc by the following formula by input coupling capacitor Ci and input impedance Ri.

$$fc = \frac{1}{2 \pi \times Ri \times Ci} [Hz]$$

In case of Ri=150k Ω , Ci=0.1uF, it becomes fc = about 10 Hz.

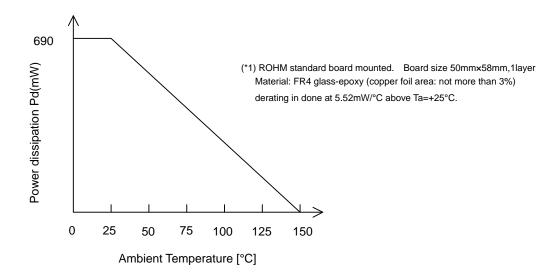
2 Power decoupling capacitor (CS)

It makes a power decoupling capacitor 10 µF.

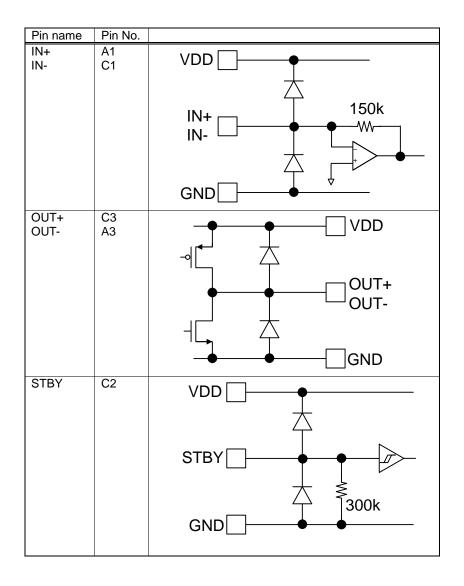
When making capacitance of the power decoupling capacitor, there is an influence in the Audio characteristic.

When making small, careful for the Audio characteristic at the actual application.

Power Dissipation



I/O equivalence circuits



Operational Notes

1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Thermal Consideration

Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the Pd stated in this specification is when the IC is mounted on a 50mmx58mm glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. Recommended Operating Conditions

These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. Operation Under Strong Electromagnetic Field

Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

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Operational Notes - continued

11. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.

When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

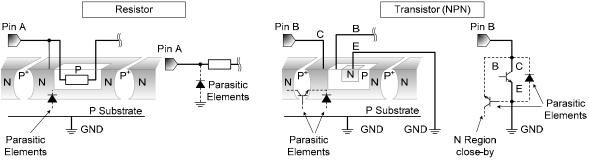


Figure 39. Example of monolithic IC structure

13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

14. Thermal Shutdown Circuit(TSD)

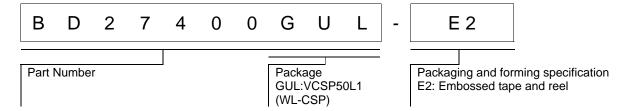
This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.

Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

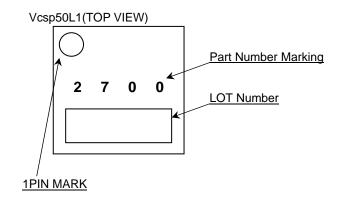
15. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

Ordering Information

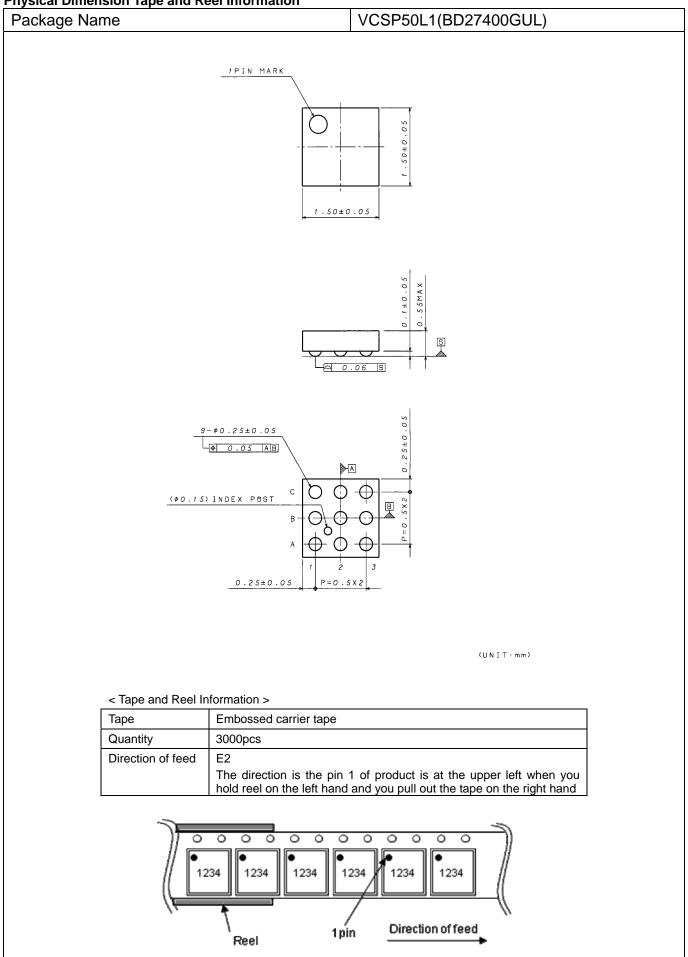


Marking Diagrams



Part Number Marking	Package	Orderable Part Number	
2700	VCSP50L1	BD27400GUL-E2	

Physical Dimension Tape and Reel Information



Revision History

Date	Revision	Changes		
05.Apr.2012	001	New Release		
05.Nov.2012	002	All. Change to a new format		
23.Apr.2014	003	 p.3. Change unit of a Output Power3 mW -> W Change the value of PSRR 56dB->64dB p.17 Change Part Number Marking p.18 Change to a new format at Physical Dimension Tape and Reel Information 		

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JAPAN	USA	EU	CHINA
CLASSⅢ	CL ACCIII	CLASSIIb	CL A C C TT
CLASSIV	CLASSⅢ	CLASSⅢ	CLASSⅢ

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 - [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
 - [f] Sealing or coating our Products with resin or other coating materials
 - [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
 - [h] Use of the Products in places subject to dew condensation
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- 6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.
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- 8. Confirm that operation temperature is within the specified range described in the product specification.
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- In principle, the reflow soldering method must be used; if flow soldering method is preferred, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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 may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is
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