



## N-Channel Enhancement MOSFET

### Features

- Drain-Source Breakdown Voltage  $V_{DSS}$  105 V
- Drain-Source On-Resistance  
 $R_{DS(ON)}$  230m $\Omega$ , at  $V_{GS} = 10V$ ,  $I_D = 1.5A$   
 $R_{DS(ON)}$  275m $\Omega$ , at  $V_{GS} = 4.5V$ ,  $I_D = 1.0A$
- Continuous Drain Current at  $T_A=25^\circ C$   $I_D = 1.5A$
- Advanced high cell density Trench Technology
- RoHS Compliance & Halogen Free

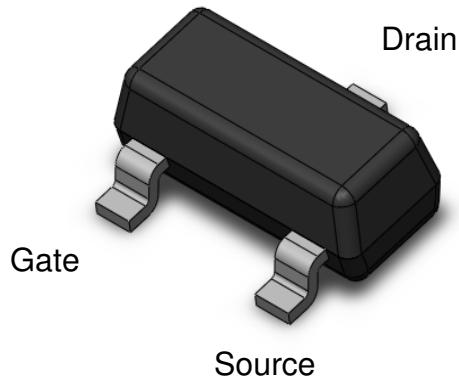
### Description

The CTL015NS10-R3 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance.

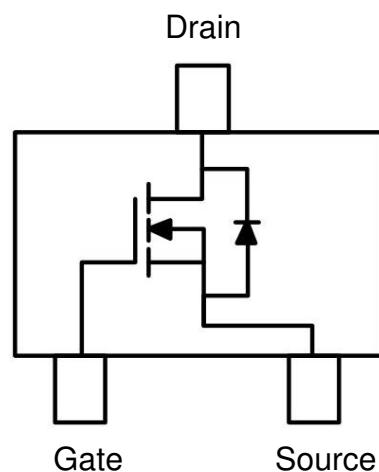
### Applications

- Power Management
- LCD Display inverter
- DC/DC Converter
- Load Switch

### Package Outline



### Schematic





CTL015NS10-R3

## N-Channel Enhancement MOSFET

### Absolute Maximum Rating at 25°C

Symbol	Parameters	Test Conditions	Min	Notes
V <sub>DS</sub>	Drain-Source Voltage	105	V	
V <sub>GS</sub>	Gate-Source Voltage	±20	V	
I <sub>D</sub>	Continuous Drain Current @T <sub>A</sub> =25°C	1.5	A	1
I <sub>DM</sub>	Pulsed Drain Current	6	A	1
P <sub>D</sub>	Total Power Dissipation @T <sub>A</sub> =25°C	1.3	W	2
T <sub>STG</sub>	Storage Temperature Range	-55 to 150	°C	
T <sub>J</sub>	Operating Junction Temperature Range	-55 to 150	°C	

### Thermal Characteristics

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units	Notes
R <sub>OJA4</sub>	Thermal Resistance Junction-Ambient (t=10s)		--	100	--	°C /W	1,4



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Electrical Characteristics  $T_A = 25^\circ\text{C}$  (unless otherwise specified)

## Static Characteristics

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units	Notes
B <sub>VDSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250µA	105	-	-	V	
I <sub>DSS</sub>	Drain-Source Leakage Current	V <sub>DS</sub> = 105V, V <sub>GS</sub> = 0V	-	-	1	µA	
I <sub>GSS</sub>	Gate-Source Leakage Current	V <sub>GS</sub> = ±20V, V <sub>DS</sub> = 0V	-	-	±100	nA	

## On Characteristics

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units	Notes
R <sub>DSON</sub>	Drain-Source On-Resistance	V <sub>GS</sub> = 10V, I <sub>D</sub> = 1.5A	-	230	270	mΩ	3
		V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 1.0A	-	275	340	mΩ	
V <sub>GS(th)</sub>	Gate-Source Threshold Voltage	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 250µA	1.0	2.0	3.0	V	3

## Dynamic Characteristics

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units	Notes
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> = 0V, V <sub>DS</sub> = 15V f=1MHz	-	325	-	pF	3
C <sub>oss</sub>	Output Capacitance		-	40	-		
C <sub>rss</sub>	Reverse Transfer Capacitance		-	10	-		

## Switching Characteristics

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units	Notes
T <sub>D(ON)</sub>	Turn-On Delay Time	V <sub>DS</sub> = 50V , R <sub>L</sub> = 33Ω , V <sub>GS</sub> = 10V , R <sub>G</sub> = 6Ω ,	-	10	-	ns	3
T <sub>R</sub>	Rise Time		-	6	-		
T <sub>D(OFF)</sub>	Turn-Off Delay Time		-	30	-		
T <sub>F</sub>	Fall Time		-	4	-		
Q <sub>G</sub>	Total Gate Charge	V <sub>DS</sub> = 50V , V <sub>GS</sub> = 4.5V , I <sub>D</sub> = 1.5A	-	6.5	-	nC	3
Q <sub>GS</sub>	Gate-Source Charge		-	2.5	-		
Q <sub>GD</sub>	Gate-Drain Charge		-	3.5	-		



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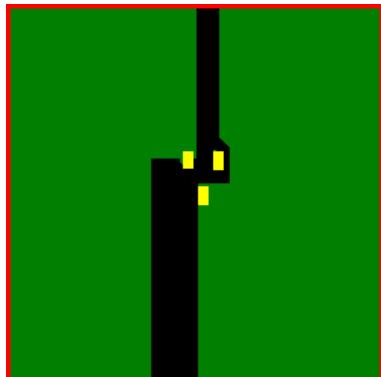
## N-Channel Enhancement MOSFET

### Drain-Source Diode Characteristics

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units	Notes
V <sub>SD</sub>	Body Diode Forward Voltage	V <sub>GS</sub> = 0V, I <sub>D</sub> = 1A	-	0.8	1.2	V	
I <sub>SD</sub>	Body Diode Continuous Current		-	-	1	A	1

Note:

1. The power dissipation is limited by 150°C junction temperature.
2. Device mounted on a glass-epoxy board



Actual Size

3. The data tested by pulsed , pulse width  $\leq 300\mu\text{s}$  , duty cycle  $\leq 2\%$
4. Thermal Resistance follow JESD51-3.



## Typical Characteristic Curves

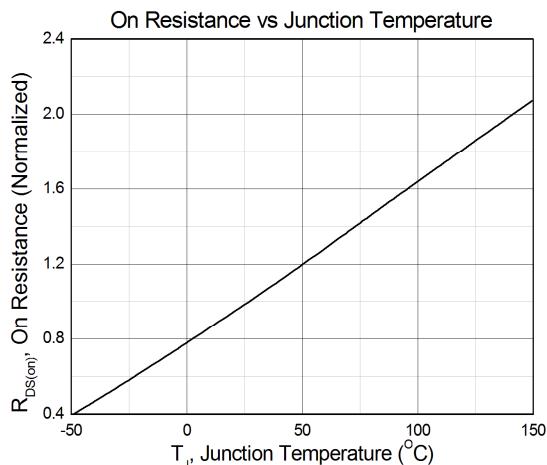


Figure 1

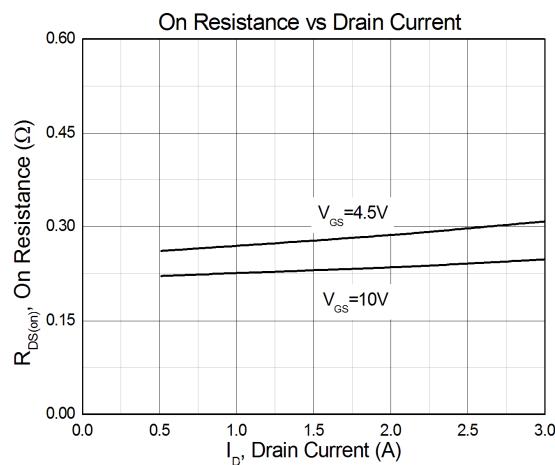


Figure 2

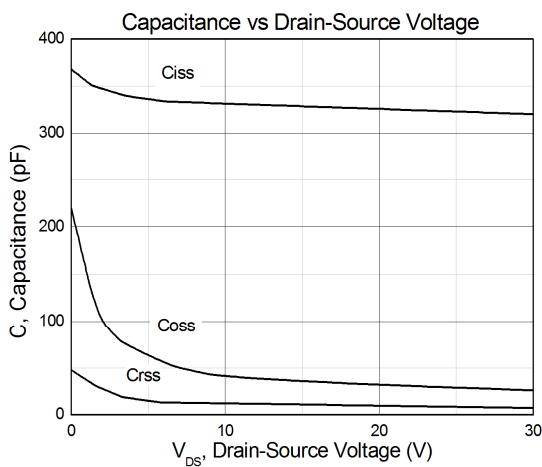


Figure 3

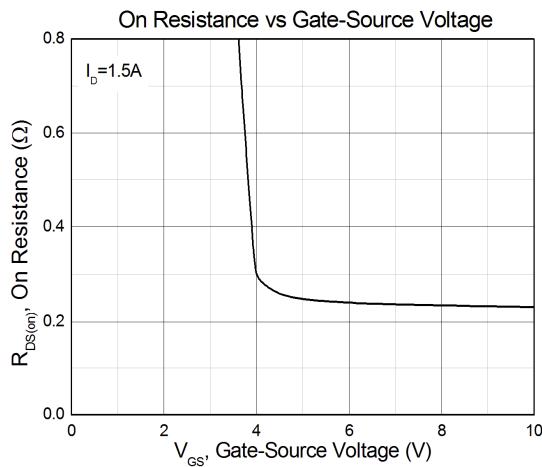


Figure 4

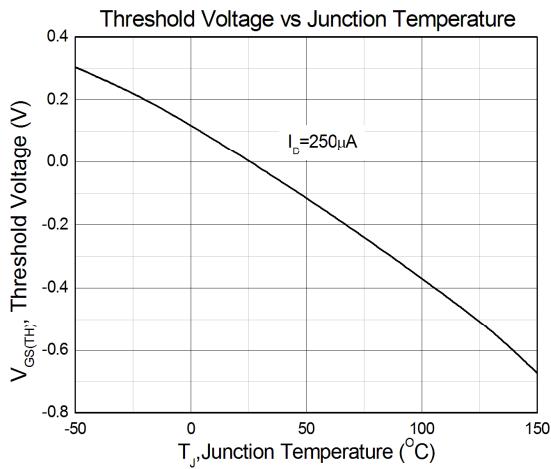


Figure 5

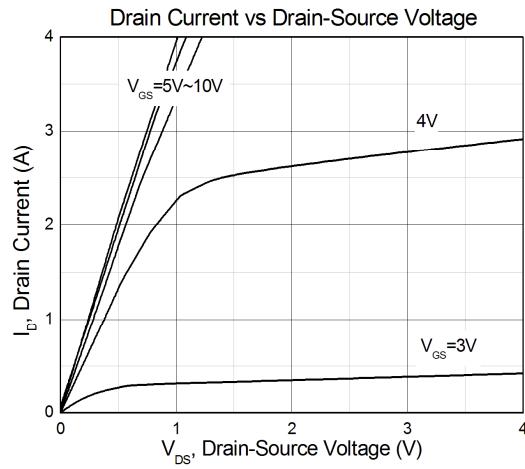


Figure 6



**CTL015NS10-R3**

## **N-Channel Enhancement MOSFET**

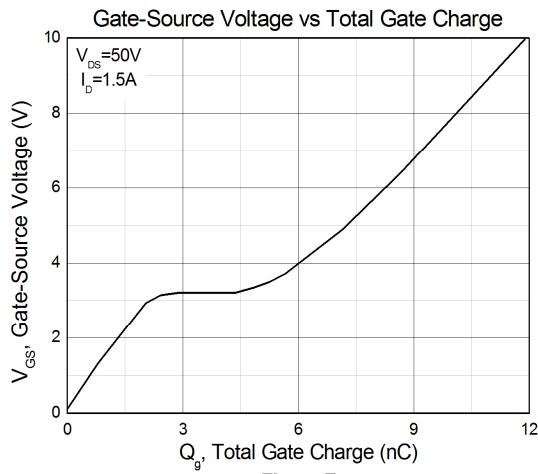


Figure 7

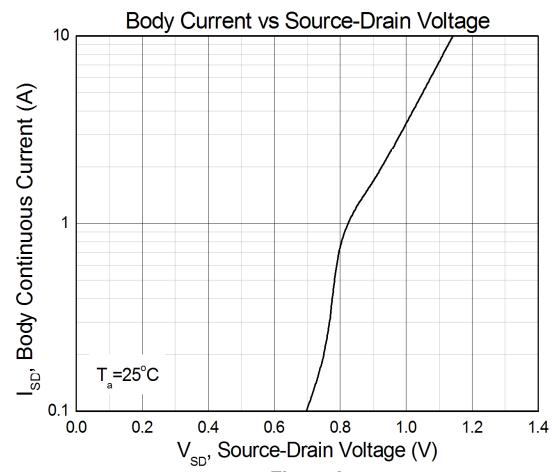


Figure 8



## Test Circuits & Waveforms

Figure 9: Gate Charge Test Circuit

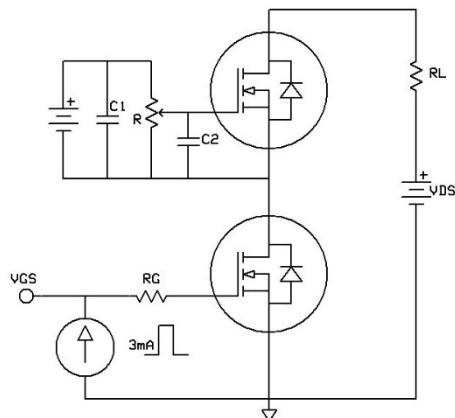


Figure 10: Gate Charge Waveform

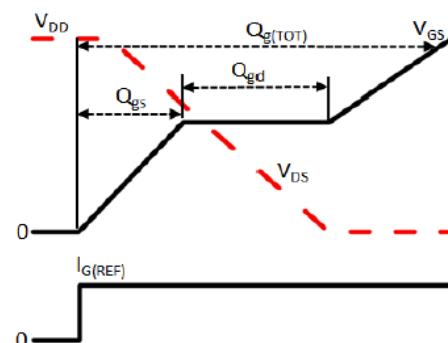


Figure 11: Switching Time Test Circuit

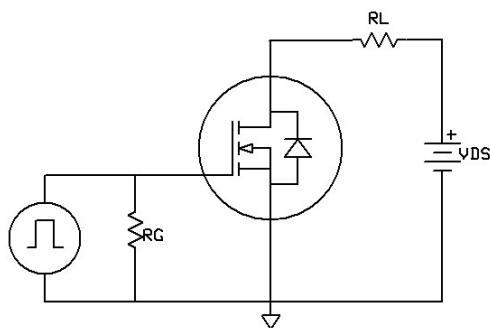
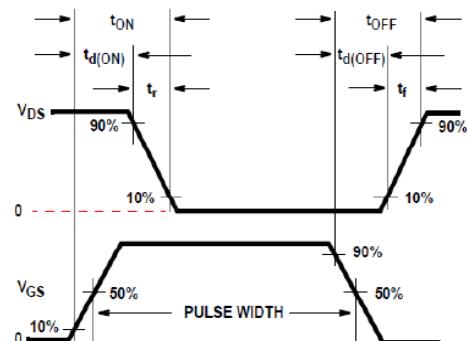
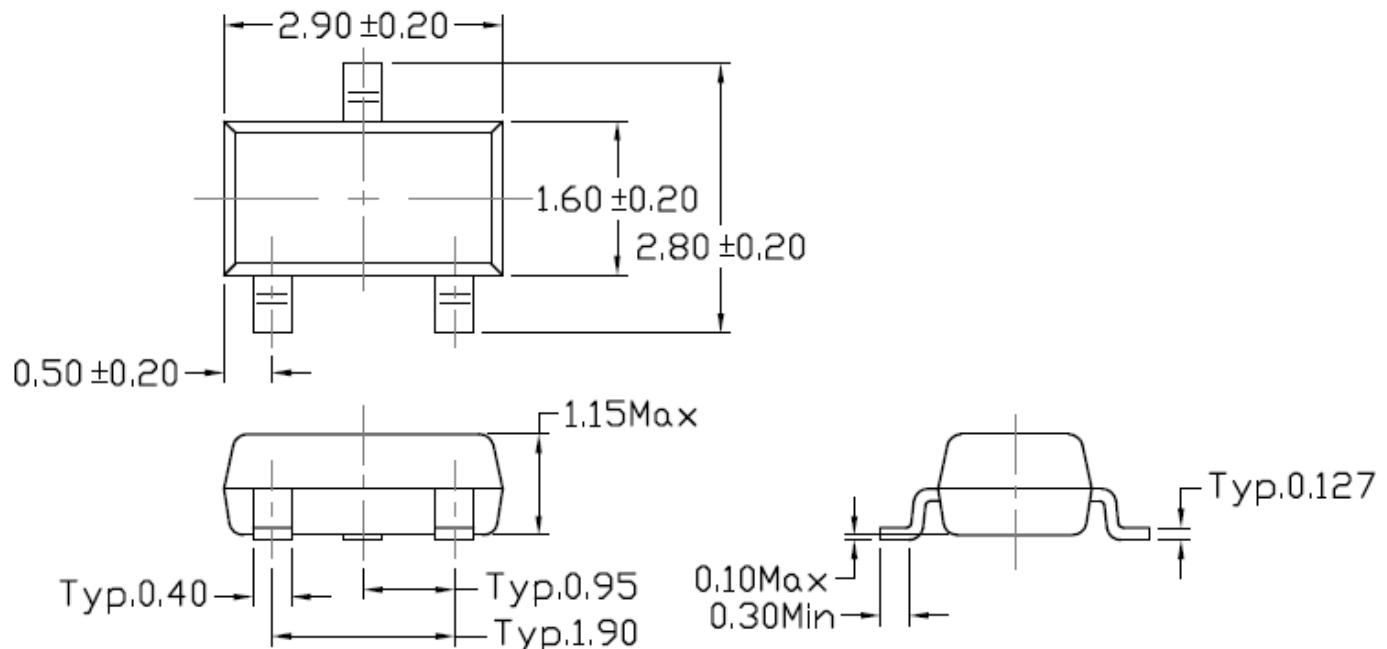


Figure 12: Switching Time Waveform



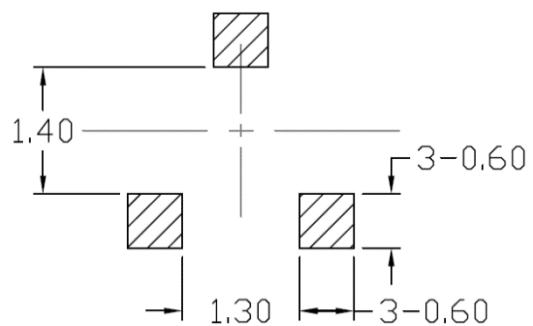


### Package Dimension (SC-59)



Note: Dimensions in mm

### Recommended pad layout for surface mount leadform



Note: Dimensions in mm

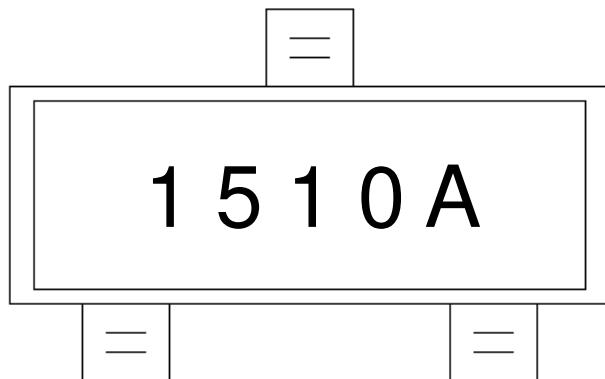


**CTL015NS10-R3**

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## **Marking Information**



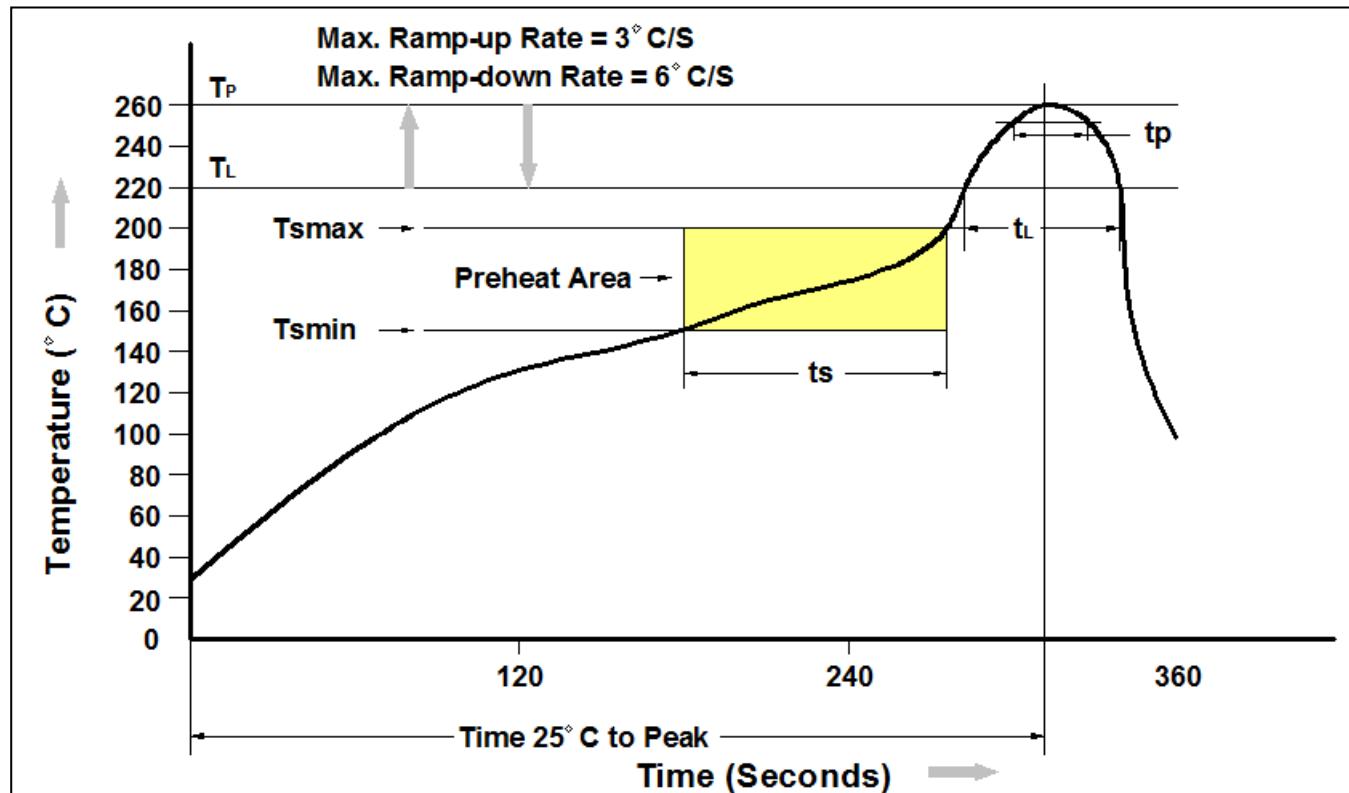
1510A: Device Number

## **Ordering Information**

<b>Part Number</b>	<b>Description</b>	<b>Quantity</b>
CTL015NS10-R3	SC-59 Reel	3000 pcs



## Reflow Profile



Profile Feature	Pb-Free Assembly Profile
Temperature Min. (T <sub>smin</sub> )	150°C
Temperature Max. (T <sub>smax</sub> )	200°C
Time (t <sub>s</sub> ) from (T <sub>smin</sub> to T <sub>smax</sub> )	60-120 seconds
Ramp-up Rate (t <sub>L</sub> to t <sub>P</sub> )	3°C/second max.
Liquidous Temperature (T <sub>L</sub> )	217°C
Time (t <sub>L</sub> ) Maintained Above (T <sub>L</sub> )	60 – 150 seconds
Peak Body Package Temperature	260°C +0°C / -5°C
Time (t <sub>P</sub> ) within 5°C of 260°C	30 seconds
Ramp-down Rate (T <sub>P</sub> to T <sub>L</sub> )	6°C/second max
Time 25°C to Peak Temperature	8 minutes max.



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