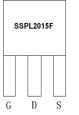


Main Product Characteristics

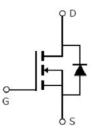
V _{DSS}	200V	
R _{DS} (on)	0.13Ω(typ.)	
I _D	18A 🗊	



TO-220F



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Features and Benefits

- Advanced Process Technology
- Special designed for PWM, load switching and general purpose applications
- Ultra low on-resistance with low gate charge
- Fast switching and reverse body recovery
- 175°C operating temperature



Schematic Diagram



Description

These N-Channel enhancement mode power field effect transistors are produced using silikron proprietary MOSFET technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switch mode power supplies.

Absolute Max Rating

Symbol	Parameter	Max.	Units
I _D @ TC = 25°C	Continuous Drain Current, V _{GS} @ 10V	18 ①	
I _D @ TC = 100°C	Continuous Drain Current, V _{GS} @ 10V	13 ①	А
I _{DM}	Pulsed Drain Current 2	72	
P _D @TC = 25°C	Power Dissipation 3	75	W
$P_D \subseteq IC = 25 C$	Linear Derating Factor	0.5	W/°C
V _{DS}	Drain-Source Voltage	200	V
V _{GS}	Gate-to-Source Voltage	± 30	V
E _{AS}	Single Pulse Avalanche Energy @ L=4.2mH	412	mJ
I _{AS}	Avalanche Current @ L=4.2mH	14	А
T _J T _{STG}	Operating Junction and Storage Temperature Range	-55 to +175	°C



Thermal Resistance

Symbol	Characteristics	Тур.	Max.	Units
R _{θJC}	Junction-to-case 3	_	2.0	°C/W
D	Junction-to-ambient (t \leq 10s) (4)	—	62	°C/W
$R_{ extsf{ heta}JA}$	Junction-to-Ambient (PCB mounted, steady-state) ④	_	40	°C/W

Electrical Characteristics $@T_A=25^{\circ}C$ unless otherwise specified

Symbol	Parameter	Min.	Тур.	Max.	Units	Conditions	
V _{(BR)DSS}	Drain-to-Source breakdown voltage	200	_	_	V	$V_{GS} = 0V, I_{D} = 250 \mu A$	
D	Static Drain-to-Source on-resistance	_	0.13	0.15	Ω	V_{GS} =10V,I _D =11A	
R _{DS(on)}	Static Dram-to-Source on-resistance	_	0.27	_		$T_J = 125^{\circ}C$	
V	Gate threshold voltage	2	—	4	v	$V_{DS} = V_{GS}, I_D = 250 \mu A$	
V _{GS(th)}	Gale intestiold voltage	_	2.26	—	v	$T_J = 125^{\circ}C$	
	Drain to Course lookens current	_	_	1		V _{DS} =200V, V _{GS} = 0V	
I _{DSS}	Drain-to-Source leakage current		_	50	μA	T _J = 125°C	
	Cata ta Sauraa farruard laakara	_	_	100	nA	V _{GS} =20V	
I _{GSS}	Gate-to-Source forward leakage		_	-100		V _{GS} = -20V	
Qg	Total gate charge	_	27	_		I _D = 11A,	
Q _{gs}	Gate-to-Source charge	_	5.4	—	nC	V _{DS} =160V,	
Q_{gd}	Gate-to-Drain("Miller") charge	_	11	_		$V_{GS} = 10V$	
t _{d(on)}	Turn-on delay time	_	11	_			
tr	Rise time	_	23	_	- 6	V_{GS} =10V, V_{DD} =100V, R _L =9.2 Ω ,R _{GEN} =2.55 Ω I _D =11A	
t _{d(off)}	Turn-Off delay time	_	22	_	nS		
t _f	Fall time	—	5.2	_			
Ciss	Input capacitance	—	1010	_		$V_{GS} = 0V$	
C _{oss}	Output capacitance	—	240	_	pF	V _{DS} = 25V <i>f</i> = 1MHz	
C _{rss}	Reverse transfer capacitance	—	57	_			

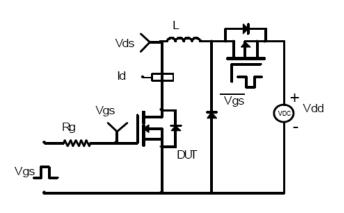
Source-Drain Ratings and Characteristics

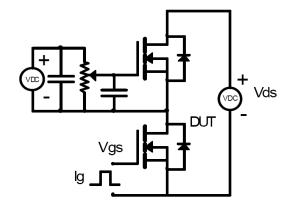
Symbol	Parameter	Min.	Тур.	Max.	Units	Conditions
I _S	Continuous Source Current		_	18 ①	А	MOSFET symbol
	(Body Diode)					showing the
I _{SM}	Pulsed Source Current	_	—	72	А	integral reverse
	(Body Diode)					p-n junction diode.
V _{SD}	Diode Forward Voltage	—	0.87	1.3	V	I_{S} =11A, V_{GS} =0V, T_{J} = 25°C
t _{rr}	Reverse Recovery Time	_	128		nS	$T_J = 25^{\circ}C, I_F = 11A,$
Q _{rr}	Reverse Recovery Charge	_	819		nC	di/dt = 100A/µs



Test circuits and Waveforms

EAS Test Circuit

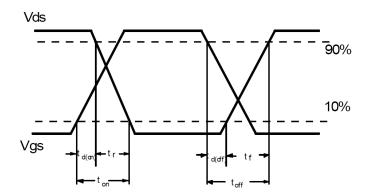




Switching Time Test Circuit

Switching Waveforms

Gate charge test circuit



Notes:

- ①Calculated continuous current based on maximum allowable junction temperature.
- 2 Repetitive rating; pulse width limited by max. junction temperature.
- ③The power dissipation PD is based on max. junction temperature, using junction-to-case thermal resistance.
- (4) The value of $R_{\theta JA}$ is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with TA =25°C





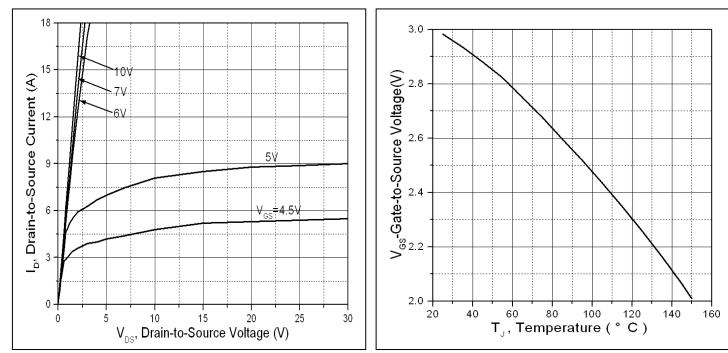


Figure 1: Typical Output Characteristics

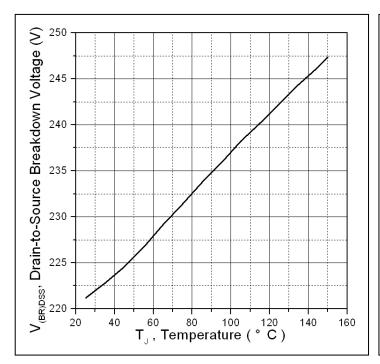
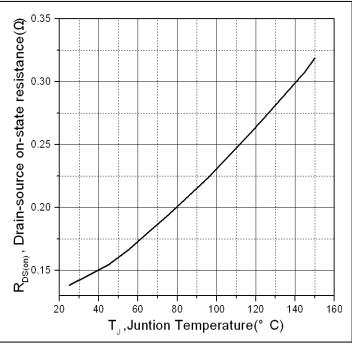


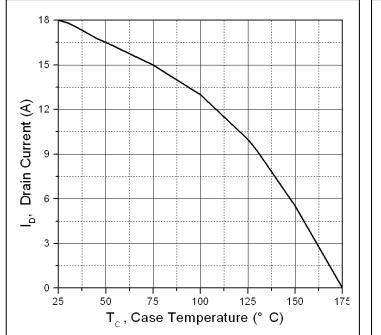


Figure 2. Gate to source cut-off voltage









Typical electrical and thermal characteristics



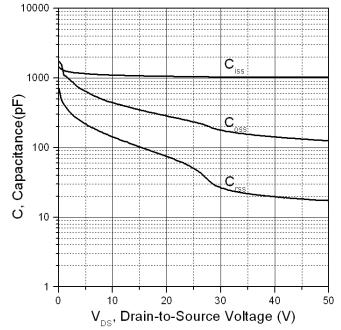


Figure 6.Typical Capacitance Vs. Drain-to-Source Voltage

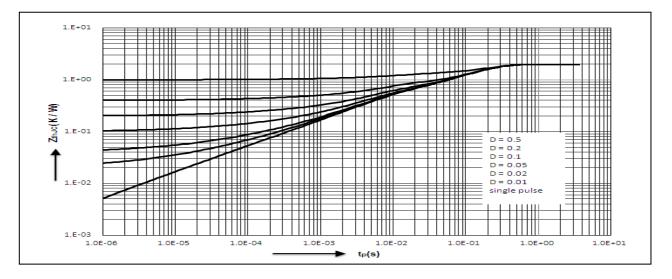
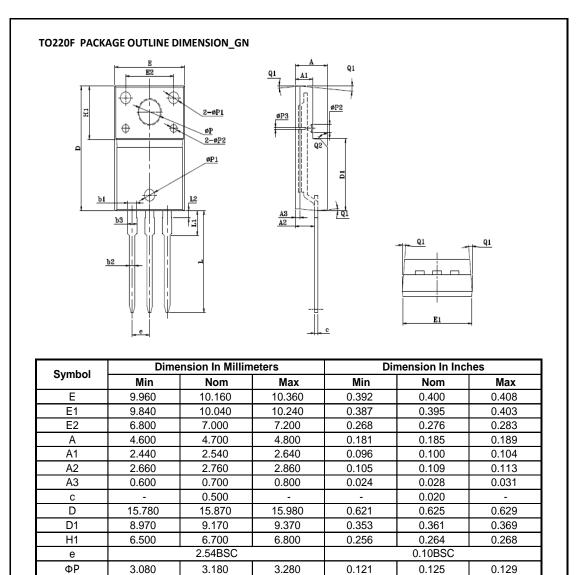


Figure7. Maximum Effective Transient Thermal Impedance, Junction-to-Case



Mechanical Data:



1.600

1.100

0.300

13.180

3.370

1.030

7°

47°

1.380

0.840

1.420

0.055

0.035

0.004

0.503

0.117

0.033

 3°

43°

0.046

0.030

-

ΦΡ1 ΦΡ2

ΦP3

L

L1

L2

Q1 Q2

b1

b2

b3

1.400

0.900

0.100

12.780

2.970

0.830

3°

43°

1.180

0.760

-

1.500

1.000

0.200

12.980

3.170

0.930

5°

45°

1.280

0.800

-

0.059

0.039

0.008

0.511

0.125

0.037

5°

45°

0.050

0.031

-

0.063

0.043

0.012

0.519

0.133

0.041

7°

47°

0.054

0.033

0.056



Ordering and Marking Information

Device Marking: SSPL2015F
Package (Available)
TO-220F
Operating Temperature Range
C : -55 to175 °C

Devices per Unit

Package Type	Units/ Tube	Tubes/Inner Box	Units/Inner Box	Inner Boxes/Carton Box	Units/Carton Box
TO-220F	50	20	1000	6	6000

Reliability Test Program

Test Item	Conditions	Duration	Sample Size
High	T _j =125℃ to 175℃ @	168 hours	3 lots x 77 devices
Temperature	80% of Max	500 hours	
Reverse	V _{DSS} /V _{CES} /VR	1000 hours	
Bias(HTRB)			
High	T _j =125℃ or 175℃ @	168 hours	3 lots x 77 devices
Temperature	100% of Max V _{GSS}	500 hours	
Gate		1000 hours	
Bias(HTGB)			



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