

Marvell Alaska C 88X5121

Dual 100 Gbps Ethernet Transceiver with Copper Cable and Backplane Drive Capability

ALASKA[®] C
transceivers

FEATURES

- Dual Port 100GbE PHY
- Octal 25G repeater
- Dual 40GbE aggregator that enables aggregation of 40GbE from 4x10G lanes to 2x20G lanes
- Ability to handle Insertion Loss of greater than 30dB at Nyquist without Forward Error Correction (FEC)
- Line interface SERDES that exceeds the equalization requirements for 100G-CR4 passive copper cables and 100G-KR4 backplanes
- OIF25G-LR compliant long reach host interface SERDES that exceeds IEEE CAUI-4 requirements
- Fully autonomous adaptive equalization on line and host receiver
- Support for 100GbE/40GbE auto-negotiation and coefficient training protocol
- Support for IEEE 802.3BJ Reed-Solomon Forward Error Correction (R-S FEC) functionality
- Low latency repeater mode for applications not requiring FEC capability with fully independent operation on each lane
- Hole-free operation from 1.25Gbps to 28Gbps
- Programmable clock divide ratios
- Recovered clock outputs for SyncE applications
- Ethernet packet and programmable packet generation and checking
- Non-destructive Eye monitoring capability on all high speed lanes
- Clause 45 MDC/MDIO management interface
- Junction temperature range of 0 to 105°
- Small 17mm x 17mm FCBGA package

MARVELL ALASKA C 88X5121 OVERVIEW

The Marvell® Alaska® C 88X5121 is a fully integrated dual port 100 Gbps device that performs all physical layer functions required to drive 100 Gbps Ethernet over a variety of media including optics, backplanes and passive copper cables. Manufactured with 28 nanometer lithography, in a 17mmx17mm package footprint, the Marvell 88X5121 enables low-power dissipation, high density 100GbE and 25GbE line card designs. The line interface of the 88X5121 is fully compliant to the IEEE 802.3BJ standard that defines the physical layer specifications for 100 Gbps Ethernet transmission over backplanes and copper cables. The device supports Reed-Solomon Forward Error Correction function required for 100G-CR4 and 100G-SR4 operation, as well as auto-negotiation and coefficient training protocol required by the IEEE 802.3 standards.

KEY BENEFITS

- Fully compliant to IEEE 802.3BJ and 803.3BM standards for 100GbE transmission over optical media, passive copper cables and backplanes
- Octal 25G mode for 25GbE and other low latency applications
- Support for speed negotiation and coefficient training

PRODUCT DESCRIPTION

The Marvell 88X5121 is a fully integrated dual port device that performs all physical layer functions required to drive 100Gbps full duplex transmission over a variety of media.

The 88X5121 connects to a MAC or switch on its host interface over a 4x25Gbps CAUI-4 link. The transmit drive and receiver equalization capabilities of the host interface are compliant to OIF CEI-25G LR specifications, significantly exceeding CAUI-4 requirements.

On the line interface, the device supports a variety of media types including single mode and multimode optical modules, passive and active copper direct attach cables, and copper backplanes.

The line interface of the 88X5121 is fully compliant to the IEEE 802.3BJ standard that defines the physical layer specifications for 100Gbps operation over backplanes and copper cables. The device supports FEC feature, as well as auto-negotiation and coefficient training protocol required by the 802.3BJ standard.

For applications not requiring the FEC functionality, the device also supports a low latency repeater mode where the functionalities associated with the Physical Coding Sublayer (PCS) and FEC are bypassed. In this mode, the device can be used to drive low latency 25GbE Direct Attach Cable links as well as backplanes and cables for non-Ethernet traffic types such as OTN and Fibre Channel. The eight lanes of the device can operate independent of the others in this mode, enabling simultaneous support for multiple standards.

The 88X5121 supports wide band of operation (from 1.25Gbps to 28.05Gbps) supports a wide variety of standards and rates.

The device also supports a 2 to 1 bit-multiplexing functionality that enables a 40GbE stream on the host side to be aggregated from 4x10Gbps lanes to 2X20Gbps lanes. This functionality can be used to double I/O density on legacy systems, as well as to expand an aggregated 40GbE stream to a standard 4X10Gbps lane format.

The 88X5121 supports auto-negotiation to 40Gbps and operation at this speed.

Internal registers can be accessed via an MDIO/MDC serial management interface which is compliant with the IEEE 802.3 specification (Clause 45). An MDC frequency of up to 25 MHz is supported.

The device includes internal PRBS generators and Ethernet packet generators and loopbacks to assist with test and debug. In addition, non-destructive eye monitoring is supported on all high speed I/Os.

The 88X5121 is housed in a 17mm x 17mm 256 pin FCBGA package, and supports an operating temperature range from 0 to 105°C.

BLOCK DIAGRAM

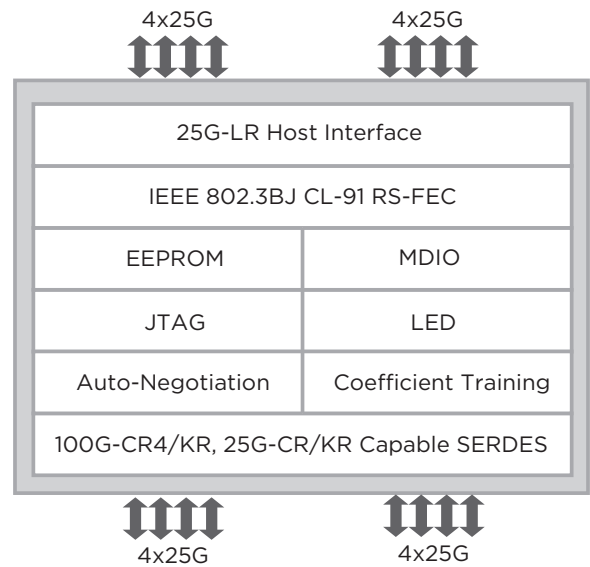


Fig 1. Marvell Alaska C 88X5121

FEATURES AND BENEFITS

SPECIAL FEATURES	BENEFITS
Long reach host and line SERDES	Capable of compensating an Insertion Loss of up to 30dB without FEC
Integrated Reed-Solomon FEC	Ability to drive 100G-CR4 cables, 100G-KR4 backplanes and 100GSR4 optical modules
Octal 25G mode	For low latency 25GbE Direct Attach cable links between servers and Top of Rack switches
Integrated IEEE auto-negotiation and training protocol	Seamless interoperability with IEEE-compliant devices from other vendors
Fully autonomous equalizer adaptation	Does not require intervention from host software

APPLICATIONS

- 100GbE/25GbE Data center switches
- 100G-KR4 backplanes
- OTL 4.4 and 32G Fibre Channel line cards

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