EMIF06-1005N12

6-line IPAD™, low capacitance EMI filter and ESD protection in narrow micro QFN package

Features

- EMI symmetrical (I/O) low-pass filter
- High efficiency in EMI filtering at frequencies from 900 MHz to 1.8 GHz
- Very low PCB space consumption: 2.5 mm x 1.2 mm
- Very thin package: 0.55 mm max
- High efficiency in ESD suppression on inputs pins (IEC 61000-4-2 level 4)
- High reliability offered by monolithic integration
- High reduction of parasitic elements through integration and wafer level packaging
- Lead-free package

Complies with the following standards

- IEC 61000-4-2 level 4 input and output pins
  - ± 15 kV (air discharge)
  - ± 8 kV (contact discharge)
- MIL STD 883G - Method 3015-7 Class 3B (all pins)

Applications

Where EMI filtering in ESD sensitive equipment is required:

- LCD and camera for mobile phones
- Computers and printers
- Communication systems
- MCU boards
- Keypad for portable equipment

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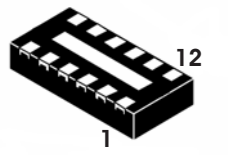


µQFN-12L

Figure 1. Pin configuration (top view)

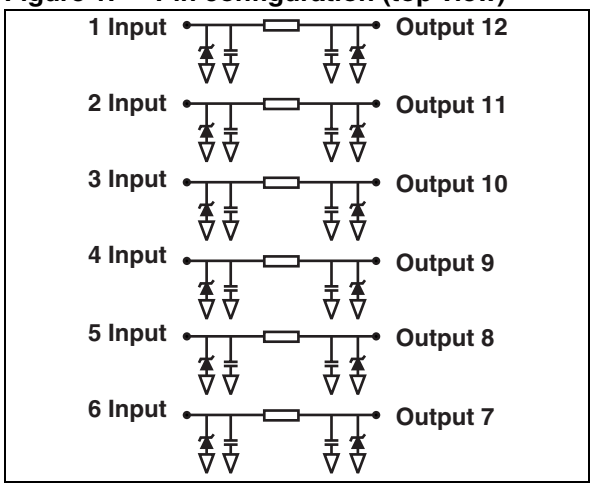
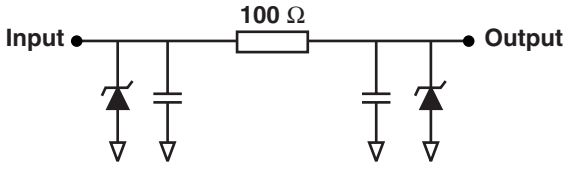


Figure 2. Basic cell configuration



Typical line capacitance = 45 pF @ 0 V

Description

EMIF06-1005N12 is a 6-line, highly integrated device designed to suppress EMI/RFI noise in all systems exposed to electromagnetic interference.This filter includes ESD protection circuitry, which prevents damage to the application when subjected to ESD surges up to 15 kV on the input pins.

1 Characteristics

Table 1. Absolute ratings (limiting values)

Symbol	Parameter and test conditions	Value	Unit
V_{PP}	ESD discharge IEC 61000-4-2, level 4 air discharge contact discharge ESD-Machine Model : (MM: C = 200 pF, R = 25 Ω L = 500 nH) ESD-Charged Device Model: (JESD22-C101D)	 15 15 2 1	kV
T_j	Junction temperature at T_{amb} = 25 °C	125	°C
T_{op}	Operating temperature range	- 40 to + 85	°C
T_{stg}	Storage temperature range	- 55 to + 150	°C

Figure 3. Electrical characteristics (definitions)

Symbol		Parameter
V_{BR}	=	Breakdown voltage
V_{CL}	=	Clamping voltage
I_{RM}	=	Leakage current @ V_{RM}
V_{RM}	=	Stand-off voltage
I_F	=	Forward current
I_{PP}	=	Peak pulse current
I_R	=	Breakdown current
V_F	=	Forward voltage drop
R_d	=	Dynamic impedance
I_{PP}	=	Forward current
$R_{I/O}$	=	Series resistanc between input and output
C_{line}	=	Input capacitance per line

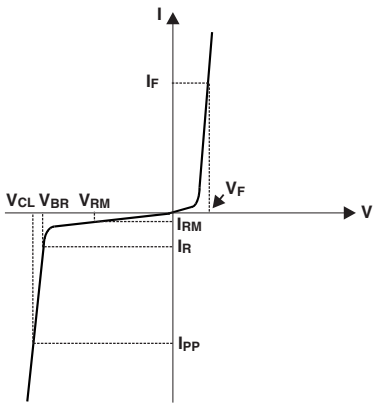


Table 2. Electrical characteristics (T_{amb} = 25 °C)

Symbol	Test conditions	Min.	Typ.	Max.	Unit
V_{BR}	I_R = 1 mA	6	8	10	V
V_F	I_F = 10 mA	0.5	1	1.5	V
I_{RM}	V_{RM} = 3 V per line			200	nA
$R_{I/O}$	Tolerance ± 15%	85	100	115	Ω
C_{line}	V_{line} = 0 V, V_{osc} = 30 mV, F = 1 MHz	38	45	52	pF

Figure 4. S21 attenuation measurement

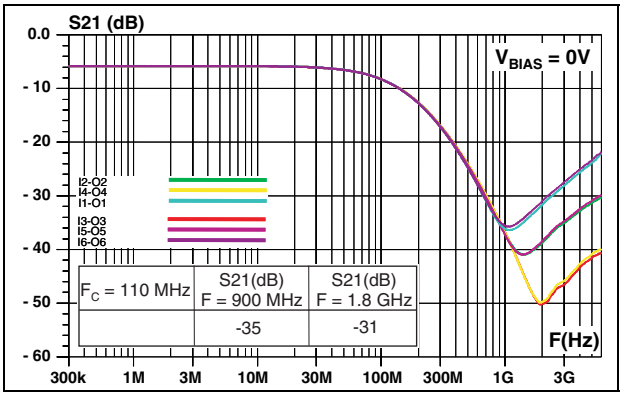


Figure 5. Analog cross talk measurements

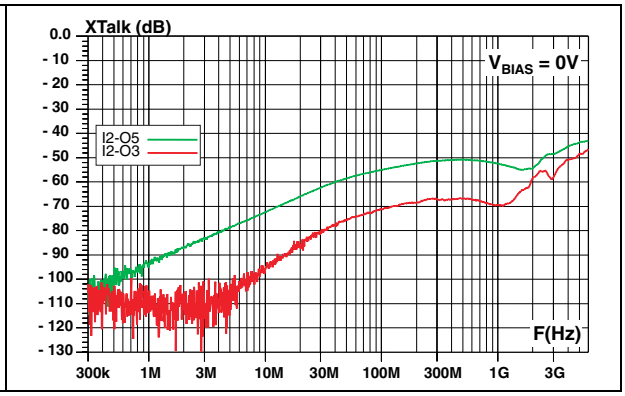


Figure 6. ESD response to IEC 61000-4-2 (+8 kV contact discharge). Remaining voltage on filter output

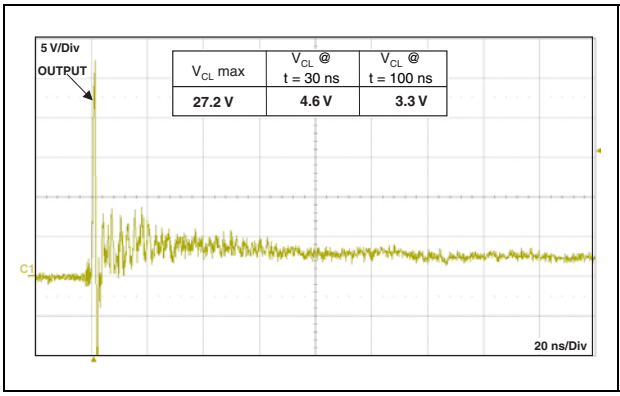


Figure 7. ESD response to IEC 61000-4-2 (-8 kV contact discharge). Remaining voltage on filter output

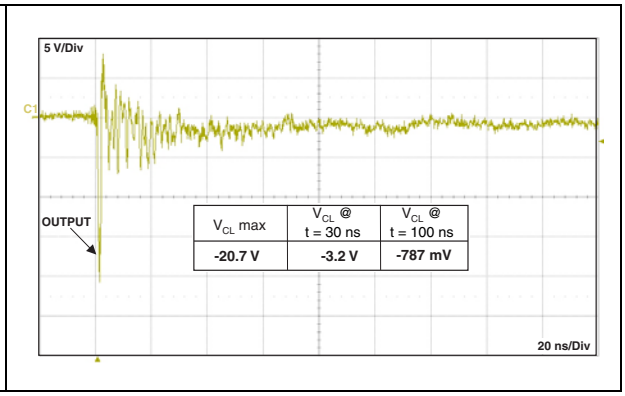


Figure 8. ESD test conditions for figure 6 and figure 7

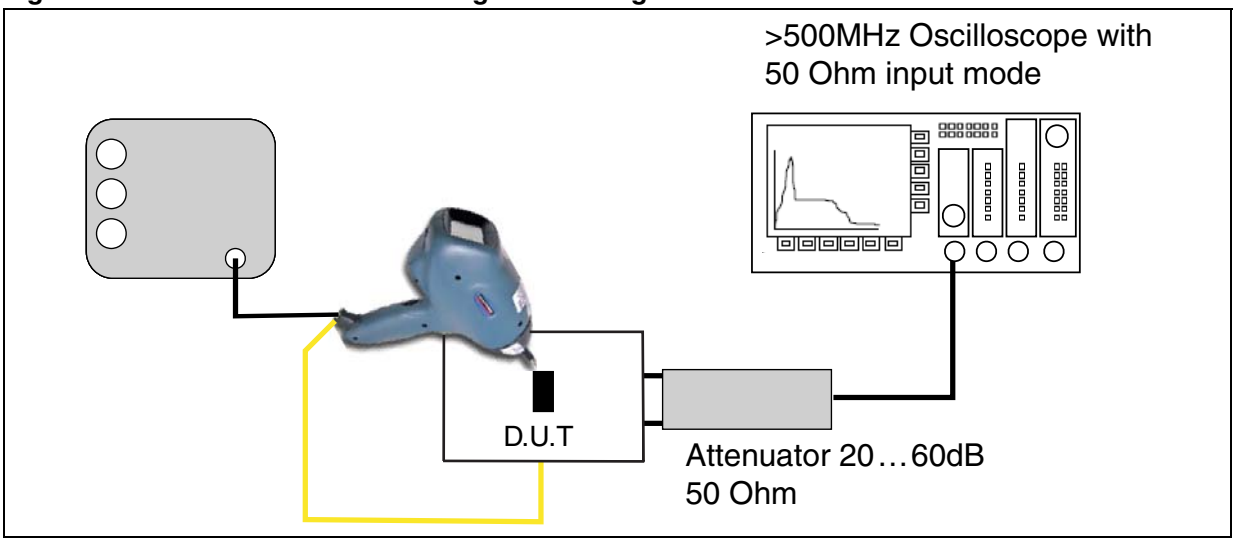


Figure 9. ESD response to IEC 61000-4-2 (+15 kV air discharge) on one line

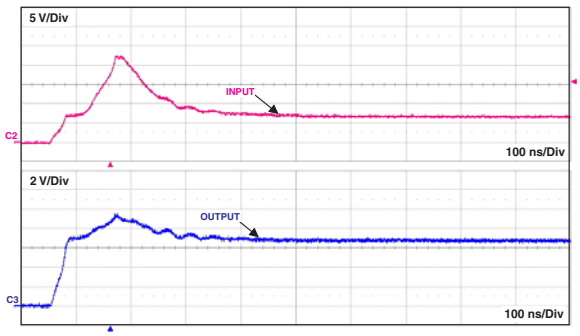


Figure 10. ESD response to IEC 61000-4-2 (-15 kV air discharge) on one line

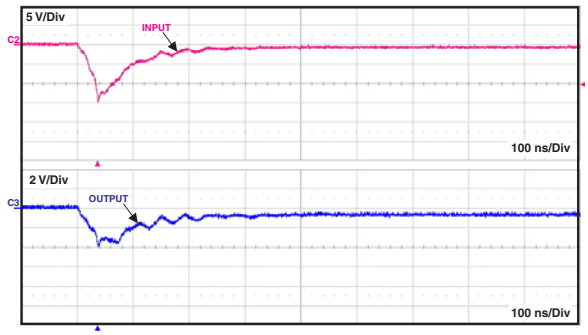
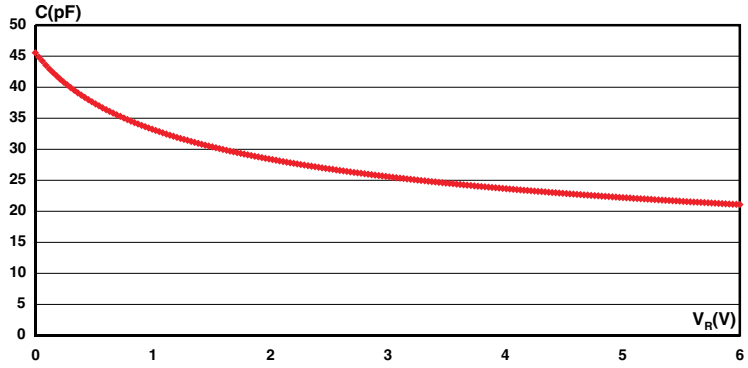
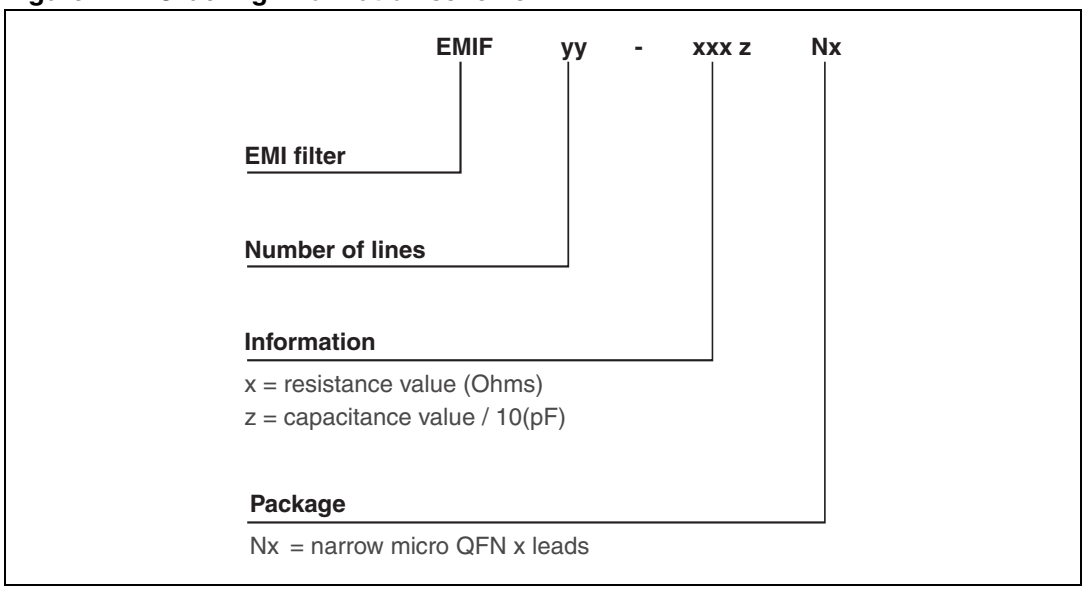


Figure 11. Line capacitance versus applied voltage



2 Ordering information scheme

Figure 12. Ordering information scheme

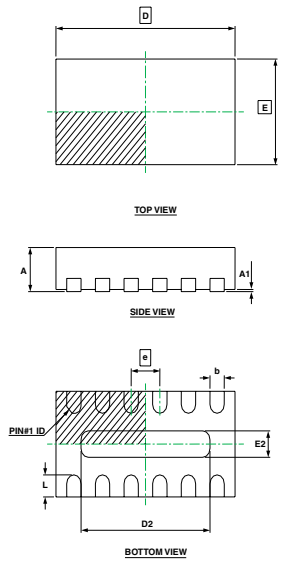


3 Package information

- Epoxy meets UL94, V0
- Lead-free package

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Table 3. µQFN-12L dimensions



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.45	0.5	0.55	0.018	0.020	0.022
A1		0.02	0.05		0.0008	0.002
b	0.15	0.2	0.25	0.006	0.008	0.010
D	2.45	2.5	2.55	0.096	0.098	0.10
D2	1.75	1.8	1.85	0.069	0.071	0.73
E	1.15	1.2	1.25	0.045	0.047	0.050
E2	0.25	0.3	0.35	0.010	0.012	0.014
e		0.4			0.016	
L	0.15	0.25	0.35	0.006	0.010	0.014

Figure 13. Footprint recommendations

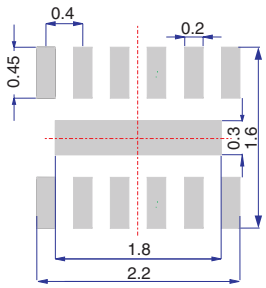


Figure 14. Marking

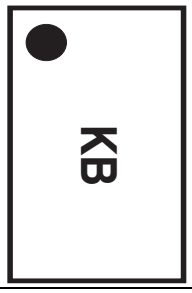
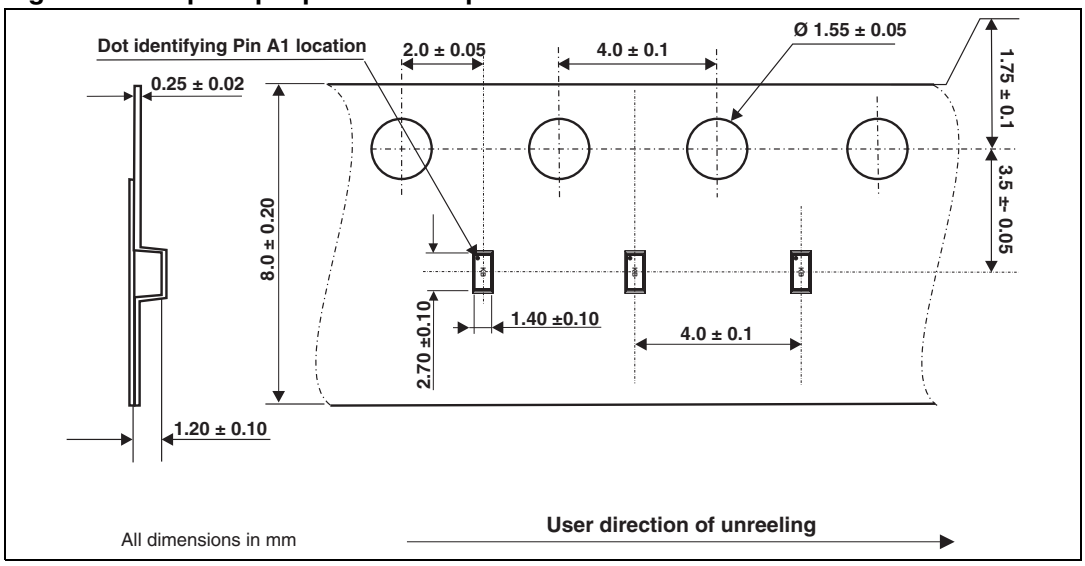


Figure 15. Flip-Chip tape and reel specification



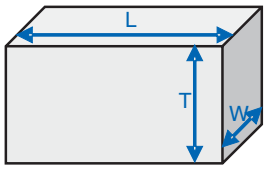
Note: Product marking may be rotated by 90° for assembly plant differentiation. In no case should this product marking be used to orient the component for its placement on a PCB. Only pin 1 mark is to be used for this purpose.

4 Recommendation on PCB assembly

4.1 Stencil opening design

1. General recommendation on stencil opening design
   a) Stencil opening dimensions: L (Length), W (Width), T (Thickness).

Figure 16. Stencil opening dimensions



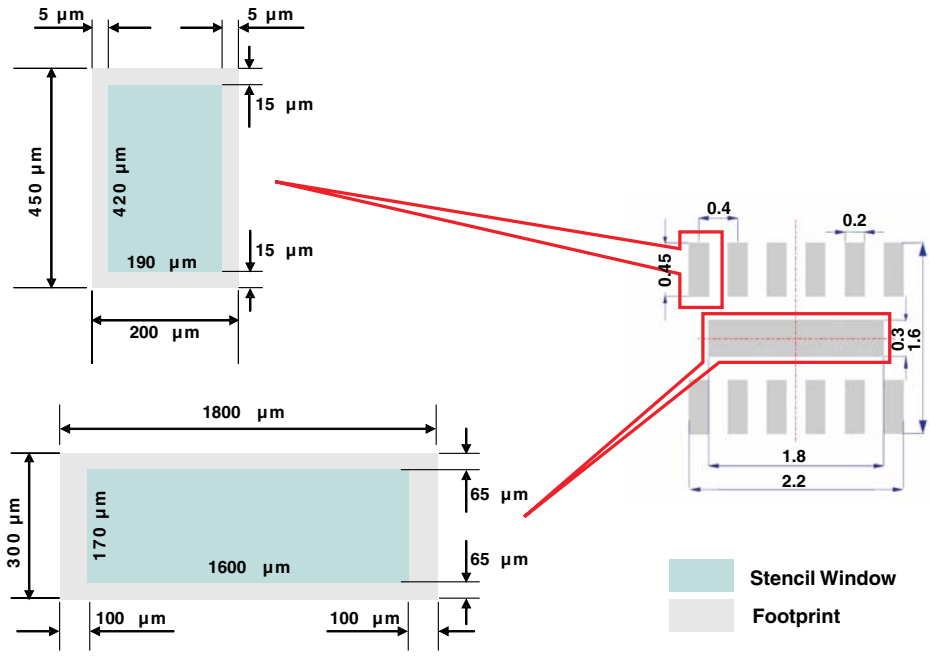
   b) General design rule
   Stencil thickness (T) = 75 ~ 125 µm

$$\text{Aspect Ratio} = \frac{W}{T} \geq 1.5$$

$$\text{Aspect Area} = \frac{L \times W}{2T(L+W)} \geq 0.66$$

2. Reference design
   a) Stencil opening thickness: 100 µm
   b) Stencil opening for central exposed pad: Opening to footprint ratio is 50%.
   c) Stencil opening for leads: Opening to footprint ratio is 90%.

Figure 17. Recommended stencil window position



4.2 Solder paste

1. Halide-free flux qualification ROL0 according to ANSI/J-STD-004.
2. “No clean” solder paste is recommended.
3. Offers a high tack force to resist component movement during high speed.
4. Solder paste with fine particles: powder particle size is 20-45 µm.

4.3 Placement

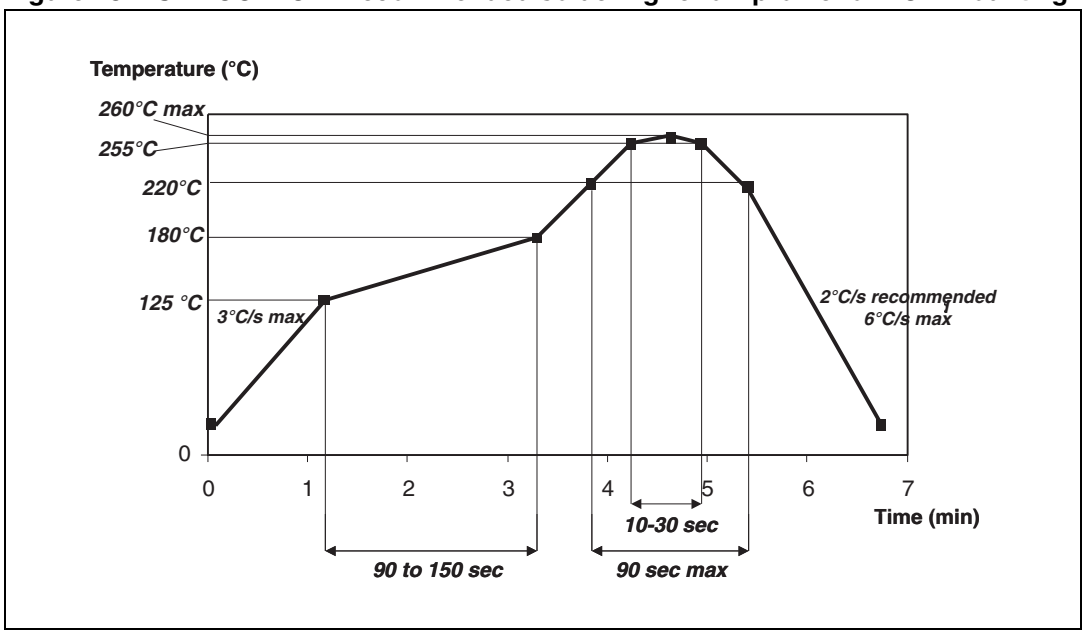
1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering.
3. Standard tolerance of ± 0.05 mm is recommended.
4. 3.5 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

4.4 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. The symmetrical layout is recommended, in case any tilt phenomena caused by asymmetrical solder paste amount due to the solder flow away.

4.5 Reflow profile

Figure 18. ST ECOPACK® recommended soldering reflow profile for PCB mounting



Note: Minimize air convection currents in the reflow oven to avoid component movement.

5 Ordering information

Table 4. Ordering information

Order code	Marking	Package	Weight	Base qty	Delivery mode
EMIF06-1005N12	KB	µQFN-12L	4.48 mg	3000	Tape and reel 7”

6 Revision history

Table 5. Document revision history

Date	Revision	Changes
12-Jan-2010	1	Initial release.
03-Jul-2011	2	Updated package name throughout the document.

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