



#### REVISION HISTORY

<u>Revision</u>	<u>Description</u>	<u>Issue Date</u>
Rev. 0.1	Initial Issue	Oct.14.2007
Rev. 0.2	Added I <sub>SB</sub> Spec.	Feb.1.2008
Rev. 0.3	Revised <b>FEATURES &amp; ORDERING INFORMATION</b> <b>Lead free and green package available</b> to <b>Green package available</b>	May.20.2009
	Added packing type in <b>ORDERING INFORMATION</b>	
	Deleted T <sub>SOLDER</sub> in <b>ABSOLUTE MAXIMUM RATINGS</b>	
Rev. 0.4	Revised V <sub>DR</sub>	Sep.11.2009
Rev. 0.5	Revised <b>ORDERING INFORMATION</b> in page 11	Aug.30.2010
Rev. 0.6	Deleted E grade	Apr.12.2011
	Revised I <sub>SB1</sub> in page 4	
Rev.1.0	Revised Notes item 1 and 2 in page 4 1. V <sub>IH</sub> (max) = V <sub>CC</sub> + 2.0V for pulse width less than 6ns. 2. V <sub>IL</sub> (min) = V <sub>SS</sub> - 2.0V for pulse width less than 6ns.	Aug.29.2013
	Revised <b>ORDERING INFORMATION</b>	

## FEATURES

- Fast access time : 55/70ns
- Low power consumption:  
 Operating current : 45/30mA (TYP.)  
 Standby current : 8 $\mu$ A (TYP.) LL-version
- Single 4.5V ~ 5.5V power supply
- All inputs and outputs TTL compatible
- Fully static operation
- Tri-state output
- Data retention voltage : 1.5V (MIN.)
- **Green package available**
- Package : 44-pin 400 mil TSOP-II  
 48-ball 6mm x 8mm TFBGA

## GENERAL DESCRIPTION

The LY6210248 is a 8,388,608-bit low power CMOS static random access memory organized as 1,048,576 words by 8 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

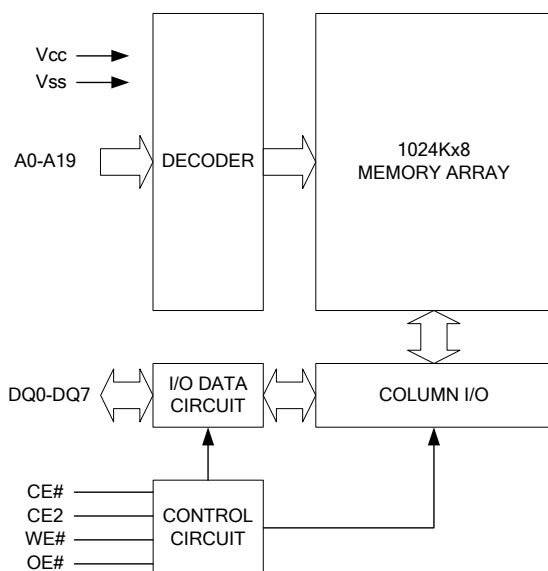
The LY6210248 is well designed for very low power system applications, and particularly well suited for battery back-up nonvolatile memory application.

The LY6210248 operates from a single power supply of 4.5V ~ 5.5V and all inputs and outputs are fully TTL compatible

## PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation	
				Standby(I <sub>SB1</sub> ,TYP.)	Operating(I <sub>CC</sub> ,TYP.)
LY6210248	0 ~ 70°C	4.5 ~ 5.5V	55/70ns	8 $\mu$ A(LL)	45/30mA
LY6210248(I)	-40 ~ 85°C	4.5 ~ 5.5V	55/70ns	8 $\mu$ A(LL)	45/30mA

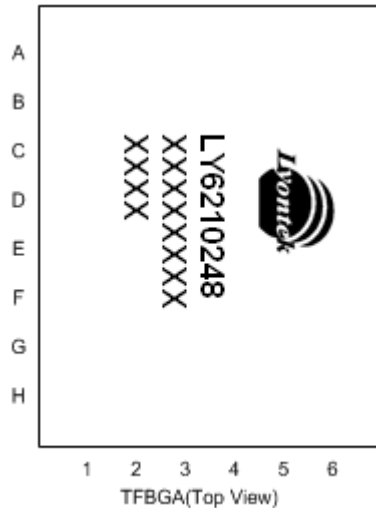
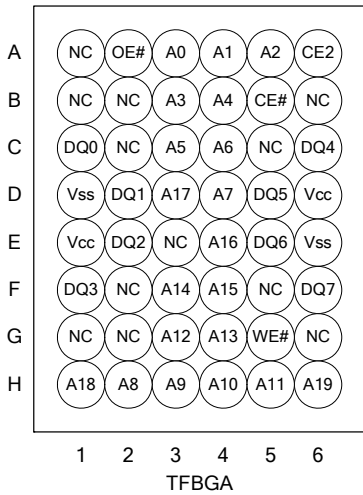
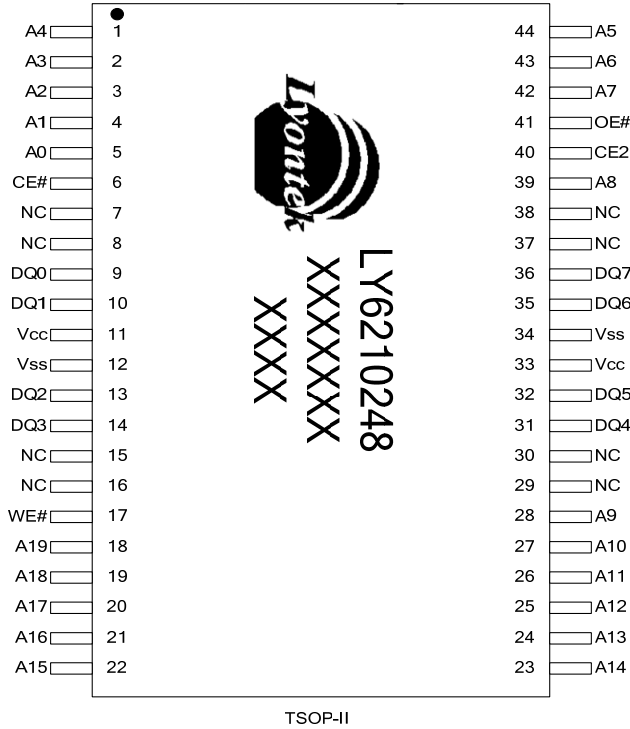
## FUNCTIONAL BLOCK DIAGRAM



## PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A19	Address Inputs
DQ0 – DQ7	Data Inputs/Outputs
CE#, CE2	Chip Enable Inputs
WE#	Write Enable Input
OE#	Output Enable Input
Vcc	Power Supply
Vss	Ground
NC	No Connection

**PIN CONFIGURATION**





#### ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Voltage on Vcc relative to Vss	V <sub>T1</sub>	-0.5 to 6.5	V
Voltage on any other pin relative to Vss	V <sub>T2</sub>	-0.5 to V <sub>CC</sub> +0.5	V
Operating Temperature	T <sub>A</sub>	0 to 70(C grade)	°C
		-40 to 85(I grade)	
Storage Temperature	T <sub>STG</sub>	-65 to 150	°C
Power Dissipation	P <sub>D</sub>	1	W
DC Output Current	I <sub>OUT</sub>	50	mA

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

#### TRUTH TABLE

MODE	CE#	CE2	OE#	WE#	I/O OPERATION	SUPPLY CURRENT
Standby	H	X	X	X	High-Z	I <sub>SB</sub> , I <sub>SB1</sub>
	X	L	X	X	High-Z	I <sub>SB</sub> , I <sub>SB1</sub>
Output Disable	L	H	H	H	High-Z	I <sub>CC</sub> , I <sub>CC1</sub>
Read	L	H	L	H	D <sub>OUT</sub>	I <sub>CC</sub> , I <sub>CC1</sub>
Write	L	H	X	L	D <sub>IN</sub>	I <sub>CC</sub> , I <sub>CC1</sub>

Note: H = V<sub>IH</sub>, L = V<sub>IL</sub>, X = Don't care.

**DC ELECTRICAL CHARACTERISTICS**

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP. <sup>4</sup>	MAX.	UNIT	
Supply Voltage	V <sub>CC</sub>		4.5	5.0	5.5	V	
Input High Voltage	V <sub>IH</sub> <sup>1</sup>		2.4	-	V <sub>CC</sub> +0.3	V	
Input Low Voltage	V <sub>IL</sub> <sup>2</sup>		- 0.2	-	0.6	V	
Input Leakage Current	I <sub>LI</sub>	V <sub>CC</sub> ≥ V <sub>IN</sub> ≥ V <sub>SS</sub>	- 1	-	1	μA	
Output Leakage Current	I <sub>LO</sub>	V <sub>CC</sub> ≥ V <sub>OUT</sub> ≥ V <sub>SS</sub> Output Disabled	- 1	-	1	μA	
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -1mA	2.4	-	-	V	
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 2mA	-	-	0.4	V	
Average Operating Power supply Current	I <sub>CC</sub>	Cycle time = Min. CE# = V <sub>IL</sub> and CE2 = V <sub>IH</sub> I <sub>I/O</sub> = 0mA Other pins at V <sub>IL</sub> or V <sub>IH</sub>	- 55	-	45	60	mA
			- 70	-	30	50	mA
	I <sub>CC1</sub>	Cycle time = 1μs CE# ≤ 0.2V and CE2 ≥ V <sub>CC</sub> -0.2V I <sub>I/O</sub> = 0mA Other pins at 0.2V or V <sub>CC</sub> -0.2V	-	6	12	mA	
Standby Power Supply Current	I <sub>SB</sub>	CE# = V <sub>IH</sub> or CE2 = V <sub>IL</sub> Other pins at V <sub>IL</sub> or V <sub>IH</sub>	-	0.2	2	mA	
	I <sub>SB1</sub>	CE# ≥ V <sub>CC</sub> -0.2V or CE2 ≤ 0.2V Other pins at 0.2V or V <sub>CC</sub> -0.2V	-LL	-	8	30	μA
			-LLI	-	8	50	μA

## Notes:

- V<sub>IH</sub>(max) = V<sub>CC</sub> + 2.0V for pulse width less than 6ns.
- V<sub>IL</sub>(min) = V<sub>SS</sub> - 2.0V for pulse width less than 6ns.
- Over/Undershoot specifications are characterized, not 100% tested.
- Typical values are included for reference only and are not guaranteed or tested.  
Typical values are measured at V<sub>CC</sub> = V<sub>CC</sub>(TYP.) and T<sub>A</sub> = 25°C

**CAPACITANCE (T<sub>A</sub> = 25°C, f = 1.0MHz)**

PARAMETER	SYMBOL	MIN.	MAX	UNIT
Input Capacitance	C <sub>IN</sub>	-	6	pF
Input/Output Capacitance	C <sub>I/O</sub>	-	8	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

**AC TEST CONDITIONS**

Input Pulse Levels	0.2V to V <sub>CC</sub> - 0.2V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	C <sub>L</sub> = 30pF + 1TTL, I <sub>OH</sub> /I <sub>OL</sub> = -1mA/2mA



#### AC ELECTRICAL CHARACTERISTICS

##### (1) READ CYCLE

PARAMETER	SYM.	LY6210248-55		LY6210248-70		UNIT
		MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t <sub>RC</sub>	55	-	70	-	ns
Address Access Time	t <sub>AA</sub>	-	55	-	70	ns
Chip Enable Access Time	t <sub>ACE</sub>	-	55	-	70	ns
Output Enable Access Time	t <sub>OE</sub>	-	30	-	35	ns
Chip Enable to Output in Low-Z	t <sub>CLZ</sub> *	10	-	10	-	ns
Output Enable to Output in Low-Z	t <sub>OLZ</sub> *	5	-	5	-	ns
Chip Disable to Output in High-Z	t <sub>CHZ</sub> *	-	20	-	25	ns
Output Disable to Output in High-Z	t <sub>OHZ</sub> *	-	20	-	25	ns
Output Hold from Address Change	t <sub>OH</sub>	10	-	10	-	ns

##### (2) WRITE CYCLE

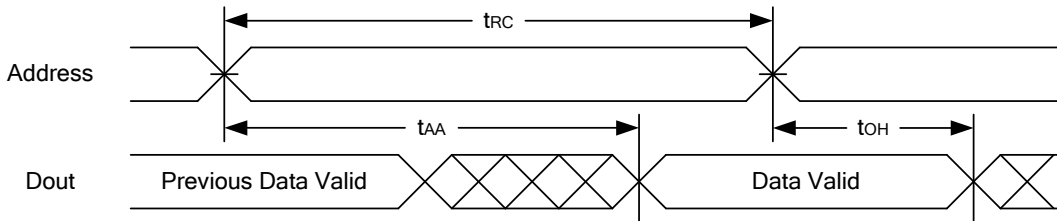
PARAMETER	SYM.	LY6210248-55		LY6210248-70		UNIT
		MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t <sub>WC</sub>	55	-	70	-	ns
Address Valid to End of Write	t <sub>AW</sub>	50	-	60	-	ns
Chip Enable to End of Write	t <sub>CW</sub>	50	-	60	-	ns
Address Set-up Time	t <sub>AS</sub>	0	-	0	-	ns
Write Pulse Width	t <sub>WP</sub>	45	-	55	-	ns
Write Recovery Time	t <sub>WR</sub>	0	-	0	-	ns
Data to Write Time Overlap	t <sub>DW</sub>	25	-	30	-	ns
Data Hold from End of Write Time	t <sub>DH</sub>	0	-	0	-	ns
Output Active from End of Write	t <sub>OW</sub> *	5	-	5	-	ns
Write to Output in High-Z	t <sub>WHZ</sub> *	-	20	-	25	ns

\*These parameters are guaranteed by device characterization, but not production tested.

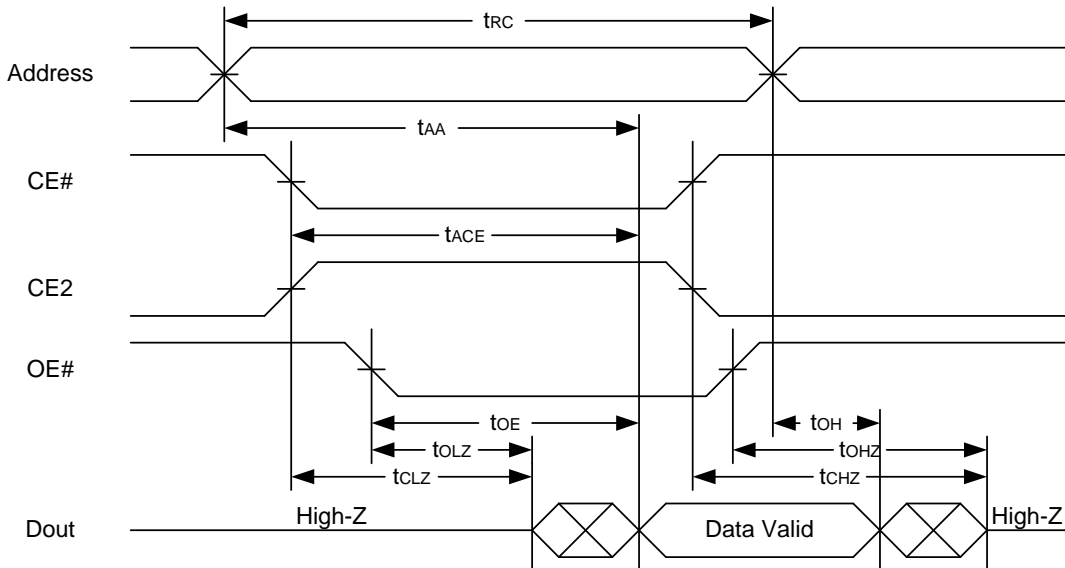


#### TIMING WAVEFORMS

##### READ CYCLE 1 (Address Controlled) (1,2)



##### READ CYCLE 2 (CE# and CE2 and OE# Controlled) (1,3,4,5)

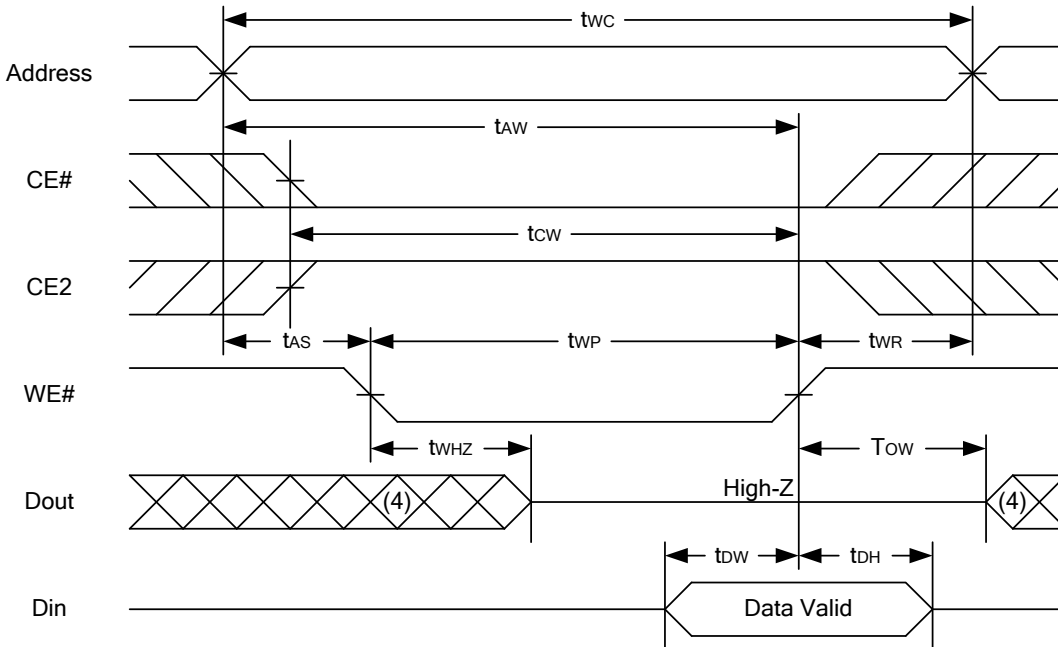


#### Notes :

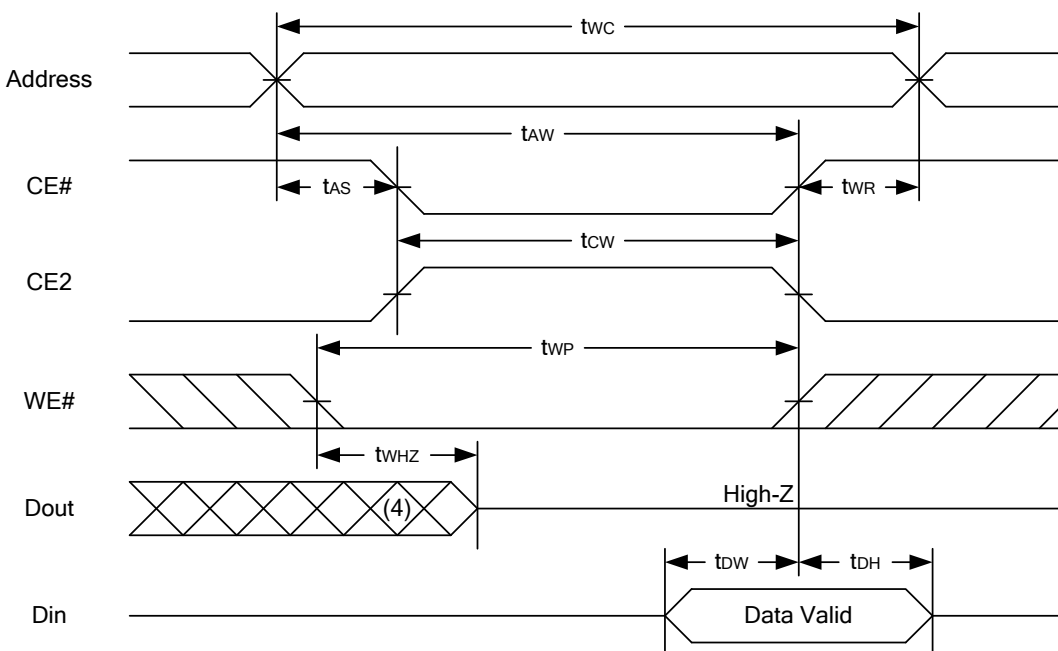
1. WE# is high for read cycle.
2. Device is continuously selected OE# = low, CE# = low, CE2 = high.
3. Address must be valid prior to or coincident with CE# = low, CE2 = high; otherwise tAA is the limiting parameter.
4. tCLZ, tOLZ, tCHZ and tOHZ are specified with CL = 5pF. Transition is measured ±500mV from steady state.
5. At any given temperature and voltage condition, tCHZ is less than tCLZ, tOHZ is less than tOLZ.



#### WRITE CYCLE 1 (WE# Controlled) (1,2,3,5,6)



#### WRITE CYCLE 2 (CE# and CE2 Controlled) (1,2,5,6)



Notes :

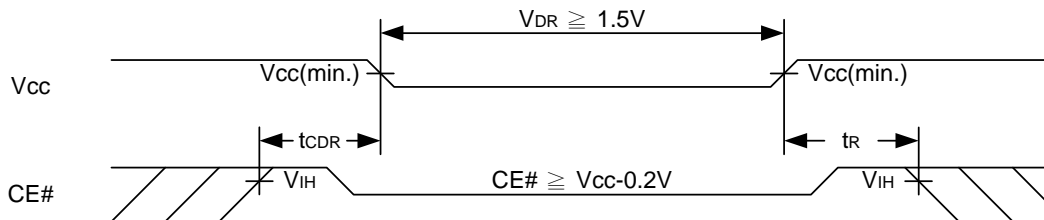
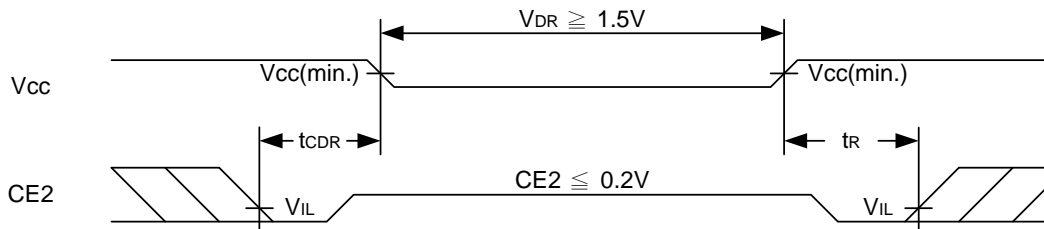
1. WE#, CE# must be high or CE2 must be low during all address transitions.
2. A write occurs during the overlap of a low CE#, high CE2, low WE#.
3. During a WE#-controlled write cycle with OE# low, twp must be greater than twhz + tdw to allow the drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the CE# low transition and CE2 high transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
6. tow and twhz are specified with CL = 5pF. Transition is measured ±500mV from steady state.

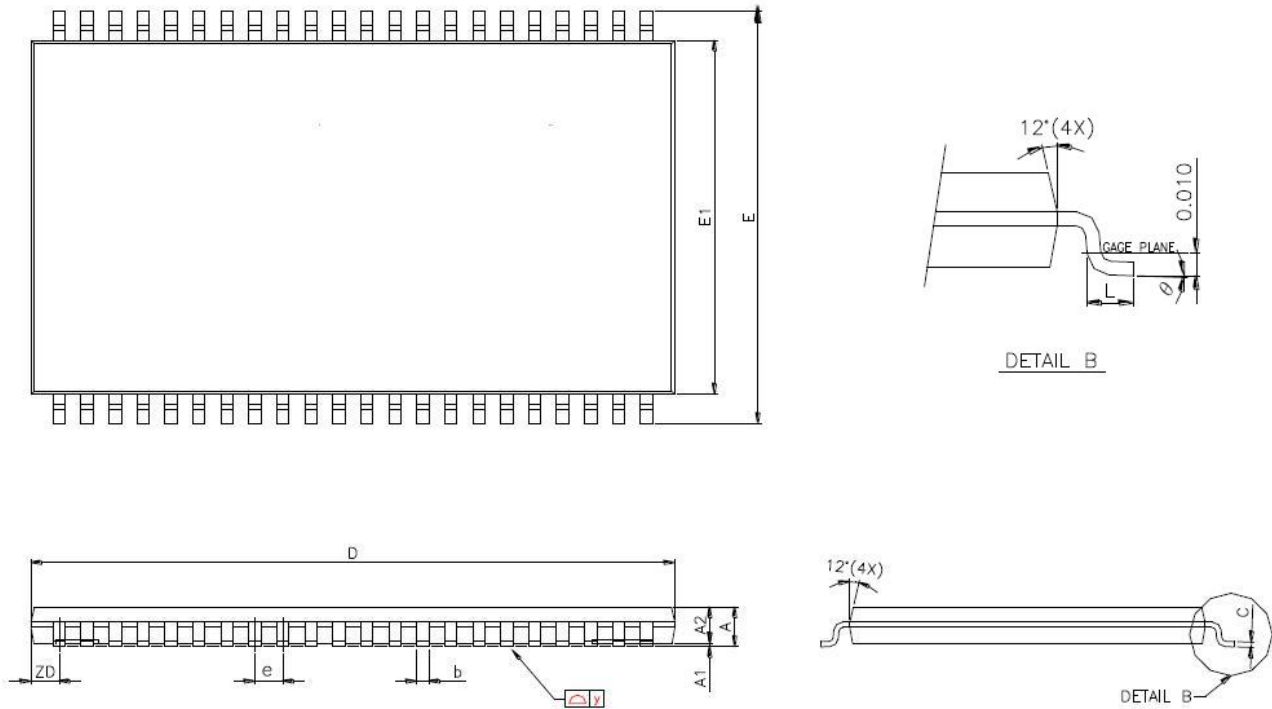


**DATA RETENTION CHARACTERISTICS**

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Vcc for Data Retention	V <sub>DR</sub>	CE# ≥ V <sub>CC</sub> - 0.2V or CE2 ≤ 0.2V	1.5	-	5.5	V
Data Retention Current	I <sub>DR</sub>	V <sub>CC</sub> = 1.5V CE# ≥ V <sub>CC</sub> - 0.2V or CE2 ≤ 0.2V Other pins at 0.2V or V <sub>CC</sub> - 0.2V	-LL	5	30	μA
			-LLI	5	50	μA
Chip Disable to Data Retention Time	t <sub>CDR</sub>	See Data Retention Waveforms (below)	0	-	-	ns
Recovery Time	t <sub>R</sub>		t <sub>RC*</sub>	-	-	ns

 t<sub>RC\*</sub> = Read Cycle Time

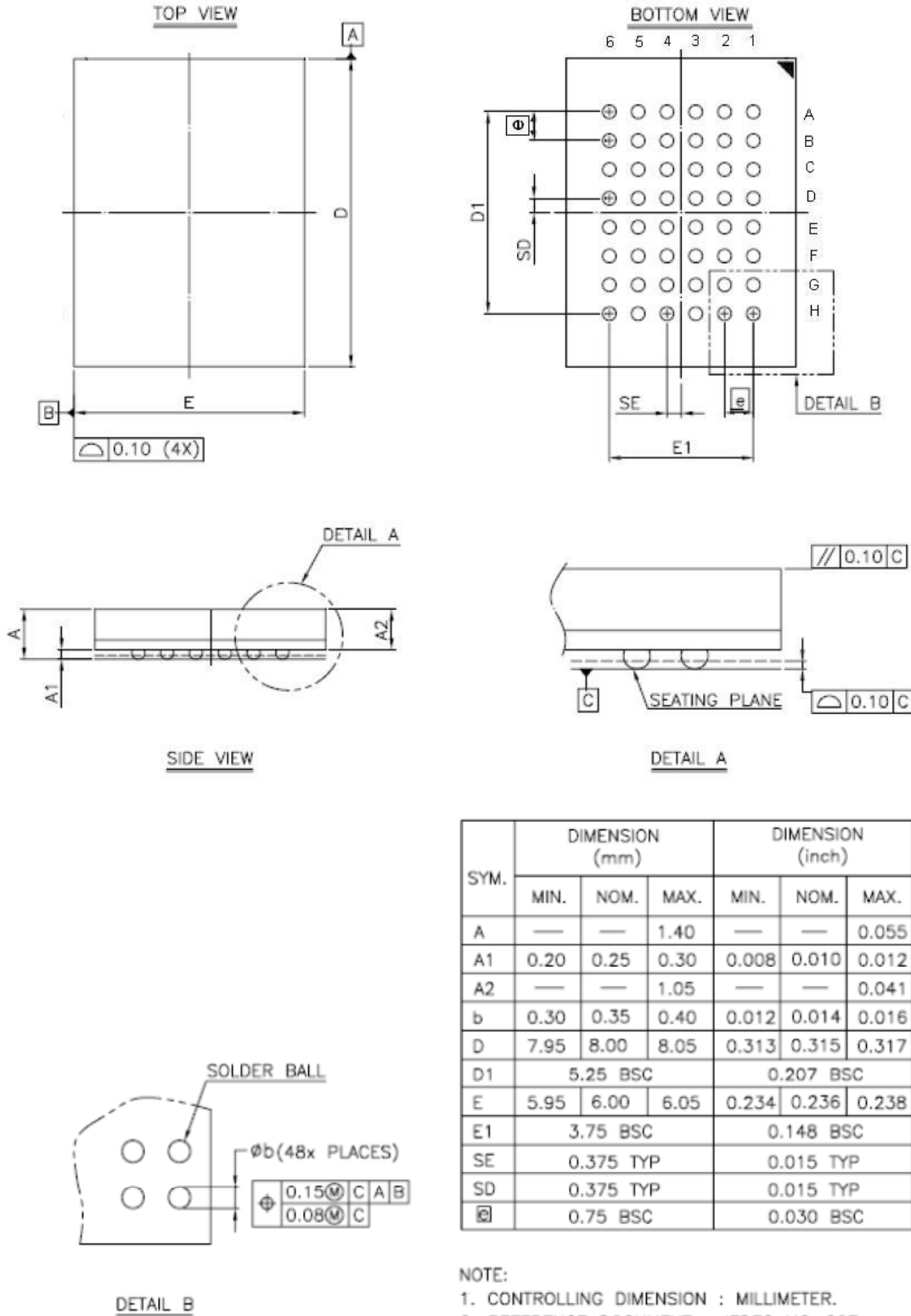
**DATA RETENTION WAVEFORM**
**Low Vcc Data Retention Waveform (1) (CE# controlled)**

**Low Vcc Data Retention Waveform (2) (CE2 controlled)**


**PACKAGE OUTLINE DIMENSION**
**44-pin 400mil TSOP-II Package Outline Dimension**


SYMBOLS	DIMENSIONS IN MILLMETERS			DIMENSIONS IN MILS		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	-	-	1.20	-	-	47.2
A1	0.05	0.10	0.15	2.0	3.9	5.9
A2	0.95	1.00	1.05	37.4	39.4	41.3
b	0.30	-	0.45	11.8	-	17.7
c	0.12	-	0.21	4.7	-	8.3
D	18.212	18.415	18.618	717	725	733
E	11.506	11.760	12.014	453	463	473
E1	9.957	10.160	10.363	392	400	408
e	-	0.800	-	-	31.5	-
L	0.40	0.50	0.60	15.7	19.7	23.6
ZD	-	0.805	-	-	31.7	-
y	-	-	0.076	-	-	3
θ	0°	3°	6°	0°	3°	6°



#### 48-ball 6mm x 8mm TFBGA Package Outline Dimension





#### ORDERING INFORMATION

Package Type	Access Time (Speed)(ns)	Power Type	Temperature Range(°C)	Packing Type	Lyontek Item No.
48Pin12mmx20mm TSOP-I	55	Ultra Low Power	0°C~70°C	Tray	LY6210248ML-55LL
				Tape Reel	LY6210248ML-55LLT
			-40°C~85°C	Tray	LY6210248ML-55LLI
				Tape Reel	LY6210248ML-55LLIT
	70	Ultra Low Power	0°C~70°C	Tray	LY6210248ML-70LL
				Tape Reel	LY6210248ML-70LLT
			-40°C~85°C	Tray	LY6210248ML-70LLI
				Tape Reel	LY6210248ML-70LLIT
48-ball 6mmx8mm TFBGA	55	Ultra Low Power	0°C~70°C	Tray	LY6210248GL-55LL
				Tape Reel	LY6210248GL-55LLT
			-40°C~85°C	Tray	LY6210248GL-55LLI
				Tape Reel	LY6210248GL-55LLIT
	70	Ultra Low Power	0°C~70°C	Tray	LY6210248GL-70LL
				Tape Reel	LY6210248GL-70LLT
			-40°C~85°C	Tray	LY6210248GL-70LLI
				Tape Reel	LY6210248GL-70LLIT



**Lyontek Inc.**

**LY6210248**

Rev. 1.0

**1024K X 8 BIT LOW POWER CMOS SRAM**

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