UT54ACS164/UT54ACTS164

8-Bit Shift Registers

Datasheet November 2010 www.aeroflex.com/logic



FEATURES □ AND-gated (enable/disable) serial inputs □ Fully buffered clock and serial inputs □ Direct clear □ 1.2μ CMOS - Latchup immune □ High speed □ Low power consumption □ Single 5 volt supply □ Available QML Q or V processes □ Flexible package

☐ UT54ACS164 - SMD 5962-96556

☐ UT54ACTS164 - SMD 5962-96557

DESCRIPTION

14-pin DIP14-lead flatpack

The UT54ACS164 and the UT54ACTS164 are 8-bit shift registers which feature AND-gated serial inputs and an asynchronous clear. The gated serial inputs (A and B) permit complete control over incoming data. A low at either input inhibits entry of new data and resets the first flip-flop to the low level at the next clock pulse. A high-level at both serial inputs sets the first flip-flop to the high level at the next clock pulse. Data at the serial inputs may be changed while the clock is high or low, providing the minimum setup time requirements are met. Clocking occurs on the low-to-high-level transition of the clock input.

The devices are characterized over full military temperature range of -55 $^{\circ}$ C to +125 $^{\circ}$ C.

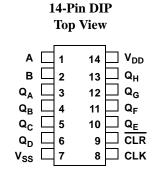
FUNCTION TABLE

INPUTS			OUTPUTS			
CLR	CLK	Α	В	Q_A	Q _B Q _H	
L	Х	Х	Х	L	L	L
Н	L	Χ	Χ	Q_{A0}	Q_{B0}	Q_{H0}
Н	\uparrow	Н	Н	Н	Q_{An}	Q_Gn
Н	\uparrow	L	Χ	L	Q_{An}	Q_Gn
Н	\uparrow	Х	L	L	Q_{An}	Q_Gn

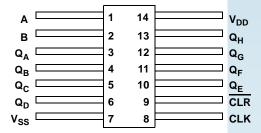
Notes:

- 1. Q_{A0} , Q_{B0} , Q_{H0} = the level of Q_A , Q_B or Q_H , respectively, before the indicated steady-state input conditions were established.
- 2. Q_{An} and Q_{Gn} = the level of Q_A or Q_G before the most recent \uparrow transition of the clock; indicates a one-bit shift.

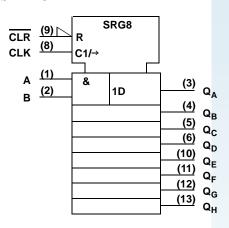
PINOUTS



14-Lead Flatpack Top View



LOGIC SYMBOL

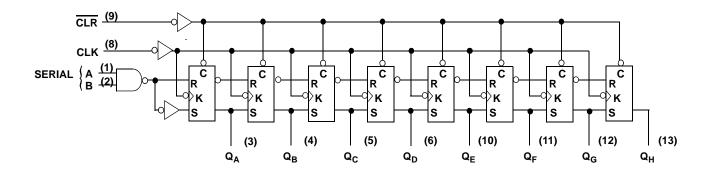


Note

 Logic symbol in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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LOGIC DIAGRAM



OPERATIONAL ENVIRONMENT¹

PARAMETER	LIMIT	UNITS
Total Dose	1.0E6	rads(Si)
SEU Threshold ²	80	MeV-cm ² /mg
SEL Threshold	120	MeV-cm ² /mg
Neutron Fluence	1.0E14	n/cm ²

Notes:

- 1. Logic will not latchup during radiation exposure within the limits defined in the table.
- 2. Device storage elements are immune to SEU affects.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	LIMIT	UNITS
V _{DD}	Supply voltage	-0.3 to 7.0	V
V _{I/O}	Voltage any pin	3 to V _{DD} +.3	V
T _{STG}	Storage Temperature range	-65 to +150	°C
T_{J}	Maximum junction temperature	+175	°C
T _{LS}	Lead temperature (soldering 5 seconds)	+300	°C
$\Theta_{ m JC}$	Thermal resistance junction to case	20	°C/W
I _I	DC input current	±10	mA
P _D	Maximum power dissipation	1	W

Note:

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMIT	UNITS
V _{DD}	Supply voltage	4.5 to 5.5	V
V _{IN}	Input voltage any pin	0 to V _{DD}	V
T _C	Temperature range	-55 to + 125	°C

^{1.} Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, functional operation of the device at these or any other conditions beyond limits indicated in the operational sections is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS 7

 $(V_{DD} = 5.0V \pm 10\%; \ V_{SS} = \ 0V^6, \ -55^\circ C < T_C < +125^\circ C); \ Unless \ otherwise \ noted, \ Tc \ is \ per \ the \ temperature \ range \ ordered.$

SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNIT
V _{IL}	Low-level input voltage ¹ ACTS ACS			0.8 .3V _{DD}	V
V _{IH}	High-level input voltage ¹ ACTS ACS		.5V _{DD} .7V _{DD}		V
I _{IN}	Input leakage current ACTS/ACS	$V_{IN} = V_{DD}$ or V_{SS}	-1	1	μΑ
V _{OL}	Low-level output voltage ³ ACTS ACS	$I_{OL} = 8.0 \text{mA}$ $I_{OL} = 100 \mu \text{A}$		0.40 0.25	V
V _{OH}	High-level output voltage ³ ACTS ACS	$I_{OH} = -8.0 \text{mA}$ $I_{OH} = -100 \mu \text{A}$.7V _{DD} V _{DD} - 0.25		V
I _{OS}	Short-circuit output current ² , ⁴ ACTS/ACS	$V_O = V_{DD}$ and V_{SS}	-200	200	mA
I _{OL}	Output current ¹⁰ (Sink)	$V_{IN} = V_{DD}$ or V_{SS} $V_{OL} = 0.4V$	8		mA
I _{OH}	Output current ¹⁰ (Source)	$V_{IN} = V_{DD}$ or V_{SS} $V_{OH} = V_{DD} - 0.4V$	-8		mA
P _{total}	Power dissipation ^{2, 8, 9}	$C_L = 50 pF$		1.9	mW/ MHz
I _{DDQ}	Quiescent Supply Current	$V_{DD} = 5.5V$		10	μА
$\Delta I_{ m DDQ}$	Quiescent Supply Current Delta ACTS	For input under test $V_{IN} = V_{DD} - 2.1V$ For all other inputs $V_{IN} = V_{DD} \text{ or } V_{SS}$ $V_{DD} = 5.5V$		1.6	mA
C _{IN}	Input capacitance ⁵	f = 1MHz @ 0V		15	pF
C _{OUT}	Output capacitance ⁵	f = 1MHz @ 0V		15	pF

Notes:

- 1. Functional tests are conducted in accordance with MIL-STD-883 with the following input test conditions: $V_{IH} = V_{IH}(min) + 20\%$, 0%; $V_{IL} = V_{IL}(max) + 0\%$, 50%, as specified herein, for TTL, CMOS, or Schmitt compatible inputs. Devices may be tested using any input voltage within the above specified range, but are guaranteed to $V_{IH}(min)$ and $V_{IL}(max)$.
- 2. Supplied as a design limit but not guaranteed or tested.
- 3. Per MIL-PRF-38535, for current density \leq 5.0E5 amps/cm², the maximum product of load capacitance (per output buffer) times frequency should not exceed 3,765 pF/MHz.
- 4. Not more than one output may be shorted at a time for maximum duration of one second.
- 5. Capacitance measured for initial qualification and when design changes may affect the value. Capacitance is measured between the designated terminal and V_{SS} at frequency of 1MHz and a signal amplitude of 50mV rms maximum.
- 6. Maximum allowable relative shift equals 50mV.
- 7. All specifications valid for radiation dose \leq 1E6 rads(Si).
- 8. Power does not include power contribution of any TTL output sink current
- 9. Power dissipation specified per switching output.
- 10. This value is guaranteed based on characterization data, but not tested.

AC ELECTRICAL CHARACTERISTICS 2

 $(V_{DD} = 5.0V \pm 10\%; \ V_{SS} = \ 0V^{-1}, \ -55^{\circ}C < T_{C} < +125^{\circ}C); \ Unless \ otherwise \ noted, \ Tc \ is \ per \ the \ temperature \ range \ ordered.$

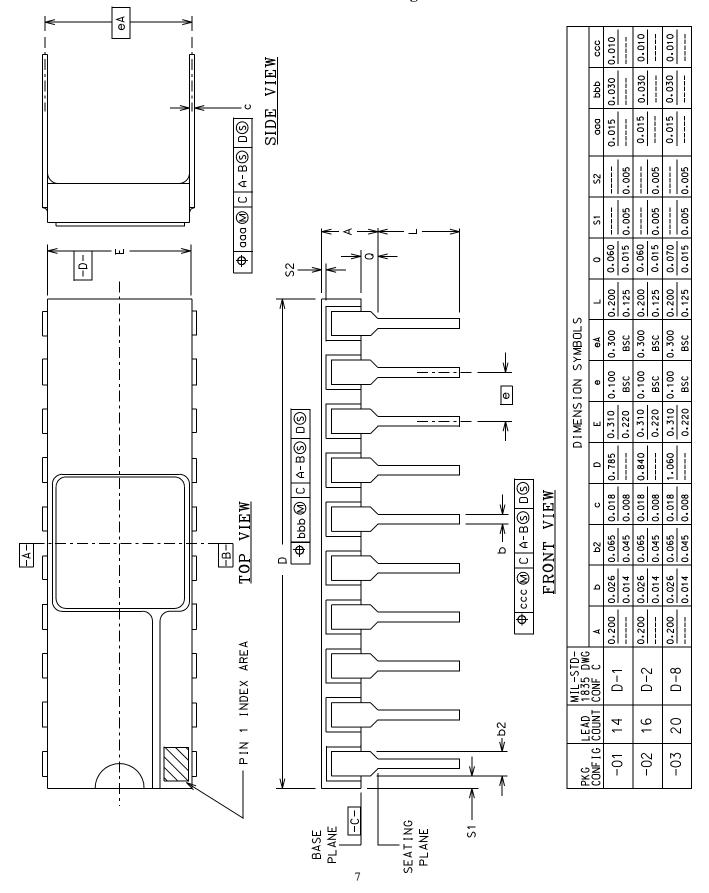
SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNIT
t _{PHL}	CLK to Qn	4	21	ns
t _{PLH}	CLK to Qn	2	18	ns
t _{PHL}	CLR to Qn	5	21	ns
f_{MAX}	Maximum clock frequency		83	MHz
t _{SU1}	CLR inactive Setup time before CLK ↑	4		ns
t _{SU2}	Data setup time before CLK↑	4		ns
t_H^3	Data hold time after CLK ↑	2		ns
t _W	Minimum pulse width CLR low CLK high CLK low	6		ns

Notes:

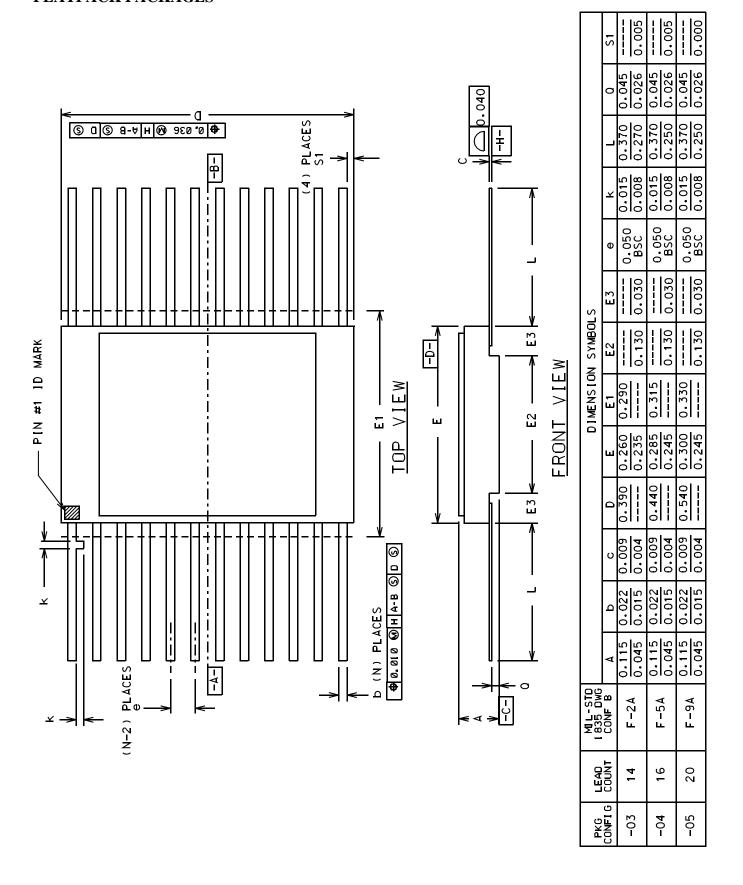
- Maximum allowable relative shift equals 50mV.
 All specifications valid for radiation dose ≤ 1E6 rads(Si).
 Based on characterization, hold time (t_H) of 0ns can be assumed if data setup time (t_{SU2}) is ≥10ns. This is guaranteed, but not tested.

PACKAGING

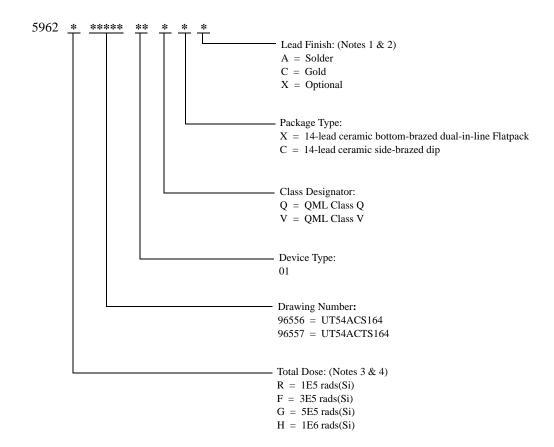
Side-Brazed Packages



FLATPACK PACKAGES



UT54ACS164/UT54ACTS164: SMD



Notes:

- 1. Lead finish (A,C, or X) must be specified.
- 2. If an "X" is specified when ordering, part marking will match the lead finish and will be either "A" (solder) or "C" (gold).
- $3. \ Total \ dose \ radiation \ must \ be \ specified \ when \ ordering. \ QML \ Q \ and \ QML \ V \ not \ available \ without \ radiation \ hardening. For \ prototype \ inquiries, \ contact \ factory.$
- 4. Device type 02 is only offered with a TID tolerance guarantee of 3E5 rads(Si) or 1E6 rads(Si) and is tested in accordance with MIL-STD-883 Test Method 1019 Condition A and section 3.11.2. Device type 03 is only offered with a TID tolerance guarantee of 1E5 rads(Si), 3E5 rads(Si), and 5E5 rads(Si), and is tested in accordance with MIL-STD-883 Test Method 1019 Condition A.

Aeroflex Colorado Springs - Datasheet Definition

Advanced Datasheet - Product In Development

Preliminary Datasheet - Shipping Prototype

Datasheet - Shipping QML & Reduced Hi-Rel

COLORADO

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