# 16-Bit, 250 kSPS PulSAR™ ADC in MSOP/QFN

# AD7685

## FEATURES

- 16-bit resolution with no missing codes
- Throughput: 250 kSPS
- INL: ±0.6 LSB typ, ±2 LSB max (±0.003 % of FSR)
- S/(N + D): 93.5 dB @ 20 kHz
- THD: −110 dB @ 20 kHz
- Pseudo-differential analog input range
  - 0 V to $V_{REF}$ with $V_{REF}$ up to VDD
- No pipeline delay
- Single-supply operation 2.3 V to 5.5 V with
  - 1.8 V to 5 V logic interface
- Serial interface SPI®/QSPI™/MICROWIRE™/DSP compatible
- Daisy chain multiple ADCs, BUSY indicator
- Power dissipation
  - 1.35 mW @ 2.5 V/100 kSPS, 4 mW @ 5 V/100 kSPS,
  - 1.4 µW @ 2.5 V/100 SPS
- Stand-by current: 1 nA
- 10-lead package: MSOP (MSOP-8 size) and
  - 3 mm × 3 mm QFN[1] (LFCSP) (SOT-23 size)
- Pin-for-pin compatible with AD7686, AD7687 and AD7688

## APPLICATIONS

- Battery-powered equipments:
  - Medical instruments
  - Mobile communications
  - Personal digital assistants
- Data acquisition
- Instrumentation
- Process controls

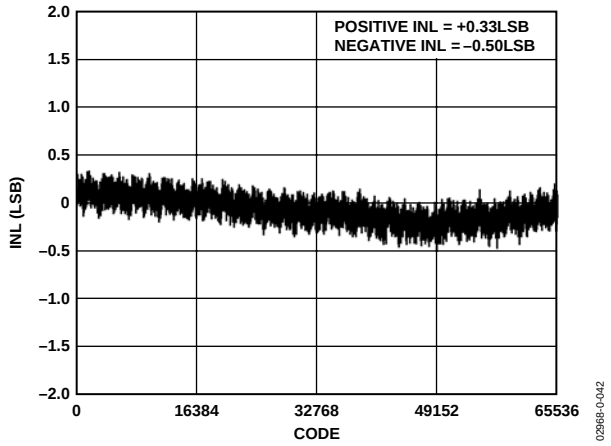


*Figure 1. Integral Nonlinearity vs. Code.*

## APPLICATION DIAGRAM

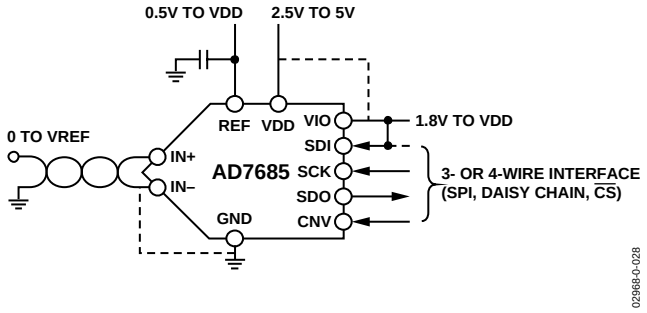


*Figure 2.*

**Table 1. MSOP, QFN (LFCSP)/SOT-23 16-Bit PulSAR ADCs**

| Type | 100 kSPS | 250 kSPS | 500 kSPS |
|---|---|---|---|
| True Differential | AD7684 | AD7687 | AD7688 |
| Pseudo | AD7683 | AD7685 | AD7686 |
| Differential/Unipolar | | AD7694 | |
| Unipolar | AD7680 | | |

## GENERAL DESCRIPTION

The AD7685 is a 16-bit, charge redistribution successive approximation, analog-to-digital converter (ADC) that operates from a single power supply, VDD, between 2.3 V to 5.5 V. It contains a low power, high speed, 16-bit sampling ADC with no missing codes, an internal conversion clock, and a versatile serial interface port. The part also contains a low noise, wide bandwidth, short aperture delay track-and-hold circuit. On the CNV rising edge, it samples an analog input IN+ between 0 V to REF with respect to a ground sense IN−. The reference voltage, REF, is applied externally and can be set up to the supply voltage.

Power dissipation scales linearly with throughput.

The SPI compatible serial interface also features the ability, using the SDI input, to daisy chain several ADCs on a single 3-wire bus or provides an optional BUSY indicator. It is compatible with 1.8 V, 2.5 V, 3 V, or 5 V logic using the separate supply VIO.

The AD7685 is housed in a 10-lead MSOP or a 10-lead QFN (LFCSP) with operation specified from −40°C to +85°C.

[1] Package in development. For QFN package, contact factory for samples and availability.

**Rev 0**


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### REVISION HISTORY

4/04—Initial Revision 0

# SPECIFICATIONS

VDD = 2.3 V to 5.5 V, VIO = 2.3 V to VDD, $V_{REF}$ = VDD, $T_A$ = −40°C to +85°C, unless otherwise noted.

**Table 2.**

| | | B Grade | | | C Grade[1] | | | |
|---|---|---|---|---|---|---|---|---|
| **Parameter** | **Conditions** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Unit** |
| RESOLUTION | | 16 | | | 16 | | | Bits |
| ANALOG INPUT | | | | | | | | |
| Voltage Range | IN+ − IN− | 0 | | $V_{REF}$ | 0 | | $V_{REF}$ | V |
| Absolute Input Voltage | IN+ | −0.1 | | VDD + 0.1 | −0.1 | | VDD + 0.1 | V |
| | IN− | −0.1 | | 0.1 | −0.1 | | 0.1 | V |
| Analog Input CMRR | $f_{IN}$ = 250 kHz | | 65 | | | 65 | | dB |
| Leakage Current at 25°C | Acquisition Phase | | 1 | | | 1 | | nA |
| Input Impedance | | See the Analog Input section. | | | | | | |
| ACCURACY | | | | | | | | |
| No Missing Codes | | 16 | | | 16 | | | Bits |
| Differential Linearity Error | | −1 | ±0.7 | | −1 | ±0.5 | +2 | LSB[2] |
| Integral Linearity Error | | −3 | ±1 | +3 | −2 | ±0.6 | +2 | LSB |
| Transition Noise | REF = VDD = 5 V | | 0.5 | | | 0.45 | | LSB |
| Gain Error[3], $T_{MIN}$ to $T_{MAX}$ | | | ±2 | ±30 | | ±2 | ±15 | LSB |
| Gain Error Temperature Drift | | | ±0.3 | | | ±0.3 | | ppm/°C |
| Offset Error[3], $T_{MIN}$ to $T_{MAX}$ | VDD = 4.5 V to 5.5 V | | ±0.1 | ±1.6 | | ±0.1 | ±1.6 | mV |
| | VDD = 2.3 V to 4.5 V | | ±0.7 | ±3.5 | | ±0.7 | ±3.5 | mV |
| Offset Temperature Drift | | | ±0.3 | | | ±0.3 | | ppm/°C |
| Power Supply Sensitivity | VDD = 5 V ± 5% | | ±0.05 | | | ±0.05 | | LSB |
| THROUGHPUT | | | | | | | | |
| Conversion Rate | VDD = 4.5 V to 5.5 V | 0 | | 250 | 0 | | 250 | kSPS |
| | VDD = 2.3 V to 4.5 V | 0 | | 200 | 0 | | 200 | kSPS |
| Transient Response | Full-Scale Step | | | 1.8 | | | 1.8 | µs |
| AC ACCURACY | | | | | | | | |
| Signal-to-Noise | $f_{IN}$ = 20 kHz, $V_{REF}$ = 5 V | 90 | 92 | | 92 | 93.5 | | dB[4] |
| | $f_{IN}$ = 20 kHz, $V_{REF}$ = 2.5 V | 86 | 88 | | 87.5 | 88.5 | | dB |
| Spurious-Free Dynamic Range | $f_{IN}$ = 20 kHz | | −106 | | | −110 | | dB |
| Total Harmonic Distortion | $f_{IN}$ = 20 kHz | | −106 | | | −110 | | dB |
| Signal-to-(Noise + Distortion) | $f_{IN}$ = 20 kHz, $V_{REF}$ = 5 V | 90 | 92 | | 92 | 93.5 | | dB |
| | $f_{IN}$ = 20 kHz, $V_{REF}$ = 5 V, −60 dB Input | | 32 | | | 33.5 | | dB |
| | $f_{IN}$ = 20 kHz, $V_{REF}$ = 2.5 V | 85.5 | 87.5 | | 87 | 88.5 | | dB |
| Intermodulation Distortion[5] | | | −110 | | | −115 | | dB |

[1] Future product. Contact factory for samples and availability.
[2] LSB means least significant bit. With the 5 V input range, 1 LSB is 76.3 µV.
[3] See Terminology section. These specifications do include full temperature range variation but do not include the error contribution from the external reference.
[4] All specifications in dB are referred to a full-scale input FS. Tested with an input signal at 0.5 dB below full-scale, unless otherwise specified.
[5] $f_{IN1}$ = 21.4 kHz, $f_{IN2}$ = 18.9 kHz, each tone at −7 dB below full-scale.

VDD = 2.3 V to 5.5 V, VIO = 2.3 V to VDD, $V_{REF}$ = VDD, $T_A$ = −40°C to +85°C, unless otherwise noted.

**Table 3.**

| Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| REFERENCE | | | | | |
| Voltage Range | | 0.5 | | VDD + 0.3 | V |
| Load Current | 250 kSPS, REF = 5 V | | 50 | | µA |
| SAMPLING DYNAMICS | | | | | |
| −3 dB Input Bandwidth | | | 2 | | MHz |
| Aperture Delay | VDD = 5 V | | 2.5 | | ns |
| DIGITAL INPUTS | | | | | |
| Logic Levels | | | | | |
| $V_{IL}$ | | −0.3 | | 0.3 × VIO | V |
| $V_{IH}$ | | 0.7 × VIO | | VIO + 0.3 | V |
| $I_{IL}$ | | −1 | | +1 | µA |
| $I_{IH}$ | | −1 | | +1 | µA |
| DIGITAL OUTPUTS | | | | | |
| Data Format | | Serial 16 Bits Straight Binary | | | |
| Pipeline Delay | | Conversion Results Available Immediately after Completed Conversion | | | |
| $V_{OL}$ | $I_{SINK}$ = +500 µA | | | 0.4 | V |
| $V_{OH}$ | $I_{SOURCE}$ = −500 µA | VIO − 0.3 | | | V |
| POWER SUPPLIES | | | | | |
| VDD | Specified Performance | 2.3 | | 5.5 | V |
| VIO | Specified Performance | 2.3 | | VDD + 0.3 | V |
| VIO Range | | 1.8 | | VDD + 0.3 | V |
| Standby Current[1, 2] | VDD and VIO = 5 V, 25°C | | 1 | 50 | nA |
| Power Dissipation | VDD = 2.5 V, 100 SPS Throughput | | 1.4 | | µW |
| | VDD = 2.5 V, 100 kSPS Throughput | | 1.35 | 2.4 | mW |
| | VDD = 2.5 V, 200 kSPS Throughput | | 2.7 | 4.8 | mW |
| | VDD = 5 V, 100 kSPS Throughput | | 4 | 6 | mW |
| | VDD = 5 V, 250 kSPS Throughput | | | 15 | mW |
| TEMPERATURE RANGE[3] | | | | | |
| Specified Performance | $T_{MIN}$ to $T_{MAX}$ | −40 | | +85 | °C |

[1] With all digital inputs forced to VIO or GND as required.
[2] During acquisition phase.
[3] Contact Analog Devices, Inc. for extended temperature range.

# TIMING SPECIFICATIONS

−40°C to +85°C, VIO = 2.3 V to 5.5 V or VDD + 0.3 V, whichever is the lowest, unless otherwise stated.

**Table 4. VDD = 4.5 V to 5.5 V[1]**

| | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Conversion Time: CNV Rising Edge to Data Available | $t_{CONV}$ | 0.5 | | 2.2 | µs |
| Acquisition Time | $t_{ACQ}$ | 1.8 | | | µs |
| Time between Conversions | $t_{CYC}$ | 4 | | | µs |
| CNV Pulse Width ($\overline{CS}$ Mode) | $t_{CNVH}$ | 10 | | | ns |
| SCK Period ($\overline{CS}$ Mode) | $t_{SCK}$ | 15 | | | ns |
| SCK Period (Chain Mode) | $t_{SCK}$ | | | | |
| VIO above 4.5 V | | 27 | | | ns |
| VIO above 3 V | | 28 | | | ns |
| VIO above 2.7 V | | 29 | | | ns |
| VIO above 2.3 V | | 30 | | | ns |
| SCK Low Time | $t_{SCKL}$ | 7 | | | ns |
| SCK High Time | $t_{SCKH}$ | 7 | | | ns |
| SCK Falling Edge to Data Remains Valid | $t_{HSDO}$ | 5 | | | ns |
| SCK Falling Edge to Data Valid Delay | $t_{DSDO}$ | | | | |
| VIO above 4.5 V | | | | 14 | ns |
| VIO above 3 V | | | | 15 | ns |
| VIO above 2.7 V | | | | 16 | ns |
| VIO above 2.3 V | | | | 17 | ns |
| CNV or SDI Low to SDO D15 MSB Valid ($\overline{CS}$ Mode) | $t_{EN}$ | | | | |
| VIO above 4.5 V | | | | 15 | ns |
| VIO above 2.7 V | | | | 18 | ns |
| VIO above 2.3 V | | | | 22 | ns |
| CNV or SDI High or Last SCK Falling Edge to SDO High Impedance ($\overline{CS}$ Mode) | $t_{DIS}$ | | | 25 | ns |
| SDI Valid Setup Time from CNV Rising Edge ($\overline{CS}$ Mode) | $t_{SSDICNV}$ | 15 | | | ns |
| SDI Valid Hold Time from CNV Rising Edge ($\overline{CS}$ Mode) | $t_{HSDICNV}$ | 0 | | | ns |
| SCK Valid Setup Time from CNV Rising Edge (Chain Mode) | $t_{SSCKCNV}$ | 5 | | | ns |
| SCK Valid Hold Time from CNV Rising Edge (Chain Mode) | $t_{HSCKCNV}$ | 5 | | | ns |
| SDI Valid Setup Time from SCK Falling Edge (Chain Mode) | $t_{SSDISCK}$ | 13 | | | ns |
| SDI Valid Hold Time from SCK Falling Edge (Chain Mode) | $t_{HSDISCK}$ | 4 | | | ns |

[1] See Figure 3 and Figure 4 for load conditions.

−40°C to +85°C, VIO = 2.3 V to 4.5 V or VDD + 0.3 V, whichever is the lowest, unless otherwise stated.

**Table 5. VDD = 2.3V to 4.5 V[1]**

| | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Conversion Time: CNV Rising Edge to Data Available | $t_{CONV}$ | 0.7 | | 3.2 | µs |
| Acquisition Time | $t_{ACQ}$ | 1.8 | | | µs |
| Time between Conversions | $t_{CYC}$ | 5 | | | µs |
| CNV Pulse Width ( $\overline{CS}$ Mode ) | $t_{CNVH}$ | 10 | | | ns |
| SCK Period ( $\overline{CS}$ Mode ) | $t_{SCK}$ | 25 | | | ns |
| SCK Period ( Chain Mode ) | $t_{SCK}$ | | | | |
| VIO above 3 V | | 54 | | | ns |
| VIO above 2.7 V | | 60 | | | ns |
| VIO above 2.3 V | | 65 | | | ns |
| SCK Low Time | $t_{SCKL}$ | 12 | | | ns |
| SCK High Time | $t_{SCKH}$ | 12 | | | ns |
| SCK Falling Edge to Data Remains Valid | $t_{HSDO}$ | 5 | | | ns |
| SCK Falling Edge to Data Valid Delay | $t_{DSDO}$ | | | | |
| VIO above 3 V | | | | 24 | ns |
| VIO above 2.7 V | | | | 30 | ns |
| VIO above 2.3 V | | | | 35 | ns |
| CNV or SDI Low to SDO D15 MSB Valid ($\overline{CS}$ Mode) | $t_{EN}$ | | | | |
| VIO above 2.7 V | | | | 18 | ns |
| VIO above 2.3 V | | | | 22 | ns |
| CNV or SDI High or Last SCK Falling Edge to SDO High Impedance ($\overline{CS}$ Mode) | $t_{DIS}$ | | | 25 | ns |
| SDI Valid Setup Time from CNV Rising Edge ($\overline{CS}$ Mode) | $t_{SSDICNV}$ | 30 | | | ns |
| SDI Valid Hold Time from CNV Rising Edge ($\overline{CS}$ Mode) | $t_{HSDICNV}$ | 0 | | | ns |
| SCK Valid Setup Time from CNV Rising Edge (Chain Mode) | $t_{SSCKCNV}$ | 5 | | | ns |
| SCK Valid Hold Time from CNV Rising Edge (Chain Mode) | $t_{HSCKCNV}$ | 8 | | | ns |
| SDI Valid Setup Time from SCK Falling Edge (Chain Mode) | $t_{SSDISCK}$ | 30 | | | ns |
| SDI Valid Hold Time from SCK Falling Edge (Chain Mode) | $t_{HSDISCK}$ | 4 | | | ns |

[1] See Figure 3 and Figure 4 for load conditions.

# ABSOLUTE MAXIMUM RATINGS

**Table 6.**

| Parameter | Ratings |
|---|---|
| Analog Inputs | |
| IN+[1], IN–[1], REF | GND – 0.3 V to VDD + 0.3 V or ±130 mA |
| Supply Voltages | |
| VDD, VIO to GND | –0.3 V to +7 V |
| VDD to VIO | ±7 V |
| Digital Inputs to GND | –0.3 V to VIO + 0.3 V |
| Digital Outputs to GND | –0.3 V to VIO + 0.3 V |
| Storage Temperature Range | –65°C to +150°C |
| Junction Temperature | 150°C |
| $\theta_{JA}$ Thermal Impedance | 200°C/W (MSOP-10) |
| $\theta_{JC}$ Thermal Impedance | 44°C/W (MSOP-10) |
| Lead Temperature Range | |
| Vapor Phase (60 sec) | 215°C |
| Infrared (15 sec) | 220°C |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[1] See the Analog Input section.

## ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.


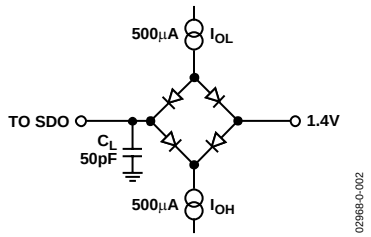


*Figure 3. Load Circuit for Digital Interface Timing*

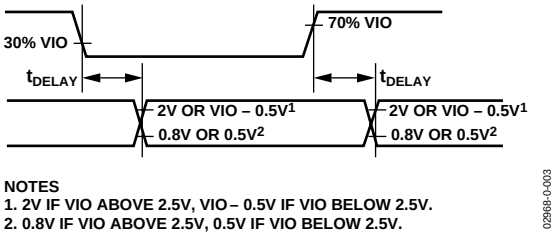


*Figure 4. Voltage Levels for Timing*

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

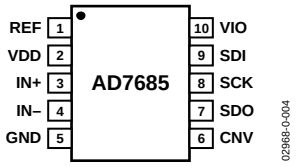


*Figure 5. 10-Lead MSOP and QFN (LFCSP) Pin Configuration*

**Table 7. Pin Function Descriptions**

| Pin No. | Mnemonic | Type[1] | Function |
|---|---|---|---|
| 1 | REF | AI | Reference Input Voltage. The REF range is from 0.5 V to VDD. It is referred to the GND pin. This pin should be decoupled closely to the pin with a 10 µF capacitor. |
| 2 | VDD | P | Power Supply. |
| 3 | IN+ | AI | Analog Input. It is referred to IN−. The voltage range, i.e., the difference between IN+ and IN−, is 0 V to $V_{REF}$. |
| 4 | IN− | AI | Analog Input Ground Sense. To be connected to the analog ground plane or to a remote sense ground. |
| 5 | GND | P | Power Supply Ground. |
| 6 | CNV | DI | Convert Input. This input has multiple functions. On its leading edge, it initiates the conversions and selects the interface mode of the part, chain or $\overline{CS}$ mode. In $\overline{CS}$ mode, it enables the SDO pin when low. In chain mode, the data should be read when CNV is high. |
| 7 | SDO | DO | Serial Data Output. The conversion result is output on this pin. It is synchronized to SCK. |
| 8 | SCK | DI | Serial Data Clock Input. When the part is selected, the conversion result is shifted out by this clock. |
| 9 | SDI | DI | Serial Data Input. This input provides multiple features. It selects the interface mode of the ADC as follows:<br>Chain mode is selected if SDI is low during the CNV rising edge. In this mode, SDI is used as a data input to daisy chain the conversion results of two or more ADCs onto a single SDO line. The digital data level on SDI is output on SDO with a delay of 16 SCK cycles.<br>$\overline{CS}$ mode is selected if SDI is high during the CNV rising edge. In this mode, either SDI or CNV can enable the serial output signals when low, and if SDI or CNV is low when the conversion is complete, the BUSY indicator feature is enabled. |
| 10 | VIO | P | Input/Output Interface Digital Power. Nominally at the same supply as the host interface (1.8 V, 2.5 V, 3 V, or 5 V). |

[1]AI = Analog Input, DI = Digital Input, DO = Digital Output, and P = Power

# TERMINOLOGY

**Integral Nonlinearity Error (INL)**
It refers to the deviation of each individual code from a line drawn from negative full scale through positive full scale. The point used as negative full scale occurs 1/2 LSB before the first code transition. Positive full scale is defined as a level 1 1/2 LSB beyond the last code transition. The deviation is measured from the middle of each code to the true straight line (Figure 25).

**Differential Nonlinearity Error (DNL)**
In an ideal ADC, code transitions are 1 LSB apart. DNL is the maximum deviation from this ideal value. It is often specified in terms of resolution for which no missing codes are guaranteed.

**Offset Error**
The first transition should occur at a level 1/2 LSB above analog ground (38.1 µV for the 0 V to 5 V range). The offset error is the deviation of the actual transition from that point.

**Gain Error**
The last transition (from 111 . . . 10 to 111 . . . 11) should occur for an analog voltage 1 1/2 LSB below the nominal full scale (4.999886 V for the 0 V to 5 V range). The gain error is the deviation of the actual level of the last transition from the ideal level after the offset has been adjusted out.

**Spurious-Free Dynamic Range (SFDR)**
The difference, in decibels (dB), between the rms amplitude of the input signal and the peak spurious signal.

**Effective Number of Bits (ENOB)**
ENOB is a measurement of the resolution with a sine wave input. It is related to S/(N+D) by the following formula

$$ENOB = (S/[N+D]_{dB} - 1.76)/6.02)$$

and is expressed in bits.

**Total Harmonic Distortion (THD)**
THD is the ratio of the rms sum of the first five harmonic components to the rms value of a full-scale input signal and is expressed in dB.

**Signal-to-Noise Ratio (SNR)**
SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in dB.

**Signal-to-(Noise + Distortion) Ratio (S/[N+D])**
S/(N+D) is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for S/(N+D) is expressed in dB.

**Aperture Delay**
Aperture delay is a measure of the acquisition performance and is the time between the rising edge of the CNV input and when the input signal is held for a conversion.

**Transient Response**
The time required for the ADC to accurately acquire its input after a full-scale step function was applied.

# TYPICAL PERFORMANCE CHARACTERISTICS

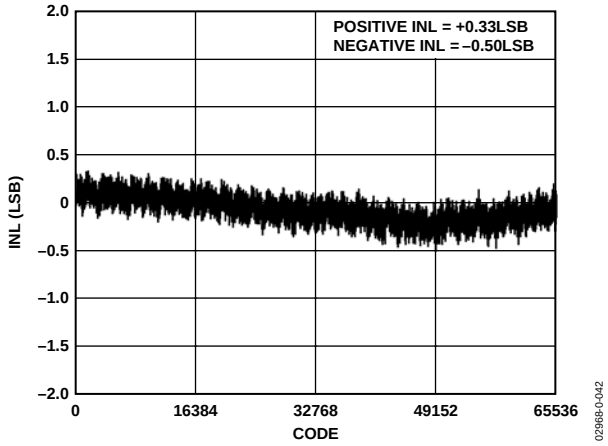


Figure 6. Integral Nonlinearity vs. Code

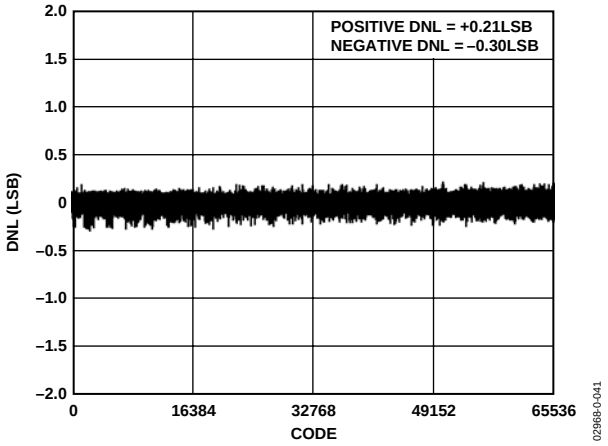


Figure 9. Differential Nonlinearity vs. Code

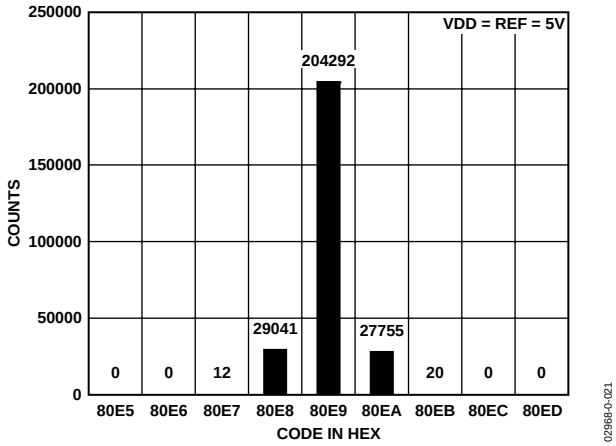


Figure 7. Histogram of a DC Input at the Code Center

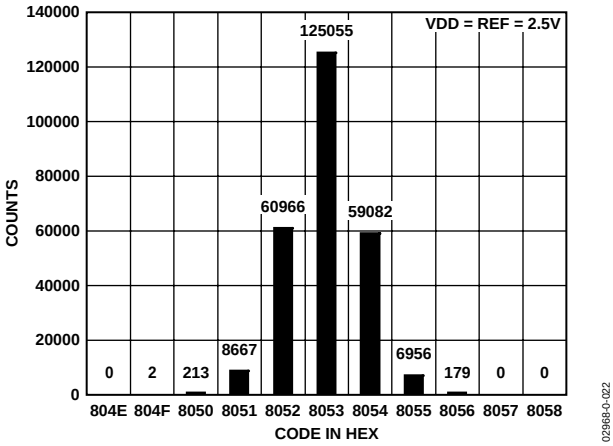


Figure 10. Histogram of a DC Input at the Code Center

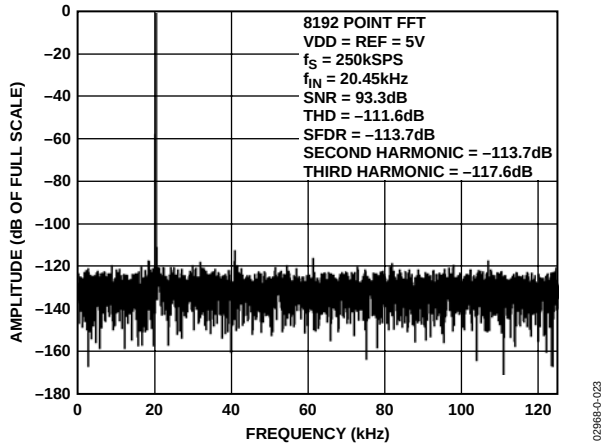


Figure 8. FFT Plot

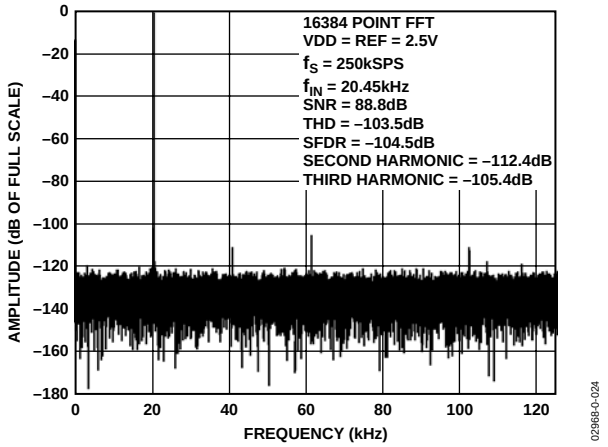


Figure 11. FFT Plot

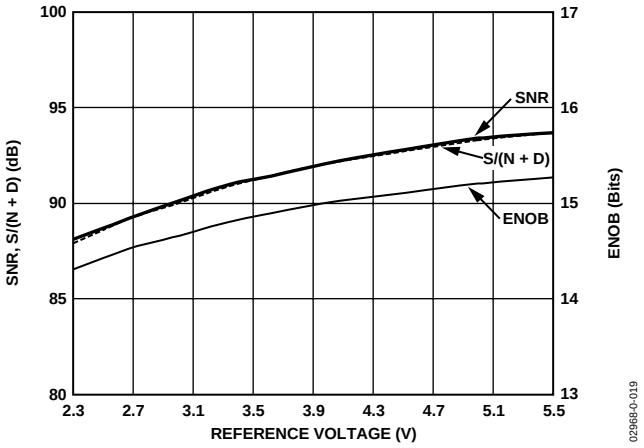


*Figure 12. SNR, S/(N + D), and ENOB vs. Reference Voltage*

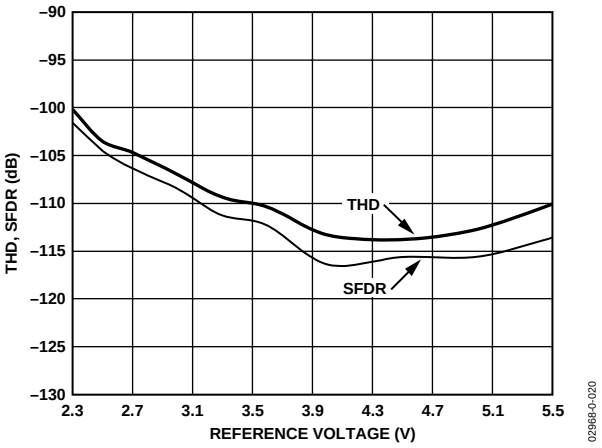


*Figure 15. THD, SFDR vs. Reference Voltage*

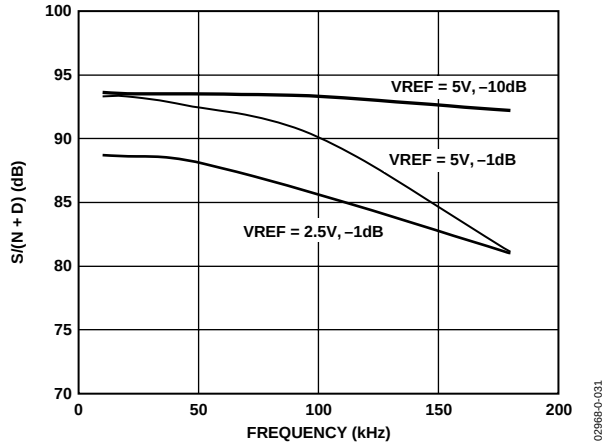


*Figure 13. S/[N + D] vs. Frequency*

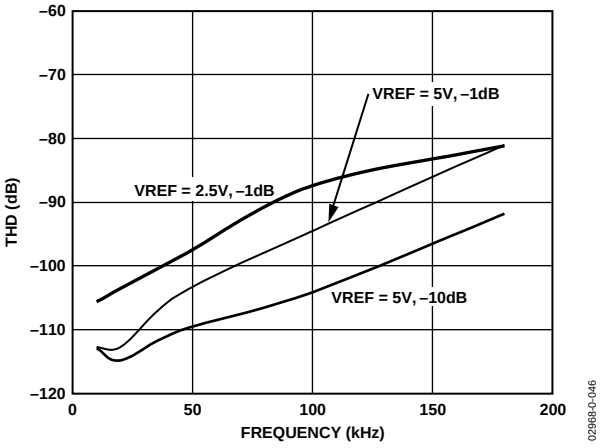


*Figure 16. THD vs. Frequency*

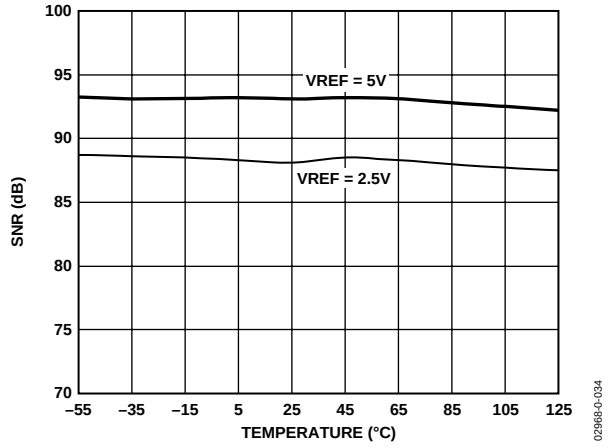


*Figure 14. SNR vs. Temperature*

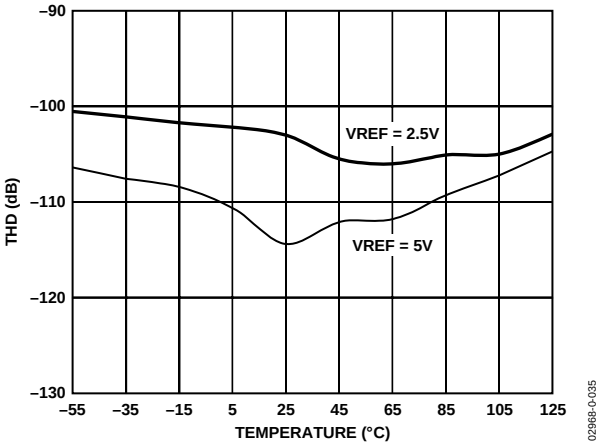


*Figure 17. THD, SFDR vs. Temperature*

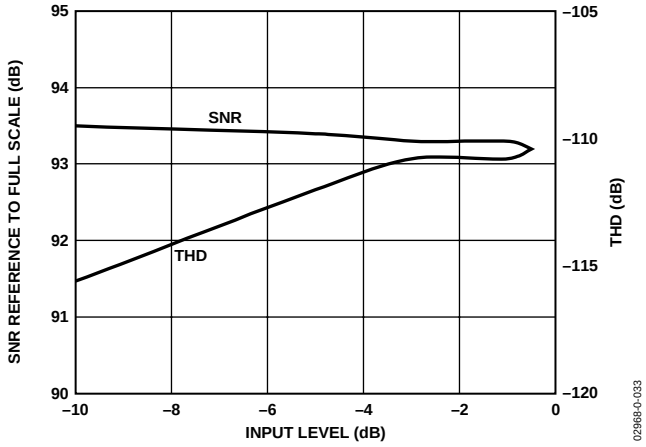


Figure 18. SNR and THD vs. Input Level

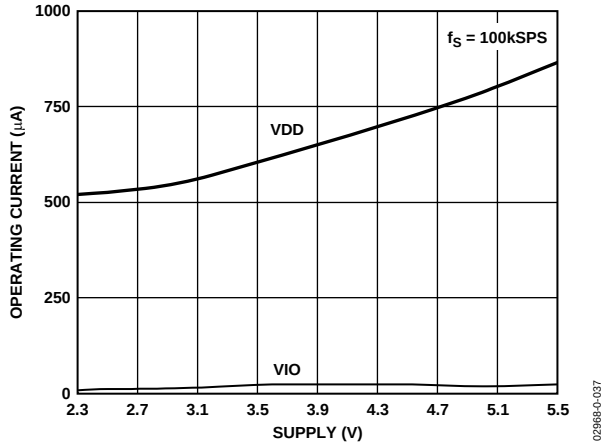


Figure 19. Operating Currents vs. Supply

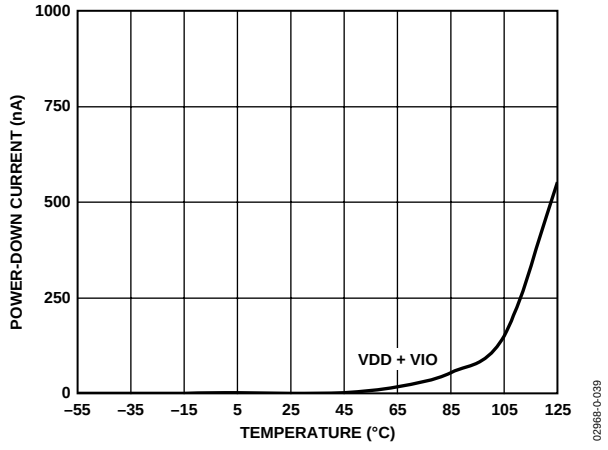


Figure 20. Power-Down Currents vs. Temperature

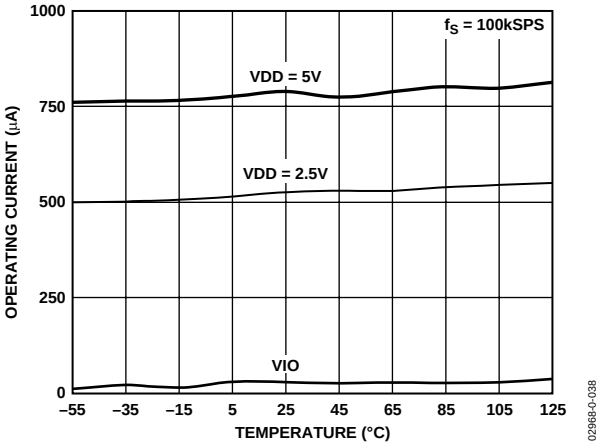


Figure 21. Operating Currents vs. Temperature

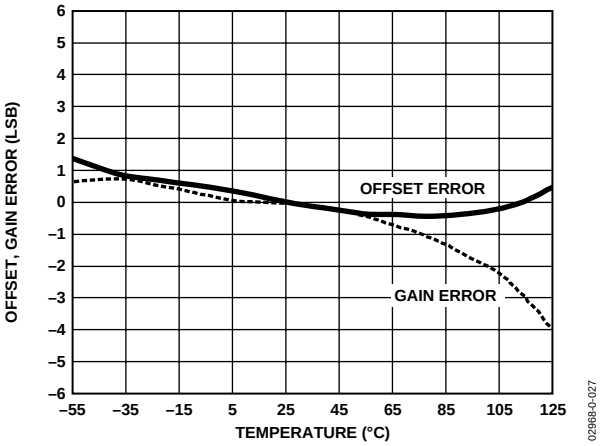


Figure 22. Offset and Gain Error vs. Temperature

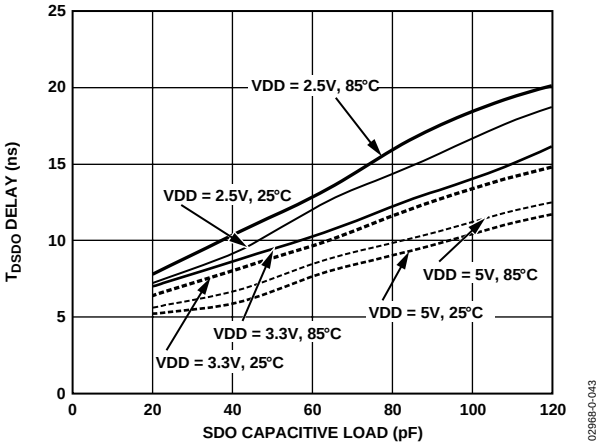


Figure 23. $t_{DSDO}$ vs. Capacitance Load and Supply

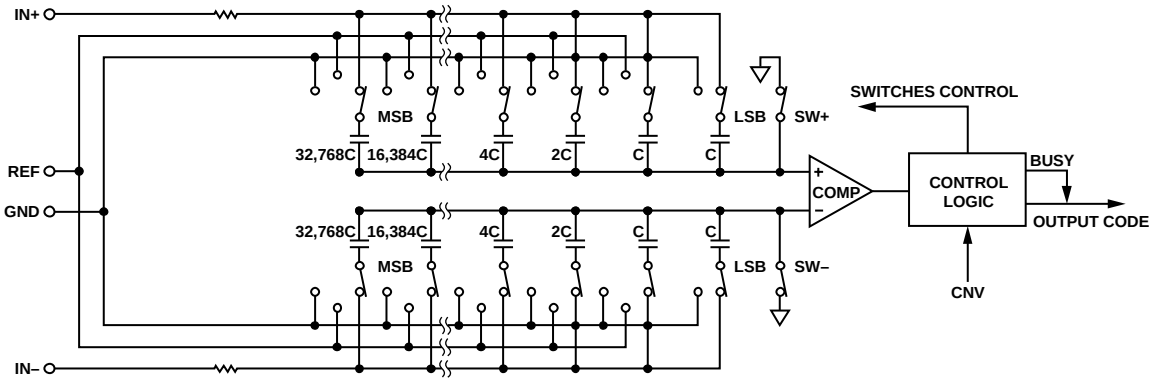


*Figure 24. ADC Simplified Schematic*

## CIRCUIT INFORMATION

The AD7685 is a fast, low power, single-supply, precise 16-bit ADC using a successive approximation architecture.

The AD7685 is capable of converting 250,000 samples per second (250 kSPS) and powers down between conversions. When operating at 100 SPS, for example, it consumes typically 1.35 µW with a 2.5 V supply, ideal for battery-powered applications.

The AD7685 provides the user with an on-chip track-and-hold and does not exhibit any pipeline delay or latency, making it ideal for multiple multiplexed channel applications.

The AD7685 is specified from 2.3 V to 5.5 V and can be interfaced to any 1.8 V to 5 V digital logic family. It is housed in a 10-lead MSOP or a tiny 10-lead QFN (LFCSP) that combines space savings and allows flexible configurations.

It is pin-for-pin-compatible with the AD7686, AD7687, and AD7688.

## CONVERTER OPERATION

The AD7685 is a successive approximation ADC based on a charge redistribution DAC. Figure 24 shows the simplified schematic of the ADC. The capacitive DAC consists of two identical arrays of 16 binary weighted capacitors, which are connected to the two comparator inputs.

During the acquisition phase, terminals of the array tied to the comparator's input are connected to GND via SW+ and SW–. All independent switches are connected to the analog inputs. Thus, the capacitor arrays are used as sampling capacitors and acquire the analog signal on the IN+ and IN– inputs. When the acquisition phase is complete and the CNV input goes high, a conversion phase is initiated. When the conversion phase begins, SW+ and SW– are opened first. The two capacitor arrays are then disconnected from the inputs and connected to the GND input. Therefore, the differential voltage between the inputs IN+ and IN– captured at the end of the acquisition phase is applied to the comparator inputs, causing the comparator to become unbalanced. By switching each element of the capacitor array between GND and REF, the comparator input varies by binary weighted voltage steps ($V_{REF}/2$, $V_{REF}/4$ . . . $V_{REF}/65536$). The control logic toggles these switches, starting with the MSB, in order to bring the comparator back into a balanced condition. After the completion of this process, the part powers down and returns to the acquisition phase and the control logic generates the ADC output code and a BUSY signal indicator.

Because the AD7685 has an on-board conversion clock, the serial clock, SCK, is not required for the conversion process.

### *Transfer Functions*

The ideal transfer characteristic for the AD7685 is shown in Figure 25 and Table 8.

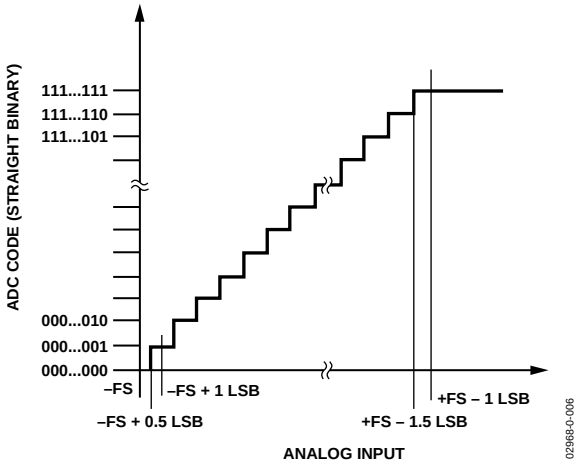


*Figure 25. ADC Ideal Transfer Function*

**Table 8. Output Codes and Ideal Input Voltages**

| Description | Analog Input $V_{REF}$ = 5 V | Digital Output Code Hexa |
|---|---|---|
| FSR – 1 LSB | 4.999924 V | FFFF[1] |
| Midscale + 1 LSB | 2.500076 V | 8001 |
| Midscale | 2.5 V | 8000 |
| Midscale – 1 LSB | 2.499924 V | 7FFF |
| –FSR + 1 LSB | 76.3 µV | 0001 |
| –FSR | 0 V | 0000[2] |

[1] This is also the code for an overranged analog input ($V_{IN+} – V_{IN}$ above $V_{REF} – V_{GND}$).
[2] This is also the code for an underranged analog input ($V_{IN+} – V_{IN}$ below $V_{GND}$).

## TYPICAL CONNECTION DIAGRAM

Figure 26 shows an example of the recommended connection diagram for the AD7685 when multiple supplies are available.

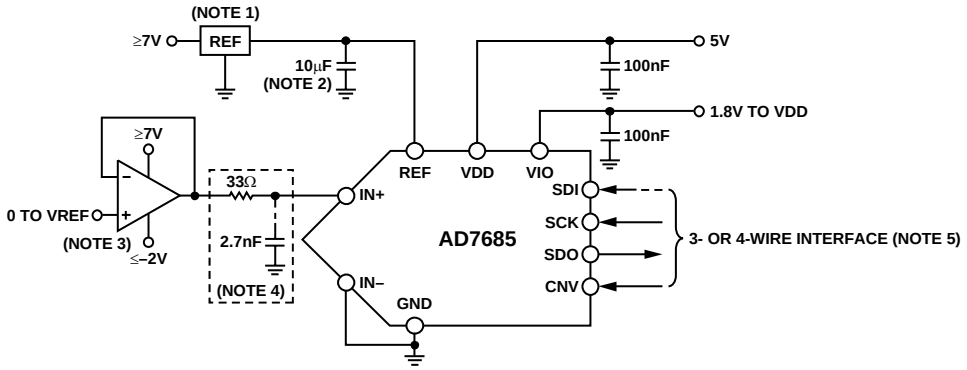


*Figure 26. Typical Application Diagram with Multiple Supplies*

### *Analog Input*

Figure 27 shows an equivalent circuit of the input structure of the AD7685.

The two diodes, D1 and D2, provide ESD protection for the analog inputs IN+ and IN−. Care must be taken to ensure that the analog input signal never exceeds the supply rails by more than 0.3 V because this will cause these diodes to begin to forward-bias and start conducting current. These diodes can handle a forward-biased current of 130 mA maximum. For instance, these conditions could eventually occur when the input buffer's (U1) supplies are different from VDD. In such a case, an input buffer with a short-circuit current limitation can be used to protect the part.

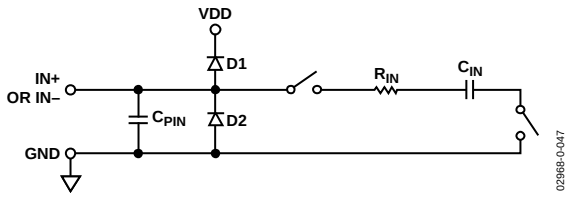


*Figure 27. Equivalent Analog Input Circuit*

This analog input structure allows the sampling of the differential signal between IN+ and IN−. By using this differential input, small signals common to both inputs are rejected, as shown in Figure 28, which represents the typical CMRR over frequency. For instance, by using IN− to sense a remote signal ground, ground potential differences between the sensor and the local ADC ground are eliminated.

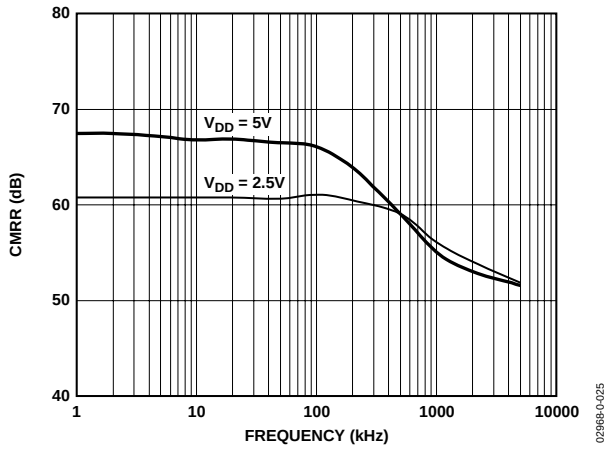


*Figure 28. Analog Input CMRR vs. Frequency*

During the acquisition phase, the impedance of the analog inputs (IN+ or IN−) can be modeled as a parallel combination of capacitor $C_{PIN}$ and the network formed by the series connection of $R_{IN}$ and $C_{IN}$. $C_{PIN}$ is primarily the pin capacitance. $R_{IN}$ is typically 3 kΩ and is a lumped component made up of some serial resistors and the on resistance of the switches. $C_{IN}$ is typically 30 pF and is mainly the ADC sampling capacitor. During the conversion phase, where the switches are opened, the input impedance is limited to $C_{PIN}$. $R_{IN}$ and $C_{IN}$ make a 1-pole, low-pass filter that reduces undesirable aliasing effects and limits the noise.

When the source impedance of the driving circuit is low, the AD7685 can be driven directly. Large source impedances significantly affect the ac performance, especially total harmonic distortion (THD). The dc performances are less sensitive to the input impedance. The maximum source impedance depends on the amount of THD that can be tolerated. The THD degrades as a function of the source impedance and the maximum input frequency, as shown in Figure 29.

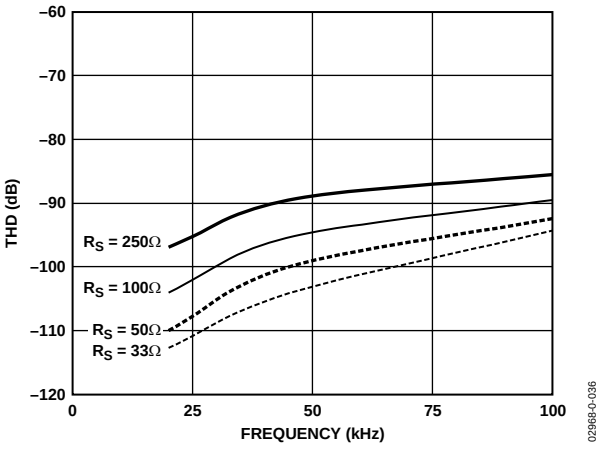


*Figure 29. THD vs. Analog Input Frequency and Source Resistance*

### *Driver Amplifier Choice*

Although the AD7685 is easy to drive, the driver amplifier needs to meet the following requirements:

- The noise generated by the driver amplifier needs to be kept as low as possible in order to preserve the SNR and transition noise performance of the AD7685. Note that the AD7685 has a noise much lower than most of the other 16-bit ADCs and, therefore, can be driven by a noisier amplifier in order to meet a given system noise specification. The noise coming from the amplifier is filtered by the AD7685 analog input circuit low-pass filter made by $R_{IN}$ and $C_{IN}$ or by an external filter, if one is used. Because the typical noise of the AD7685 is 35 µV rms, the SNR degradation due to the amplifier is

$$SNR_{LOSS} = 20\log\left(\frac{35}{\sqrt{35^2 + \frac{\pi}{2} f_{-3dB} (Ne_N)^2}}\right)$$

  where:
  $f_{-3dB}$ is the input bandwidth in MHz of the AD7685 (2 MHz) or the cutoff frequency of the input filter, if one is used.

  $N$ is the noise gain of the amplifier (e.g., +1 in buffer configuration).

  $e_N$ is the equivalent input noise voltage of the op amp, in nV/√Hz.

- For ac applications, the driver should have a THD performance commensurate with the AD7685. Figure 16 shows the AD7685's THD versus frequency.

- For multichannel, multiplexed applications, the driver amplifier and the AD7685 analog input circuit must settle a full-scale step onto the capacitor array at a 16-bit level (0.0015%). In the amplifier's data sheet, settling at 0.1% to 0.01% is more commonly specified. This could differ significantly from the settling time at a 16-bit level and should be verified prior to driver selection.

**Table 9. Recommended Driver Amplifiers.**

| Amplifier | Typical Application |
|---|---|
| AD8021 | Very low noise and high frequency |
| AD8022 | Low noise and high frequency |
| OP184 | Low power, low noise, and low frequency |
| AD8605, AD8615 | 5 V single-supply, low power |
| AD8519 | Small, low power and low frequency |
| AD8031 | High frequency and low power |

### *Voltage Reference Input*

The AD7685 voltage reference input, REF, has a dynamic input impedance and should therefore be driven by a low impedance source with efficient decoupling between the REF and GND pins as explained in the Layout section.

When REF is driven by a very low impedance source, e.g., a reference buffer using the AD8031 or the AD8605, a 10 µF (X5R, 0805 size) ceramic chip capacitor is appropriate for optimum performance.

If an unbuffered reference voltage is used, the decoupling value depends on the reference used. For instance, a 22 µF (X5R, 1206 size) ceramic chip capacitor is appropriate for optimum performance using a low temperature drift ADR43x reference.

If desired, smaller reference decoupling capacitor values down to 2.2 µF can be used with a minimal impact on performance, especially DNL.

### Power Supply

The AD7685 is specified over a wide operating range from 2.3 V to 5.5 V. It has, unlike other low voltage converters, a noise low enough to design a 16-bit resolution system with respectable performance. It uses two power supply pins: a core supply VDD and a digital input/output interface supply VIO. VIO allows direct interface with any logic between 1.8 V and VDD. To reduce the number of supplies needed, the VIO and VDD can be tied together. The AD7685 is independent of power supply sequencing between VIO and VDD. Additionally, it is very insensitive to power supply variations over a wide frequency range, as shown in Figure 30, which represents PSRR over frequency.

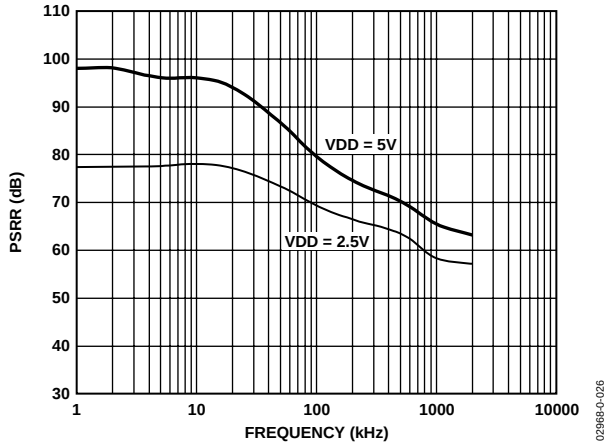


*Figure 30. PSRR vs. Frequency*

The AD7685 powers down automatically at the end of each conversion phase and, therefore, the power scales linearly with the sampling rate as shown in see Figure 31. This makes the part ideal for low sampling rate (even a few Hz) and low battery-powered applications.

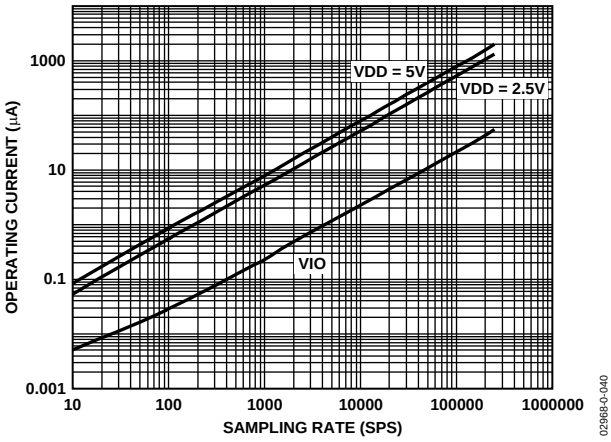


*Figure 31. Operating Currents vs. Sampling Rate*

### Supplying the ADC from the Reference

For simplified applications, the AD7685, with its low operating current, can be supplied directly using the reference circuit, as shown in Figure 32. The reference line can be driven by either:

- The system power supply directly
- A reference voltage with enough current output capability, such as the ADR43x
- A reference buffer, such as the AD8031, that can also filter the system power supply, as shown in Figure 32.

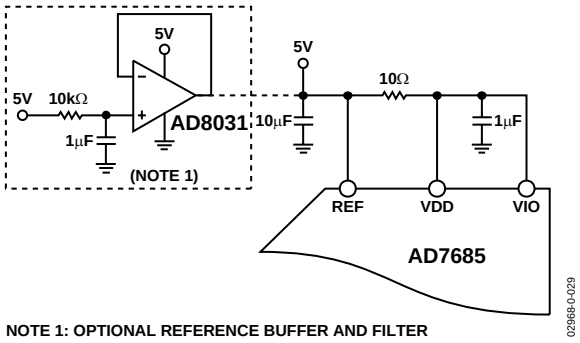


*Figure 32. Example of Application Circuit*

## DIGITAL INTERFACE

Though the AD7685 has a reduced number of pins, it offers substantial flexibility in its serial interface modes.

The AD7685, when in $\overline{CS}$ mode, is compatible with SPI, QSPI, digital hosts, and DSPs, e.g., Blackfin® ADSP-BF53x or ADSP-219x). This interface can use either 3-wire or 4-wire. A 3-wire interface using the CNV, SCK, and SDO signals minimizes wiring connections, useful, for instance, in isolated applications. A 4-wire interface using the SDI, CNV, SCK, and SDO signals allows CNV, which initiates the conversions, to be independent of the readback timing (SDI). This is useful in low jitter sampling or simultaneous sampling applications.

The AD7685, when in chain mode, provides a daisy chain feature using the SDI input for cascading multiple ADCs on a single data line similar to a shift register.

The mode in which the part operates depends on the SDI level when the CNV rising edge occurs. The $\overline{CS}$ mode is selected if SDI is high and the chain mode is selected if SDI is low. The SDI hold time is such that when SDI and CNV are connected together, the chain mode is always selected.

In the $\overline{CS}$ mode, the AD7685 offers the flexibility to optionally force a start bit in front of the data bits. This start bit can be used as a BUSY signal indicator to interrupt the digital host and trigger the data reading. Otherwise, without a BUSY indicator, the user must time out the maximum conversion time prior to readback.

The BUSY indicator feature is enabled as follows:

- In the $\overline{CS}$ mode, if CNV or SDI is low when the ADC conversion ends (Figure 36).

### $\overline{CS}$ Mode 3-Wire, No BUSY Indicator

This mode is usually used when a single AD7685 is connected to an SPI compatible digital host. The connection diagram is shown in Figure 33 and the corresponding timing is given in Figure 34.

With SDI tied to VIO, a rising edge on CNV initiates a conversion, selects the $\overline{CS}$ mode, and forces SDO to high impedance. Once a conversion is initiated, it will continue to completion irrespective of the state of CNV. For instance, it could be useful to bring CNV low to select other SPI devices, such as analog multiplexers, but CNV must be returned high before the minimum conversion time and held high until the maximum conversion time to avoid the generation of the BUSY signal indicator. When the conversion is complete, the AD7685 enters the acquisition phase and powers down. When CNV goes low, the MSB is output onto SDO. The remaining data bits are then clocked by subsequent SCK falling edges. The data is valid on both SCK edges. Although the rising edge can be used to capture the data, a digital host using the SCK falling edge will allow a faster reading rate provided it has an acceptable hold time. After the 16th SCK falling edge or when CNV goes high, whichever is earlier, SDO returns to high impedance.

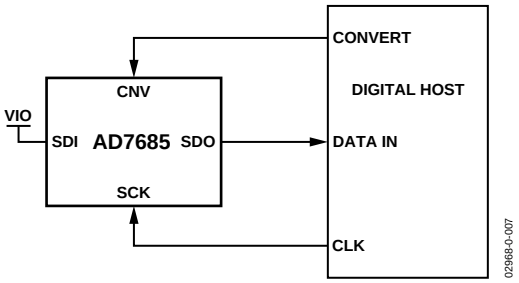


*Figure 33. $\overline{CS}$ Mode 3-Wire, No BUSY Indicator Connection Diagram (SDI High)*

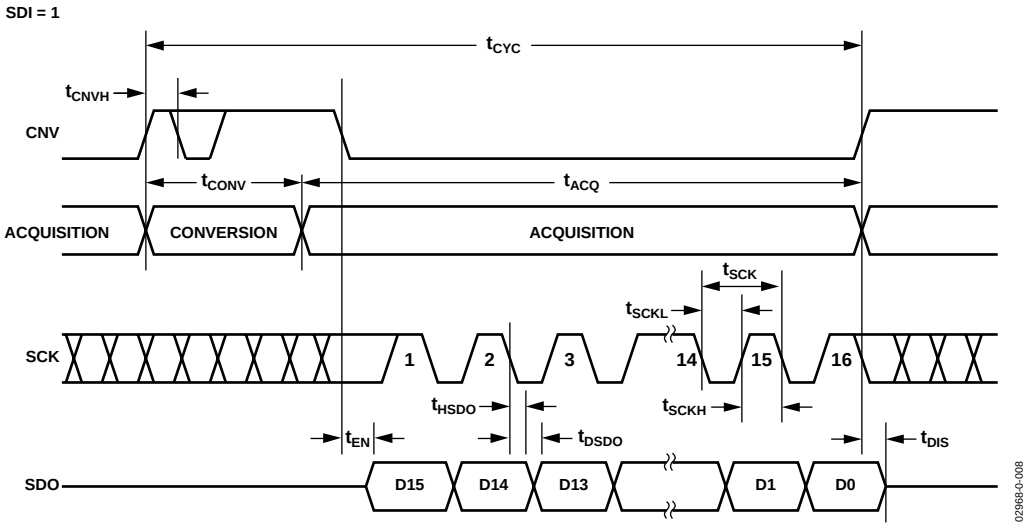


*Figure 34. $\overline{CS}$ Mode 3-Wire, No BUSY Indicator Serial Interface Timing (SDI High)*

### $\overline{CS}$ Mode 3-Wire with BUSY Indicator

This mode is usually used when a single AD7685 is connected to an SPI compatible digital host having an interrupt input.

The connection diagram is shown in Figure 35 and the corresponding timing is given in Figure 36.

With SDI tied to VIO, a rising edge on CNV initiates a conversion, selects the $\overline{CS}$ mode, and forces SDO to high impedance. SDO is maintained in high impedance until the completion of the conversion irrespective of the state of CNV. Prior to the minimum conversion time, CNV could be used to select other SPI devices, such as analog multiplexers, but CNV must be returned low before the minimum conversion time and held low until the maximum conversion time to guarantee the generation of the BUSY signal indicator. When the conversion is complete, SDO goes from high impedance to low. With a pull-up on the SDO line, this transition can be used as an interrupt signal to initiate the data reading controlled by the digital host. The AD7685 then enters the acquisition phase and powers down. The data bits are then clocked out, MSB first, by subsequent SCK falling edges. The data is valid on both SCK edges. Although the rising edge can be used to capture the data, a digital host using the SCK falling edge will allow a faster reading rate provided it has an acceptable hold time. After the optional 17th SCK falling edge, or when CNV goes high, whichever is earlier, SDO returns to high impedance.

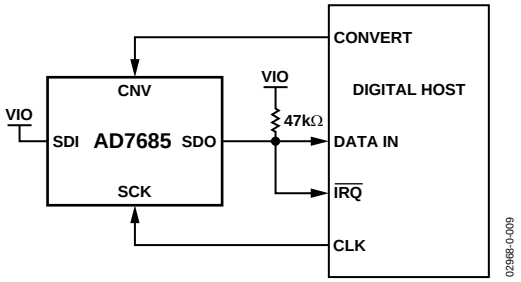


*Figure 35. $\overline{CS}$ Mode 3-Wire with BUSY Indicator Connection Diagram (SDI High)*

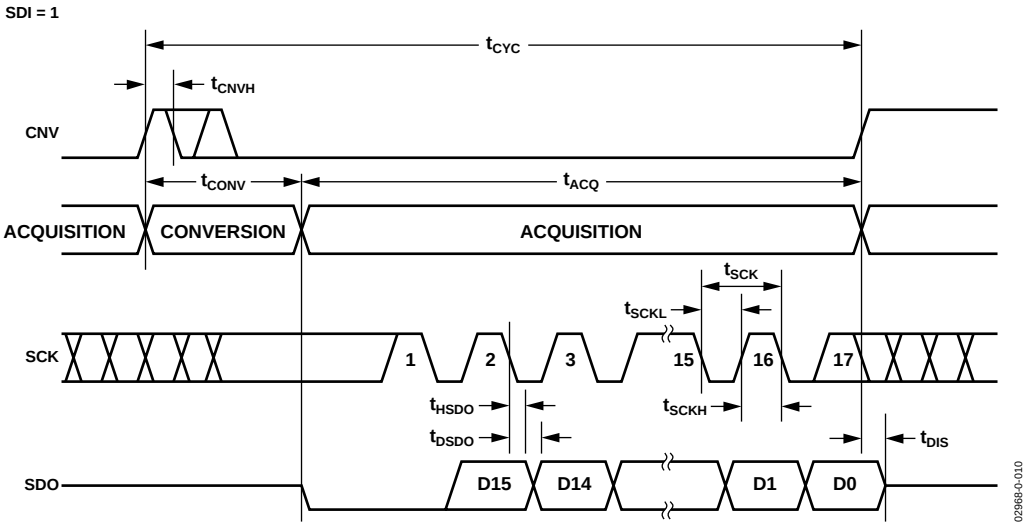


*Figure 36. $\overline{CS}$ Mode 3-Wire with BUSY Indicator Serial Interface Timing (SDI High)*

### $\overline{CS}$ Mode 4-Wire, No BUSY Indicator

This mode is usually used when multiple AD7685s are connected to an SPI compatible digital host.

A connection diagram example using two AD7685s is shown in Figure 37 and the corresponding timing is given in Figure 38.

With SDI high, a rising edge on CNV initiates a conversion, selects the $\overline{CS}$ mode, and forces SDO to high impedance. In this mode, CNV must be held high during the conversion phase and the subsequent data readback (if SDI and CNV are low, SDO is driven low). Prior to the minimum conversion time, SDI could be used to select other SPI devices, such as analog multiplexers, but SDI must be returned high before the minimum conversion time and held high until the maximum conversion time to avoid the generation of the BUSY signal indicator. When the conversion is complete, the AD7685 enters the acquisition phase and powers down. Each ADC result can be read by bringing low its SDI input which consequently outputs the MSB onto SDO. The remaining data bits are then clocked by subsequent SCK driving edges. The data is valid on both SCK edges. Although the rising edge can be used to capture the data, a digital host using the SCK falling edge will allow a faster reading rate provided it has an acceptable hold time. After the 16th SCK falling edge, or when SDI goes high, whichever is earlier, SDO returns to high impedance and another AD7685 can be read.

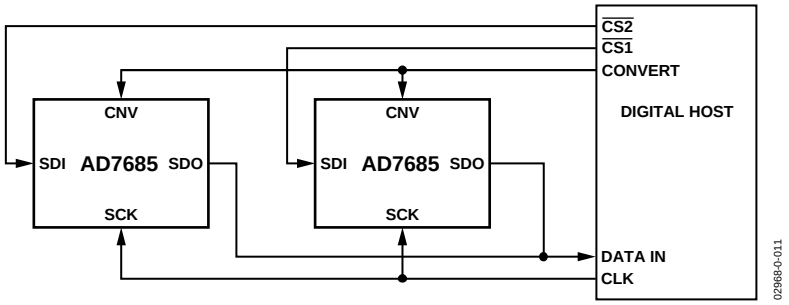


*Figure 37. $\overline{CS}$ Mode 4-Wire, No BUSY Indicator Connection Diagram*

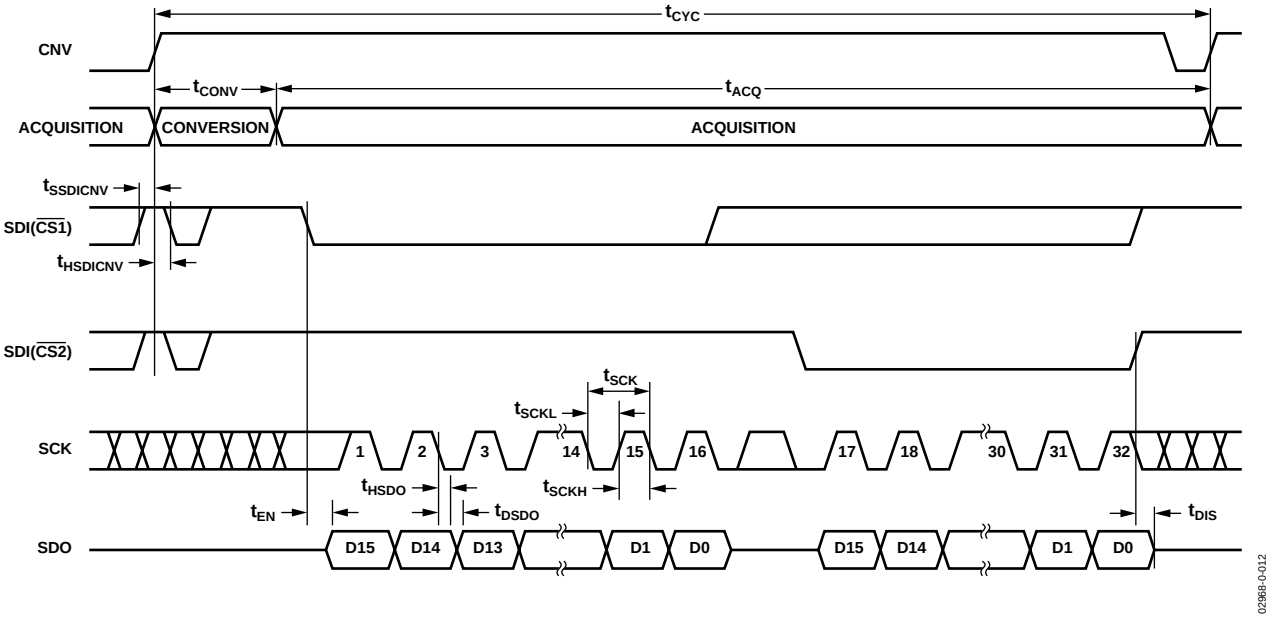


*Figure 38. $\overline{CS}$ Mode 4-Wire, No BUSY Indicator Serial Interface Timing*

### $\overline{CS}$ Mode 4-Wire with BUSY Indicator

This mode is usually used when a single AD7685 is connected to an SPI compatible digital host, which has an interrupt input, and it is desired to keep CNV, which is used to sample the analog input, independent of the signal used to select the data reading. This requirement is particularly important in applications where low jitter on CNV is desired.

The connection diagram is shown in Figure 39 and the corresponding timing is given in Figure 40.

With SDI high, a rising edge on CNV initiates a conversion, selects the $\overline{CS}$ mode, and forces SDO to high impedance. In this mode, CNV must be held high during the conversion phase and the subsequent data readback (if SDI and CNV are low, SDO is driven low). Prior to the minimum conversion time, SDI could be used to select other SPI devices, such as analog multiplexers, but SDI must be returned low before the minimum conversion time and held low until the maximum conversion time to guarantee the generation of the BUSY signal indicator. When the conversion is complete, SDO goes from high impedance to low. With a pull-up on the SDO line, this transition can be used as an interrupt signal to initiate the data readback controlled by the digital host. The AD7685 then enters the acquisition phase and powers down. The data bits are then clocked out, MSB first, by subsequent SCK driving edges. The data is valid on both SCK edges. Although the rising edge can be used to capture the data, a digital host using the SCK falling edge will allow a faster reading rate provided it has an acceptable hold time. After the optional 17th SCK falling edge, or SDI going high, whichever is earlier, the SDO returns to high impedance.

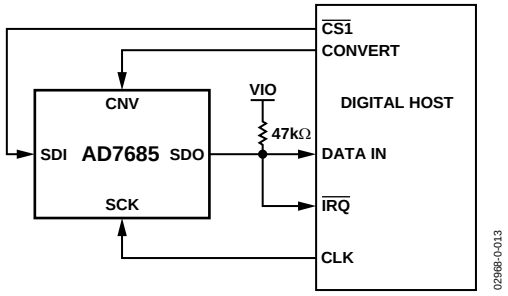


*Figure 39. $\overline{CS}$ Mode 4-Wire with BUSY Indicator Connection Diagram*

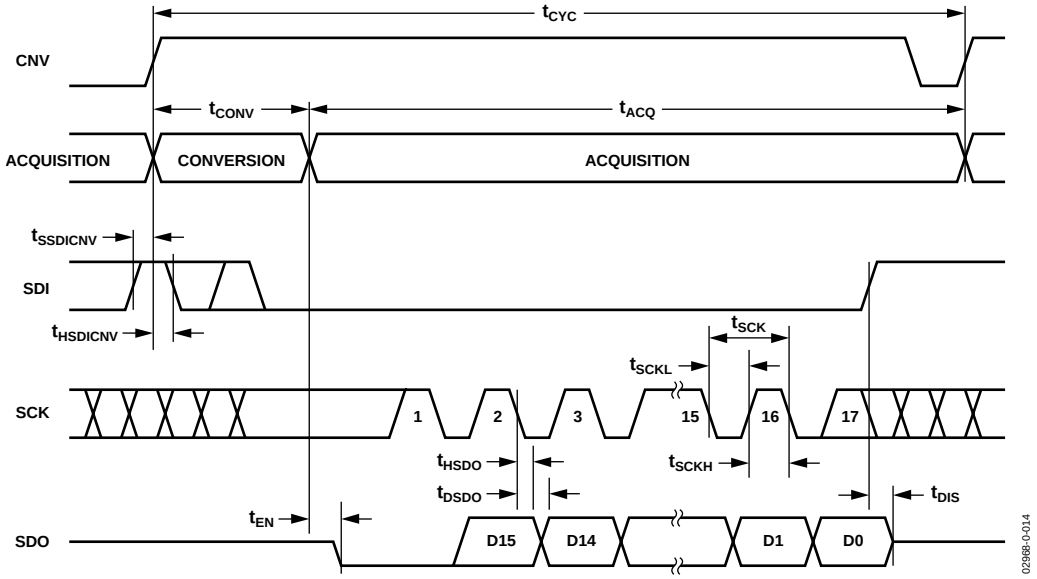


*Figure 40. $\overline{CS}$ Mode 4-Wire with BUSY Indicator Serial Interface Timing*

### *Chain Mode*

This mode can be used to daisy chain multiple AD7685s on a 3-wire serial interface. This feature is useful for reducing component count and wiring connections, e.g., in isolated multiconverter applications or for systems with a limited interfacing capacity. Data readback is analogous to clocking a shift register.

A connection diagram example using two AD7685s is shown in Figure 41 and the corresponding timing is given in Figure 42.

When SDI and CNV are low, SDO is driven low. With SCK low, a rising edge on CNV initiates a conversion and selects the chain mode. In this mode, CNV is held high during the conversion phase and the subsequent data readback. When the conversion is complete, the MSB is output onto SDO and the AD7685 enters the acquisition phase and powers down. The remaining data bits stored in the internal shift register are then clocked by subsequent SCK falling edges. For each ADC, SDI feeds the input of the internal shift register and is clocked by the SCK falling edge. Each ADC in the chain outputs its data MSB first, and 16 × N clocks are required to readback the N ADCs. The data is valid on both SCK edges. Although the rising edge can be used to capture the data, a digital host using the SCK falling edge will allow a faster reading rate and, consequently more AD7685s in the chain, provided the digital host has an acceptable hold time. The maximum conversion rate may be reduced due to the total readback time. For instance, with a 5 ns digital host set-up time and 3 V interface, up to five AD7685s running at a conversion rate of 200 kSPS can be daisy-chained on a 3-wire port.

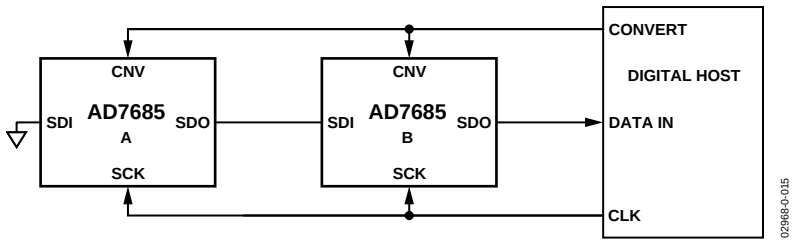


*Figure 41. Chain Mode Connection Diagram*

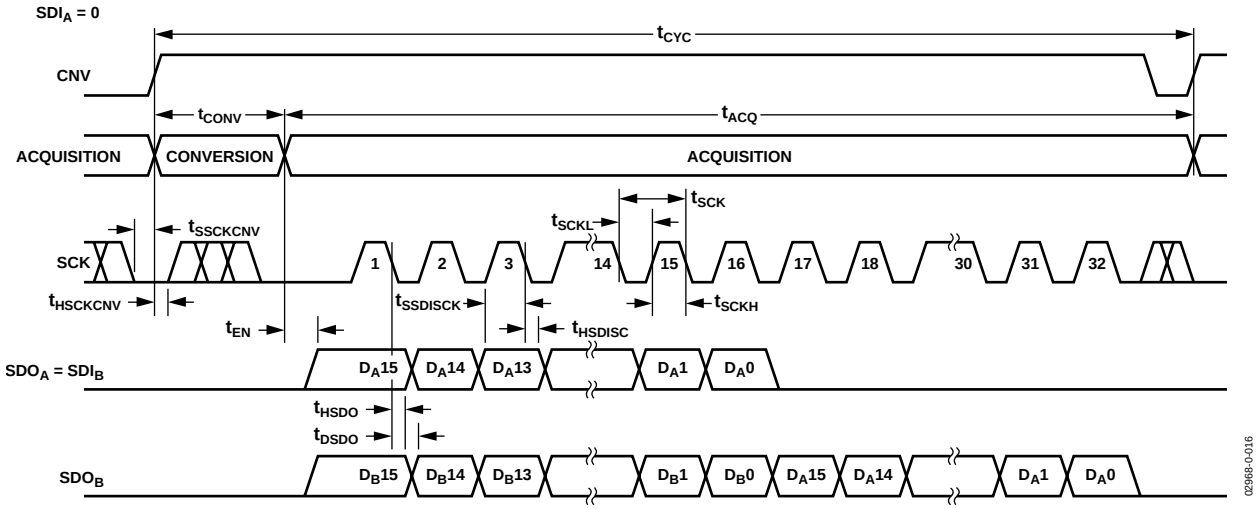


*Figure 42. Chain Mode Serial Interface Timing*

# APPLICATION HINTS

## LAYOUT

The printed circuit board that houses the AD7685 should be designed so that the analog and digital sections are separated and confined to certain areas of the board. The pinout of the AD7685 with all its analog signals on the left side and all its digital signals on the right side eases this task.

Avoid running digital lines under the device because these couple noise onto the die, unless a ground plane under the AD7685 is used as a shield. Fast switching signals, such as CNV or clocks, should never run near analog signal paths. Crossover of digital and analog signals should be avoided

At least one ground plane should be used. It could be common or split between the digital and analog section. In the latter case, the planes should be joined underneath the AD7685.

The AD7685 voltage reference input REF has a dynamic input impedance and should be decoupled with minimal parasitic inductances. This is done by placing the reference decoupling ceramic capacitor close to, and ideally right up against, the REF and GND pins and connected with wide, low impedance traces.

Finally, the power supplies VDD and VIO should be decoupled with ceramic capacitors, typically 100 nF, placed close to the AD7685 and connected using short and wide traces to provide low impedance paths and reduce the effect of glitches on the power supply lines.

An example layout following these rules is shown in Figure 43 and Figure 44.

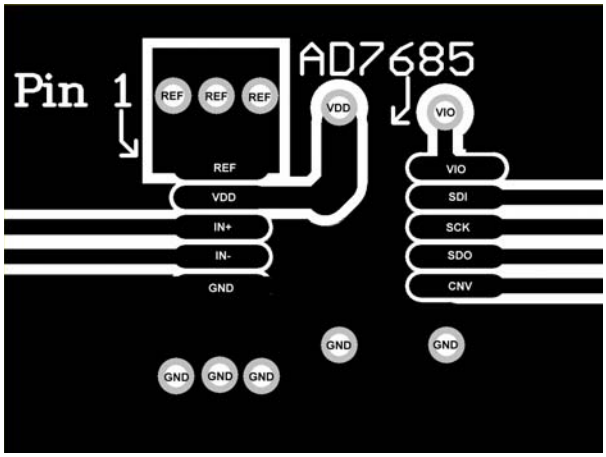


*Figure 43. Example of Layout of the AD7685 (Top Layer)*

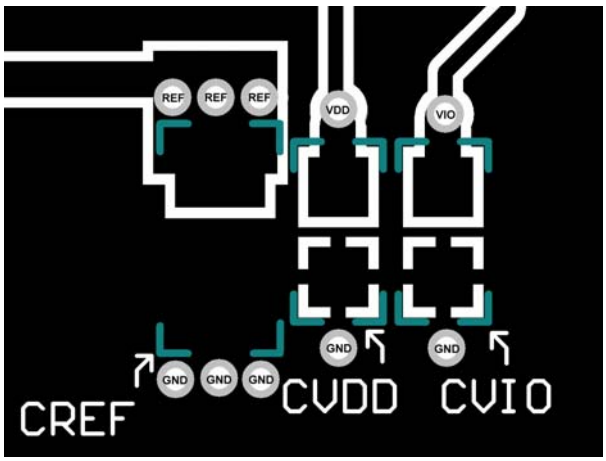


*Figure 44. Example of Layout of the AD7685 (Bottom Layer)*

## EVALUATING THE AD7685'S PERFORMANCE

Other recommended layouts for the AD7685 are outlined in the documentation of the evaluation board for the AD7685 (EVAL-AD7685). The evaluation board package includes a fully assembled and tested evaluation board, documentation, and software for controlling the board from a PC via the EVAL-CONTROL BRD2.

# OUTLINE DIMENSIONS

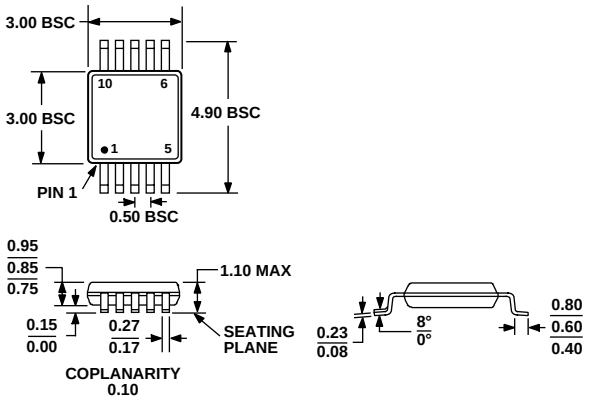


*Figure 45.10-Lead Micro Small Outline Package [MSOP]*
*(RM-10)*
*Dimensions shown in millimeters*

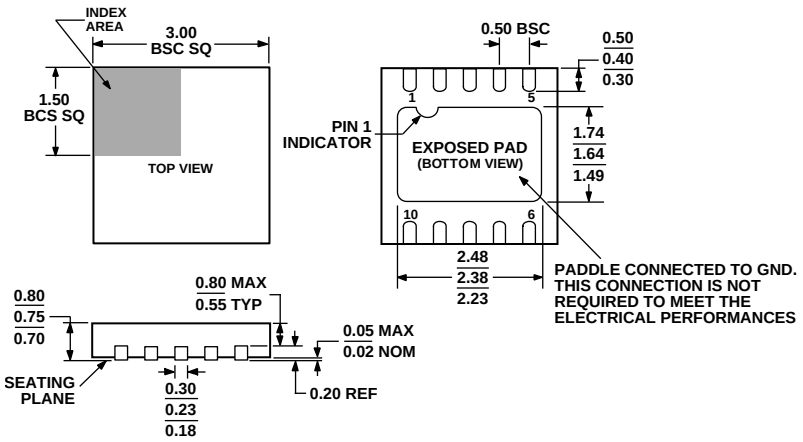


*Figure 46. 10-Terminal Quad Flat No Lead Package[QFN (LFCSP)]*
*3 mm × 3 mm Body*
*(CP-10-9)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Models | Integral Nonlinearity | Temperature Range | Package (Option) | Transport Media, Quantity | Branding |
|---|---|---|---|---|---|
| AD7685BRM | ±3 LSB max | –40°C to +85°C | MSOP (RM-10) | Tube, 50 | C01 |
| AD7685BRMRL7 | ±3 LSB max | –40°C to +85°C | MSOP (RM-10) | Reel, 1,000 | C01 |
| EVAL-AD7685CB[1] | | | Evaluation Board | | |
| EVAL-CONTROL BRD2[2] | | | Controller Board | | |
| EVAL-CONTROL BRD3[2] | | | Controller Board | | |

[1] This board can be used as a standalone evaluation board or in conjunction with the EVAL-CONTROL BRDx for evaluation/demonstration purposes.
[2] These boards allow a PC to control and communicate with all Analog Devices evaluation boards ending in the CB designators.

## NOTES

# NOTES


D02968–0–4/04(0)