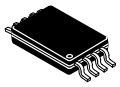
ASM3P622S00B, ASM3P622S00E

Product Preview

Low Frequency TIMING SAFE™ Peak EMI Reduction IC

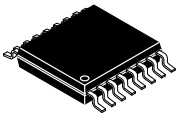
ON Semiconductor®

http://onsemi.com

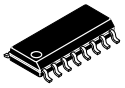


TSSOP−8
T SUFFIX
CASE 948AL

SOIC−8
S SUFFIX
CASE 751BD



TSSOP−16
T SUFFIX
CASE 948AN



SOIC−16
S SUFFIX
CASE 751BG

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 12 of this data sheet.

Description

ASM3P622S00B/E is a versatile, 3.3 V Zero−delay buffer designed to distribute low frequency Timing−Safe clocks with Peak EMI reduction. ASM3P622S00B is an eight−pin version, accepts one reference input and drives out one low−skew Timing−Safe clock. ASM3P622S00E accepts one reference input and drives out eight low−skew Timing−Safe clocks.

ASM3P622S00B/E has an SS% that selects 2 different Deviation and associated Input−Output Skew (TSKEW). Refer to *Spread Spectrum Control* and *Input−Output Skew* table for details.

ASM3P622S00E has a CLKOUT for adjusting the Input−Output clock delay, depending upon the value of capacitor connected at this pin to GND.

ASM3P622S00B/E operates from a 3.3 V supply and is available in two different packages, as shown in the ordering information table, over commercial and Industrial temperature range.

Application

ASM3P622S00B/E is targeted for use in Displays and memory interface systems.

Features

- Low Frequency Clock Distribution with Timing−Safe Peak EMI Reduction
- Input Frequency Range: 4 MHz − 20 MHz
- 2 Different Spread Selection Options
- Spread Spectrum can be Turned ON/OFF
- External Input−Output Delay Control Option
- Supply Voltage: 3.3 V ± 0.3 V
- Commercial and Industrial Temperature Range
- Packaging Information:
  ASM3P622S00B: 8 pin SOIC, and TSSOP
  ASM3P622S00E: 16 pin SOIC, and TSSOP
- The First True Drop−in Solution
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

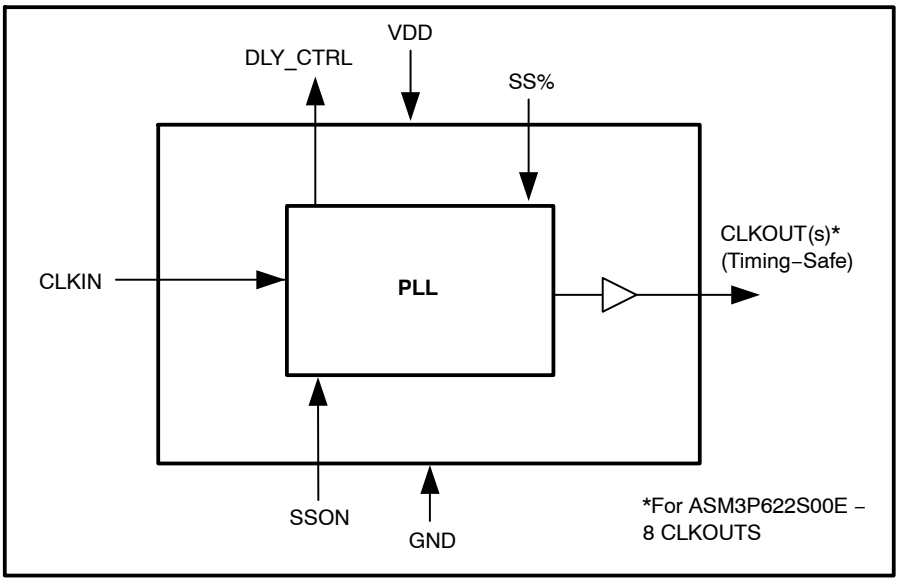


Figure 1. General Block Diagram

Spread Spectrum Frequency Generation

The clocks in digital systems are typically square waves with a 50% duty cycle and as frequencies increase the edge rates also get faster. Analysis shows that a square wave is composed of fundamental frequency and harmonics. The fundamental frequency and harmonics generate the energy peaks that become the source of EMI. Regulatory agencies test electronic equipment by measuring the amount of peak energy radiated from the equipment. In fact, the peak level allowed decreases as the frequency increases. The standard methods of reducing EMI are to use shielding, filtering, multi−layer PCBs, etc. These methods are expensive. Spread spectrum clocking reduces the peak energy by reducing the Q factor of the clock. This is done by slowly modulating the clock frequency. The ASM3P622S00B/E uses the center modulation spread spectrum technique in which the modulated output frequency varies above and below the reference frequency with a specified modulation rate. With center modulation, the average frequency is the same as the unmodulated frequency and there is no performance degradation.

Zero Delay and Skew Control

All outputs should be uniformly loaded to achieve Zero Delay between input and output. Since the CLKOUT pin is the internal feedback to the PLL, its relative loading can adjust the input−output delay.

For applications requiring zero input−output delay, all outputs, including CLKOUT, must be equally loaded. Even if CLKOUT is not used, it must have a capacitive load equal to that on other outputs, for obtaining zero input−output delay.

Timing−Safe Technology

Timing−Safe technology is the ability to modulate a clock source with Spread Spectrum technology and maintain synchronization with any associated data path.

Pin Configuration for ASM3P622S00B

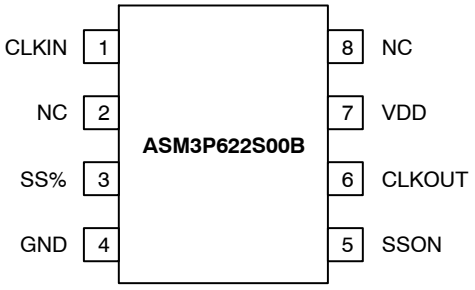


Table 1. PIN DESCRIPTION FOR ASM3P622S00B

Pin #	Pin Name	Type	Description
1	CLKIN (Note 1)	I	External reference Clock input , 5 V tolerant input
2	NC		No Connect
3	SS% (Note 3)	I	Spread Spectrum Selection. Has an internal pull up resistor
4	GND	P	Ground
5	SSON (Note 3)	I	Spread Spectrum enable and disable option. When SSON is HIGH, the spread spectrum is enabled and when LOW, it turns off the spread spectrum. Has an internal pull up resistor.
6	CLKOUT (Note 2)	O	Buffered clock output (Note 4)
7	VDD	P	3.3 V supply
8	NC		No Connect

1. Weak pull down
2. Weak pull−down on all outputs
3. Weak pull−up on these Inputs
4. Buffered clock output is Timing−Safe

Pin Configuration for ASM3P622S00E

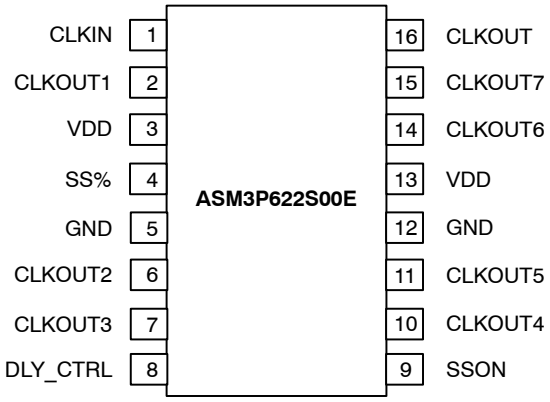


Table 2. PIN DESCRIPTION FOR ASM3P622S00E

Pin #	Pin Name	Type	Description
1	CLKIN (Note 5)	I	External reference Clock input, 5 V tolerant input
2	CLKOUT1 (Note 6)	O	Buffered clock output (Note 8)
3	V_{DD}	P	3.3 V supply
4	SS% (Note 7)	I	Spread Spectrum Selection. Refer to *Spread Spectrum Control* and *Input−Output* Skew Table. Has an internal pull up resistor.
5	GND	P	Ground
6	CLKOUT2 (Note 6)	O	Buffered clock output (Note 8)
7	CLKOUT3 (Note 6)	O	Buffered clock output (Note 8)
8	DLY_CTRL	O	External Input−Output Delay control.
9	SSON (Note 7)	I	Spread Spectrum enable and disable option. When SSON is HIGH, the spread spectrum is enabled and when LOW, it turns off the spread spectrum. Has an internal pull up resistor.
10	CLKOUT4 (Note 6)	O	Buffered clock output (Note 8)
11	CLKOUT5 (Note 6)	O	Buffered clock output (Note 8)
12	GND	P	Ground
13	V_{DD}	P	3.3 V supply
14	CLKOUT6 (Note 6)	O	Buffered clock output (Note 8)
15	CLKOUT7 (Note 6)	O	Buffered clock output (Note 8)
16	CLKOUT (Note 6)	O	Buffered clock output (Note 8)

5. Weak pull down
6. Weak pull−down on all outputs
7. Weak pull−up on these Inputs
8. Buffered clock output is Timing−Safe

Table 3. SPREAD SPECTRUM CONTROL AND INPUT−OUTPUT SKEW TABLE

Device	Input Frequency	SS %	Deviation	Input−Output Skew ($\pm T_{SKEW}$)
ASM3P622S00B/E	12 MHz	0	±0.25 %	0.0625 (Note 9)
		1	±0.50 %	0.125 (Note 9)

9. T_{SKEW} is measured in units of the Clock Period

Table 4. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating	Unit
VDD	Supply Voltage to Ground Potential	−0.5 to +4.6	V
VIN	DC Input Voltage (CLKIN)	−0.5 to +7	V
T_{STG}	Storage temperature	−65 to +125	°C
T_s	Max. Soldering Temperature (10 sec)	260	°C
T_J	Junction Temperature	150	°C
T_{DV}	Static Discharge Voltage (As per JEDEC STD22− A114−B)	2	KV

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 5. OPERATING CONDITIONS

Parameter	Description	Min	Max	Unit
VDD	Supply Voltage	3.0	3.6	V
T_A	Operating Temperature (Ambient Temperature)	−40	+85	°C
C_L	Load Capacitance		30	pF
C_{IN}	Input Capacitance		7	pF

Table 6. ELECTRICAL CHARACTERISTICS

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
V_{IL}	Input LOW Voltage (Note 10)				0.8	V
V_{IH}	Input HIGH Voltage (Note 10)		2.0			V
I_{IL}	Input LOW Current	V_{IN} = 0 V			50	μA
I_{IH}	Input HIGH Current	V_{IN} = VDD			100	μA
V_{OL}	Output LOW Voltage (Note 11)	I_{OL} = 8 mA			0.4	V
V_{OH}	Output HIGH Voltage (Note 11)	I_{OH} = −8 mA	2.4			V
I_{DD}	Supply Current	Unloaded outputs			18	mA
Z_o	Output Impedance			23		Ω

10. CLKIN input has a threshold voltage of VDD/2
11. Parameter is guaranteed by design and characterization. Not 100% tested in production

Table 7. SWITCHING CHARACTERISTICS FOR ASM3P622S00B/E

Parameter	Test Conditions		Min	Typ	Max	Unit
Input Frequency			4		20	MHz
Output Frequency	30 pF load		4		20	MHz
Duty Cycle = (t_2 / t_1) * 100 (Notes 12, 13)	Measured at VDD/2		40	50	60	%
Output Rise Time (Notes 12, 13)	Measured between 0.8 V and 2.0 V				2.5	nS
Output Fall Time (Notes 12, 13)	Measured between 2.0 V and 0.8 V				2.5	nS
Output−to−output skew (Notes 12, 13)	All outputs equally loaded with SSOFF				250	pS
Delay, CLKIN Rising Edge to CLKOUT Rising Edge (Note 13)	Measured at VDD/2 with SSOFF				±350	pS
Device−to−Device Skew (Note 13)	Measured at VDD/2 on the CLKOUT pins of the device				700	pS
Cycle−to−Cycle Jitter (Notes 12, 13)	Loaded outputs	< 8 MHz			±1.6	nS
		> 8 MHz			±200	pS
PLL Lock Time (Note 13)	Stable power supply, valid clock presented on CLKIN pin				1.0	mS

12. All parameters specified with 30 pF loaded outputs.
13. Parameter is guaranteed by design and characterization. Not 100% tested in production.

Switching Waveforms

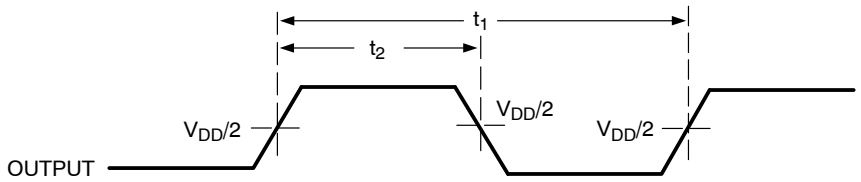


Figure 2. Duty Cycle Timing

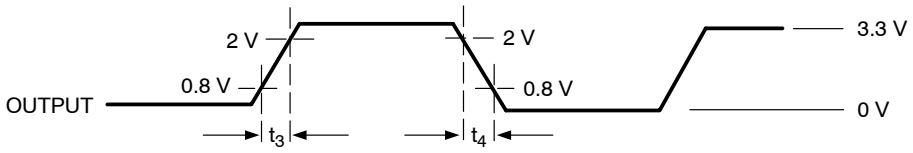


Figure 3. All Outputs Rise/Fall Time

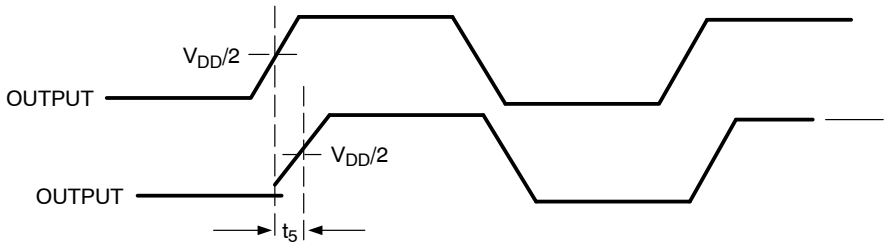


Figure 4. Output − Output Skew

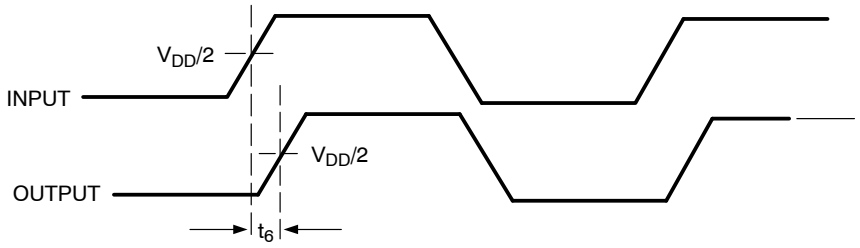


Figure 5. Input − Output Propagation Delay

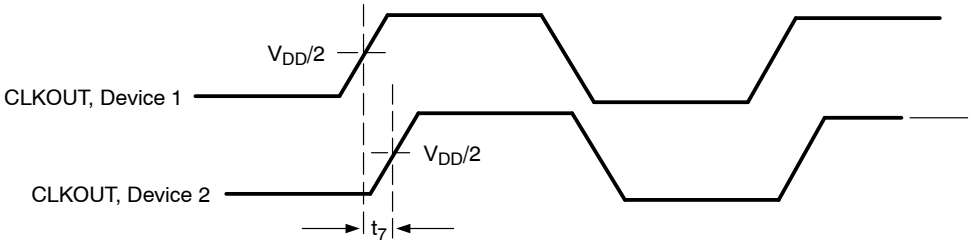
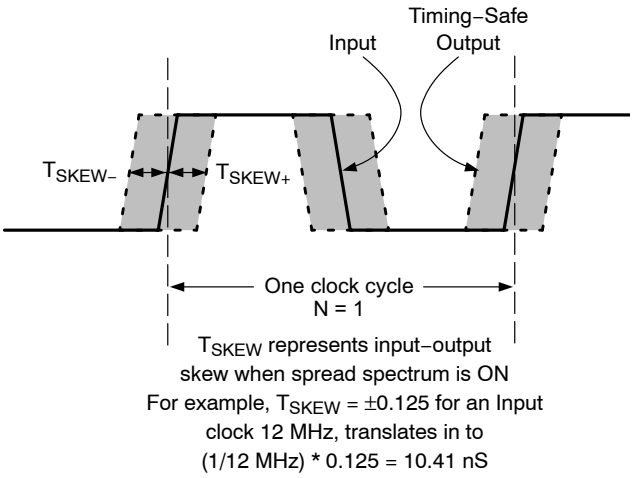


Figure 6. Device − Device Skew



T_{SKEW} represents input−output skew when spread spectrum is ON
For example, T_{SKEW} = ±0.125 for an Input clock 12 MHz, translates in to (1/12 MHz) * 0.125 = 10.41 nS

Figure 7. Input − Output Skew

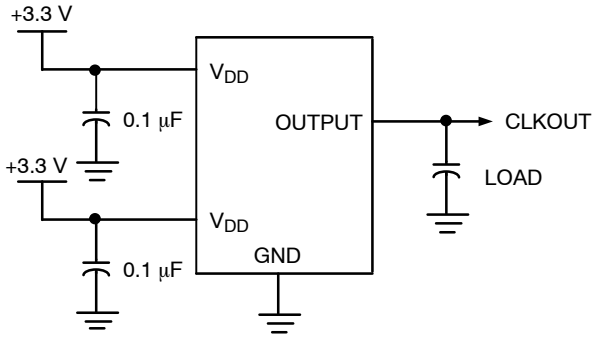


Figure 8. Test Circuit

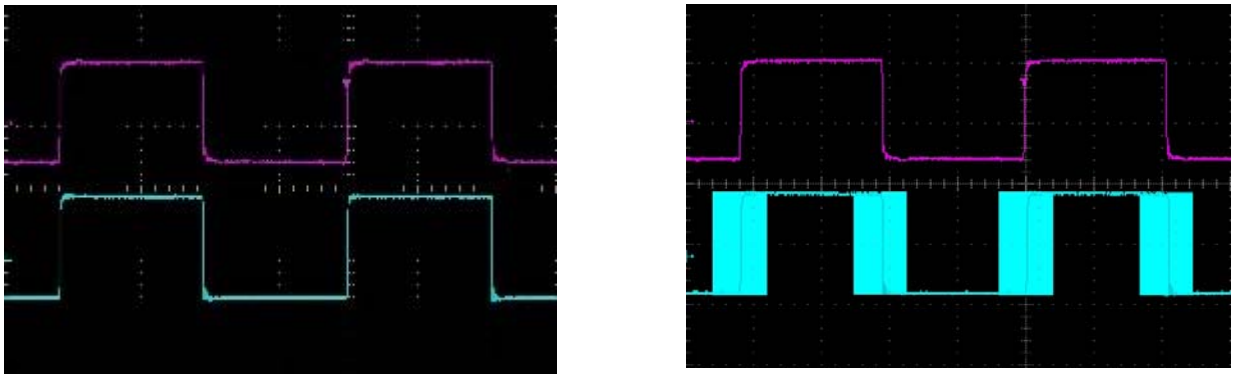
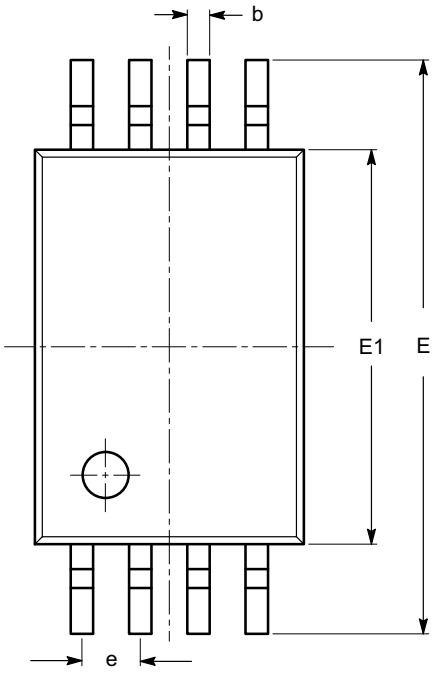


Figure 9. Typical Example of Timing−Safe Waveform

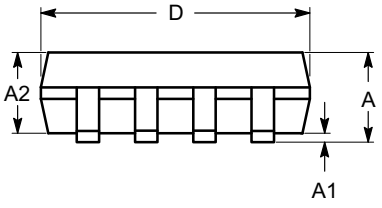
PACKAGE DIMENSIONS

TSSOP8, 4.4x3
CASE 948AL−01
ISSUE O

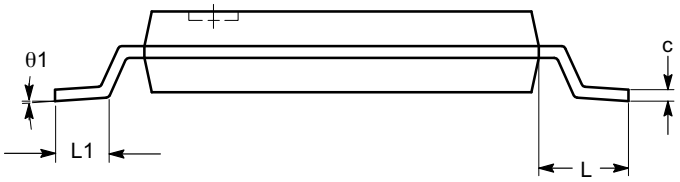


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			1.20
A1	0.05		0.15
A2	0.80	0.90	1.05
b	0.19		0.30
c	0.09		0.20
D	2.90	3.00	3.10
E	6.30	6.40	6.50
E1	4.30	4.40	4.50
e	0.65 BSC		
L	1.00 REF		
L1	0.50	0.60	0.75
θ	0º		8º



SIDE VIEW



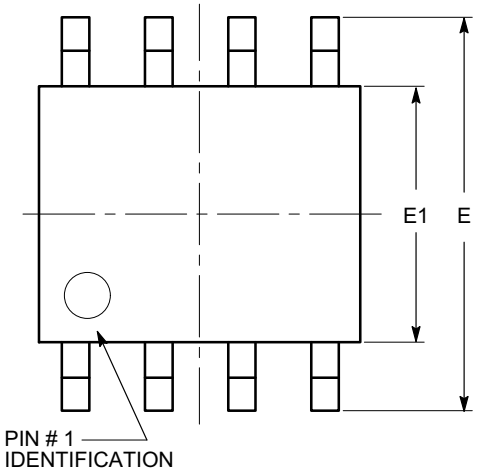
END VIEW

Notes:

(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-153.

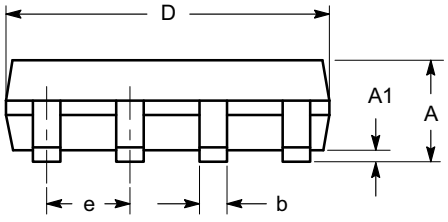
PACKAGE DIMENSIONS

SOIC 8, 150 mils
CASE 751BD−01
ISSUE O

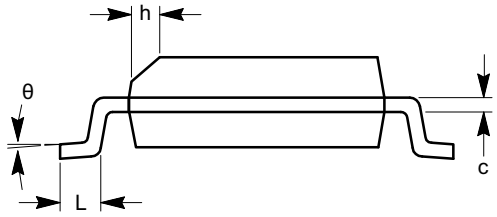


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	1.35		1.75
A1	0.10		0.25
b	0.33		0.51
c	0.19		0.25
D	4.80		5.00
E	5.80		6.20
E1	3.80		4.00
e	1.27 BSC		
h	0.25		0.50
L	0.40		1.27
θ	0º		8º



SIDE VIEW

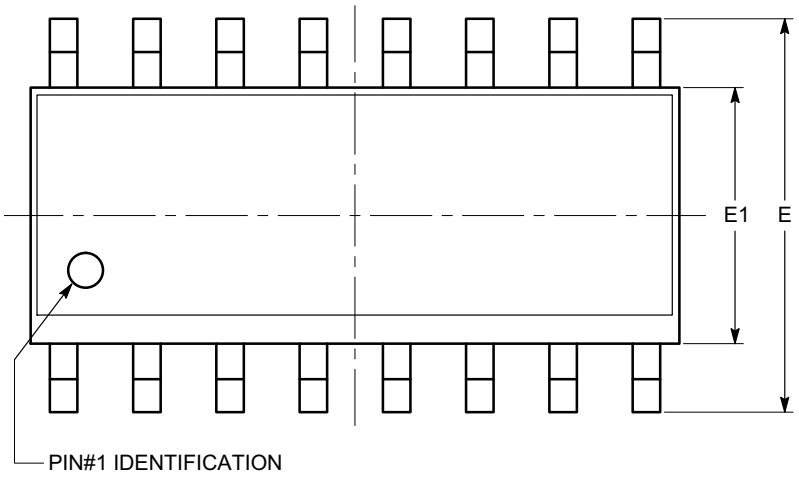


END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MS-012.

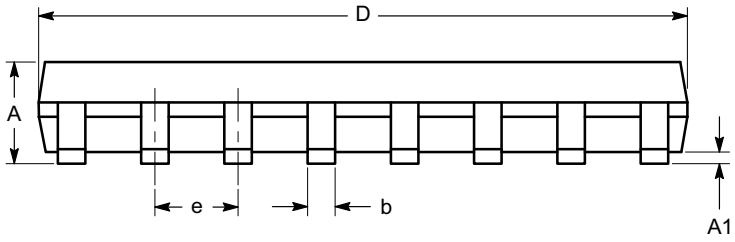
PACKAGE DIMENSIONS

SOIC−16, 150 mils
CASE 751BG−01
ISSUE O

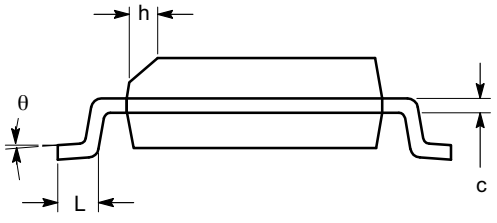


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	1.35		1.75
A1	0.10		0.25
b	0.33		0.51
c	0.19		0.25
D	9.80	9.90	10.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27 BSC	
h	0.25		0.50
L	0.40		1.27
θ	0º		8º



SIDE VIEW

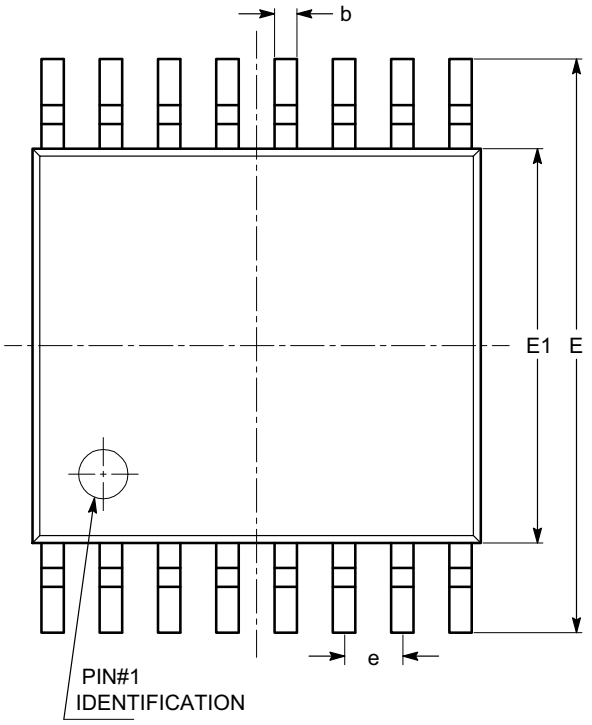


END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MS-012.

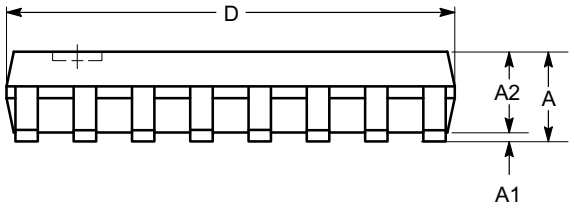
PACKAGE DIMENSIONS

TSSOP16, 4.4x5
CASE 948AN−01
ISSUE O

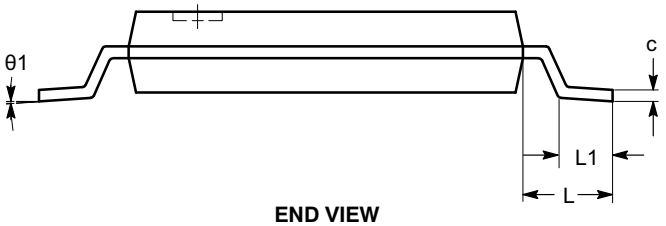


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			1.10
A1	0.05		0.15
A2	0.85		0.95
b	0.19		0.30
c	0.13		0.20
D	4.90		5.10
E	6.30		6.50
E1	4.30		4.50
e	0.65 BSC		
L	1.00 REF		
L1	0.45		0.75
θ	0°		8°



SIDE VIEW



END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-153.

Table 8. ORDERING INFORMATION

Part Number	Marking	Package Type	Temperature
ASM3P622S00BF−08−ST	3P622S00BF	8−pin 150−mil SOIC−TUBE, Pb Free	Commercial
ASM3I622S00BF−08−ST	3I622S00BF	8−pin 150−mil SOIC−TUBE, Pb Free	Industrial
ASM3P622S00BF−08−SR	3P622S00BF	8−pin 150−mil SOIC−TAPE & REEL, Pb Free	Commercial
ASM3I622S00BF−08−SR	3I622S00BF	8−pin 150−mil SOIC−TAPE & REEL, Pb Free	Industrial
ASM3P622S00BF−08−TT	3P622S00BF	8−pin 4.4−mm TSSOP − TUBE, Pb Free	Commercial
ASM3I622S00BF−08−TT	3I622S00BF	8−pin 4.4−mm TSSOP − TUBE, Pb Free	Industrial
ASM3P622S00BF−08−TR	3P622S00BF	8−pin 4.4−mm TSSOP − TAPE & REEL, Pb Free	Commercial
ASM3I622S00BF−08−TR	3I622S00BF	8−pin 4.4−mm TSSOP − TAPE & REEL, Pb Free	Industrial
ASM3P622S00EF−16−ST	3P622S00EF	16−pin 150−mil SOIC−TUBE, Pb Free	Commercial
ASM3I622S00EF−16−ST	3I622S00EF	16−pin 150−mil SOIC−TUBE, Pb Free	Industrial
ASM3P622S00EF−16−SR	3P622S00EF	16−pin 150−mil SOIC−TAPE & REEL, Pb Free	Commercial
ASM3I622S00EF−16−SR	3I622S00EF	16−pin 150−mil SOIC−TAPE & REEL, Pb Free	Industrial
ASM3P622S00EF−16−TT	3P622S00EF	16−pin 4.4−mm TSSOP − TUBE, Pb Free	Commercial
ASM3I622S00EF−16−TT	3I622S00EF	16−pin 4.4−mm TSSOP − TUBE, Pb Free	Industrial
ASM3P622S00EF−16−TR	3P622S00EF	16−pin 4.4−mm TSSOP − TAPE & REEL, Pb Free	Commercial
ASM3I622S00EF−16−TR	3I622S00EF	16−pin 4.4−mm TSSOP − TAPE & REEL, Pb Free	Industrial
ASM3P622S00BG−08−ST	3P622S00BG	8−pin 150−mil SOIC−TUBE, Pb Free	Commercial
ASM3I622S00BG−08−ST	3I622S00BG	8−pin 150−mil SOIC−TUBE, Pb Free	Industrial
ASM3P622S00BG−08−SR	3P622S00BG	8−pin 150−mil SOIC−TAPE & REEL, Pb Free	Commercial
ASM3I622S00BG−08−SR	3I622S00BG	8−pin 150−mil SOIC−TAPE & REEL, Pb Free	Industrial
ASM3P622S00BG−08−TT	3P622S00BG	8−pin 4.4−mm TSSOP − TUBE, Pb Free	Commercial
ASM3I622S00BG−08−TT	3I622S00BG	8−pin 4.4−mm TSSOP − TUBE, Pb Free	Industrial
ASM3P622S00BG−08−TR	3P622S00BG	8−pin 4.4−mm TSSOP − TAPE & REEL, Pb Free	Commercial
ASM3I622S00BG−08−TR	3I622S00BG	8−pin 4.4−mm TSSOP − TAPE & REEL, Pb Free	Industrial
ASM3P622S00EG−16−ST	3P622S00EG	16−pin 150−mil SOIC−TUBE, Green	Commercial
ASM3I622S00EG−16−ST	3I622S00EG	16−pin 150−mil SOIC−TUBE, Green	Industrial
ASM3P622S00EG−16−SR	3P622S00EG	16−pin 150−mil SOIC−TAPE & REEL, Green	Commercial
ASM3I622S00EG−16−SR	3I622S00EG	16−pin 150−mil SOIC−TAPE & REEL, Green	Industrial
ASM3P622S00EG−16−TT	3P622S00EG	16−pin 4.4−mm TSSOP − TUBE, Green	Commercial
ASM3I622S00EG−16−TT	3I622S00EG	16−pin 4.4−mm TSSOP − TUBE, Green	Industrial
ASM3P622S00EG−16−TR	3P622S00EG	16−pin 4.4−mm TSSOP − TAPE & REEL, Green	Commercial
ASM3I622S00EG−16−TR	3I622S00EG	16−pin 4.4−mm TSSOP − TAPE & REEL, Green	Industrial

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